Chapter 3

CMV reduction in USMC using Auxiliary shoot-through switches

3.1 Introduction

The preceding chapters have highlighted the imperative of reducing CMV to improve the reliability of the drive system. This can be done by modifying switching strategies that are used in USMC. In USMC, SVM is preferred over other PWM methods due to its inherent flexibility in selecting active and zero vectors and their strategic placement within a switching cycle [66, 68, 83, 88]. The conventional SVM technique for USMC is discussed in [29], which emphasizes only the production of required output voltage and frequencies without considering CMV reduction. The modulation technique in [66] reduces peak CMV by selecting proper zero vectors (at the input side) in each sector. In this method, medium phase voltage is used as a zero vector. In a three-phase balanced supply, the medium voltage changes from one phase to another for every 60^0. More switching transitions, reduced operating range of the modulation index (m), and loss of soft switching capability are the main limitations of this method. Authors in [83] presented two methods. The first method used four active vectors at the output stage. Two of the four are the same as the conventional method, and the remaining two are their neighbours. The second method uses the medium and lowest line voltages to set up the DC link voltage produced by the CSR stage. This arrangement reduces the maximum voltage at the DC link, resulting in limited voltage gain. The control strategy presented in [69, 70] used the near space vector pulse width modulation (NSPWM)

technique, which results in a limited modulation index range, no soft switching, and increased harmonics on the output side. The control strategy presented in [68] used two modulation techniques to reduce CMV. In one method, three active vectors on the rectifier side and two active vectors on VSI are used to reduce peak CMV. The modulation index range for this method is $0.667 < m < 1$. Another method uses a combination of two alternate active vectors and zero vectors in CSR to construct the current reference vector. Using this combination, the maximum available DC link voltage remains limited with the modulation index range of $0< m <0.577$. By switching off all the CSR switches, peak CMV can be reduced [67] to get a better control range of the modulation index. Still, this control strategy is inconvenient under transient conditions and unsuitable for high gain impedance matrix converters. The open-end winding method [71, 72] eliminated the CMV by introducing a multi-phase converter, but it requires multi phase system (more than 3 phases). Tuyen et al. suggested another modulation technique using three active vectors in the VSI stage [69]. This method also faces limitations in [70]. Though CMV can also be reduced by averaging DC link voltage [87], the voltage gain range is limited. The open current vector method in [89] is another way to reduce peak CMV. This control strategy suffers from the same problem presented in [67] and does not apply to USMC. In [90], the peak of the CMV is reduced by switching off all VSI stage switches. But that modulation scheme is used for higher m values. The methods mentioned above suffer from a limited modulation index range or a lack of CSR soft-switching. This chapter defines new zero vectors with the help of three additional Auxiliary Shoot-Through (AST) switches on the VSI side to avoid hard switching at CSR and reduce CMV. The main contribution of this chapter is to propose new zero vectors by using AST switches for an AC-AC converter with the following salient features:

- Selection of newly defined new zero vectors in modified SVM technique for reducing peak-peak CMV.

- Achieving soft switching at CSR side.

- Regaining modulation index range $0 < m < 1$ as a conventional SVM technique.

3.2 Proposed SVM modulation

The proposed method reduces CMV by inserting an AST switche, as shown in Figure 3.1. AST switches are placed between VSI and three phase load. The SVM technique

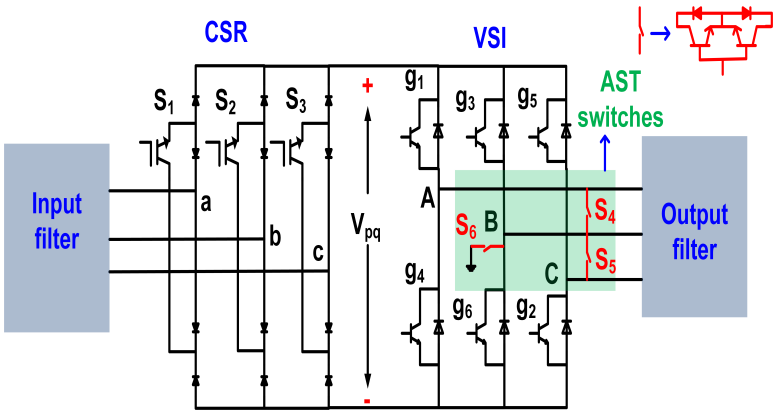


Figure 3.1: Circuit diagram for the proposed method

controls all the switches. As illustrated in Figure 2.3 the CSR SVM is formed by the six equal sectors with active vectors $[I_{ab}, I_{ac}, I_{bc}, I_{ba}, I_{ca}, I_{cb}]$. Two neighboring active vectors in each sector create the input reference vector I_{ref}. Equation (3.1) provides the duty ratios for these active vectors in terms of CSR modulation $m_i(= 1)$ and the angle between the active vector and reference vector (α).

$$d_{iab} = m_i sin(\frac{\pi}{3} - \alpha), \quad d_{iac} = m_i sin(\alpha) \tag{3.1}$$

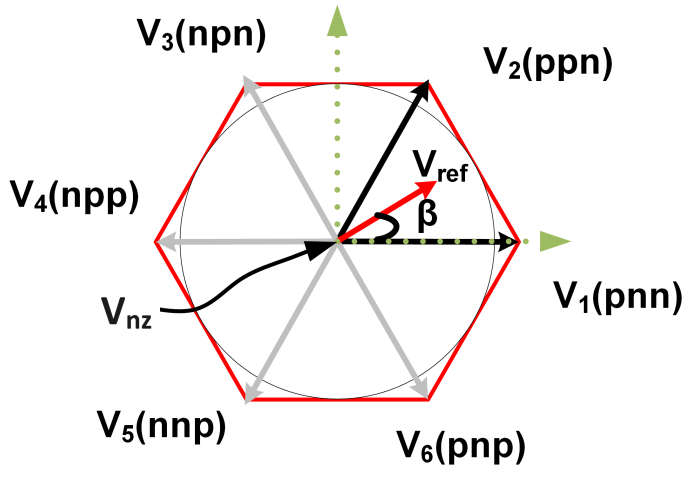


Figure 3.2: VSI space vector diagram

Table 3.1: Newly defined zero vectors

Sector	$[S_1, S_2, S_3, S_4, S_5, S_6, g_1, g_3, g_5, g_4, g_6, g_2]$
Sector 1	[1, 1, 0, 1, 1, 1, 0, 0, 0, 0, 0, 0]
	[1, 0, 1, 1, 1, 1, 0, 0, 0, 0, 0, 0]
Sector 2	[1, 0, 1, 1, 1, 1, 0, 0, 0, 0, 0, 0]
	[0, 1, 1, 1, 1, 1, 0, 0, 0, 0, 0, 0]
Sector 3	[0, 1, 1, 1, 1, 1, 0, 0, 0, 0, 0, 0]
	[1, 1, 0, 1, 1, 1, 0, 0, 0, 0, 0, 0]
Sector 4	[1, 1, 0, 1, 1, 1, 0, 0, 0, 0, 0, 0]
	[1, 0, 1, 1, 1, 1, 0, 0, 0, 0, 0, 0]
Sector 5	[1, 0, 1, 1, 1, 1, 0, 0, 0, 0, 0, 0]
	[0, 1, 1, 1, 1, 1, 0, 0, 0, 0, 0, 0]
Sector 6	[0, 1, 1, 1, 1, 1, 0, 0, 0, 0, 0, 0]
	[1, 1, 0, 1, 1, 1, 0, 0, 0, 0, 0, 0]

Fig.3.2 depicts the VSI SVM, consisting of six active vectors $[V_1 - V_6]$ and zero vectors $[V_{nz}]$. The newly defined zero vectors are given in Table. 3.1. The neighbouring active and zero vectors are used to create the reference output voltage vector (V_{ref}). Equation (3.2) gives the VSI active vector duty ratios. Here, m_v is the VSI modulation index.

$$\begin{aligned} d_{Vp} &= m_v sin(\frac{\pi}{3} - \beta) \quad d_{Vq} = m_v sin(\beta) \\ m_v &= \frac{\sqrt{3}V_{ref}}{V_{pq}} \end{aligned} \tag{3.2}$$

To permit a continuous rotation of the input current space vector I_{ref} and the output voltage space vector V_{ref}, the switching sequence of the USMC must include at least two distinct active switching states at the input stage, two different active switching states at the output stage, and a zero state for USMC switching. For instance if both I_{ref} and V_{ref} are in sector 1, then the switching sequence is given in equation (3.3) and

shown in Figure 3.3.

$$_0|(I_{ab})(V_1) - (I_{ab})(V_2) - (I_{ab})(V_{nz}) - (I_{ac})(V_{nz}) - (I_{ac})(V_2) - (I_{ac})(V_1) - (I_{ac})(V_1) - (I_{ac})(V_2) - (I_{ac})(V_{nz}) - (I_{ab})(V_{nz}) - (I_{ab})(V_2) - (I_{ab})(V_1)|_{T_s} \quad (3.3)$$

In this switching strategy, only active vectors synthesize the current reference vector to achieve maximum DC-link voltage and combination of active and new zero vectors synthesize the VSI reference vector to control the output voltage. Dwell times of the each switching state is given in equation (2.5). From Figure 3.3, the CSR stage switching states are changed during the VSI zero vector stage, and during this switching state, no DC-link flows. Thus, it has the benefit that the input stage switching status changes when the link current is equal to zero (zero current switching), achieving soft switching at CSR stage.

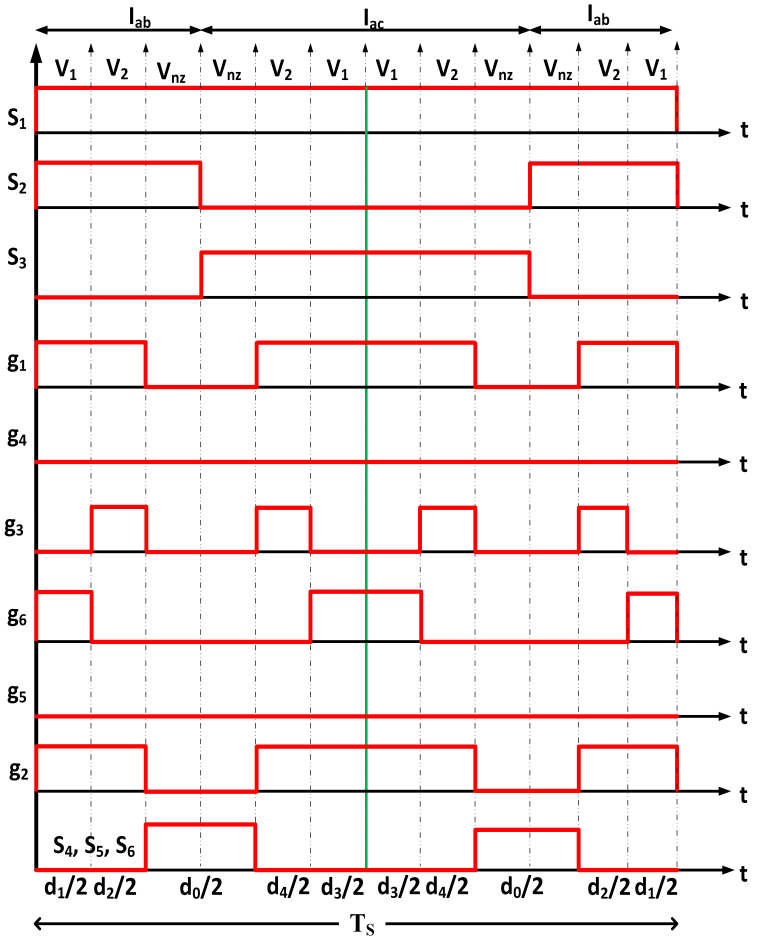
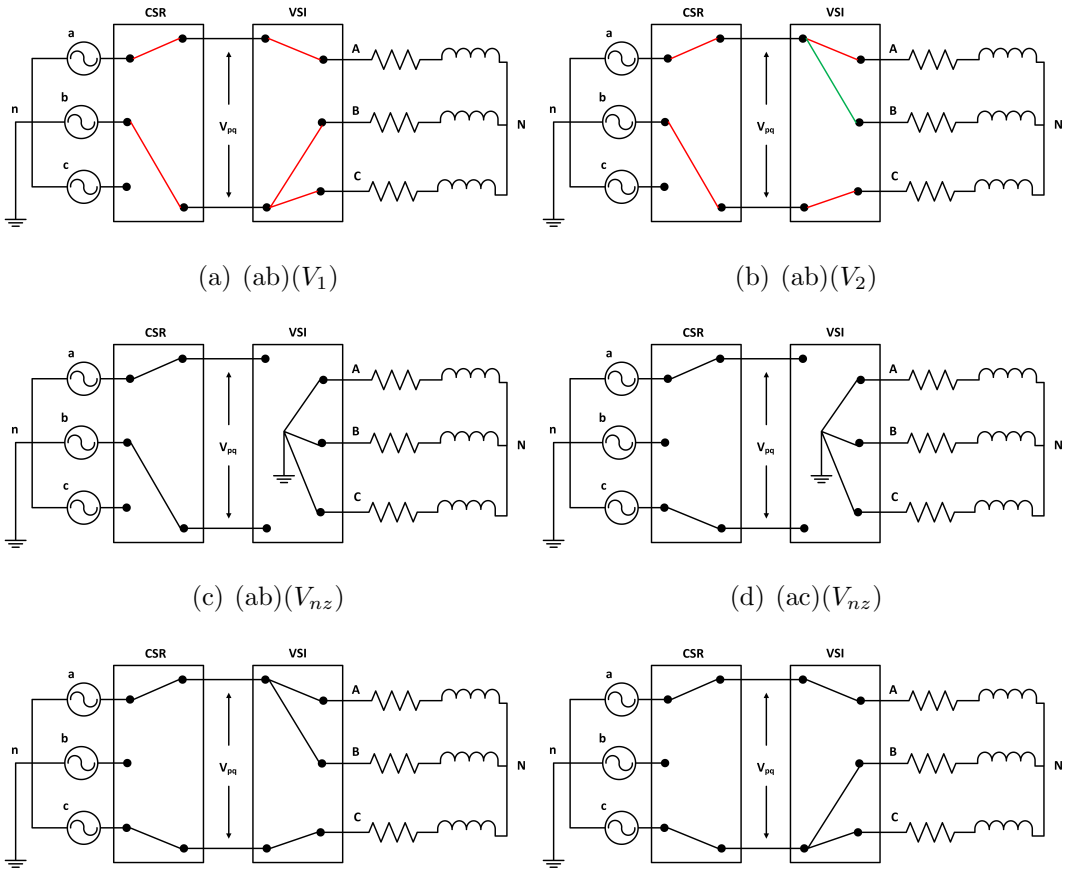


Figure 3.3: Sector 1 switching sequence for the proposed method

Figures 3.4(a) - 3.4(f) show the connection diagrams for each switching state.



(a) (ab)(V_1) (b) (ab)(V_2)

(c) (ab)(V_{nz}) (d) (ac)(V_{nz})

(e) (ac)(V_2) (f) (ac)(V_1)

Figure 3.4: Sector 1 switching sequence for the proposed method

Figure 3.4(a) shows $(I_{ab})(V_1)$ switching state. From equation (2.10), CMV of the converter during this $(I_{ab})(V_1)$ state is equal to $\frac{1}{\sqrt{3}}v_{ab}$. For the next switching state as shown in Figure 3.4(b), S_1, S_3, g_1, g_3, g_6 are ON, which has peak CMV $\frac{1}{\sqrt{3}}v_{ab}$. During zero state as depicted in Figures 3.4(c) and 3.4(d), all switches of the VSI are OFF, and the three phase load is connected to the ground through AST switches S_4, S_5, S_6. The voltage across v_{An}, v_{Bn}, v_{Cn} during this zero state is zero. So from the equation (2.10), zero CMV is developed during zero states. In contrast, the conventional method has a peak CMV equal to $\hat{V}_m$ under a similar situation. The modulation index range for the proposed method is the same as the conventional method ($0 \leq m \leq 1$).

3.3 Voltage equations

Only active vectors are used to generate DC-link voltage on the input side. So, the output of the CSR pulsates between maximum and minimum line voltages. Average DC Link voltage (V_{pq}) is given by equation (3.4)

$$V_{pq} = d_{iab}v_{ab} + d_{iac}v_{ac} = \frac{3}{2}m_i\hat{V}_m \quad (m_i = 1) \tag{3.4}$$

The output phase voltage for the SVM is given by equation (3.5). Here $m = m_i \times m_v$

$$\hat{v}_{AN} = \frac{m_v V_{pq}}{\sqrt{3}} \implies \hat{v}_{AN} = \frac{1.5m\hat{V}_m}{\sqrt{3}} \tag{3.5}$$

By using the proposed switching sequence, the peak CMV ($\frac{1}{\sqrt{3}}\hat{V}_m$) is reduced to 42.2%. By eliminating the zero vector states at the CSR stage, the proposed switching sequence minimizes the ripple ($\frac{dV_{pq}}{dt}$) in the DC link voltage, CSR switching state changes during zero DC link current to achieve ZCS, and the VSI switching sequence is repeated after $T_S/2$ to improve the quality of the output By including these arrangements the proposed modulation has wider modulation index range with lesser peak CMV and holds soft switching capability. The following section gives the validation of the proposed method.

3.4 Simulation results and analysis

Table 3.2: Parameters for the simulation

S. no	***Parameter***	***Value***
1	Three phase input	325 V
2	Input frequency	50 Hz
3	Input filter (L_{in}, C_{in})	0.5 mH, 36 uF
4	Output frequency	100 Hz
5	Output filter (L_o)	0.5 mH
6	Power Rating	2.5 kW
7	Switching frequency	5 kHz

MATLAB platform is used to simulate the proposed method. The USMC converter is fed by 325 V, 50 Hz phase voltage with a 2.5 kW load. The important simulation parameters are given in Table 3.2. After connecting the three-phase input to the USMC, the CSR output voltage (V_{pq}) is shown in Figure 3.5. DC link voltage has a ripple with six times the input frequency and varies from 570 V to 290 V. The average value of the DC link voltage V_{pq} is measured as 485 V, which is nearly theoretical. This DC link acts as a source to the VSI whose modulation index m_v is taken as 0.8. Simulation waveform of the common mode voltage for both conven-

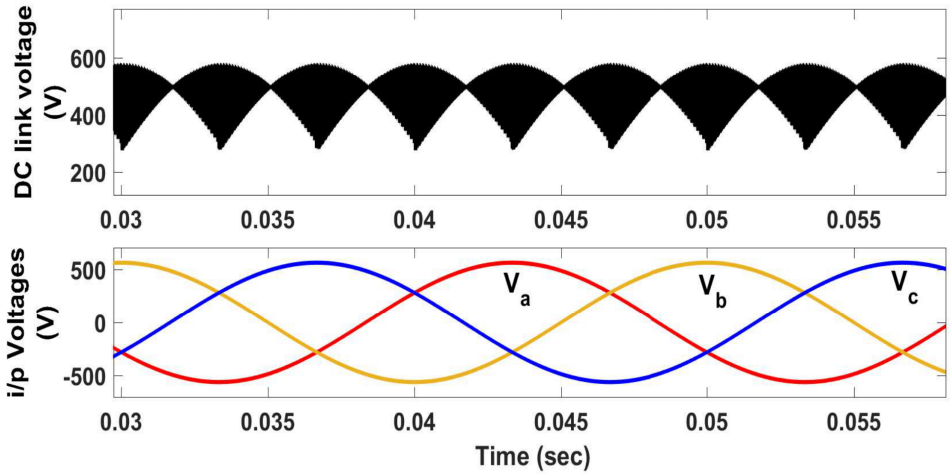


Figure 3.5: Simulation waveforms for three phase supply and DC link voltage

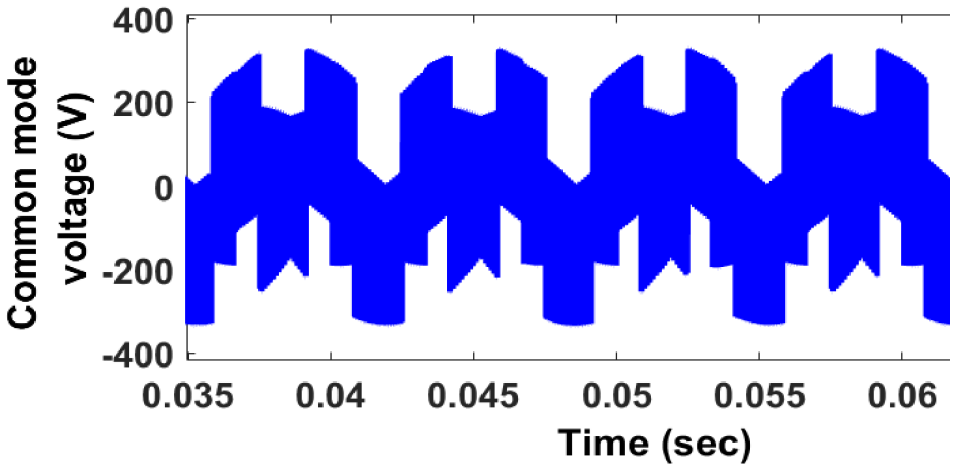
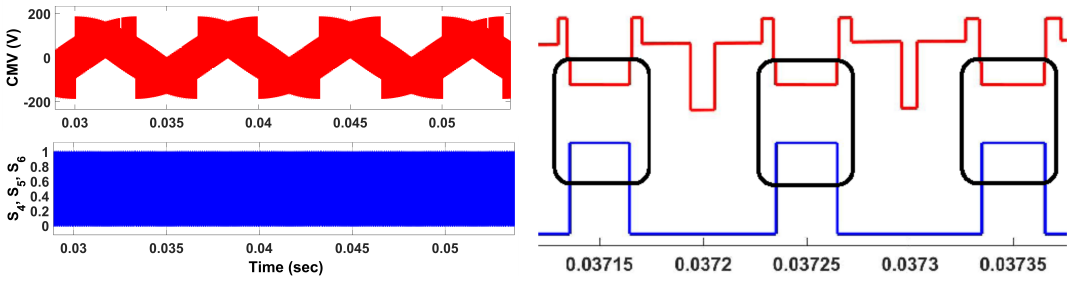


Figure 3.6: Common mode voltage in conventional method

tional and proposed methods are depicted in Figure 3.6 and Figure 3.7, respectively. Conventional method CMV varies from -321 V to 321 V, and peak CMV is measured as 321 V. Whereas proposed method CMV varies from -192 V to 192 V with a peak



(a) (b)

Figure 3.7: a) CMV for the proposed converter b)Zoomed portion

value of 192 V. Reduction in peak CMV is due to using the new zero vector states. CMV behaviour during the new zero vector state is shown in Figure 3.7(b). During the zero vector state, CMV is measured as zero in the proposed method and ± 321 V in the conventional method. The output load voltage is measured as 225 V, 100 Hz. Various performance parameters are observed to understand the impact of the proposed modulation scheme. Figure 3.8 shows the FFT analysis of the input current.

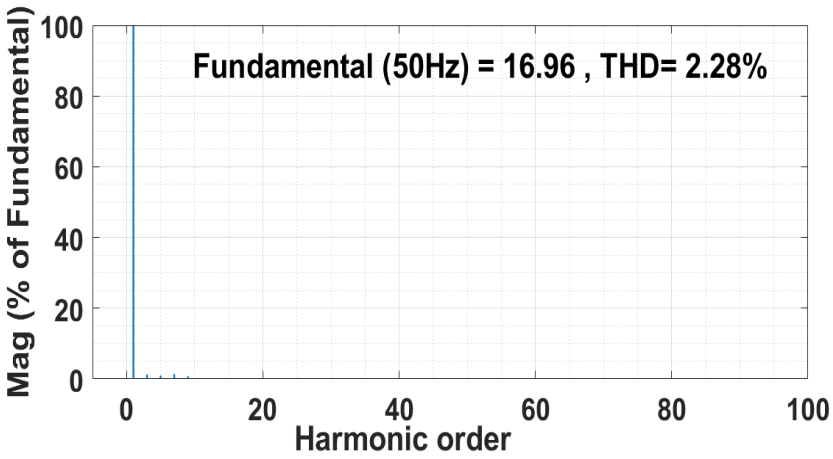


Figure 3.8: Input current FFT analysis

3.4.1 Rating of the AST switch

Figure 3.9 shows the voltage stress across the AST switch. During active vector switching states, the switches S_4 and S_5 block the maximum voltage of 567 V, and the switch S_6 blocks the voltage of 328 V. From Figure 3.10, the maximum blocking voltage of

the VSI switch is the same(567 V) as AST switches. So, from the above information, the rating of the AST switches is the same as that of VSI switches.

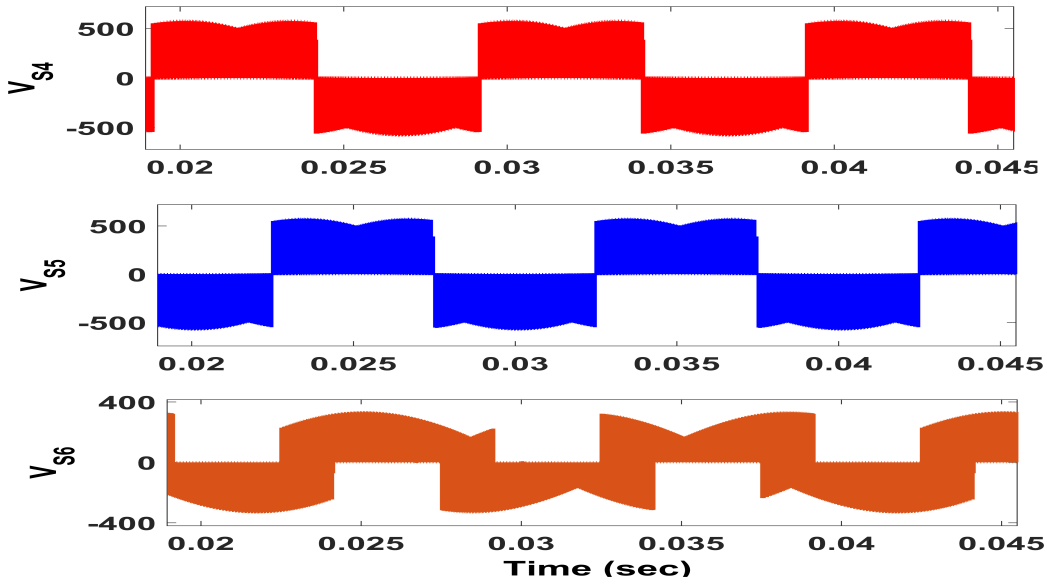


Figure 3.9: Voltage stress across AST switches S_4, S_5, S_6

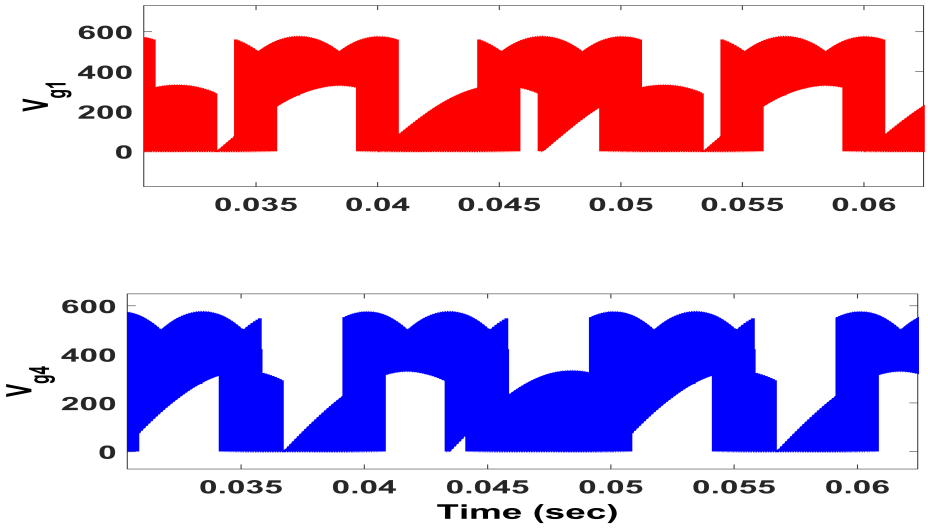


Figure 3.10: Voltage stress across VSI switch g_3

3.4.2 Frequency spectrum of CMV

CMV spectrum analysis is presented in this session to understand the impact of the proposed method. The proposed method reduces the peak CMV by $\frac{1}{\sqrt{3}}$ as compared to the conventional method. Figure 3.11 compares the Fast Fourier Transform (FFT)

analysis for conventional and the proposed methods at a modulation index of 0.8. For a frequency range of 1 kHz to 50 kHz, the proposed method has a lesser CMV magnitude compared to the conventional method. A smaller magnitude implies a reduction in the EMI effect, offering better operating conditions.

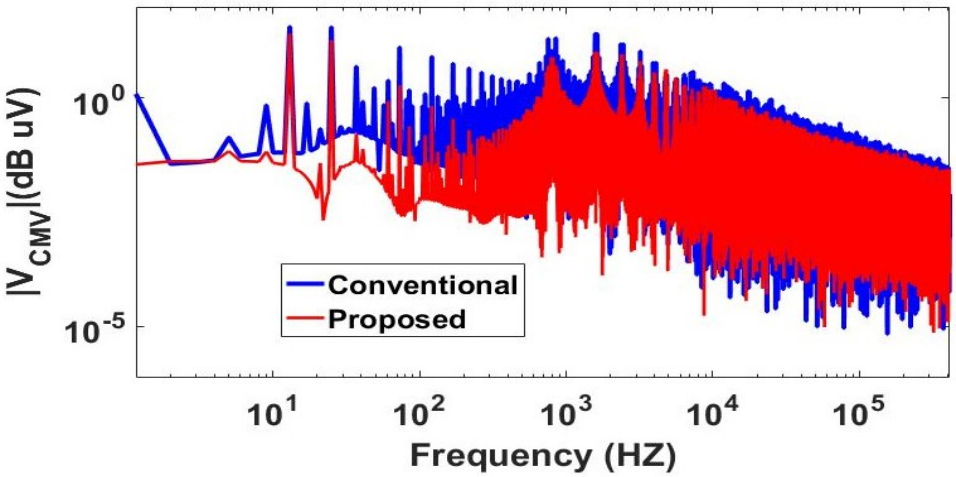


Figure 3.11: FFT analysis for CMV of the proposed method at m = 0.8

3.4.3 Modulation index effect

Figure 3.12 shows the simulation results of the dynamic behaviour of the CMV by varying modulation index m from 0.4 to 0.8 at $t = 0.04$ sec. For both cases, the peak of the CMV is 192 V and is always less than conventional. Fig. 3.13 shows the effect of the RMS value of the CMV ($V_{CMV_{rms(P.U.)}}$). It depends on the modulation index m. Here the input voltage RMS value is taken as the base value. From Table. 2.1 and equation (2.10), zero vector state (ppp or nnn) produces maximum CMV in the conventional method. The zero vector state utilization is increased by decreasing m. Hence, the RMS value of CMV for the conventional method increases by decreasing the modulation index. For $m = 1$, $V_{CMV_{rms(P.U.)}} = 0.57$ and for $m = 0.1$, $V_{CMV_{rms(P.U.)}} = 1.08$. But in the proposed method, zero vector states produce zero CMV, so $V_{CMV_{rms(P.U.)}}$ is decreasing with lower m. For $m = 1$, $V_{CMV_{rms(P.U.)}} = 0.46$ and for $m = 0.1$, $V_{CMV_{rms(P.U.)}} = 0.15$. Further studied the effect of peak CMV by changing m from 0.1 to 0.9, shown in Figure 3.14. Proposed method has a peak CMV 192 V ($\frac{\hat{V}_{an}}{\sqrt{3}}$) irrespective of modulation index value. For the same operating conditions, the conventional method has 325 V.

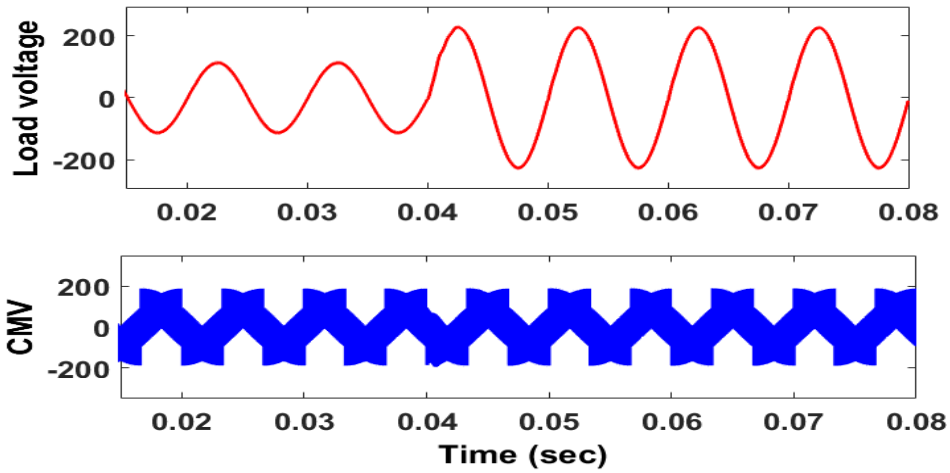


Figure 3.12: Behaviour of load voltage and CMV by sudden change in modulation index $t = 0.04$ sec

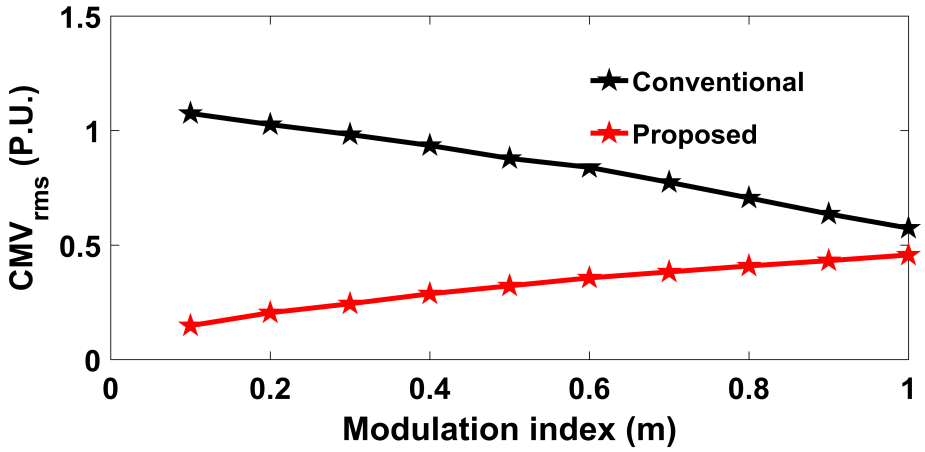


Figure 3.13: RMS value of CMV (P.U.) with change in modulation index

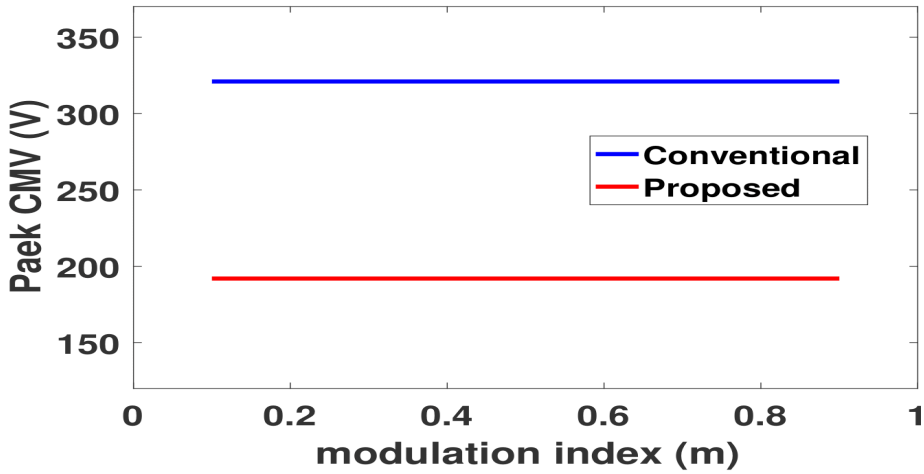


Figure 3.14: Variation of peak CMV by changing modulation index

3.4.4 Effect on input and output frequencies

CMV frequency is three times the supply frequency. By increasing the supply frequency from 50 Hz to 100 Hz, the CMV frequency is also increased twice, which is shown in Figure 3.15. The peak value of the CMV is the same in both cases, so input frequency affects the frequency of the CMV but not the peak of the CMV. Figure 3.16 depicts the Behaviour of CMV and output voltage by changing output frequency. In the simulation, at time $t = 0.04$ sec, the output load frequency changed from 50 Hz to 100 Hz, and observed the corresponding CMV. The peak CMV of the USMC is not impacted by output frequency. Furthermore, the output frequency varied from (20 Hz) to (120 Hz), and the corresponding peak CMV was measured, which is shown in Figure 3.17.

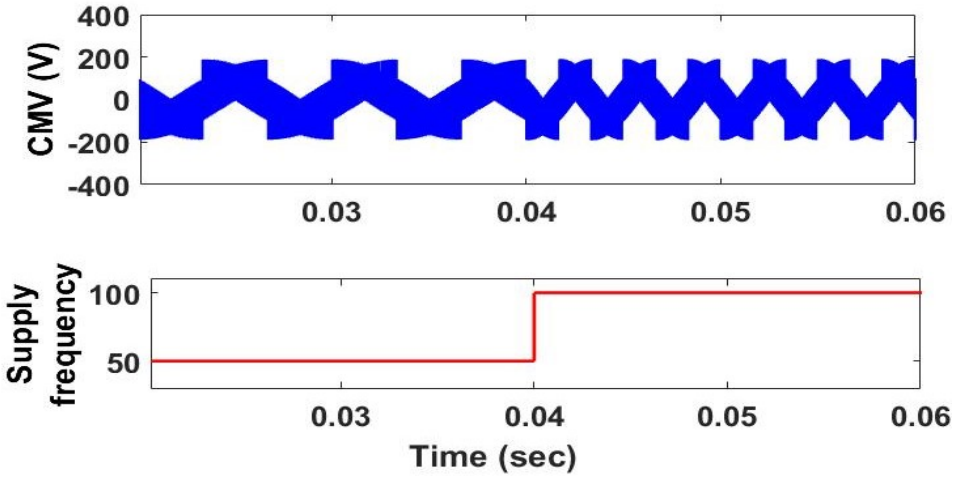


Figure 3.15: Behaviour of CMV by changing VSI reference frequency at $t = 0.04$ sec

3.4.5 Ripple in the DC link voltage

From Figure 3.5, the DC Link voltage attains a maximum voltage of 570 V and minimum voltage of 290 V ($\sqrt{3}\hat{V}_m$ to $\hat{V}_m$). This ripple in the DC link voltage is lesser in comparison to some other modulation techniques and the same as the conventional SVM method. So, the proposed method gives lower peak CMV, decreases DC Link voltage variation, and extends the modulation index range.

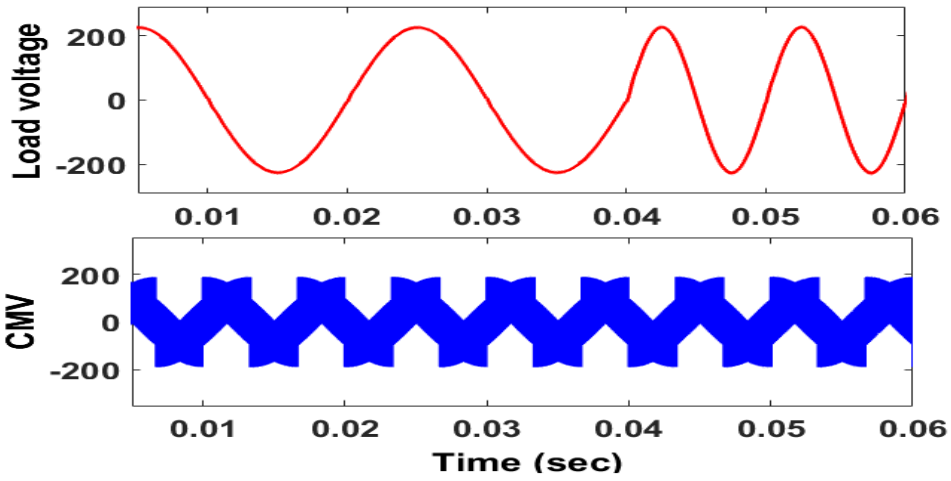


Figure 3.16: Behaviour of load voltage and CMV by changing VSI reference frequency at $t = 0.04$ sec

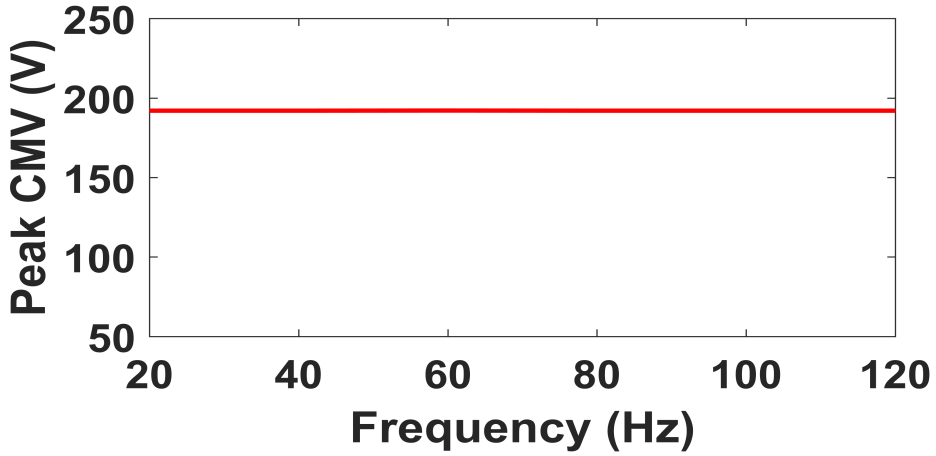


Figure 3.17: Peak of the CMV for output frequency variation

3.4.6 Load power factor angle effect

USMC allows load with power factor angle ($-\frac{\pi}{6}$ to $\frac{\pi}{6}$). To show the effectiveness of the proposed converter, peak CMV is observed by varying load power factor angle within the permissible range. Figure 3.18 shows the peak CMV at different load power factor angles. Here, the power factor angle varied from -25^o to 0^o, from 0.9 lag to unity power factor. For all cases, the peak CMV is 192 V. Hence, the proposed converter effectively works for different load power factors.

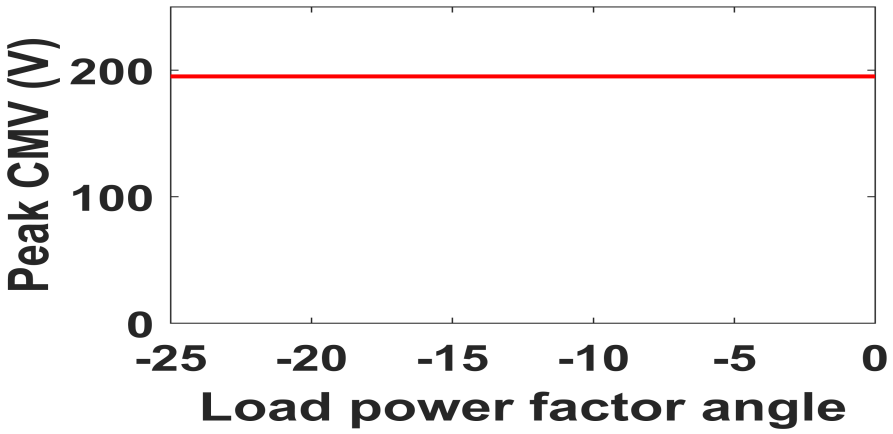


Figure 3.18: Variation of the CMV by changing load power factor angle

3.4.7 Power loss and Efficiency

The efficiency of the USMC depends on the input and output stage semiconductor's conduction and switching losses.

Conduction losses

Conduction losses of each switch and diode can be calculated by using equation (3.6).

$$\begin{aligned} P_{C,S} &= U_{S,F} I_{S,avg} + r_{S,} I^2_{S,rms} \\ P_{C,D} &= U_{D,F} I_{D,avg} + r_D I^2_{D,rms} \end{aligned} \tag{3.6}$$

Here, $P_{C,S}$ is the switch conduction loss, $P_{D,S}$ is the diode conduction loss, $U_{S,F}$ is the switch forward voltage drop, $U_{D,F}$ is the diode forward voltage drop, $I_{S,avg}, I_{D,avg}$ are average currents flows through switch, diode and $I_{S,rms}, I_{D,rms}$ are the RMS currents through switch, diode. The average and RMS currents of the switch and diodes are derived from the equations (3.7) and (3.8) [91].

$$\begin{aligned} I_{D,avg} &= \frac{1}{4} m \hat{I}_o cos\theta_o \\ I_{S,avg} &= 2 I_{D,avg} \end{aligned} \tag{3.7}$$

$$\begin{aligned} I^2_{D,rms} &= \frac{1}{\sqrt{3}\pi} m \hat{I}^2_o (\frac{1}{4} + cos^2\theta_o) \\ I^2_{S,rms} &= 2 I^2_{D,rms} \end{aligned} \tag{3.8}$$

Here, m is the modulation index, θ_o load power factor, and $\hat{I}_o$ is the fundamental of the output current. In the proposed USMC, there are nine switches, three additional AST

switches, and eighteen diodes. These AST switches are tuned on during zero vector as shown in Figure 3.3. Power losses of these switches depend on the nature of the load.

Switching losses

Switching losses of the USMC can be calculated [92] by using the below equations

$$\begin{aligned} E_{sw,off} &= \int_{t_{off}} i(t)v(t)dt \\ E_{sw,on} &= \int_{t_{on}} i(t)v(t)dt \end{aligned} \tag{3.9}$$

Here, $i_S(t)$ is the current passing through the switch, $v_S(t)$ is the voltage across the switch, $E_{sw,on}$ and $E_{sw,off}$ are the switching energy losses of the switch which are calculated during its turn-on transition time t_{on} and turn-off transition time t_{off}. After solving the equation. (3.9) using simplified approximations, an analytical expression is obtained for switching losses E_{sw} and given in equation (3.10)

$$E_{sw} = \frac{2}{6} V_{DS} \times I_{DS} \times (t_{on} + t_{off}) \tag{3.10}$$

Here, V_{DS} is the off-state voltage of the switch, I_{DS} is the on-state current of the switch. The average amount of switching power losses of a switch P_{sw,S_x}, can be calculated as equation (3.11)

$$P_{sw,S_x} = f_S(E_{sw,off} + E_{sw,on}) = f_S(E_{sw}) \tag{3.11}$$

Resistive load

From Figure 3.3, during zero switching state, AST switches are in conduction. For a balanced three-phase resistive load, current flows through switches S_4, S_5, and S_6 is zero. So, total conduction losses P_C will be equal to sum of the conduction loss of each switch and diode in the USMC.

$$\begin{aligned} P_C &= 9P_{C,S} + 18P_{C,D} \\ P_C &= 9(U_{S,F}I_{S,avg} + r_{S,F}I^2_{S,rms}) + 18(U_{D,F}I_{D,avg} + r_{D,F}I^2_{D,rms}) \end{aligned} \tag{3.12}$$

Switching transitions of the CSR switches for the proposed method occur during the output zero vector state. So, CSR switches switching losses are zero. Switching losses of the AST switches S_4, S_5, and S_6 are zero since no current flows. Switching of g_1

occurs four times in a cycle. Hence switching losses of g_1 is $4P_{sw,g_1}$. By a similar calculation, the total switching losses of the proposed method are

$$\begin{aligned} P_{sw_prop} &= 4P_{sw,g_1} + 4P_{sw,g_2} + 8P_{sw,g_3} + 4P_{sw,g_6} \\ P_{sw_prop} &= 20f_S(\frac{1}{3}V_{DS} \times I_{DS} \times (t_{on} + t_{off})) \end{aligned} \tag{3.13}$$

RL load

For balanced three-phase RL load, current flows through switch S_4 is i_A, switch S_5 is i_C, and switch S_6 is zero. So, the total conduction losses in the proposed method is

$$P_C = 11(U_{S,F}I_{S,avg} + r_{S,F}I_{S,rms}^2) + 18(U_{D,F}I_{D,avg} + r_{D,F}I_{D,rms}^2) \tag{3.14}$$

switching transition of the switch S_4 takes place during V_2 (ppn) vector. During this vector, voltage levels of both the A and B phases are equal. So, no voltage across switch S_4 during its OFF position. The switching loss of this switch is zero. For balanced load S_6, switching losses are zero since no current flows through it. CSR switches switching losses are also zero due to soft switching. So, the total switching losses of the proposed method is

$$\begin{aligned} P_{sw_prop} &= 4P_{sw,g_1} + 4P_{sw,g_2} + 8P_{sw,g_3} + 4P_{sw,g_6} + 4P_{sw,S_5} \\ P_{sw_prop} &= 24f_S(\frac{1}{3}V_{DS} \times I_{DS} \times (t_{on} + t_{off})) \end{aligned} \tag{3.15}$$

Analytical efficiency

In this study, the authors chose SKM100GB12T4 as a switch, SKM100GAL12T4 as diode, and switching frequency of 5 kHz. Loss calculations take into account details from the data sheet. Analyzing the efficiency curve in Fig. 3.19 for both conventional and proposed methods, efficiency is gauged by varying the load power at an input supply of 325 V, maintaining a unity load power factor, and a 0.8 modulation index. The proposed method achieves slightly more efficiency than the conventional method for resistive load due to lower switching losses. However, for RL loads, the proposed converter exhibits lower efficiency compared to the conventional method due to increased conduction losses. For 2.5 kW load power, the conventional method achieved 94.4%, whereas the proposed method shows 94.5% and 93.5% for R and RL loads, respectively.

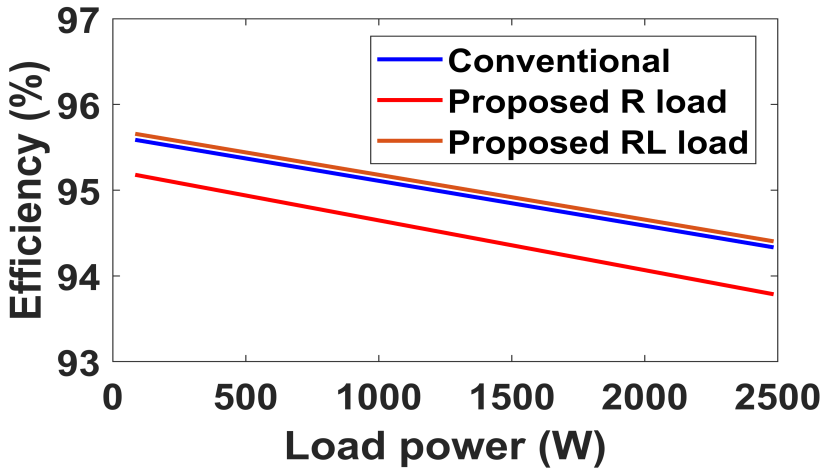


Figure 3.19: Efficiency comparison between conventional and proposed methods

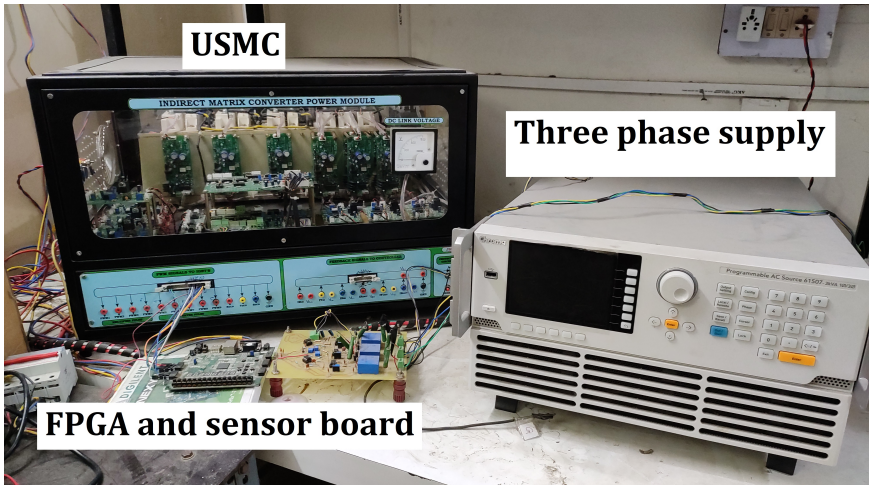
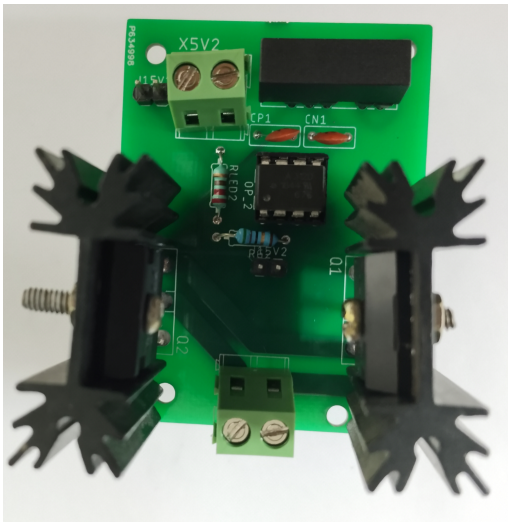


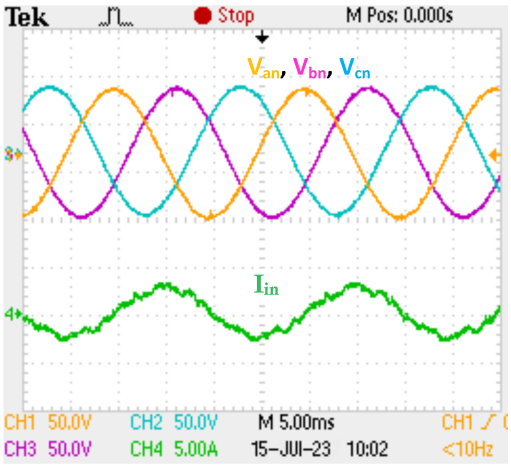
Figure 3.20: Experimental setup for the proposed method

3.5 Experimental results

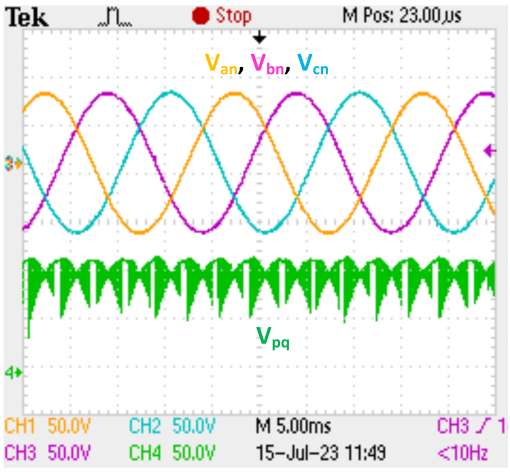
For experimental verification, a hardware prototype is developed as shown in Figure 3.20. FPGA (Artix7100CGS324-1) is used to generate switching signals with a switching frequency of 5 KHz. In this experiment, USMC was fed with 75 V, 50 Hz phase supply at 300 W load. Input voltages and currents are shown in Figure 3.21(b). The input current is measured as 3 A. The intermediate DC link voltage is shown in Figure 3.21(c). The DC link voltage is pulsed in nature and varies six times the input frequency. The average DC link voltage is measured as 104 V. By applying modulation index 0.8, the output voltage depicted in Figure 3.21(d) has a magnitude of 49 V at 100 Hz. For the above operating condition the conventional method has peak to peak CMV value 193 V, which is shown in Figure 3.21(e) and the proposed method decreases



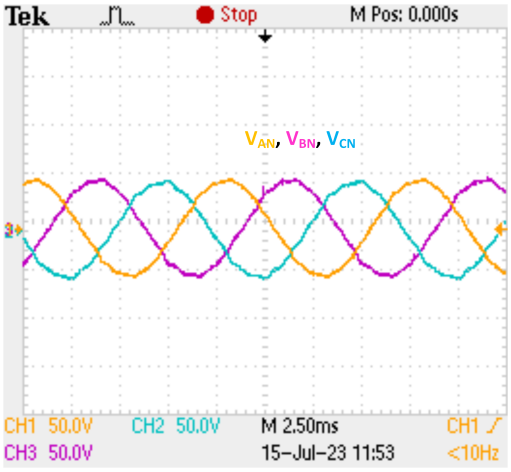
(a) AST switch



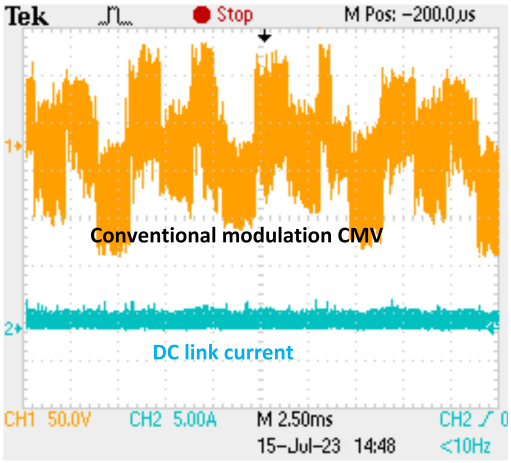
(b) Input supply



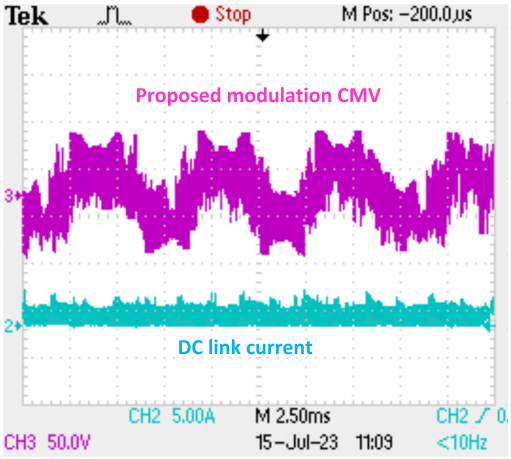
(c) DC-link voltage



(d) Output voltages



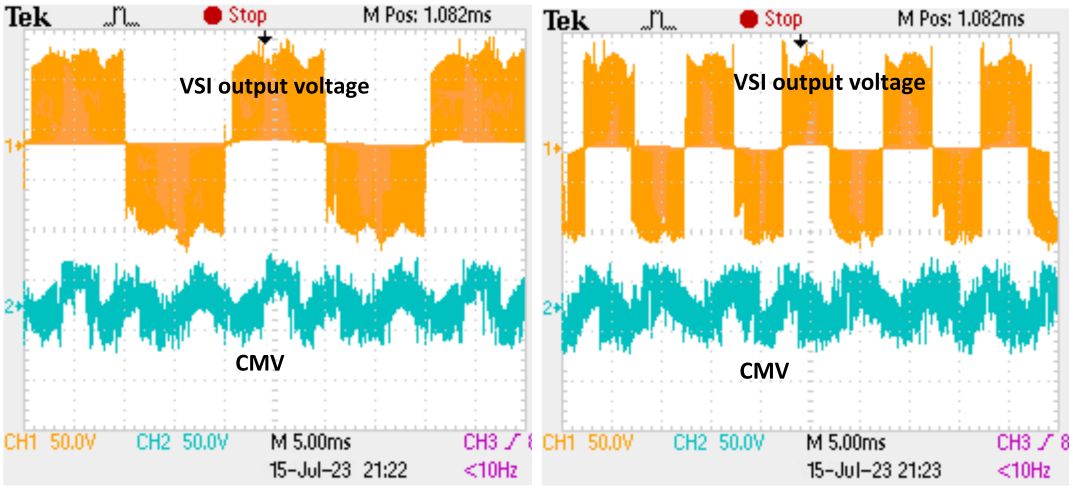
(e) CMV in conventional SVM



(f) CVM in the proposed method

Figure 3.21: Experimental waveforms for the proposed method (modulation index = 0.8)

this CMV to 116 V as shown in Figure 3.21(f). Figure 3.22(a) shows the behaviour of the CMV at 100 Hz output frequencies and Figure 3.22(b) shows the CMV behaviour at 50 Hz output frequency, remaining parameters are the same for both cases. From Figure 3.22 it is observed that the peak CMV is the same for 50 Hz and 100 Hz load frequency. Thus, the VSI output frequency does not affect the peak CMV.



(a) (b)

Figure 3.22: Experimental waveforms for CMV of the proposed method at output frequency 50 Hz, 100 Hz

A comparison of all CMV reduction methods for matrix converters is given in Table 3.3. Here various parameters like the number of switching states, peak CMV, deviation of DC link voltage, and switching losses are compared. Control strategy methods [68, 69, 83], and [72] have reduced voltage gain and [87] have the least voltage gain range. For the switching states in one cycle, almost all methods have either 16 states or 12 states except for the method [67]. The proposed converter gives better DC link voltage deviation ($\hat{V}_m$ to $\sqrt{3}\hat{V}_m$) compared to methods [67, 68], and [89]. The conventional method takes a total of 16 switching transitions to complete one cycle. So, stress across the switches is more compared to the proposed method since $V_{commu,(total)}$ is directly proportional to the number of switching states. Method [66] has hard switching (non-zero current commutation) at the CSR side, and method [83] using four active vectors results in more computational cost and more distortion in the DC link current. Method [69] also has a hard switching problem. Methods [68, 69], and [72] shorten the modulation index range ($0.667 < m < 1$). Method [68] requires fewer switching

transitions but reduces the voltage gain range and maximum available DC link voltage.

Table 3.3: Comparison with other AC - AC converters

Method	m range	max. voltage gain	Deviation of V_{pq}	S.S. at CSR	Switching losses	Peak CMV
[29]	$0 < m < 1$	$0.866\hat{V}_m$	$\hat{V}_m$ - $\sqrt{3}\hat{V}_m$	yes	$24E_{sw}$	$\hat{V}_m$
[66]	$0.667 < m < 1$	$0.866\hat{V}_m$	0 - $\sqrt{3}\hat{V}_m$	No	$20E_{sw}$	$\frac{\hat{V}_m}{\sqrt{3}}$
[83]	$0.6677 < m < 1$	$0.866\hat{V}_m$	$\hat{V}_m$ - $\sqrt{3}\hat{V}_m$	No	$26E_{sw}$	$\frac{\hat{V}_m}{\sqrt{3}}$
[83]	$0 < m < 0.5$	$0.5\hat{V}_m$	0 - $1.5\hat{V}_m$	No	$26E_{sw}$	$\frac{\hat{V}_m}{\sqrt{3}}$
[69]	$0.667 < m < 1$	$0.866\hat{V}_m$	$\hat{V}_m$ - $\sqrt{3}\hat{V}_m$	No	$24E_{sw}$	$\frac{\hat{V}_m}{\sqrt{3}}$
[68]	$0.667 < m < 1$	$0.866\hat{V}_m$	0 - $1.5\hat{V}_m$	No	$20E_{sw}$	$\frac{\hat{V}_m}{\sqrt{3}}$
[68]	$0 < m < 0.667$	$0.5\hat{V}_m$	0 - $1.5\hat{V}_m$	No	$20E_{sw}$	$\frac{\hat{V}_m}{\sqrt{3}}$
[72]	$0 < m < 1$	$0.866\hat{V}_m$	0 - $\sqrt{3}\hat{V}_m$	No	$24E_{sw}$	$\frac{\hat{V}_m}{\sqrt{3}}$
[87]	$0.667 < m < 1$	$0.866\hat{V}_m$	$\hat{V}_m$ to $\sqrt{3}\hat{V}_m$	No	$20E_{sw}$	$\frac{\hat{V}_m}{\sqrt{3}}$
[89]	$0 < m < 1$	$0.866\hat{V}_m$	0 - $\sqrt{3}\hat{V}_m$	No	$24E_{sw}$	$\frac{\hat{V}_m}{\sqrt{3}}$
Proposed	$0 < m < 1$	$0.866\hat{V}_m$	$\hat{V}_m$ - $\sqrt{3}\hat{V}_m$	yes	$24E_{sw}$ (RL)	$\frac{\hat{V}_m}{\sqrt{3}}$

$^{S.S.}$ Soft switching, ^{RL} RL load

3.6 Summary

This chapter introduces an enhanced modulation technique for the USMC, incorporating a novel modulation approach. The analysis demonstrates its efficacy in significantly reducing the CMV of the USMC. Notably, the proposed method ensures a zero CMV in the zero vector state, effectively suppressing the CMV peak to 57.7% compared to traditional modulation techniques. Compares various SVM methods for CMV reduction, highlighting the unique capability of the proposed method to achieve soft switching on the CSR side. Unlike many CMV reduction methods that limit the modulation index range, the proposed method maintains the modulation index range similar to conventional methods, providing an extended voltage control range.

Additionally, the proposed method outperforms other techniques in minimizing ripple content in the DC link voltage, promoting stable operation. Furthermore, the modulation scheme introduces a considerably longer duration ($\frac{do}{2}$) for the zero vector compared to the conventional method ($\frac{do}{4}$), contributing to the enhanced safety of the modified USMC. Overall, the proposed modulation offers a broader range of modulation indices ($0 < m < 1$) with minimal CMV impact, thereby improving the performance of the USMC.

Meanwhile, the proposed SVM approach using AST switches effectively diminishes the peak CMV but attains a maximum voltage gain of 0.867. The next chapter introduces a quasi Z-source USMC to improve the voltage gain, reducing the CMV and ripple in the inductor current.