HARMONIC OPTIMIZATION AND REDUCTION IN COMPONENT COUNT IN MULTILEVEL INVERTERS

Thesis submitted in partial fulfilment for the requirements for the award of the degree of

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ELECTRICAL ENGINEERING

by

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Abstract

Multilevel inverters (MLIs) have drawn much attention in recent years in medium and higher power applications because of their low switching frequencies and ability to withstand higher voltages without requiring high voltage rated power devices. The primary benefits of MLIs are lower electromagnetic interference, lower total harmonic distortion of the output voltage, higher efficiency and the ability to operate at higher voltages. In general, MLIs can be classified into diode-clamped MLIs (DC-MLIs), flying capacitor MLIs (FC-MLIs) and cascaded H-bridge MLIs (CHB-MLIs). DC-MLIs have been utilized in high power AC motor drives, pumps and mills. FC-MLIs have been used in medium voltage traction drives. CHB-MLIs have been used in applications such as reactive power compensation, uninterrupted power supplies and photovoltaic inverters. DC-MLIs have been much prevalent in the industrial applications due to their simple structure. However, they require large number of diodes. On the other hand, FC-MLIs provide more flexibility than DC-MLIs, but require higher number of floating capacitors. Hence, complicated capacitor voltage balancing mechanism is required in them. CHB-MLIs avoid the use of diodes or capacitors, but larger number of isolated DC voltage sources are required to generate higher output voltage levels, which makes it uneconomical.

In earlier published works related to CHB-MLIs, each H-bridge module was supplied by separate DC sources. Subsequent works showed that single DC source or a battery can be used to supply some of the H-bridges of MLI and the remaining H-bridges of MLI can be

supplied by capacitors. Such a topology is known as hybrid cascaded MLI (HC-MLI), wherein the capacitor voltages are maintained constant at desired values.

The methods used for switching HC-MLIs are either based on sinusoidal pulse width modulation (SPWM) or space vector modulation (SVM) techniques for higher switching frequencies and staircase modulation technique for fundamental switching frequency. The switching losses are more and harmonics also appear at higher frequencies in SPWM. The computational intricacy is considered as a significant drawback of SVM, which limits its real-time applications. In case of staircase modulation technique, the switching losses are less but harmonics appear at lower frequencies of the generated output voltage. Several methods have been reported to selectively eliminate lower order harmonics of HC-MLIs in case of staircase modulation technique, out of which the selective harmonics elimination PWM (SHE-PWM) is the most widely used technique. The major complexity associated with SHE-PWM method is to solve the non-linear transcendental equations using Newton–Raphson or mathematical theory of resultant method. These methods are not suitable for solving large number of switching angles as the degree of polynomials in the equations become high and it becomes difficult to solve them.

The aforementioned problems can be solved using modern stochastic search techniques such as genetic algorithm (GA), particle swarm optimization (PSO), whale optimization (WO), grey wolf optimization (GWO), etc. These optimization methods have many limitations. The two major limitations related to GA are its premature convergence and weak local search ability. Unlike GA, PSO has no evolution operators, such as crossover and mutation. PSO locates nearly optimal solution with a fast convergence speed. However, increase in number of switching angles in PSO results in increase in complexity of the search

space and ultimately it is trapped in the local optima of the search domain. In order to take care of this problem, a local search technique, named as mesh adaptive direct search is combined with PSO to accelerate the convergence rate and refine the local search of the algorithm to prevent it being stuck in the local optima. The method thus evolved is named as modified PSO (MPSO).

WO is a recently developed optimization algorithm, which mimics the social behaviour of humpback whales. WO has improved feature of exploration due to its rapid position updating mechanism. However, the encircling mechanism in WO mostly focuses on the exploration in search domain. Hence, WO has less capability to jump out from local optima, in case it falls in it. To improve the convergence speed and to avoid local optima stagnation during encircling mechanism, a local search algorithm, called chaotic search mechanism is combined with WO. The evolved method is named as modified WO (MWO) in this work.

GWO is one of the recently developed meta-heuristic algorithms, which mimics the hunting mechanism and leadership hierarchy of grey wolves. The GWO algorithm also suffers from premature convergence and weak local search ability. In order to take care this problem, a local search algorithm, called chaotic searching mechanism is combined with GWO to enhance the rate of convergence and avoid it from being stuck at local optima. The method thus evolved is known as modified GWO (MGWO).

SHE-PWM technique implemented through MPSO, MWO and MGWO has been used for synthesizing an eleven-level output voltage of three-phase HC-MLIs in this work. The capacitor voltage balancing, even at higher modulation indices, has been resolved by exploiting the redundant switching states of HC-MLI. Finally, the performance of the three-phase, eleven-level HC-MLI has been verified through simulation and experimentation in

this work. The results obtained through MPSO, MWO and MGWO are compared with the results obtained through GA, PSO, WO and GWO in terms of convergence rate and harmonic content. It has been found that MGWO gives improved results in comparison to other optimization methods discussed in this work.

In order to reduce the number active, passive components and capacitor voltage balancing issues in HC-MLIs, switched-capacitor multilevel inverters (SC-MLIs) have been evolved recently. To further improve the SC-MLIs, two new topologies, namely, a 17-level diode assisted switched-capacitor MLI (DASC-MLI) and a 17-level reduced voltage stress switched-capacitor MLI (RVSC-MLI) are proposed in this work. These topologies generate higher output voltages using single DC voltage source and lower number of active and passive components along with reduced total standing voltage (TSV) and peak inverse voltage (PIV). The capacitors are periodically charged and discharged without any additional balancing circuit in DASC-MLI and RVSC-MLI. The performance of the proposed DASC-MLI and RVSC-MLI are validated through simulation studies and experimental prototypes.

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List of Acronyms

MLI	Multilevel Inverter
NPC-MLI	Neutral Point Clamped-MLI
FC-MLI	Flying Capacitor-MLI
CHB-MLI	Cascaded H-Bridge-MLI
HC-MLI	Hybrid Cascaded-MLI
THD	Total Harmonic Distortion
SVM	Space Vector Modulation
SPWM	Sinusoidal Pulse Width Modulation
SHE-PWM	Selective Harmonic Elimination-Pulse Width Modulation
GA	Genetic Algorithm
ACO	Ant Colony Optimisation
BEE	Bee algorithm
PSO	Particle Swarm Optimization
MPSO	Modified Particle Swarm Optimization
WO	Whale Optimization
MWO	Modified Whale Optimization
GWO	Grey Wolf Optimization
MGWO	Modified Grey Wolf Optimization
CDF	Cumulative Distribution Function
SRF	Synchronous Reference Frame
AC	Alternating Current
DC	Direct Current
DSP	Digital Signal Processor
PIV	Peak Inverse Voltage
TSV	Total Standing Voltage
TSV_{pu}	Total Standing Voltage Per Unit
LDC	Longest Discharge Cycle
SC-MLI	Switched Capacitor MLI
DASC-MLI	Diode Assisted Switched Capacitor-MLI

RVSC-MLI	Reduced Voltage Switched Capacitor-MLI
CF	Cost Function
TI	Texas Instruments
FPGA	Field Programmable Gate Array
dSPACE	Digital Signal Processing and Control engineering
RT-LAB	Real Time-Laboratory

Notations

V_{DC}	DC voltage
V_{CAP}	Capacitor voltage
ω	Fundamental switching frequency
H_1, H_2	Principal H-bridge modules
H_3	Additional H-bridge module
V_1, V_2, V_3	Output voltages of H_1, H_2 and H_3 module
V_0	Total output voltage
m_a	Modulation index
a_n and b_n	Fourier co-efficient
θ_n	Switching angles
S	Number of sources
D	Position of best search agent
$\vec{A}$ and $\vec{C}$	Coefficient vectors
j	Current iteration
$\vec{X}$	Position vector
$\vec{X}^*(j)$	Position vector of the best solution
a	Exponential decay function
m	Maximum number of iterations
n	Current iteration; x_j, variable ($j = 0, 1, 2 \cdots$)
μ	Control parameter
cx_j^n	Chaotic variable
$x_{min,j}$	Minimum value of interval for mapping of decision variable
$x_{max,j}$	Maximum value of interval for mapping of decision variable
$\vec{X}(j+1)$	Spiral updating position
$\vec{D}'$	Distance of the i^{th} humpback whale to search prey
p	Constant which outlines the shape of the logarithmic spiral

q	Random number in the interval [−1, 1]
r	Random number in the interval [0, 1]
$\vec{X}_{rand}$	Random whale position vector
V_1	Actual fundamental component voltage
V_1^*	Desired fundamental component voltage
V_5/V_1, V_7/V_1, V_{11}/V_1, V_{13}/V_1	Harmonic components (5^{th}, 7^{th}, 11^{th} and 13^{th}) with respect to fundamental component
ΔV_C	Change in capacitor voltage
τ	Time constant
Q_{stored}	Charged stored in capacitor
V_d	*d*-axis voltage
V_q	*q*-axis voltage
I_d	*d*-axis current
I_q	*q*-axis current
V_d^*	Reference signal to *d*-axis voltage controller
V_q^*	Reference signal to *q*-axis voltage controller
I_d^*	Reference of *d*-axis current controller
I_q^*	Reference of *q*-axis current controller
V_{DC}^*	Reference signal to controller
V_{AC}	Controlled output voltage
V_{md}	Modulation signal in *d*-axis reference frame
V_{mq}	Modulation signal in *q*-axis reference frame
V_m (t)	Sinusoidal modulation signa
R	Load resistance
L	Filter inductor
C	Filter capacitor
I_L	Load current
V_A, V_B, V_C	Three phase voltages
V_{AB}, V_{BC}, V_{CA}	Three phase line-line voltages
M_{of}	Modulation index
$P_{CL,SS}$	Steady state conduction loss
$P_{sw,\,i(on)}$	Switching loss during turn ON
$P_{sw,\,i(off)}$	Switching loss during turn OFF

N_{Switch}	Number of switches
N_{Diode}	Number of diodes
N_{Source}	Number of DC sources
$V_{sw,\,i}$	OFF-state voltage of the i^{th} switch
I_i	Current of the i^{th} switch when the switch is turned ON
I_i'	Current of the i^{th} switch before the turn OFF of the switch
t_{on}	Duration when the switch is turned ON
t_{off}	Duration when the switch is turned OFF
f_{sw}	Switching frequency
N_{on}	Number ON cycles per one cycle
N_{off}	Number OFF cycles per one cycle
ΔV_{Ci}	Voltage ripple of capacitors
P_0	Output power
P_C	Conduction loss
P_S	Switching loss
P_R	Ripple loss
η	Efficiency

Chapter 1

Introduction

1.1 Background and Motivation

Increasing higher power quality requirements in industrial applications and renewable energy sources such as photovoltaic, wind and fuel cell, classical three-level inverters have limitations in meeting the requirements of clean non-polluted sinusoidal waveforms with minimal distortion. To generate nearly sinusoidal waveform with low distortion, multilevel inverters (MLIs) have been evolved and have drawn much attention in medium and high voltage power applications [1]-[10]. The basic concept of MLIs is to perform the power conversion by synthesizing staircase voltage waveforms from input DC sources. Several low voltage DC capacitors, batteries and renewable energy voltage sources are used as input to the MLIs. The commutation of the power switches aggregates these multiple DC sources to achieve required AC voltage at the output. The rated voltage of the power switches depends only on the rating of the DC voltage sources to which they are connected. The attractive features of MLIs can be summarized as

- **Staircase waveform quality and modularity**

  MLIs generate staircase output voltages with very low distortion at reduced *dv/dt* stress, hence electromagnetic interference is reduced.

- **Common-mode voltage**

  MLIs generate reduced common-mode voltage and this can be further reduced using advanced modulation strategies.

- **Input current**

  MLIs draw input current with low distortion.

- **Switching frequency**

  MLIs can also operate at fundamental switching frequency leading to lower switching loss and higher efficiency.

Due to aforementioned advantages, MLIs have been widely utilized in many applications such as renewable energy [3], [4], flexible AC transmission systems, static compensators [5], dynamic voltage restorers, unified power flow controllers, active power filters [7], solid state transformers [8], motor drives, marine propulsion, mine hoists, conveyors, uninterred power supplies and fans/pumps [7]-[10].

1.2 Literature Review

Many MLI topologies have been proposed during the last two decades. MLIs are categorized according to number of DC sources used, such as common DC source and separate DC source based MLIs, as shown in Fig. 1.1. The common DC source based MLIs are diode clamped (neutral clamped) MLI [10]-[16] and flying capacitor (capacitor clamped) MLI [17]-[19]. The cascaded H-bridge MLIs [20]-[28], hybrid cascaded H-bridge [29]-[34] and switched capacitor MLIs [35]-[63] utilize separate DC sources to generate the output voltage levels. Different pulse width modulation (PWM) techniques have been reported to control the output voltage of MLIs, which are sinusoidal PWM (SPWM), selective harmonic elimination PWM (SHE-PWM), selective harmonic mitigation PWM, SHE pulse amplitude modulation and space vector modulation (SVM). This chapter reviews the state of the art of MLIs, their different structures and the different PWM schemes used in MLIs with their relative advantages and disadvantages.

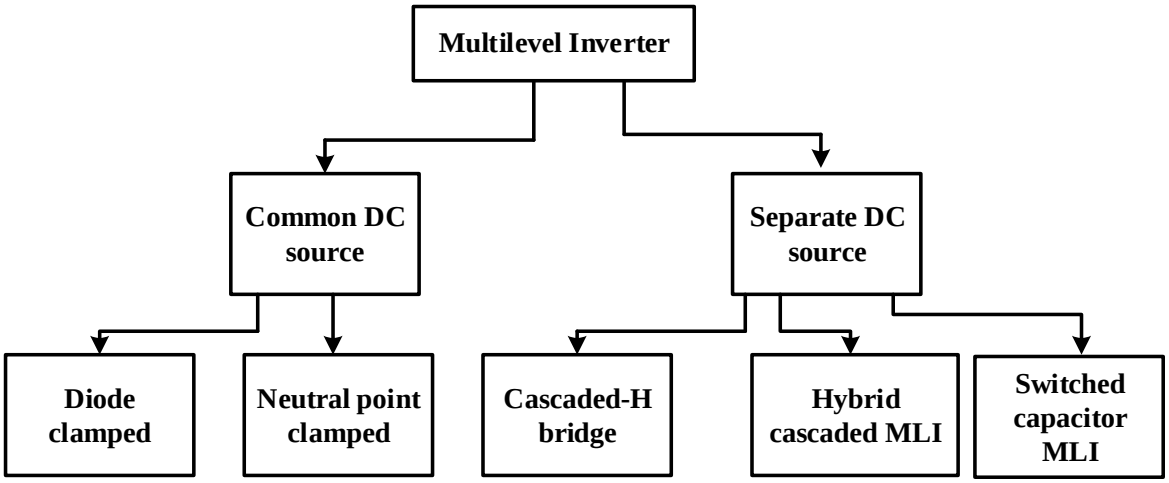


Fig. 1.1 Multilevel inverter topologies.

1.2.1 Neutral Point Clamped MLI

The neutral point clamped MLI (NPC-MLI) is also known diode clamped MLI, which consists of four pair of switches (upper and lower arm) as shown in Fig. 1.2 [10]. The switches are in parallel with series connected capacitors. The positive end of diode is connected to neutral point (O) of NPC-MLI and negative end is connected to the midpoint of upper or lower arm switches.

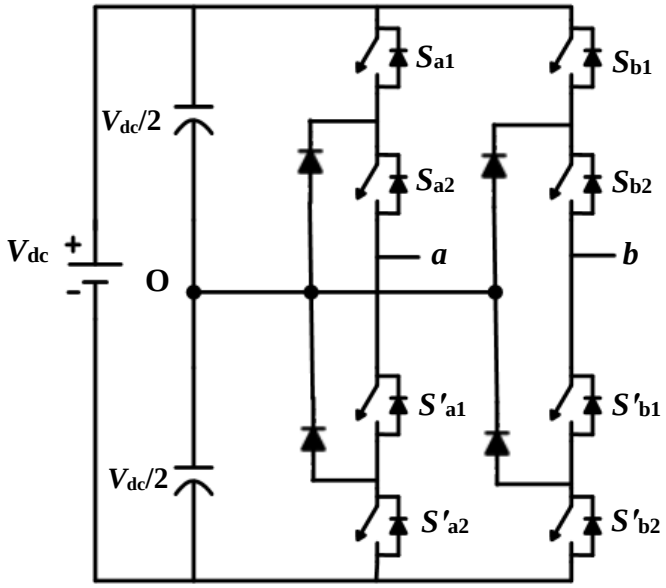


Fig. 1.2 Neutral point clamped MLI [10].

For a three-level NPC-MLI, as shown in Fig. 1.2, the generated output voltage levels are 0, $+1/2V_{dc}$ and $-1/2V_{dc}$.

The NPC-MLI has following advantages:

- All phases share a common DC bus voltage, which minimizes the number of capacitors required.
- Its efficiency is high, when operates at fundamental switching frequency.
- The capacitors can be pre-charged.

The NPC-MLI, however has following limitations:

- The number of diodes increases quadratically with number of voltage levels.
- Real-power flow is difficult to control as DC voltage levels fluctuate without precise control.
- Different current ratings of the switching power devices are required due to difference in conduction periods of devices.

1.2.2 Flying Capacitor MLI

A single-phase five level flying capacitor MLI (FC-MLI), also known as capacitor clamped MLI is shown in Fig. 1.3 [17]. The FC-MLI provides more flexibility in output voltage synthesis and capacitor voltage balancing. The voltage difference between the capacitors regulates the magnitude of output voltage levels.

The existing redundancy in switching states regulates the voltage of capacitor and obtain required voltage level. In the present circuit, switches S_{a1}, S_{a2} and S'_{a1}, S'_{a2} are complementary to each other. The voltage of capacitor is maintained at $V_{dc}/2$. The generated five level output voltage levels in FC-MLI are $+V_{dc}$, $+ V_{dc/2}$, 0, $-V_{dc}$ and $-V_{dc/2}$. In FC-MLI, the output voltage is generated by utilizing different combinations of switches.

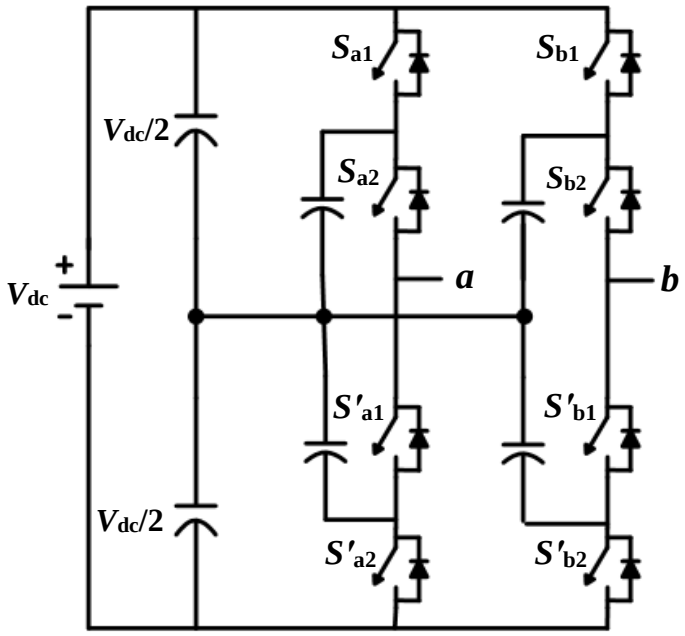


Fig. 1.3 Flying capacitor MLI [17].

The different switching combinations are used to charge or discharge the capacitors, which helps in balancing of capacitor voltages. The advantages of FC-MLI are as follows:

- Redundancies are available for balancing the voltage levels of the capacitors.
- Active and reactive power flow can be controlled.

FC-MLI, however has some disadvantages also, which are:

- The large number of capacitors makes the overall system expensive and bulkier.
- Packaging is more difficult with higher number of voltage levels.
- Complex control is required to maintain the voltages across capacitors.

1.2.3 Cascaded H-Bridge MLI

CHB-MLI uses series connected H-bridge inverters to generate several voltage levels, as shown in Fig.1.4 [20]. The output of each H-bridge has three discrete voltage levels such as $+V_{dc}$, 0 and $-V_{dc}$, which results into a staircase waveform. A single-phase five level CHB-MLI generates voltages $+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$ and $-2V_{dc}$ respectively.

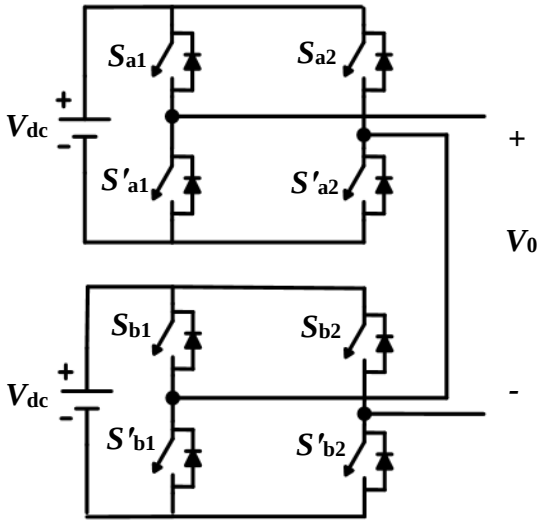


Fig. 1.4 Cascaded H-bridge MLI [20].

The switches S_{a1}, S_{a2}, S'_{a1}, S'_{a2} and S_{b1}, S_{b2}, S'_{b1}, S'_{b2} are used to generate five different voltage levels such as $+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$ and $-2V_{dc}$. When four switches S_{a1}, S'_{a2}, S_{b1} and S'_{b2} are turned ON, the output voltage level is $2V_{dc}$ obtained; when S_{a1} and S'_{a2} or S_{b1} and S'_{b2} are ON, the generated voltage level is V_{dc}; when either pair S_{a1} and S_{a2}, or S_{b1} and S_{b2} are ON, the voltage level is 0. Switch pairs S_{a1}, S'_{a1} and S_{b1}, S'_{b1} are complementary to each other. The voltage levels can be increased by including identical inverters in cascade.

The advantages for CHB-MLI are as

- It can be easily extended to obtain higher voltage levels and control circuit is simple.
- Clamping diodes and balancing capacitors are not required.

However, CHB-MLI has a disadvantage that separate DC sources are required for each of the H-bridges. This limits its application and increases the cost.

1.2.4 Hybrid Cascaded MLI

To reduce the number of DC sources and switches in CHB-MLIs, hybrid cascaded MLI (HC-MLI) has been proposed. HC-MLIs use a single DC voltage source and the remaining DC

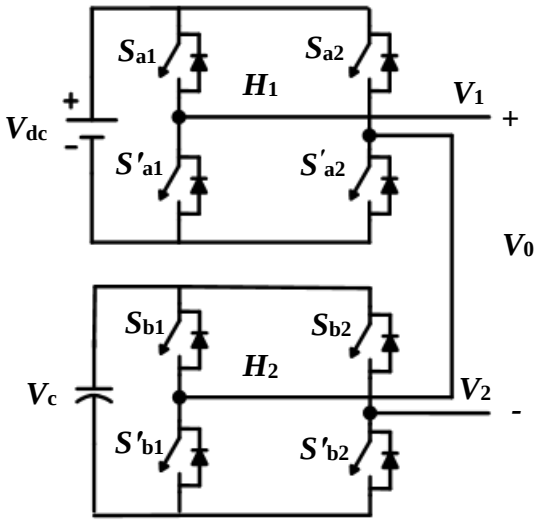


Fig. 1.5 Hybrid cascaded MLI [29].

sources are replaced by capacitors, as shown in Fig. 1.5 [29]. The DC source of the first H-bridge (H_1) is a battery or fuel cell, which generates output voltage of V_{dc}, while the DC source of the second H-bridge (H_2) is a capacitor, whose voltage is held at V_C.

The output voltage of the first H-bridge is denoted by V_1 and the output of the second H-bridge is denoted by V_2, so that the output voltage of HC-MLI is $V_0 = V_1 + V_2$. By using the switches of H_1 properly, the output voltages are $+V_{dc}$, 0 and $-V_{dc}$, while the output voltage of H_2 are $+V_c$, 0 and $-V_c$. Hence, the output voltage of HC-MLI can have the values $+(V_{dc} + V_c)$, $+V_{dc}$, $+V_c$, 0, $-V_c$, $-V_{dc}$ and $-(V_{dc} + V_c)$, which constitute 7 possible output voltage levels. A 7-level output voltage is generated through voltage steps $+3V_{dc}/2$, $+V_{dc}$, $+V_{dc}/2$, 0, $-V_{dc}/2$, $-V_{dc}$ and $-3V_{dc}/2$, when the capacitor's voltage V_c is chosen as $V_{dc}/2$.

The HC-MLI have some disadvantages which are as follows:

- As HC-MLI uses capacitors and DC sources, balancing of capacitor voltages is an inherent problem in these topologies.
- The possibility of extending the number of output voltage levels is not feasible in HC-MLIs.

1.2.5 Switched Capacitor MLI

SC-MLIs have been reported to mitigate the use of large number of circuit components and the challenges of capacitor voltage balancing in conventional MLIs [35]-[60]. The SC-MLIs use capacitors in combination with power switches in a specific way to generate the output voltage. Using different circuit configurations and connections of switched capacitor (SC) cell can generate high or low-voltage gains. The low-voltage gain SC-MLI has a simple structure with fewer elements and also its control is simple. On the contrary, high-voltage gain SC-MLIs have bulky circuit due to the use of multiple SC circuits. The basic circuit of SC cell consists of switches, diodes and capacitors as shown in Fig. 1.6(a) [38]. The DC voltage source is connected to capacitor *C* using switches *S* and *P*. The switches *S* and *P* have opposite operation. When switch *S* is switched ON, switch *P* is OFF and vice versa. Fig. 1.6(b) and (c) shows different the operation modes of basic unit of SC cell. In the positive half cycle, when switch *P* is switched ON, the diode *D* is forward biased and capacitor *C* is charged to input DC voltage, shown in Fig. 16(b). During the second half of cycle, when switch *S* is turned ON, capacitor *C* starts discharging and diode *D* becomes reverse-biased. The voltage source is connected in series with the previously charged capacitor *C*. So, the two voltages are added to generate $V_L = V_{dc} + V_c$, as shown in Fig. 16(c). In order to obtain higher voltage levels, multiple units of SC cells are connected in cascade.

A switched capacitor based 9-level circuit is made up of a SC cell at front end and cascaded H-bridge at back end is shown in Fig. 1.7 [39]. If the numbers of voltage levels obtained by SC cell at front end and cascaded H-bridge back end are N_1 and N_2 respectively, then the number of obtained voltage levels are $(2\times N_1\times N_2) +1$ in entire operation cycle. The switches S_1, S_2, S'_1 and S'_2 of SC cells (SC_1 and SC_2) connect the capacitors C_1 and C_2 with the voltage source V_{dc1} and V_{dc2} in series or parallel to generate the output voltage levels.

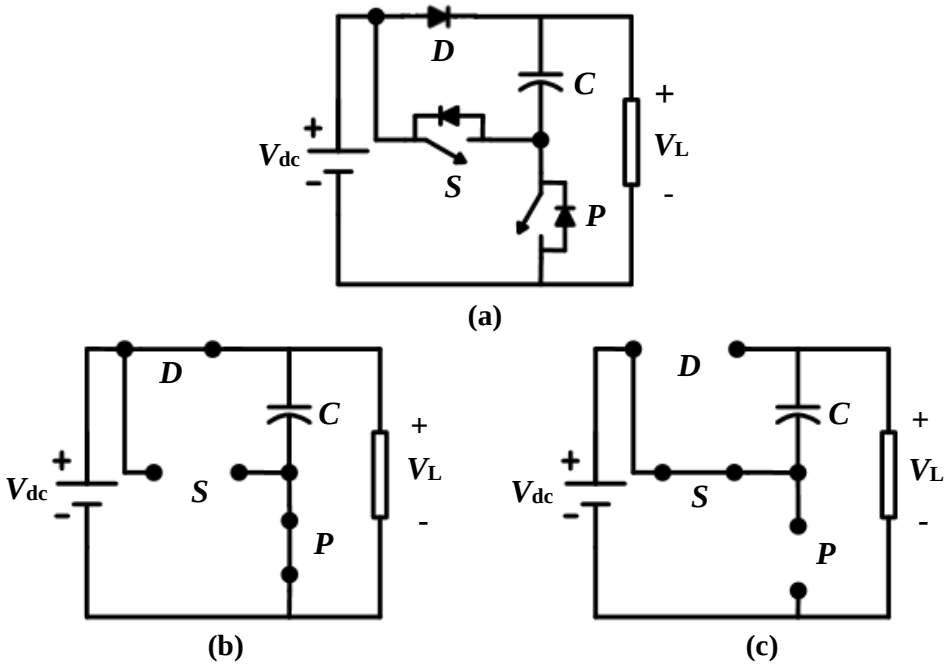


Fig. 1.6 SC cell operation. (a) Basic unit of SC cell. (b) Capacitor charging. (c) Capacitor discharging [35].

The switches S_{1a}, S_{1b}, S_{1c}, S_{1d}, S_{2a}, S_{2b}, S_{2c} and S_{2d} of the cascaded H-bridge are used for polarity generation of the output voltage and the diodes D_1 and D_2 are used to restrict the current direction.

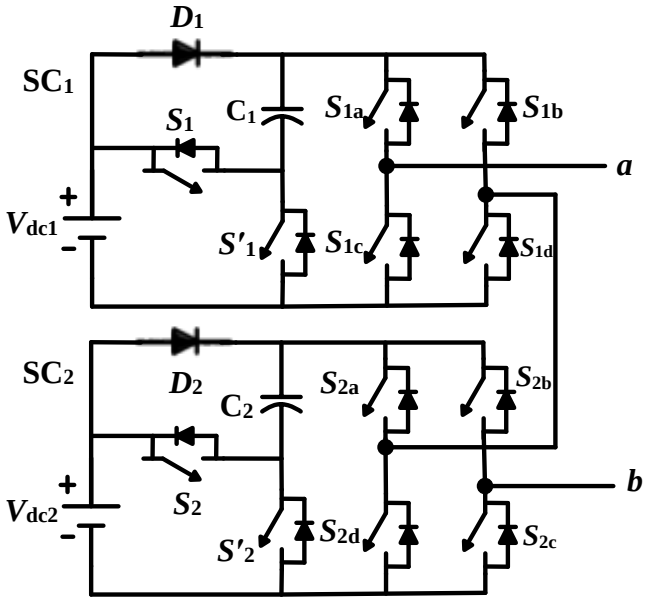


Fig. 1.7 Cascaded switched capacitor MLI [39].

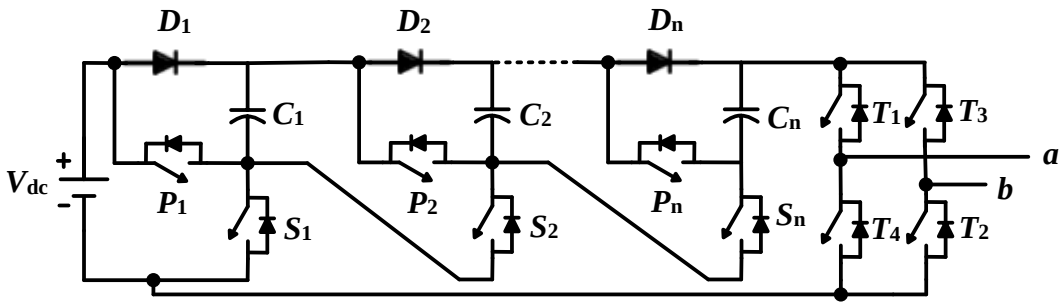


Fig. 1.8 Switched capacitor cell [38].

One of the major limitations of the said SC-MLI is that it requires higher number of DC sources and power switches to generate output voltage levels and this limitation increases at higher voltage levels. As the PIV of switches becomes high, the application of the said SC-MLI is restricted.

In order to achieve higher voltage gain using reduced the number of DC voltage source, another SC-MLI has been proposed in [38], as shown in Fig. 1.8. This proposed SC-MLI uses the series combination of different basic SC cells to generate multiple voltage levels. The capacitors are connected in series using switches S_i (i = 1, 2, . . ., n) and in parallel with the voltage sources by the use of switches P_i (i = 1, 2, . . ., n). An H-bridge is used at the front end to generate polarity. One of the advantages of the proposed topology is that the voltage blocked by each switch is limited to input voltage V_{dc}. The other advantage of the proposed SC-MLI is its high voltage boosting capability due to cascaded connection of several SC cells. However, the reported SC-MLI requires large number of power switches to generate the output voltage at higher voltage levels and the PIV of switches are also high due to the presence H-bridge.

Subsequently, another single sourced SC-MLI with front end H-bridge is proposed in [40], as shown in Fig. 1.9, where in each SC cell consists of a capacitor, an active switch and two diodes. The output voltage levels of the proposed SC-MLI can be changed by utilizing

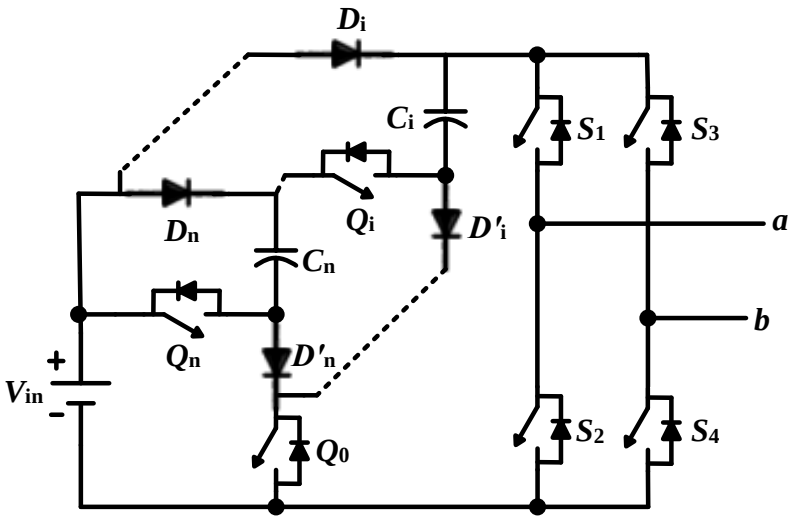


Fig. 1.9 Topology of the proposed switched capacitor MLI [40].

different SC cells. A total of $2n + 3$ voltage levels 0, $\pm V_{in}$, $\pm 2V_{in}$, ..., $\pm (n + 1) V_{in}$ can be generated using the proposed topology, where n is the number of SC cells. To obtain zero voltage level, Q_0 is turned ON, while the other switches are in OFF condition. The voltage across capacitors C_i are equal to input voltage V_{in}, i.e., $V_{Ci} = V_{in}$ ($i = 1, 2, \ldots, n$), when switches S_1 and S_4 are turned ON and S_2 and S_3 are in OFF condition. Similarly, when S_2 and S_3 are ON and S_1 and S_4 are OFF, the generated output voltage is $-V_{in}$. One of the major advantages of this SC-MLI is that it requires a single DC voltage source to produce output voltage levels. However, the total standing voltage (TSV) and peak inverse voltage (PIV) of the proposed SC-MLI increases drastically for higher number of voltage levels, which restricts its applications.

To reduce the number of active/passive components and obtain comparatively higher voltage gain, a new high step-up SC-MLI has been proposed in [54], as shown in Fig. 1.10. The proposed SC-MLI has two separate DC sources (V_{S1} and V_{S2}) along with several SC cells in each side of H-bridge. When the switch T_1 is ON, the capacitor C_1 is connected in parallel with the DC voltage source V_{S1} and C_1 is charged to V_{S1}.

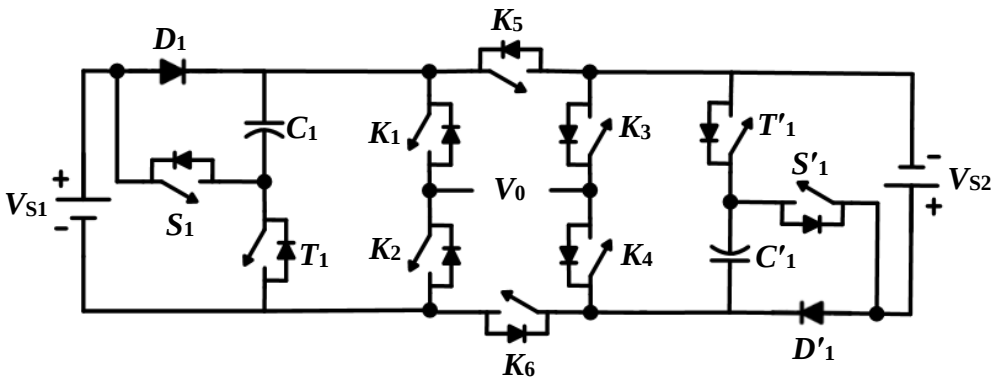


Fig. 1.10 Proposed switched capacitor-based unit [54].

Similarly, when the switch T'_1 the capacitor C'_1 charged to V_{S2}. When switches S_1 and S'_1 are in ON, both the capacitors C_1 and C'_1 are in series with V_{S1} and V_{S2} to generate high voltage gain. The switches K_1-K_5 of H-bridge module are used for voltage addition and polarity generation in SC-MLI. In this topology, higher number of voltage levels are obtained using lesser number of passive components. However, the number of DC sources required is high which leads to increased cost and restricted operation.

1.3 Pulse Width Modulation (PWM) Techniques for Control of MLI

Different pulse width modulation (PWM) techniques are reported in literature for the control of the output voltage of MLIs and reducing the distortion in it [64]-[76]. They are classified according to their switching frequency as

- High switching frequency PWM
- Fundamental switching frequency PWM

The well-known high switching frequency PWM techniques for the control of MLIs are multicarrier sinusoidal pulse width modulation (SPWM) [64] and space vector PWM (SVM-PWM) [66]. The fundamental switching frequency PWM methods are selective harmonic elimination PWM (SHE-PWM) and space vector modulation (SVM). The different modulation techniques are shown in Fig. 1.11.

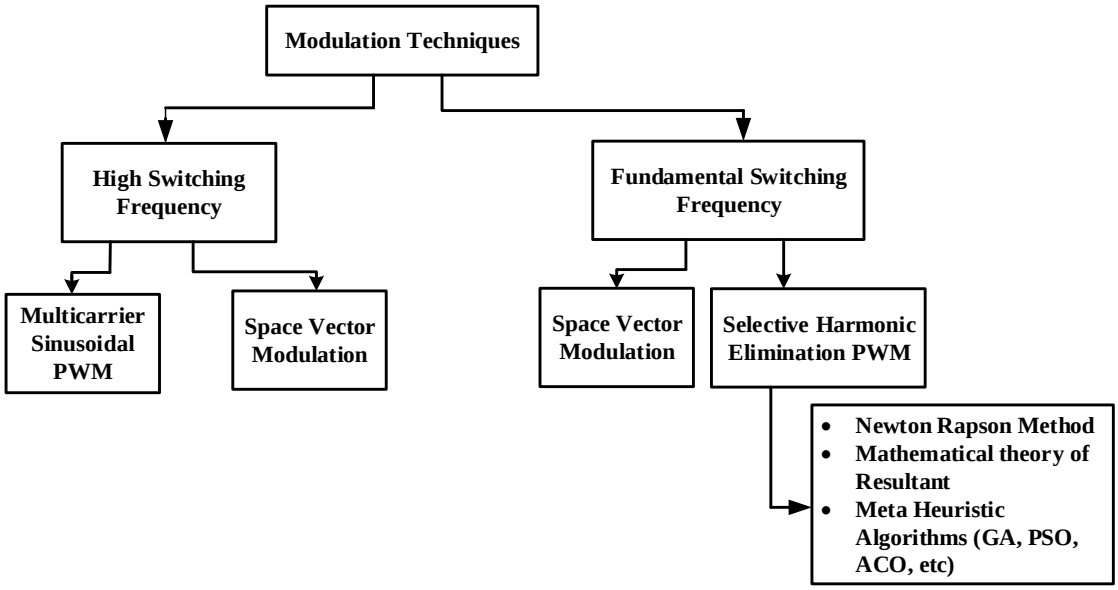
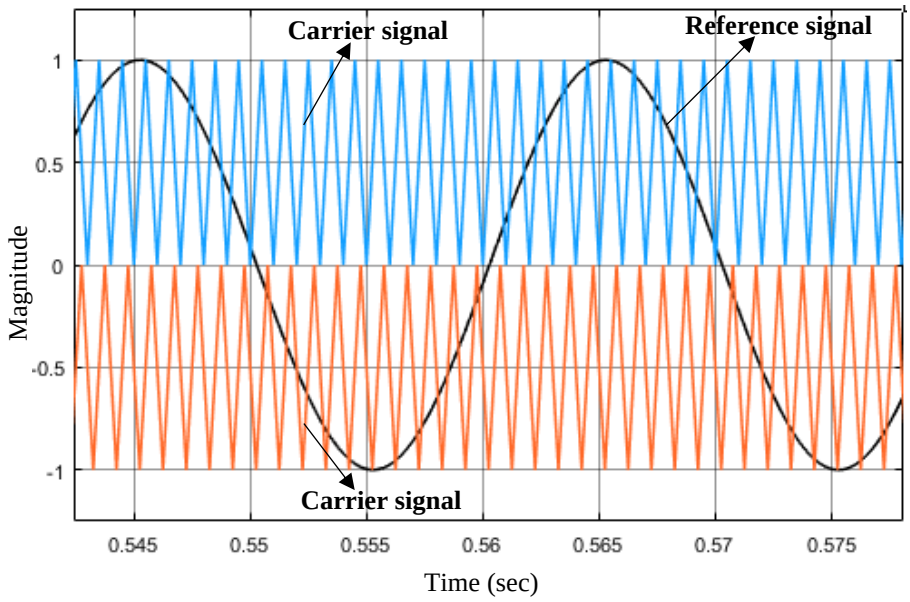


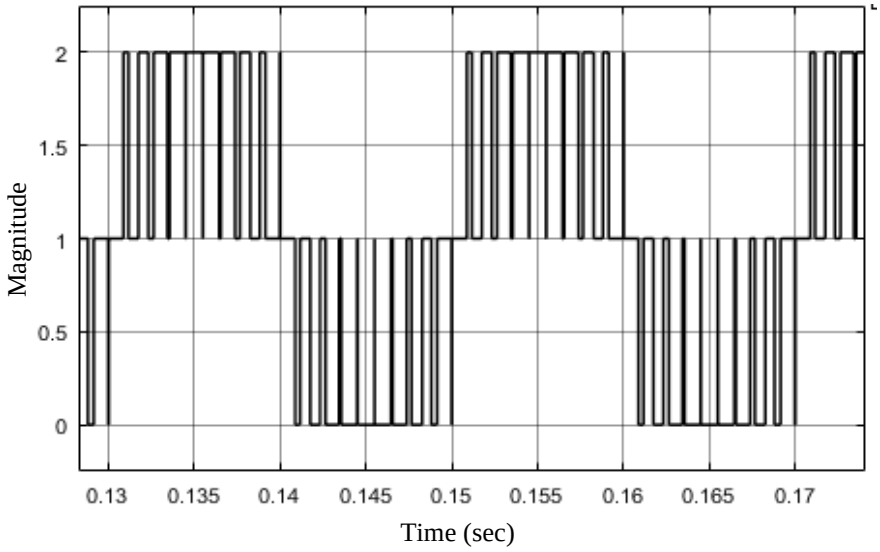
Fig. 1.11 PWM techniques for the control of MLIs.

1.3.1 Multicarrier SPWM

Different multicarrier SPWM techniques have been developed over the years to reduce the distortion in the output voltage of MLIs based on phase shifting and disposition of several carrier signals [70]-[75]. In SPWM, a reference signal is used to compare the carrier signals. If the reference signal is higher than the carrier signal, the output voltage is positive, otherwise it negative as shown in Fig. 1.12. One of the major advantages of multicarrier SPWM is that the switching frequency of the output voltage is the number of cascaded cells used times the switching frequency of each cell. Hence, the switching frequency of each cell decreases, which reduces the switching loss. However, the major limitation of multicarrier SPWM is that it cannot totally mitigate the low order dominant harmonics and thus additional filters are required at the output end of the MLIs.



(a)



(b)

Fig. 1.12 Multicarrier SPWM. (a) Reference signal and carrier signals. (b) Output voltage.

1.3.2 Space Vector Modulation PWM

SVM-PWM is one of the popular modulation techniques to regulate the output voltage of MLIs [66]. Fig. 1.13 shows basic diagram of SVM for conventional three-level MLI. In SVM-PWM, the output voltage is obtained as weighted mean of three different vectors in *d*-*q* reference frame. The reference voltage vector is generated by switching the three adjacent

voltage vectors and these vectors synthesize the required voltage vector by calculating the duty cycle of each the vectors using

$$\vec{V} = \frac{\vec{V}_J\vec{T}_J+\vec{V}_{J+1}\vec{T}_{J+1}+\vec{V}_{J+2}\vec{T}_{J+2}}{T} \quad (1.1)$$

where V_J, T_J are voltage and time vectors and T is the total time.

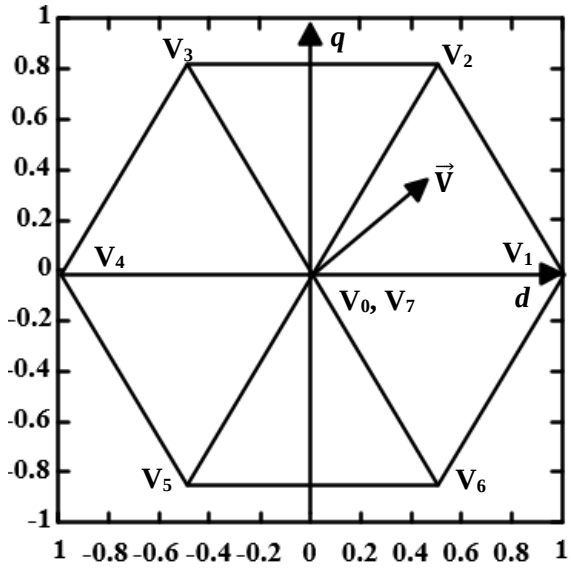


Fig. 1.13 Vector diagram of SVM-PWM [76].

Generally, SVM is relatively easy to control and flexible in improving the switching's per cycle and provides better performance in low modulation range. However, difficulty of selecting switching states increase at higher voltage levels [66]. SVM cannot also entirely eliminate the low order dominant harmonics from the output voltage of inverters.

1.3.3 Selective Harmonic Elimination PWM

In general, MLI generates quarter-wave symmetric staircase voltage waveform, synthesized by several DC voltages [77]. The generalized Fourier expression of the output voltage V_0 is given by

$$V_0 = \sum_{n=1,3,5\ldots}^{\infty} b_n \sin(n\omega t) + a_n \cos(n\omega t) \quad (1.2)$$

where b_n is the magnitude of nth harmonic component and ω is the fundamental switching frequency. Due to half and quarter wave symmetry of the output voltage, $a_n = 0$. The expression of b_n can be written as

$$b_n = \begin{cases} \frac{4V_{DC}}{n\pi}[cos(n\theta_1) + cos(n\theta_2) + \cdots\cdots + cos(n\theta_n)] & \text{for odd} \\ 0 & \text{for even} \end{cases} \quad (1.3)$$

$$0 \leq \theta_1 \leq \theta_2 \leq \theta_3 \cdots \theta_n < \frac{\pi}{2} \quad (1.4)$$

A 7-level staircase output voltage waveform using SHE-PWM is shown in Fig. 1.14. The set of non-linear transcendental equations for the output voltage waveform of a three-phase, 7-level MLI are

$$\begin{cases} m_a = \frac{1}{3}(cos(\theta_1) + cos(\theta_2) + cos(\theta_3) + cos(\theta_4) + cos\,\theta_5)) \\ 0 = cos(5\theta_1) + cos(5\theta_2) + cos(5\theta_3) + cos(5\theta_4) + cos(5\theta_5) \\ 0 = cos(7\theta_1) + cos(7\theta_2) + cos(7\theta_3) + cos(7\theta_4) + cos(7\theta_5) \end{cases} \quad (1.5)$$

where m_a is the modulation index and is defined as

$$m_a = \frac{V_{\text{desired}}}{4S\left(\frac{V_{DC}}{\pi}\right)} \quad (1.6)$$

where V_{desired} is the desired fundamental component of the output voltage and S is the number of separate DC sources.

In general, the most significant low frequency harmonics (5^{th} and 7^{th}) are eliminated by properly selecting the switching angles and high frequency harmonics are eliminated by using additional filters. The step angles of the MLI can be optimized to cancel some of the specified harmonics in SHE-PWM. The major complexity associated with SHE-PWM is that to solve nonlinear transcendental equations. Newton-Raphson theory or mathematical resultant theory are used to solve these transcendental equations [78]-[81].

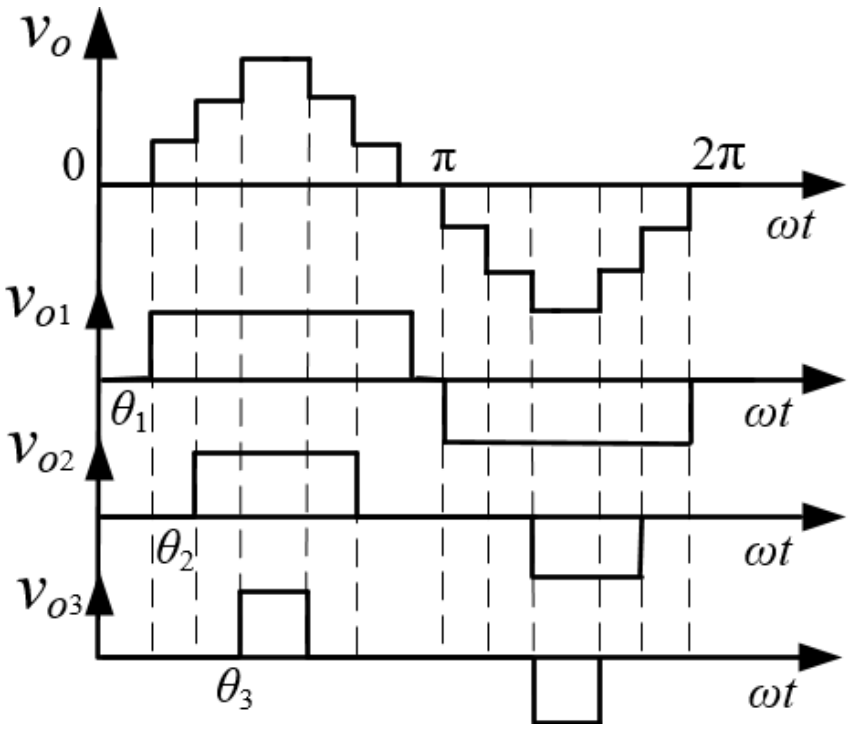


Fig. 1.14 Staircase output voltage waveform in SHE-PWM.

However, the degrees of the polynomials in those transcendental equations increase with the increase switching angles and it becomes difficult to solve them.

1.4 Meta-Heuristic Optimization Algorithms

Meta-heuristic optimization techniques become extremely popular over past a few decades for solving the aforementioned problems because they are simple, flexible, derivation free and local minima avoided [82]-[98]. These techniques are inspired by animals' behaviour and evolutionary concepts. Meta-heuristic algorithms are grouped in two main categories, evolution-based and swarm-based algorithms. Evolution-based methods are stimulated by the laws of natural evolution. Some evolution and swarm inspired optimization algorithms such as genetic algorithm (GA), particle swarm optimization (PSO), ant colony optimization (ACO), grey wolf optimization (GWO) and wolf optimization (WO) are discussed in the following sub-sections [84]-[98].

1.4.1 Genetic Algorithm

GA is an evolution-based method inspired by the process of natural selection and is widely used for finding near optimal solutions [84]-[88]. The process of evolution of species in GA is mimicked by biologically inspired mechanisms e.g. selection, crossover and mutation. The GA is derivative free and can be used for both discrete and continuous optimization. However, GA can be time consuming for large and complex problems due to its repeated fitness function evaluation. The slow, untimely convergence rate and weak local search capability are the limitations of GA. The flow chart of GA is shown in Fig. 1.15.

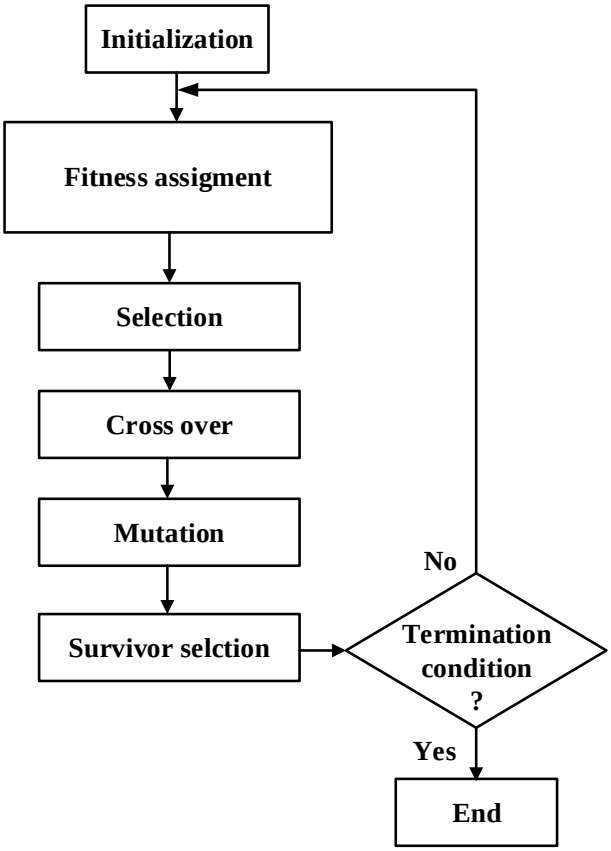


Fig. 1.15 Flow chart of GA [88].

1.4.2 Particle Swarm Optimization

PSO algorithm is inspired by social behaviour organisms such as birds or fish [89]-[94]. This method searches the optimal solution through agents, referred as particles. Every particle is

influenced by its own best position (*pbest*) and the group best position (*gbest*). The basic diagram of PSO is depicted in Fig. 1.16. PSO algorithm does not possesses any evolutionary variables such as crossover and mutation, which improves its convergence rate and local search ability. It also requires short computational time and can be used precisely to solve optimization problems. However, the primary drawback of PSO is that it cannot modify its velocity step size for fine tuning in local search, which results in premature convergence and stagnation in local optima. Also, it is difficult to define initial design parameters accurately in PSO.

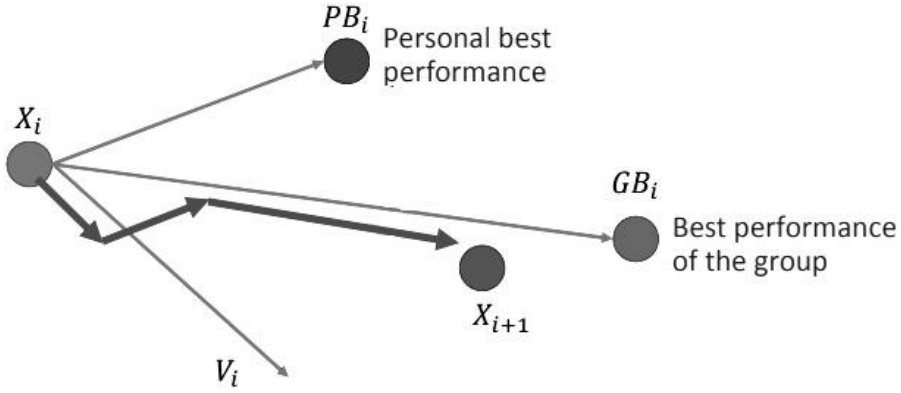


Fig. 1.16 Basic diagram of PSO [89].

1.4.3 Ant Colony Optimization

ACO algorithm is inspired by the social behaviour of ants [94]. The social intelligence of ants used for searching the closest path from the nest to the source of food, is the key inspiration ACO algorithm. A pheromone matrix is evolved over the course of iteration for finding the optimal solution in ACO algorithm. The artificial ants locate optimal solutions by moving through a parameter space, which represents all possible solutions. In ACO, ants lay down pheromones, directing each other towards the resources while exploring their environment. The simulated ants record their positions, so that in later simulation iterations more ants locate better solutions. The ACO can adapt to changes such as new distances and

guarantees the convergence probability in each iteration. However, ACO needs a difficult theoretical analysis and requires more experimentation than theoretical analysis to reach global optima. It also suffers from uncertainty in convergence rate. The flow chart of ACO is shown in Fig. 1.17.

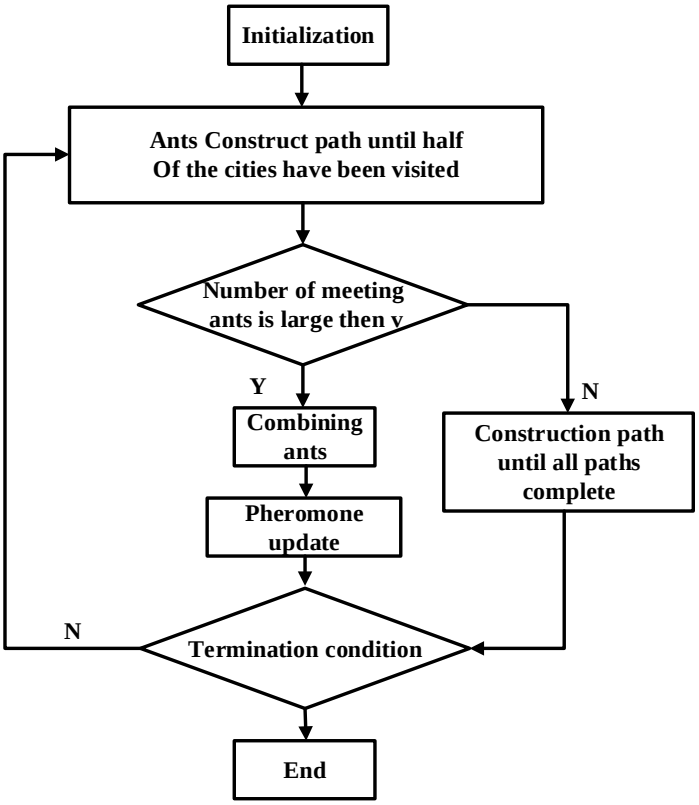


Fig. 1.17 Flow chart of ACO [85].

1.4.5 Whale Optimization

WO algorithm is swarm based meta-heuristic optimization method, which mimics the social behaviour of humpback whales. The humpback whales use a special hunting method, known as bubble-net hunting [95], [96]. Humpback whales prefer to hunt small fishes close to the surface. Hunting mechanism is done by creating bubbles along a spiral path as shown in Fig. 1.18. The humpback whales find two movements named as upward-spirals and double loops in their search mechanism. The location update in WO algorithm is divided into three phase

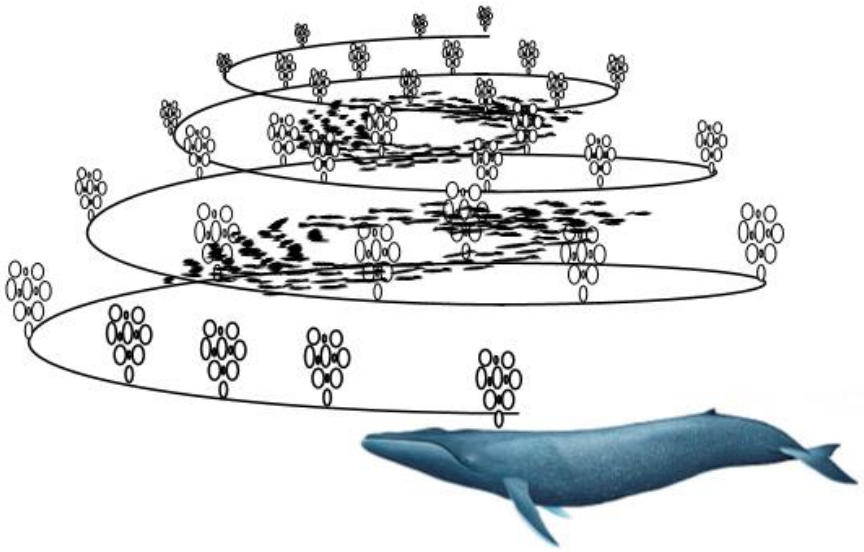


Fig. 1.18 Movement of whale [95].

such as encircling prey, spiral bubble-net feeding movement and search for prey. During the exploitation process, humpback whales adjust their positions toward the global optima using two mechanisms which are encircling the prey and spiral bubble-net feeding movement. The exploration phase deals with search for prey.

WO algorithm is simple, flexible, easy to programmed and maintains good balance between exploitation and exploration. Also, it has very few algorithm parameters. In WO, the position of the optimal design in the search space is not known earlier. This procedure of update of WO may bring about getting caught in local optima.

1.4.4 Grey Wolf Optimization

GWO algorithm is a swarm intelligent technique, which mimics the leadership hierarchy of grey wolves [97], [98]. Grey wolf belongs to canidae family and mostly prefer to live in groups. They have a strict social dominant hierarchy; the leader is a male or female, called alpha (α). The α is generally responsible for decision making. The beta (β) wolves are subordinate wolves, which help the α wolves in decision making. The β is an advisor to α

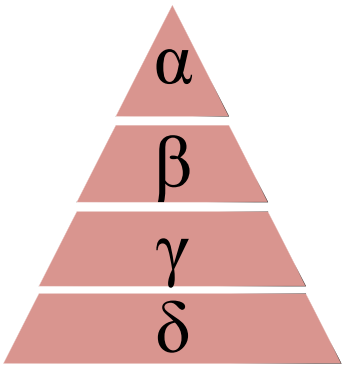


Fig. 1.19 Hierarchy diagram of GWO [97].

and maintains the discipline of the entire pack. The lower ranking grey wolf is omega (ω), which has to pass the information to all other dominant wolves. The wolves which do not fall in α, β and ω are called delta (δ). The δ wolves dominate ω and reports to α and β. The social hierarchy of wolves in GWO algorithm is shown in Fig. 1.19. The GWO algorithm has superior exploration and exploitation characteristics than other swarm intelligence techniques. Further, the GWO has been successfully applied for solving various engineering optimization problems. GWO requires only few parameters and is easy to implement, which makes it superior than earlier discussed evolutionary algorithms. However, GWO simulates internal leadership hierarchy of wolves, thus, in the searching process, the position of best solution is evaluated by using three solutions (three different wolves) instead of a single solution, which decreases the probability of premature convergence and falling into the local optima.

1.5 Objectives of Thesis

It is evident from the literature study that there is scope of further improvement with regard to MLIs in terms of harmonic content in the output voltage, number active/passive components used, PIV and TSV of devices and the cost involved in MLI configurations. The following points have been identified as the main objectives of the thesis.

- Applying optimization techniques in HC-MLI for harmonic minimization and faster convergence.
- Selecting a PWM technique for harmonic optimized HC-MLIs.
- Capacitor voltage balancing in HC-MLIs, specially at higher modulation indices using modified optimization techniques.
- Proposing SC-MLIs for active and passive components reduction and reduced TSV and PIV of devices used.

1.6 Conclusion

In this chapter, different MLI topologies such as NPC-MLI, FC-MLI, CHB-MLI, HC-MLI and SC-MLIs with their relative advantages and disadvantages are discussed in detail. For controlling the output voltage of MLIs different types of PWM schemes such as SPWM, SVM and SHE-PWM have been proposed in the literature over the years. The salient features of these PWM schemes has been critically examined and it has been found that as the number of harmonics to be eliminated increases, the degrees of the polynomials in the transcendental equations become so large that solving them becomes very difficult. This problem can be solved by meta-heuristic optimization methods such as GA, PSO, ACO, WOA, GWO, etc. Out of the different optimization methods reported in the literature PSO, WOA and GWO has been selected for further investigation in this thesis. With modifications in the algorithm of these optimization methods and subsequently applying to HC-MLI, it has been found that the performance these optimization methods can be improved in terms of convergence speed and harmonic minimization.

The balancing of capacitor voltage is an inherent challenge in HC-MLI. Several schemes have been reported for capacitor voltage balance in HC-MLIs. However, these schemes make the overall control technique complicated. The control schemes become even more complex with the increase in voltage levels, which makes the overall system expensive and bulky.

Advanced MLI topologies like SC-MLIs have emerged in recent years as a promising technology to counter these problems. In SC-MLIs, capacitor voltage is balanced inherently without using extra control circuit. However, in SC-MLIs, the number of circuit components increases with higher number of output voltage levels. Further, TSV and PIV also increase rapidly with the increase in voltage levels. In this work, two new configurations of SC-MLI, named as diode assisted switched-capacitor MLI (DASC-MLI) and reduced voltage stress switched-capacitor MLI (RVSC-MLI) have been proposed, which can generate up to 17-level output voltages using lesser number circuit components as compared to other existing SC-MLIs. The proposed SC-MLIs can generate even higher output voltage levels with lesser number of DC sources and passive components as compared to the existing SC-MLIs. The PIV of the power switches reduce in the proposed SC-MLIs in comparison to existing topologies, leading to reduction in cost of the proposed SC-MLIs.

1.7 Organization of Thesis

Apart from this chapter, the thesis consists of six more chapters. The brief description of the remaining chapters is outlined as follows:

Chapter 2 presents modified particle swarm optimization (MPSO) method for harmonic minimization in three-phase, HC-MLI using SHE-PWM. Simulation and experimentation have been carried out to exhibit the merits MPSO optimized HC-MLI as compared to GA and PSO optimized HC-MLI.

Chapter 3 represents modified whale optimization (MWO) for selective harmonic elimination in three-phase, HC-MLI so as to eliminate the lower order harmonics from the output voltage. A comparison is made among GA, PSO, WO and MWO optimized HC-MLIs through simulation and experimental studies.

Chapter 4 represents a modified grey wolf optimization (MGWO) technique through SHE-PWM for harmonic reduction in three-phase, HC-MLI. The performance of the proposed MGWO is validated through simulation and experimentation. The results obtained show that MGWO algorithm is more efficient and accurate than other reported algorithms such as GA, PSO and GWO in terms of performance, harmonic reduction and convergence rate.

Chapter 5 represents a new diode assisted switched-capacitor MLI (DASC-MLI). The proposed DASC-MLI is compared with other existing SC-MLIs to exhibits its advantages in terms of circuit components, voltage gain, TSV and cost.

Chapter 6 represents a new reduced voltage stress switched-capacitor MLI (RVSC-MLI). The proposed RVSC-MLI is compared with other existing SC-MLIs to exhibits its merits in terms of circuit components, PIV and TSV.

Chapter 7 delineates the overall conclusion of the thesis and discusses the scope of future work in this field.

Chapter 2

Harmonic Minimization in HC-MLI Using Modified Particle Swarm Optimization

2.1 Introduction

In this chapter, a modified particle swarm optimization (MPSO) for fast convergence and harmonic minimization in three-phase, 11-level hybrid cascaded multilevel inverter (HC-MLI) has been proposed [99]. Selective harmonic elimination pulse width modulation (SHE-PWM) technique implemented through MPSO has been used in the proposed work for synthesizing an 11-level output voltage using two DC sources, a pre-charged capacitor and twelve switches. The switching angles of the three-phase, 11-level HC-MLI has been computed for eliminating specified lower order odd harmonics such as 5^{th}, 7^{th}, 11^{th} and 13^{th} from the output voltage of the HC-MLI. In the proposed MPSO optimized HC-MLI, capacitor voltage balance is also ensured even at higher modulation indices by utilizing the redundant switching states available at different switching instances of the HC-MLI. The redundant switching states affects the charging and discharging sequences of the capacitors depending on the direction of the load current in the HC-MLI. Based on analytical studies, a constraint for capacitor voltage balancing has been derived. Subsequently, using this constraint in MPSO and applying a voltage averaging technique to three-phase, 11-level HC-MLI, capacitor voltage balancing has been ensured, even at higher modulation indices. The results obtained through MPSO are compared with the results obtained through genetic

algorithm (GA) and particle swarm optimization (PSO) in terms of convergence rate and harmonic content.

2.2 Hybrid Cascaded MLI

A three-phase, 11-level HC-MLI is shown in Fig. 2.1. In the Fig. 2.1; H_1, H_2 are primary and H_3 is the supplementary H-bridge cells. The H-bridges are connected in cascade and the output voltage waveform is the sum of the outputs of all the individual H-bridges. The DC voltage source V_{dc} is used in primary H-bridges (H_1 and H_2). The DC source used in the supplementary bridge (H_3) is a pre-charged capacitor, whose voltage (V_{CAP}) is kept at $V_{dc}/2$. The output voltages of H_1, H_2 and H_3 are denoted as V_1, V_2 and V_3 respectively.

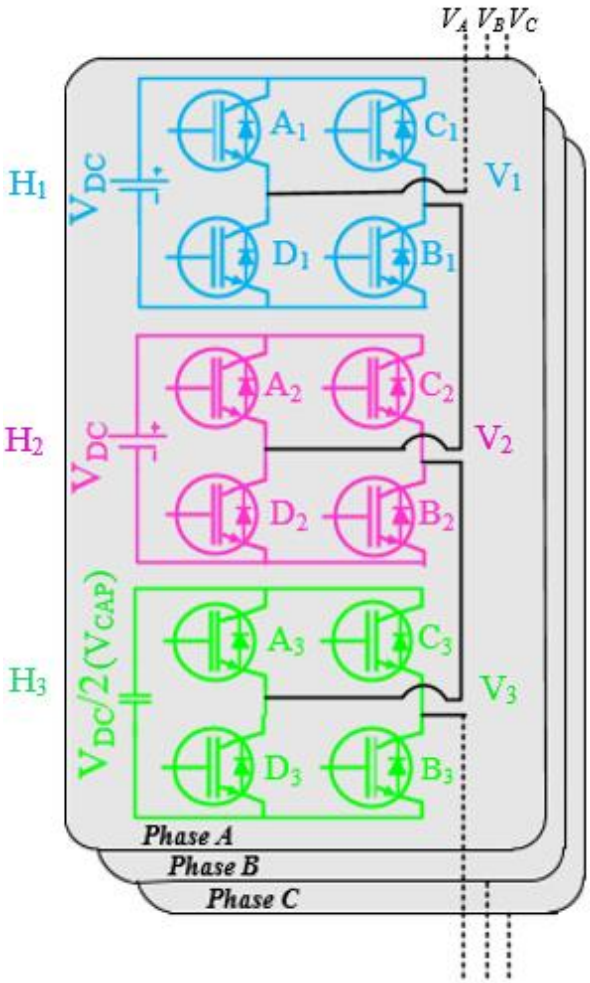


Fig. 2.1 Configuration of three-phase 11-level HC-MLI.

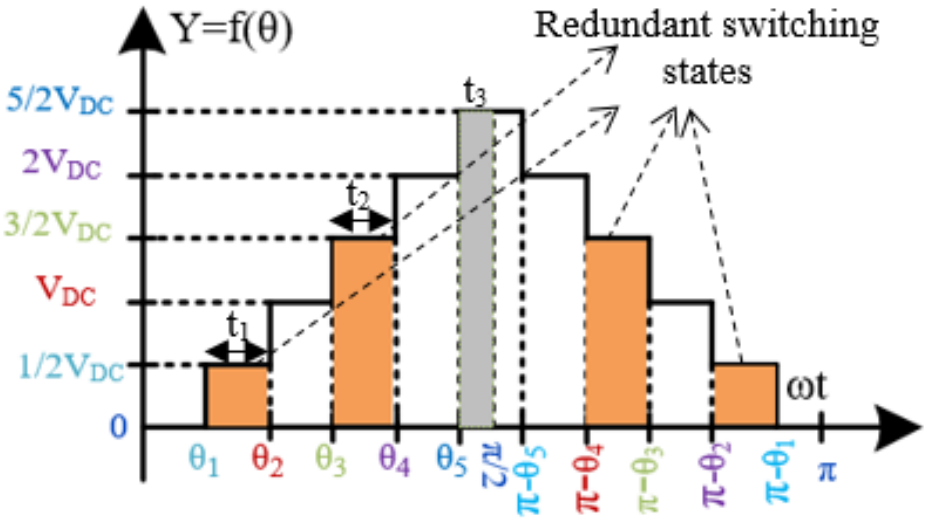


Fig. 2.2 Staircase waveform of 11-level HC-MLI.

Table 2.1
Switching States for Voltage Level Synthesis

Level	A_1	C_1	D_1	B_1	A_2	C_2	D_2	B_2	A_3	C_3	D_3	B_3	Output
	0	1	1	0	0	1	1	0	0	1	1	0	$-5V_{dc}$
	0	1	1	0	0	1	1	0	1	1	0	0	$-2V_{dc}$
	1	1	0	0	0	1	1	0	0	1	1	0	$-3V_{dc}/2$ (Redundancy1)
	0	1	1	0	1	1	0	0	0	1	1	0	$-3V_{dc}/2$ (Redundancy2)
	0	1	1	0	0	1	1	0	1	0	0	1	$-3V_{dc}/2$ (Redundancy3)
Negative	0	1	1	0	1	1	0	0	1	1	0	0	$-V_{dc}$ (Redundancy1)
	1	1	0	0	0	1	1	0	1	1	0	0	$-V_{dc}$ (Redundancy2)
	1	1	0	0	1	1	0	0	0	1	1	0	$-V_{dc}/2$ (Redundancy1)
	0	1	1	0	1	1	0	0	1	0	0	1	$-V_{dc}/2$ (Redundancy2)
	1	1	0	0	0	1	1	0	1	0	0	1	$-V_{dc}/2$ (Redundancy3)
	1	1	0	0	1	1	0	0	1	1	0	0	0
Zero	1	0	0	1	0	1	1	0	1	1	0	0	0
	0	1	1	0	1	0	0	1	1	1	0	0	0
	1	1	0	0	1	1	0	0	1	0	0	1	$+V_{dc}/2$ (Redundancy1)
	1	0	0	1	1	1	0	0	0	1	1	0	$+V_{dc}/2$ (Redundancy2)
	1	1	0	0	1	0	0	1	0	1	1	0	$+V_{dc}/2$ (Redundancy3)
	1	0	0	1	1	1	0	0	1	1	0	0	$+V_{dc}$ (Redundancy1)
	1	1	0	0	1	0	0	1	1	1	0	0	$+V_{dc}$ (Redundancy2)
Positive	1	0	0	1	1	1	0	0	1	0	0	1	$+3V_{dc}/2$ (Redundancy1)
	1	1	0	0	1	0	0	1	1	0	0	1	$+3V_{dc}/2$ (Redundancy1)
	1	0	0	1	1	0	0	1	0	1	1	0	$+3V_{dc}/2$ (Redundancy1)
	1	0	0	1	1	0	0	1	0	1	1	0	$+5V_{dc}$
	1	0	0	1	1	0	0	1	1	1	0	1	$+2V_{dc}$

The generated output voltage V_0 of the 11-level HC-MLI is obtained using combinations of V_1, V_2 and V_3 as, $V_0 = V_1 \pm V_2 \pm V_3$. Utilizing the switches of H_1, H_2 and H_3 of Fig. 2.1 appropriately, V_0 can be made $+5V_{dc}/2$, $+2V_{dc}$, $+3V_{dc}/2$, $+V_{dc}$, $+V_{dc}/2$, 0, $-5V_{dc}/2$, $-2V_{dc}$, $-3V_{dc}/2$, $-V_{dc}$ and $-V_{dc}/2$. The output voltage V_0 and the redundant switching states of the staircase waveform is shown Fig. 2.2. The switching logic for the 11-level HC-MLI is given in Table 2.1.

2.3 Solution Using PSO

PSO algorithm is an evolutionary algorithm capable of solving difficult multidimensional and multi-objective optimization problems in various fields. In PSO, particles keep searching to find the optimum solution based on the best experience of the swarm (global best, or g_{best}) by using their past experiences (personal best, or p_{best}). The particles are randomly generated initially. Each particle i (i = 1 to swarm size) possesses a current position $x_i = [x_{i1}, x_{i2} \ldots l_{id}]$ and velocity $v_i = [v_{i1}, v_{i2} \ldots v_{id}]$, where, d is the dimension of search space. The velocity of the particle indicates the change in the position from one step to the next. Every particle in search space memorizes its *pbest*, which corresponds to the best fitness value in the searching places. Every particle tries to attain the *gbest* that is the whole best place searched by one member of the swarm. Exploration is the ability of a search algorithm to explore different region of the search space in order to locate a good optimum solution. Exploitation is the ability to concentrate around a suitable search space in order to get better solution. With their exploration and exploitation, the particle of the swarm fly through the space and have two essential capabilities: the memory of their own best *pbest* position and knowledge of the global or their neighborhood's *gbest.* The basic concept behind the PSO technique is to change the velocity of each particle towards its *pbest* and *gbest* positions at every time step.

Each particle tends to modify its current position and velocity. Let *x* and *v* denotes the co-ordinates (position) and fly speed (velocity) of a particle in a search space respectively [90]-[93]. The velocity and position of each particle can be calculated using the current velocity and the distance from $pbest_{id}$ and $gbest_{id}$ as

$$V_{id}^{k+1} = wV_{id}^{k+1} + c_1 r_1 \left(pbest_{id} - X_{id}^{k}\right) + c_2 r_2 \left(gbest_{id} - X_{id}^{k}\right) \quad (2.1)$$

$$x_{id}^{k+1} = x_{id}^{k} + v_{id}^{k+1} \quad (2.2)$$

where *k*: number of iterations; *d*: number of dimensions corresponds to number of members of each particle; v_{id}^{k+1}: velocity of member *d* of particle *i* at iteration *k*+1; v_{id}^{k}: velocity of member *d* of particle *i* at iteration *k*; x_{id}^{k+1}: position of member *d* of particle *i* at iteration *k*+1; x_{id}^{k}: position of member *d* of particle *i* at iteration *k*; c_1: constant weighing factor corresponding to *pbest*; c_2: constant weighing factor corresponding to *gbest*; r_1 and r_2: random number between 0 and 1. The constants c_1 and c_2 represents the learning co-efficient (cognitive and social) that tries to attract each particle toward its *pbest* and *gbest* position. The acceleration constants c_1 and c_2 are often set to 1.8 according to past experiences. The new velocity for every particle is based on the particle's previous velocity, location of the particle at which the best fitness has been achieved so far and the population's global location at which the best fitness achieved. PSO simple to implement and have few parameters to adjust and do not overlap or mutate.

2.3.1 Limitations of PSO

PSO locates nearly optimal solution with a fast convergence speed. However, the major limitation of PSO is that it fails to adjust its velocity step size for fine tuning in the search

space. This often leads to premature convergence. Moreover, increase in number of switching angles in PSO results in increase in complexity of the search space and ultimately it is trapped in the local optima of the search domain [90]-[94]. To take care of this problem, a local search technique, named as mesh adaptive direct search (MADS) is combined with PSO to accelerate the convergence to an adjacent local optimum and refine the local search of the algorithm to prevent it being stuck in the local optima [100]. The method thus evolved is named as modified PSO (MPSO). To increase the fitness value of particles, mutation in velocity is applied in MPSO. Mutation is also applied in MPSO on the velocities of those particles that are not able to find a better position in search space. Combining the advantages of MADS and mutation strategy in MPSO obtains time-optimal solutions.

2.4 Proposed Modified PSO

In the proposed MPSO, MADS is used for local refinement of particles because of its fast convergence towards local optima. MADS has two types of grids, known as mesh and frame. The mesh is the set of conventional grids and the frame consists of mesh points. MADS has two steps at each iteration; called the search step which is done around the mesh points and the poll step which is done when there is no more improvement found by the mesh points in the search step. MADS searches optimal solution by reducing the mesh size until a better solution is achieved. When the mesh size is reduced below the accepted value, MADS finds optimal solution and terminates the iteration process [100]. The proposed algorithm starts with initialization of random particles (switching angles). After evaluating fitness of each particle, personal best (*pbest*) and global best (*gbest*) positions are updated. In case of conventional PSO, the subsequent iteration starts and new particles are estimated according to their initial position, velocities, *pbest* and *gbest* positions. In contrast to this, in MPSO, the subsequent

iteration will not start till local refinement around the best particle is achieved. The best particles of the population are taken as starting search points in MADS. Finally, MPSO locates the local minimum around each initial point. The idea of using mutation in MPSO is that, if a particle cannot improve its fitness in search domain, its future velocity will not be affected by its previous velocity. So, if n^{th} particle fails to achieve a better fitness at the end of i^{th} iteration, its velocity components $V_{nd}(i)$ are mutated. In MPSO, mutation mechanism is achieved using differential evolution (DE)/current-to-best/1 mutation strategy [101]-[103]. The magnitude of mutation is determined by past velocity, *pbest* and *gbest*. The iteration of mutation process does not terminate till better fitness of particles are found.

2.4.1 Improvement in Weighting Factor

To control the search speed of the particle, proper tuning of weight factor (w) is necessary. The balance between exploitation and exploration is maintained by w. The direction of particle in which it was moving previously is also maintained by w. This operation is advantageous at the start of the search operation, where the particles are extensively dispersed. MPSO has drawback of increasing the convergence time when the particles oscillate near *gbest* position. So, a non-linear w is more useful than linearly decreasing w. A new exponential decaying weighting factor $(w_{\exp})$, which adapts the value of w with respect to distance of the ith particle from the *gbest* position. It decays to a low value, resulting in reducing convergence time with number of iterations. The modified weight factor is given as

$$w_{i,\exp}^{k} = \left(\left(\frac{x_{gb} - x_i^k}{v_{\text{orms}}} \right) - f_1 \right) \cdot \exp\left(\frac{k_{\max}}{f_2 + k_{\max}} \right) \tag{2.3}$$

where f_1 and f_2 are controlling factors taken as 0.2 and 5 respectively, $k_{\max}$ is number of iterations and v_{orms} is the rms value of output voltage whose value depend upon modulation indices of HC-MLI.

2.4.2 Improvements in Cognitive and Social Parameters

The cognitive c_1 and social c_2 parameters are modified in this proposed algorithm as

$$c_1 = \frac{c_2 \cdot v_{\text{orms}}}{\left| d_{\text{lbest}} - d_{\text{gbest}} \right| + 1} \tag{2.4}$$

$$c_2(k) = c_{2,\min} + \frac{k}{k_{\max}}(c_{2,\max} - c_{2,\min}) \tag{2.5}$$

where d_{lbest} and d_{gbest} are the local best and global best positions of the particle, v_{orms} is the rms output voltage of inverter, $c_{2,\max}$, and $c_{2,\min}$ are the maximum and minimum values of social parameter.

The values of $c_{2,\min}$ and $c_{2,\max}$ lie between 0.1 to 2 respectively. The cognitive parameter c_1 and social parameter c_2 are used to calculate velocity of each particle in MPSO algorithm. The cognitive parameter c_1 helps the particles to explore the search space, while the social parameter c_2 helps the particles to exploit the search space. The expression of c_1 has been proposed in this work which decreases linearly in each iteration. This helps the particles to escape any local minima. This adaptive nature of cognitive parameter ensures faster convergence of the algorithm towards the global best.

The modified velocity expression utilizing the modified weight factor and cognitive factor as follows

$$V_{id}^{k+1} = w_{i\exp}^{k} \cdot V_{id}^{k} + c_1 r_1 (x_{lb\_i} - x_{id}^{k}) + c_2 r_2 (x_{gb\_i} - x_{id}^{k}) \tag{2.6}$$

$$x_{id}^{k+1} = x_{id}^{k} + v_{id}^{k+1} \tag{2.7}$$

where k is the pointer of iterations, d is the position number of D-dimensions, V_{id}^{k+1} is the velocity particle of i at $(k+1)^{\text{th}}$ iteration, V_{id}^{k} is the velocity of particle i at k^{th} iteration, x_{id}^{k+1} is

the position of particle *i* at $(k+1)^{th}$ iteration, x_{id}^{k} is the position of particle *i* at k^{th} iteration, c_1 is the cognitive parameter corresponding to *pbest*, c_2 is the social factor corresponding to *gbest* and $r_1, r_2 \in R(0,1)$.

2.4.3 Mutation in Velocity Using DE/best/1 Mutation Strategy

The list of procedures for mutation in velocity are as follows:

Step1: Initialization

Generate V_P, initial particle's velocity vectors and $vel_g = \{v_{1g}, v_{1g} \cdot v_{N_P,g}\}$, which denotes population of velocity vector. It consists of number of target velocity particles. Each particle in velocity vector, $v_{ig} = (v_{i,1,g}, v_{i,2,g} \cdots v_{i,\mathrm{D},g})$ is a *D*-dimensional vector. A mutant vector is generated using mutation operator for each target vector v_{ig} .

Step 2: Mutation in Velocity Vector

Two different particles (v_{r1}, v_{r2}) are chosen from population. The best velocity vector is obtained by sorting the generated population vector according to their fitness value. The mutant vector is generated as follows

$$vel_{i,g}(mut) = v_{pbest,g} + f \cdot (v_{r1,g} - v_{r2,g}) \tag{2.8}$$

where $v_{pbest,g}$ best velocity particle in the population and *f* is the DE scaling factor lies between 0 to 1.

2.4.4 Velocity Limits

The velocity operator updates the position of the particle which depends on the distance from the *gbest* to *lbest* position. If the distance between *gbest* and *lbest* is less, the velocity changes

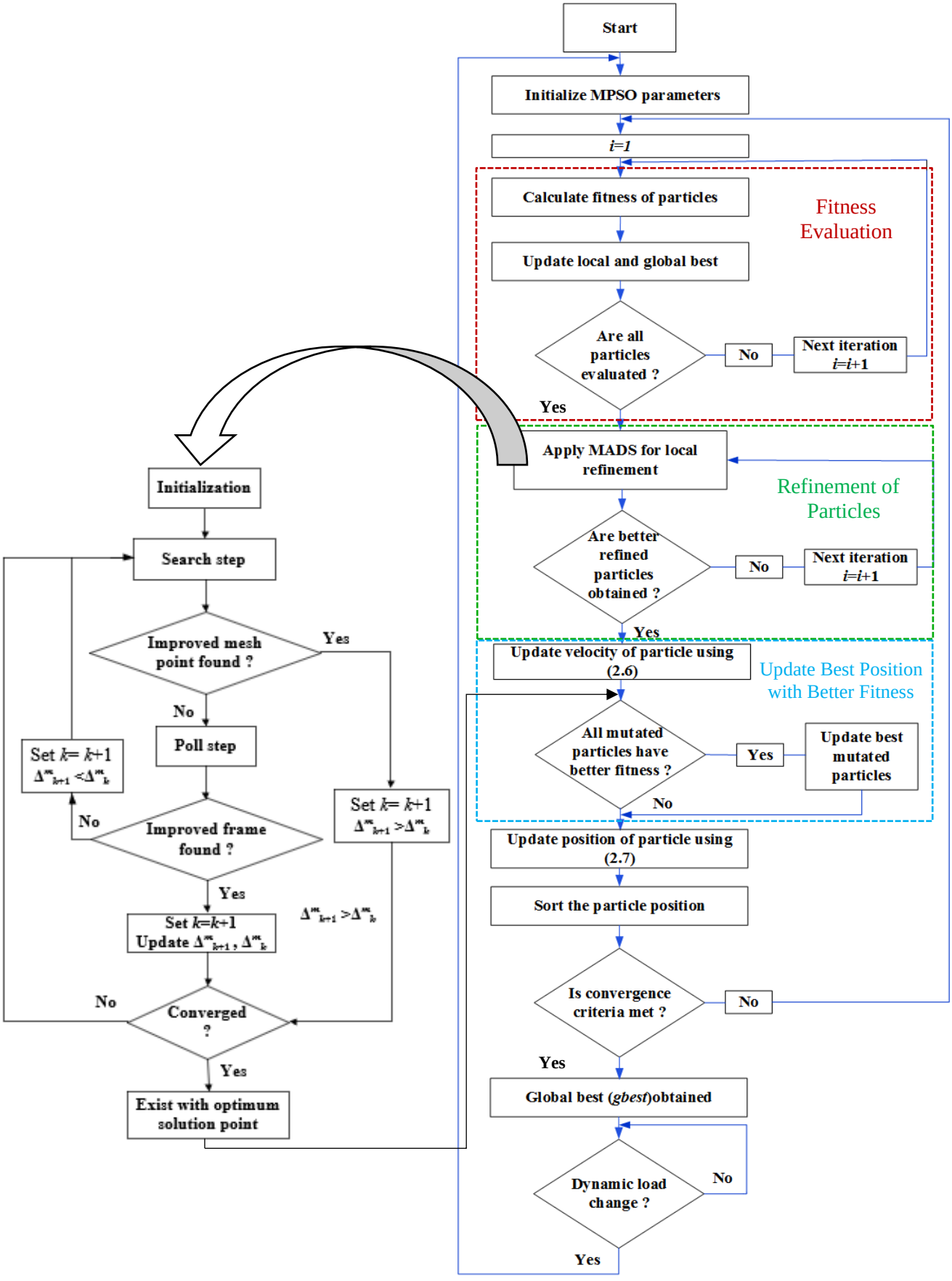


Fig. 2.3 Flow chart of MPSO.

is small, and if they are large, the corresponding velocity is large. This creates interruption in algorithm for detecting the global position. The solution to this problem is to limit the velocity up to certain maximum value, such that $\left[-\Delta v_{\max}, \Delta v_{\max}\right]$. In case of violation of these limits, the closest point to the boundary is selected. The flowchart of the complete algorithm is shown in Fig. 2.3.

The algorithm for solving the harmonics optimization problem is as follows:

Step 1: Generate initial population with randomly generated particles.

Step 2: Evaluate fitness values of all particle in the population and discard the particles those have same fitness value.

Step 3: If the fitness is better than the best fitness value, i.e., *lbest*, set current value as the new *lbest*. The particle with the best fitness value among all the particles is chosen as the *gbest*.

Step 4: Apply MADS for local refinement of particles.

Step 5: Adjust particle position and velocity.

Step 6: The global maximum value changes during dynamic loading conditions. In such a case, the particles are reinitialized to search the new global maximum again.

Step 7: Go to step 2, until the termination condition is met.

2.5 SHE-PWM Applied to MPSO Optimized HC-MLI

The mathematical representation of proper fitness function *f* is defined as

$$f = \min\left\{\left(100\frac{V_1^* - V_1}{V_1^*}\right)^4 + \sum_{s=4}^{S}\frac{1}{h_s}\left(50\frac{V_{h_s}}{V_1}\right)^2\right\} \tag{2.9}$$

subjected to

$$0 \le \theta_1 \le \theta_2 \le \theta_3 \cdots \theta_n < \frac{\pi}{2} \tag{2.10}$$

where V_1^* is the desired fundamental component and h_s is the order of s^{th} harmonic e.g., h_2 =5, h_3 = 7, h_4=11 and h_5=13. The weighting factors specify the reduction of lower harmonics. The fitness function signifies THD minimization. The population size and number of iterations are taken as 100 and 300 respectively. The iteration is started with the initialization of particles (switching angles) and then the fitness value of each particle is evaluated. In MPSO, local refinement of particles is achieved using MADS and particles with more precise value are taken. Mutation is applied to the velocity of particles to obtain better fitness value. The above process is repeated for different modulation indices until last iteration is achieved. Fig. 2.4 shows the optimal switching angles versus modulation index (m_a) for MPSO optimized HC-MLI to eliminate lower order harmonics using SHE-PWM. It can be noticed that switching angles decrease by increasing the modulation indices. Fig. 2.5 shows the content of lower order harmonics (5^{th}, 7^{th}, 11^{th} and 13^{th}) versus modulation indices using the proposed MPSO algorithm. It clearly shows that the lower-order harmonics have decreased significantly.

To verify the effectiveness of the proposed algorithm, cumulative distribution function (CDF) is determined for the proposed MPSO and compared with PSO and GA at different fitness function values as shown in Fig. 2.6 [104], [105]. The results obtained establishes the superiority of MPSO in terms of convergence rate as compared to PSO and GA. Table 2.2 gives the comparison of convergence rate and fitness values of different algorithms. It can be noticed that the convergence rate and fitness value of MPSO is better than GA and PSO.

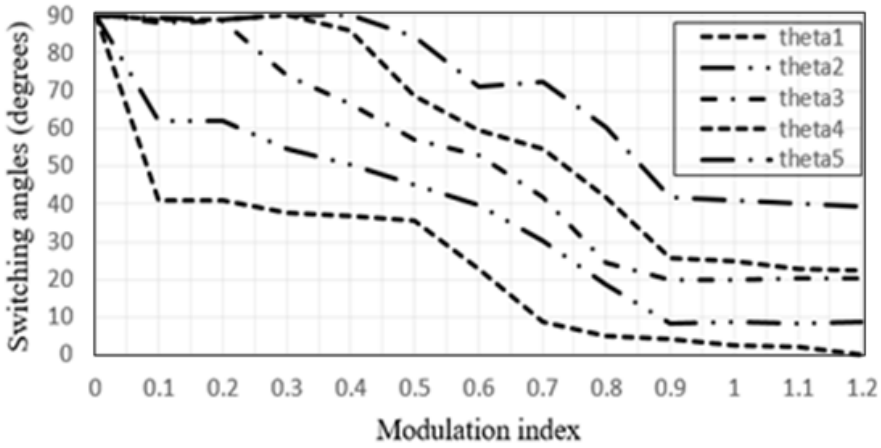


Fig. 2.4 Switching angles for different modulation indices.

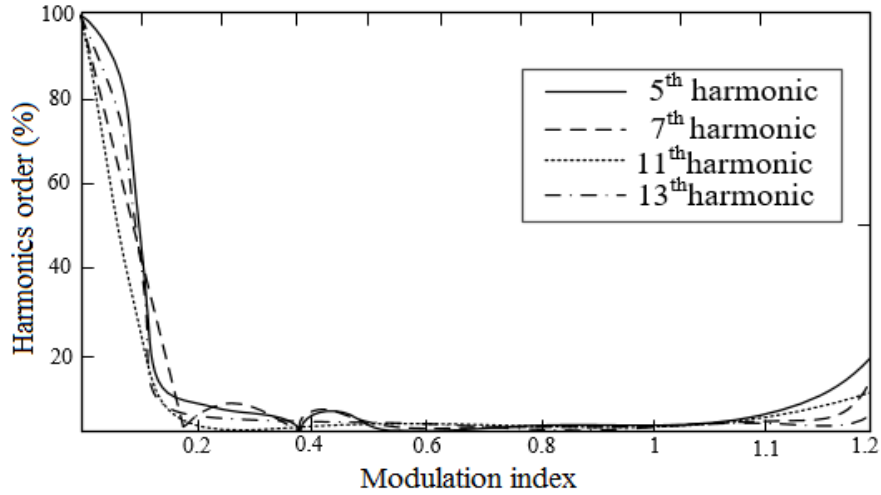


Fig. 2.5 The 5^{th},7^{th},11^{th} and 13^{th} harmonics versus modulation indices.

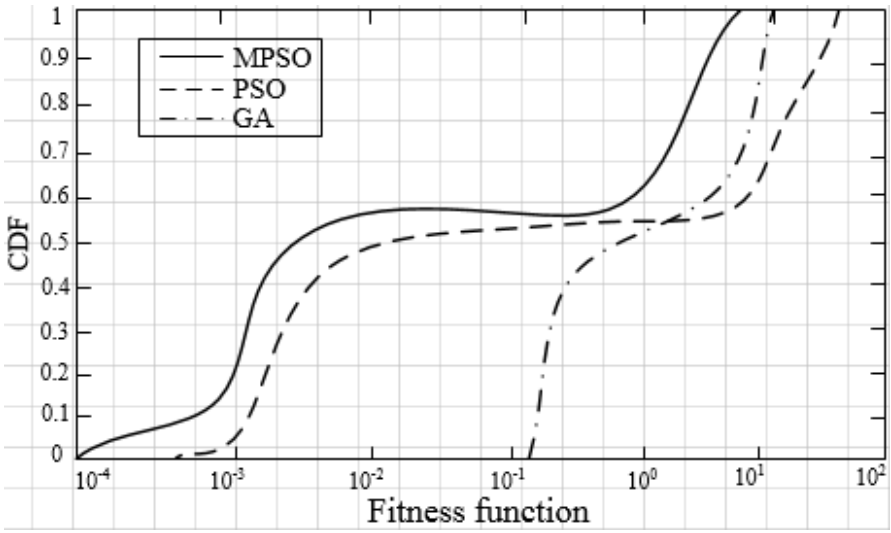


Fig. 2.6 Comparison of convergence rate between GA, PSO and MPSO.

Table 2.2
Constraints of MPSO, PSO and GA
Population size =100 and No. of Iteration=300

Parameters	MPSO	PSO	GA
Fitness value	$6.05X10^{-13}$	$1.15X10^{-03}$	0.4670
Convergence rate towards global minima	very high	high	low

Table 2.3
%THD Comparison for Different Algorithms

Modulation index	%THD (MPSO)	%THD (PSO)	%THD (GA)
0.5	8.41	10.27	13.87
0.6	7.53	9.21	12.35
0.7	7.69	9.73	12.86
0.8	5.23	7.42	11.32
0.9	4.17	6.05	10.85
1	5.03	7.09	9.87
1.1	5.64	7.71	8.05
1.2	6.21	8.03	9.31

%THD at different modulation indices are calculated for MPSO, PSO, and GA as given in Table 2.3. The result shows that for MPSO, the %THD is less as compared to GA and PSO.

2.6 Capacitor Voltage Balancing in HC-MLI Through MPSO

For proper operation of 11-level HC-MLI, the capacitor voltage has to be balanced over the entire cycle. The essential condition for capacitor voltage balance is to ensure that the net charge stored in the capacitor during the entire cycle must be greater than zero. If the net charge stored in the capacitor during the entire cycle is less than zero, the capacitor voltage falls, which leads to depletion of subsequent voltage levels [32], [33]. An optimal control strategy ensures that the net charge stored in the entire cycle should be greater than zero to

keep the average capacitor voltage constant. Different redundant switching states of the three-phase, 11-level HC-MLI are used for capacitor voltage balancing, depending on the direction of load current and sensed capacitor voltage. This is done as per the time interval of the staircase waveform and the available redundancies for that level. For obtaining the required voltage level, the capacitor voltage is used either in addition or in opposition with dc voltage sources. In one cycle, the net amount of stored charge is given as

$$Q_{stored} = Q_{charging} - Q_{discharging} \tag{2.11}$$

Applying fundamental switching to the 11-level HC-MLI and assuming the power factor angle to be Φ, load current is

$$I_{load} = I \sin(\theta - \Phi) \tag{2.12}$$

Capacitor charge balance condition for the MPSO optimized 11 HC-MLI is contented for a quarter cycle as

$$Q_{stored} = \pm \int_{\theta 1}^{\theta 2} I \sin(\theta - \Phi)\, d\theta \pm \int_{\theta 3}^{\theta 4} I \sin(\theta - \Phi)\, d\theta - \int_{\theta 5}^{\pi/2} I \sin(\theta - \Phi)\, d\theta \geq 0 \tag{2.13}$$

The ± sign in the period θ_1 to θ_2 and θ_3 to θ_4 indicates that there are both charging and discharging conditions.

2.6.1 Capacitor Voltage Balancing Conditions

The charging and discharging patterns of capacitor voltage are repeated in every quarter cycle. The first quarter cycle is divided into six intervals as shown in Fig. 2.2. Conditional switching states for capacitor voltage is given in Table 2.4. The voltage level of the capacitor

is investigated in each of the six intervals. The six intervals in one quarter cycle are as follows:

Interval 1: 0 to θ_1

No charging or discharging occurs in this interval.

Interval 2: θ_1 to θ_2

The capacitor charges or discharges in this interval. Fig. 2.7(a) and (b) shows charging interval for positive and negative load currents (I_{load}). Similarly, Fig. 2.7(c) and (d) shows discharging interval for positive and negative load currents. Considering charging interval for positive load current, the switches A_1, C_1 (of H_1), switches A_2, B_2 (of H_2) and switches C_3, D_3 (of H_3) are operated. The capacitor voltage is given by

$$V_c = (2V_{dc} - \frac{V_{dc}}{2} e^{-\frac{t_1}{\tau}}) \tag{2.14}$$

where $\tau = RC$ is the time constant. The capacitor voltage increment in this interval is given as

$$\Delta V_{C1} = \frac{V_{dc}}{2}(1 - e^{-\frac{t_1}{\tau}}) \tag{2.15}$$

Expanding the exponential term of (2.15) and considering that the capacitor used in H_3 is a large capacitor, the changes in the capacitor voltage is given as

$$\Delta V_{C1} = \frac{V_{dc}}{2} \cdot \frac{t_1}{\tau} \tag{2.16}$$

Substituting $t_1 = \frac{\theta_2 - \theta_1}{\omega}$ in (2.16)

$$\Delta V_{C1} = \frac{V_{dc}}{2} \cdot \frac{\theta_2 - \theta_1}{\omega\tau} \tag{2.17}$$

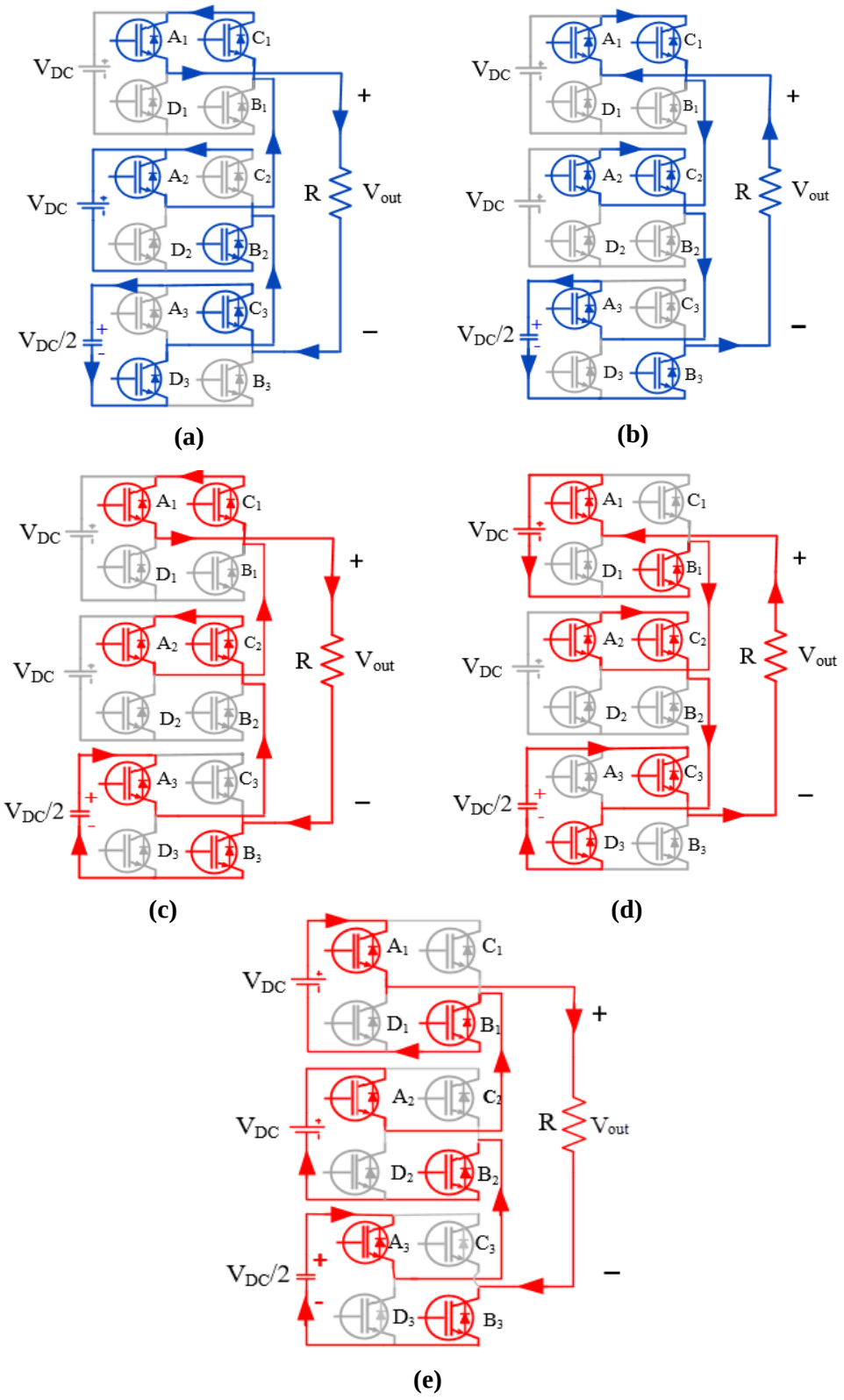


Fig. 2.7 Capacitor voltage balancing conditions.
Charging interval I_{load}>0. (b) Charging interval I_{load}<0. (c) Discharging interval I_{load}>0. (d) Discharging interval I_{load}<0. (e) Discharging interval (t_3) of peak voltage.

Table 2.4
Conditional Switching States for Capacitor Voltage Balance

Angles	Level	$V_{cap} > V_{dc}$		$V_{cap} < V_{dc}$	
		$I_{load}>0$	$I_{load}<0$	$I_{load}>0$	$I_{load}<0$
$0 \le \theta < \theta_1$	0	-	-	-	-
$\theta_1 \le \theta < \theta_2$	$V_{dc}/2$	Redundancy 1	Redundancy 2/3	Redundancy 2/3	Redundancy 1
$\theta_2 \le \theta < \theta_3$	V_{dc}	Redundancy 1/2	Redundancy 1/2	Redundancy 1/2	Redundancy 1/2
$\theta_3 \le \theta < \theta_4$	$3V_{dc}/2$	Redundancy 1/2	Redundancy 3	Redundancy 3	Redundancy 1/2
$\theta_4 \le \theta < \theta_5$	$2V_{dc}/2$	-	-	-	-
$\theta_5 \le \theta < 90$	$5V_{dc}/2$	-	-	-	-
$90 \le \theta < 180 - \theta_5$	$5V_{dc}/2$	-	-	-	-
$180 - \theta_5 \le 180 - \theta_4$	$2V_{dc}/2$	-	-	-	-
$180 - \theta_4 \le 180 - \theta_3$	$3V_{dc}/2$	Redundancy 1/2	Redundancy 3	Redundancy 3	Redundancy 1/2
$180 - \theta_3 \le 180 - \theta_2$	$V_{dc}/2$	Redundancy 1/2	Redundancy 1/2	Redundancy 1/2	Redundancy 1/2
$180 - \theta_2 \le 180 - \theta_1$	$V_{dc}/2$	Redundancy 1	Redundancy 2/3	Redundancy 2/3	Redundancy 1
$180 - \theta_1 \le 180$	0	-	-	-	-

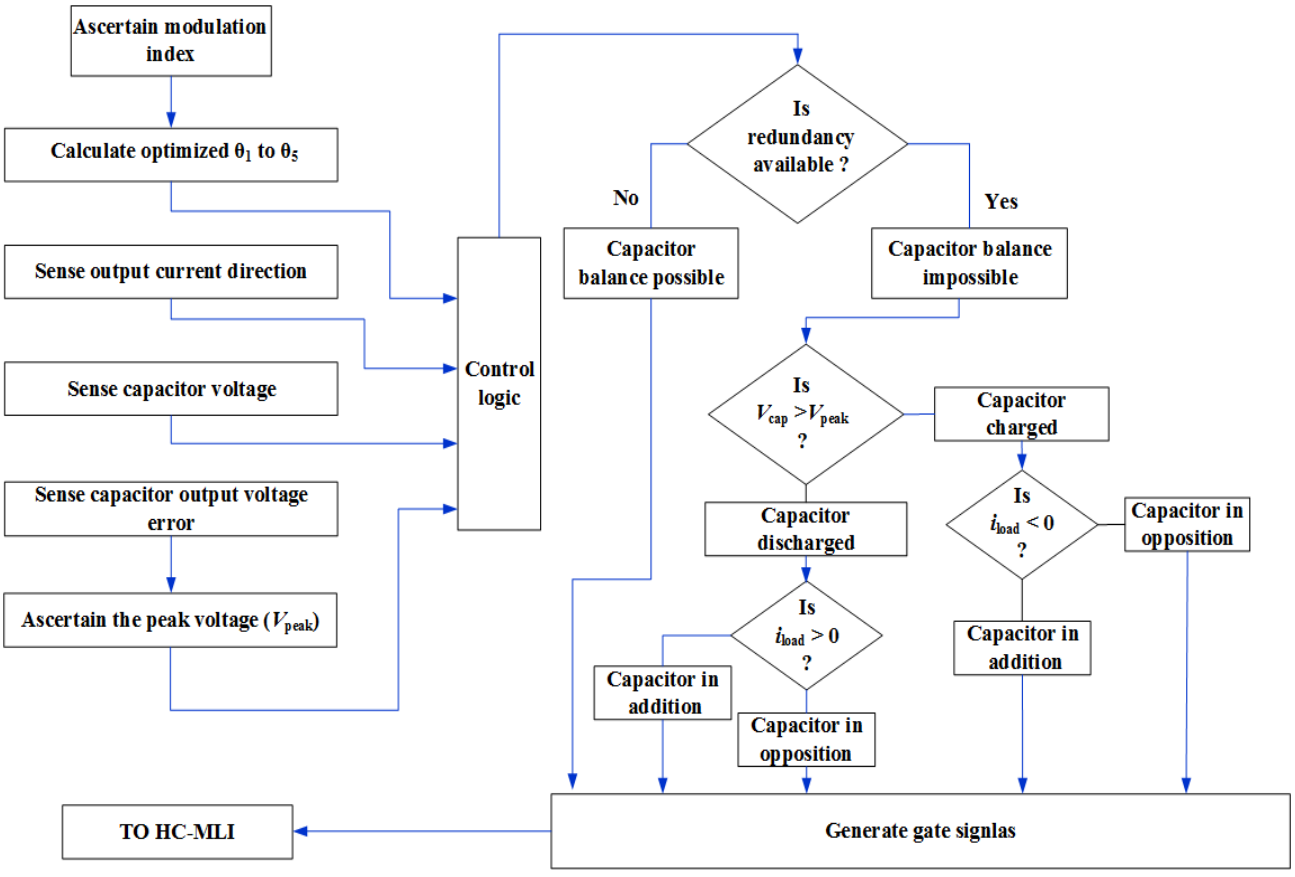


Fig. 2.8 Flow chart of control algorithm.

Interval 3: θ_2 to θ_3

No charging or discharging occurs in this interval.

Interval 4: θ_3 to θ_4

The capacitor charges or discharges in this interval. The changes in the capacitor voltage in this interval is given as

$$\Delta V_{C2} = \frac{V_{dc}}{2} \cdot \frac{t_2}{\tau} \tag{2.18}$$

Substituting $t_2 = \frac{\theta_4 - \theta_3}{\omega}$ in (2.18),

$$\Delta V_{C2} = \frac{V_{dc}}{2} \cdot \frac{\theta_4 - \theta_3}{w\tau} \tag{2.19}$$

Interval 5: θ_4 to θ_5

No charging or discharging occurs in this interval.

Interval 6: θ_5 to $\frac{\pi}{2}$

The capacitor must be discharged by the load current in this interval. Fig. 2.7(e) shows the discharging interval of the capacitor. The switches A_1, B_1 (of H_1), switches A_2, B_2 (of H_2) and switches A_3, B_3 (of H_3) are operated for discharging interval. The capacitor voltage increment in this interval is given as

$$\Delta V_{c3} = -(\frac{5V_{dc}}{2} + \Delta V_{C1} + \Delta V_{C2})(1 - e^{-\frac{t_3}{\tau}}) \tag{2.20}$$

Since the capacitor used in the third H-bridge cell is a large capacitor, using (2.17) and (2.19) in (2.20), the following is obtained

$$\Delta V_{C3} = -5\frac{V_{dc}}{2} \cdot (1 - e^{-\frac{t_3}{\tau}}) \simeq -5\frac{V_{dc}}{2} \cdot \frac{t_3}{\tau} \tag{2.21}$$

Substituting $t_3 = \dfrac{\frac{\pi}{2} - \theta_5}{\omega}$ in (2.21),

$$\Delta V_{C3} = -5\frac{V_{dc}}{2} \cdot \frac{\frac{\pi}{2} - \theta_5}{\omega\tau} \tag{2.22}$$

The capacitor voltage increment during the charging intervals should be more than the voltage decrement during the discharging interval to ensure capacitor voltage balancing. During the interval θ_1 to θ_2, the capacitor charges or discharges. It is assumed that the output voltage is constant in this interval. The capacitor current in this interval is given as

$$I_{C1} = \frac{V_{dc}}{2R} \tag{2.23}$$

where R is output resistance. Increment in the capacitor charge in this interval can be expressed as

$$\Delta Q_1 = \frac{V_{dc}}{2R} \cdot \frac{\theta_2 - \theta_1}{\omega} \tag{2.24}$$

During the interval θ_3 to θ_4, the capacitor charges or discharges. It is assumed that the output voltage is constant in this interval. The capacitor current in this interval given as

$$I_{C2} = \frac{V_{dc}}{2R} \tag{2.25}$$

Changes in the capacitor charge in this interval (θ_3 to θ_4) is given as

$$\Delta Q_2 = \frac{V_{dc}}{2R} \cdot \frac{\theta_4 - \theta_3}{\omega} \tag{2.26}$$

During the interval θ_5 to $\frac{\pi}{2}$, the capacitor discharges. The capacitor current is opposite to the load current in this interval and is given as

$$I_{C3} = -\frac{5V_{dc}}{2R} \tag{2.27}$$

Changes in the capacitor charge in this interval is given as

$$\Delta Q_3 = -\frac{5V_{dc}}{2R} \cdot \frac{\frac{\pi}{2} - \theta_5}{\omega} \tag{2.28}$$

The capacitor voltage can be balanced if the net charge stored in quarter cycle of operation is greater than zero. In other words, the balancing of capacitor voltage is possible if

$$\Delta Q_1 + \Delta Q_2 + \Delta Q_3 > 0 \tag{2.29}$$

Using (2.24), (2.26) and (2.28) in (2.29),

$$\frac{V_{dc}}{2R} \cdot \frac{\theta_2 - \theta_1}{\omega} + \frac{V_{dc}}{2R} \cdot \frac{\theta_4 - \theta_3}{\omega} - \frac{5V_{dc}}{2R} \cdot \frac{\frac{\pi}{2} - \theta_5}{\omega} > 0 \tag{2.30}$$

(2.30) can be simplified as

$$\theta_2 + \theta_4 + 5\theta_5 - (\theta_1 + \theta_3) > \frac{5\pi}{2} \tag{2.31}$$

For capacitor voltage balancing, (2.31) is to be satisfied. The modulation indices are obtained by using the constraint presented in (2.31) to ensure capacitor voltage balancing. Using the redundancies of 11-level HC-MLI, the conditional switching states for capacitor voltage balancing is given in Table 2.4. If $V_{CAP} < V_{dc}/2$, the capacitor has to be charged and if $V_{CAP} > V_{dc}/2$, the capacitor has to be discharged depending on the available redundancies. As the steady state error in the capacitor voltage decreases in subsequent voltage levels, capacitor voltage averaging technique is used to reduce the steady state error by charging the capacitor to a value slightly higher than $V_{dc}/2$ during allowable periods. The average DC voltage of the capacitor is compared with the reference voltage value ($V_{dc}/2$) and then the optimum gate signals for the proposed three-phase HC-MLI are generated. The flow chart of the control algorithm for capacitor voltage balance is shown in Fig. 2.8.

2.6.2 Capacitor Voltage Balancing at Higher Modulation Indices

The capacitor charge is unable to balance at higher modulation indices ($m_a > 0.9$) because of long discharging periods at voltage peaks. At a higher modulation index, discharging period is more than the charging period for which net charge accumulation in capacitor is less than zero [32]. To balance charge at higher modulation indices, third harmonic voltage is injected into the output voltage of HC-MLI through a square wave having frequency three times the fundamental frequency with magnitude $V_{dc}/2$ as shown in Fig. 2.9. Fig. 2.9(a) shows original 11-level voltage waveform. Fig. 2.9(b) shows injected third harmonic voltage and Fig. 2.9(c) shows final output voltage waveform. The Fourier series expression of the injected third harmonic voltage can be written as:

$$V_{(\omega t)} = \sum_{1,3,5..n}^{\infty} \frac{2V_{dc}}{n\pi} \cos n\theta_3 \cdot \sin 3n\omega t \qquad (2.32)$$

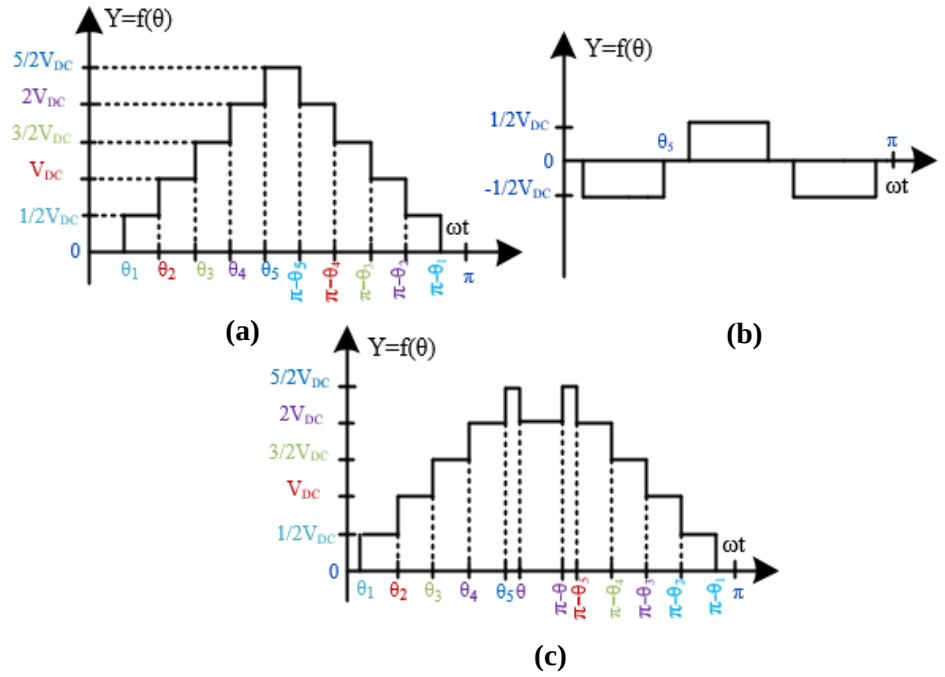


Fig. 2.9 Capacitor voltage balancing at higher modulation index for 11-level HC-MLI. (a) Original 11-level waveform. (b) Injected 3rd harmonic voltage. (c) Final voltage waveform.

The triplen-harmonic voltages will automatically cancel in the line-line voltages of three-phase systems, and will not change the fundamental frequency contents. The only effect is to change the charging period and discharging period. The condition of capacitor voltage balancing for the elven level HC-MLI in a quarter cycle operation at higher modulation index is given as:

$$Q_{stored} = \pm \int_{\theta_1}^{\theta_2} I \sin(\theta - \Phi)\ d\theta\ \pm \int_{\theta_3}^{\theta_4} I \sin(\theta - \Phi)\ d\theta\ - \int_{\theta_5}^{\theta} I \sin(\theta - \Phi)\ d\theta - \int_{\pi-\theta}^{\pi-\theta_5} I \sin(\theta - \Phi)\ d\theta \geq 0 \tag{2.33}$$

2.7 Closed-loop control of HC-MLI Using Proposed Algorithm

In the closed-loop operation of the HC-MLI, the controller generates optimized gate signals in such a way that the AC bus voltage (V_{AC}) is regulated to the reference value V_{AC}^{*}. The analog to digital converter (ADC) of DSP converts the analog signals (V_{CAP}, V_{AC}, V_{DC}) and

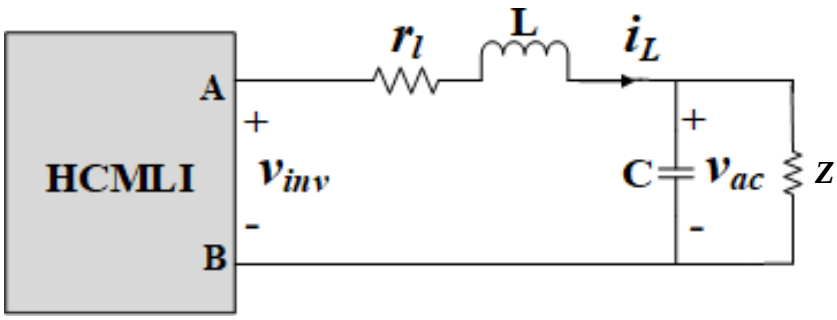


Fig. 2.10 Equivalent circuit of HC-MLI feeding an AC load (r_l: DC series resistance of the inductor L, R: impedance of load).

i_{AC}) into digital domain by sensing the feedback signals of HC-MLI. These feedback signals along with the reference signals and DC capacitor voltage are given as inputs to the controller blocks. The controller has two different control loops for controlling the capacitor voltage (V_{CAP}) and output voltage (V_{AC}). The AC output controller is designed using synchronous

reference control (SRF) method [106]-[108]. The outer voltage loop generates reference current I_L^* for the inner current loop and the inner current loop generates the gate signals.

2.7.1 Voltage Controller

The equivalent circuit of HC-MLI feeding a resistive load is shown in Fig. 2.10. The three-phase HC-MLI can be represented as

$$\frac{di_x}{dt} = -\frac{r_x}{L} + \frac{1}{L}(\mathrm{V}_{inv} - V_{ox}); x = a, b, c \tag{2.34}$$

$$\frac{dV_{ox}}{dt} = \frac{1}{C} i_{lx} - \frac{V_{ox}}{Z.C}; x = a,\ b,\ c \tag{2.35}$$

The variables *a*, *b*, *c* in three-phase stationary coordinates are transformed into rotating *d*-*q* coordinates as

$$\frac{d}{dt}\begin{bmatrix} I_d \\ I_q \end{bmatrix} = \begin{bmatrix} -\frac{r_l}{L} & \omega \\ -\omega & \frac{-r_l}{L} \end{bmatrix} \cdot \begin{bmatrix} I_d \\ I_q \end{bmatrix} + \frac{1}{L} \cdot \begin{bmatrix} V_{invd} - V_d \\ V_{invq} - V_q \end{bmatrix} \tag{2.36}$$

$$\frac{d}{dt}\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} -\frac{1}{RC} & \omega \\ -\omega & -\frac{1}{ZC} \end{bmatrix} \cdot \begin{bmatrix} V_d \\ V_q \end{bmatrix} + \frac{1}{C} \cdot \begin{bmatrix} I_d \\ I_q \end{bmatrix} \tag{2.37}$$

The output transfer functions of inner current control loop and outer voltage control loop are obtained by transforming (2.36) and (2.37) into *s* domain as

$$\begin{cases} \dfrac{I_d(S)}{U_{id}(S)} = \dfrac{I_q(S)}{U_{iq}(S)} = \dfrac{1}{sL + r_l} \\ \dfrac{V_d(S)}{U_{id}(S)} = \dfrac{V_q(S)}{U_{iq}(S)} = \dfrac{Z}{ZCS + 1} \end{cases} \tag{2.38}$$

$$\begin{cases} U_{id} = V_{invd} - V_d + \omega \cdot L \cdot I_q \\ U_{iq} = V_{invq} - V_q - \omega \cdot L \cdot I_d \\ U_{vd} = I_d + \omega \cdot C \cdot V_q \\ U_{vq} = I_q - \omega \cdot C \cdot V_d \end{cases} \tag{2.39}$$

The controller of converter adopts a double feedback loop control strategy including an outer voltage feedback loop and an inner current feedback loop. The schematic of complete DSP-based controller for HC-MLI is shown in Fig. 2.11(a). Fig. 2.11(b) and 2.11(c) show the schematics of the inner current controller and outer voltage controller of the proposed HC-MLI. The output of *d* and *q* axis voltage controller are u_{vd}^* and u_{vq}^*. From these reference signals, the inner control loop currents i_d^* and i_q^* are written as

$$\begin{cases} i_d^* = u_{vd}^* - \omega c v_q \\ i_q^* = u_{vq}^* + \omega c v_d \end{cases} \tag{2.40}$$

Similarly, the outputs of *d* and *q* axis voltage controllers are u_{iq}^* and u_{id}^*. respectively. From these signals, *d-q* components of modulating signals can be written as

$$\begin{cases} V_{mq} = \frac{1}{V_{dc}} . \left(u_{iq}^* + \omega L i_d + v_q \right) \\ V_{md} = \frac{1}{V_{dc}} . \left(u_{id}^* - \omega L i_q + v_d \right) \end{cases} \tag{2.41}$$

The AC voltage controller outputs are the modulation signals V_{md} and V_{mq} in *d-q* reference frame. The sinusoidal modulation signal, $V_{\mathrm{m}}(t)$ of the HC-MLI is obtained as

$$V_m(t) = m_a = V_{\mathrm{md}} \sin\theta + V_{\mathrm{mq}} \cos\theta \tag{2.42}$$

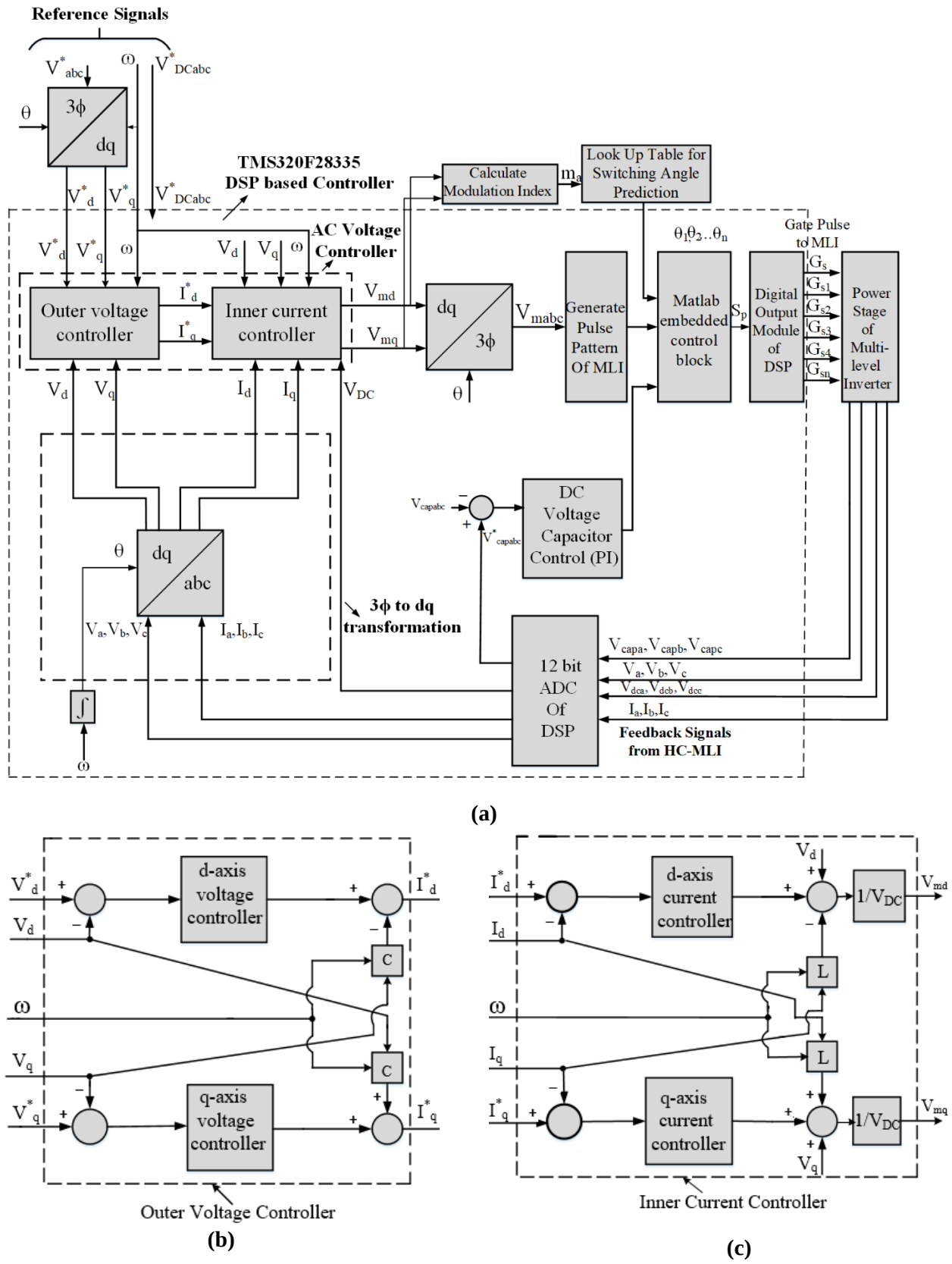


Fig. 2.11 Closed loop controller of HC-MLI.
(a) DSP based closed loop control of HC-MLI. (b) Schematic of inner current controller. (c) Schematic of DSP-based controller for HC-MLI.

An inner current loop control based on *d-q* synchronous reference frame is used to follow the accuracy of the desired reference current. The modulation index can be obtained from *d*-axis and *q*-axis voltages as

$$m_a = \frac{\sqrt{{v_{md}}^2 + {v_{mq}}^2}}{V_{DC}} \tag{2.43}$$

2.8 Capacitor Calculation

To calculate appropriate value of capacitance, the intermittent discharging period of the capacitor is considered. The capacitor has the intermittent discharging period in the interval θ_1 - θ_2; in the interval θ_3 - θ_4; in the interval θ_5 - $\pi/2$. The maximum discharging value Q_c is given as

$$Q_c = \frac{2}{\omega}\left[\int_{\theta_1}^{\theta_2} i_l d\theta + \int_{\theta_3}^{\theta_4} i_l d\theta + \int_{\theta_5}^{\pi/2} i_l d\theta\right] \tag{2.44}$$

For inductive load, load current (i_l) can be represented as

$$i_l = i_0 \sin(\omega t - \phi) \tag{2.45}$$

The maximum allowable voltage ripple across the capacitor is kV_{dc}, where *k* is the ripple factor. The optimal value of capacitance is given as

$$C_{Opt} \geq \frac{Q_c}{kV_{dc}} \tag{2.46}$$

Substituting (2.45) in (2.44) and using (2.46), the optimum capacitance for inductive loading condition can be obtained as

$$C_{Opt} = \frac{1}{k \times \omega \times |Z|} \cdot \left[\begin{array}{l} \sin\left(\frac{\theta_1 + \theta_2}{2} - \phi\right) \cdot \sin\left(\frac{\theta_2 - \theta_1}{2}\right) + \sin\left(\frac{\theta_3 + \theta_4}{2} - \phi\right) \cdot \sin\left(\frac{\theta_4 - \theta_3}{2}\right) \\ + \cos(\theta_5 - \phi) - \sin\phi \end{array}\right] \tag{2.47}$$

For 10% voltage ripple (k = 0.1), power factor $\cos\phi$ = 0.7 and load impedance Z = 17 Ω (R=12 Ω and L= 37 mH), the optimum capacitance value is calculated using (2.47) for different m_a are given in Table 2.5.

Table 2.5
Capacitance Values at Different m_a

m_a	Capacitance
0.6	234 µF
1	323 µF
1.1	351 µF

Table 2.6
Parameters Used for Simulation

Parameters	Attributes
Switching frequency	50 Hz
Output Filter Inductor	20 mH
Output Filter Capacitor	10 µF
Load (Resistive)	10 Ω
DC-link Capacitors	350 µF/200 V

2.9 Simulation Studies

A 1.5-kW three-phase, 11-level HC-MLI is simulated through MATLAB/Simulink using proposed MPSO optimization method. Table 2.6 lists the parameters used to verify the proposed work. The population size is taken as 100. The MPSO optimized switching angles θ_1 to θ_5 are calculated for different modulation indices and are shown in Fig. 2.4. The DC sources (V_{DC}) of two primary H-bridges and capacitor voltage (V_{CAP}) of supplementary H-bridge are taken as 60 V and 30 V. Device switching frequency is kept at 50 Hz. The SHE-PWM modulation technique using MPSO has been used for generating the optimal gate

control signals. The reference signal for the closed-loop control of the HC-MLI is taken as V_{AC}^{*} = 240 V (peak-peak) in the controller of HC-MLI as shown in Fig. 2.11. The value of capacitor voltage is controlled using proportional integral (PI) controller. The values of K_p and K_i obtained through MPSO algorithm are 0.14 and 4, respectively. The sensed capacitor voltages (V_{CAP}) of the respective three-phases phase *A*, phase *B* and phase *C* are fed back to the ADC of DSP through a signal conditioning circuit. The sensed average capacitor voltage is compared with the reference value and given to the embedded code logic block of MATLAB/Simulink. The direction of the load current is sensed using a current sensor for capacitor voltage balancing at available redundancies. During allowable periods, the capacitor is allowed to charge up to the maximum voltage decided by the PI controller as shown in Fig. 2.15. The steady state mean error is eliminated and the average capacitor voltage is maintained at 30 V.

2.9.1 Operation at m_a = 0.55

Based on Fig. 2.4, obtained switching angles are θ_1 = 32.14, θ_2 = 49.25, θ_3 = 61.15, θ_4 = 71 .45 and θ_5 = 84 .68. As shown in Fig. 2.12 the output voltages of the H_1, H_2 and H_3 are V_{a1}, V_{a2} and V_{a3} respectively. The total output voltage of the elven level HC-MLI is V_a, and the voltage of the capacitor is V_c. The output voltages of each H-bridge cell of 11-level HC-MLI are shown in Fig. 2.12. It can be observed that the average value of the capacitor is maintained at 30 V.

2.9.2 Operation at m_a = 1.2

For higher modulation index m_a=1.4, using on Fig. 2.4, switching angles are obatained as θ_1=5.21, θ_2=18.45, θ_3=30.05, θ_4= 41.67 and θ_5=65.47. With these set of switching angles, the constraint for the capacitor voltage balance as given in (2.31) is not satisfied. Therefore, the

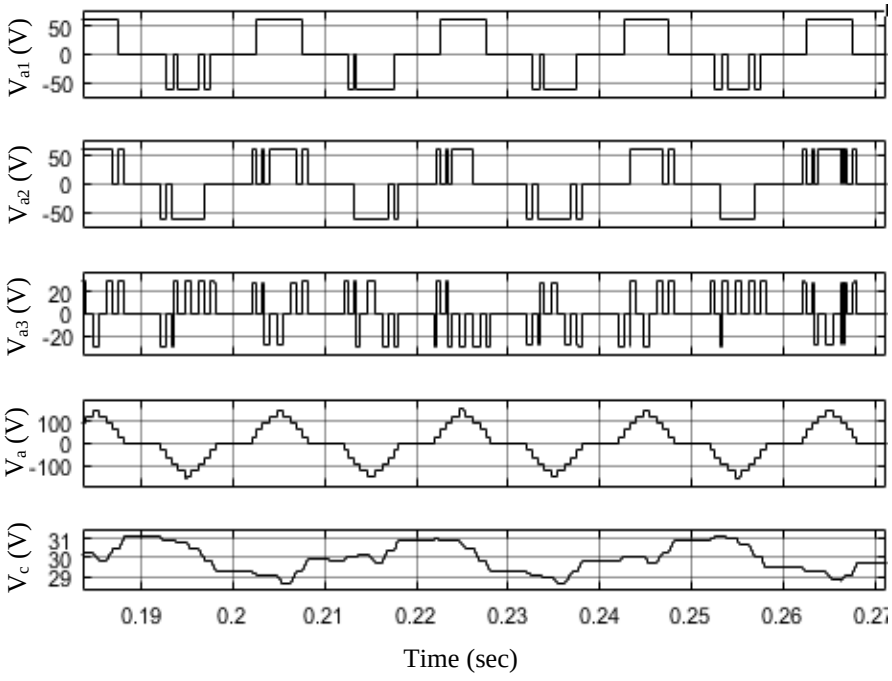


Fig. 2.12 Output voltages of each H-bridge cells with total output voltage at m_a =0.55.

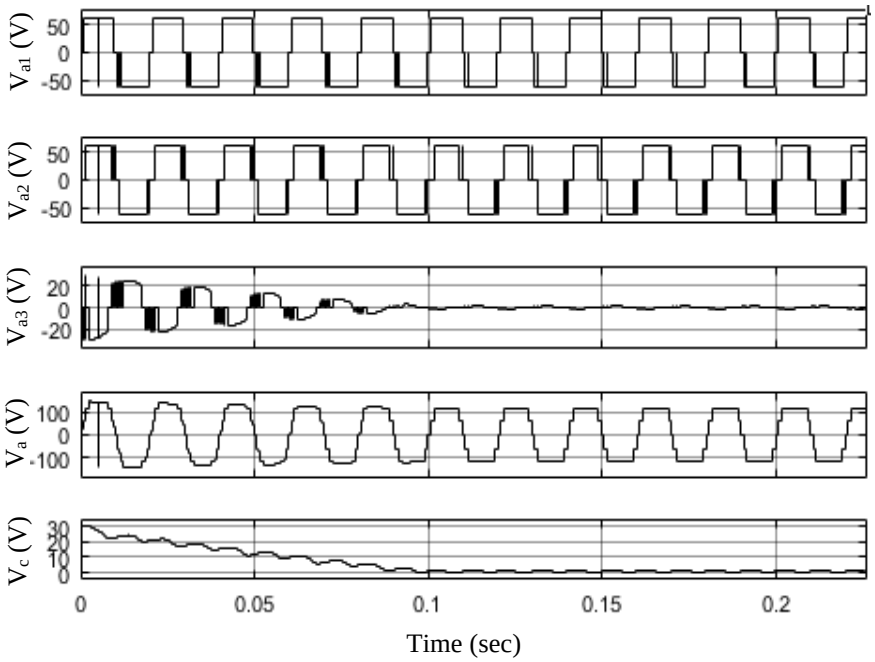


Fig. 2.13 Output voltages of each H-bridge cells with total output voltage at m_a =1.2 without capacitor voltage balance.

capacitor voltage will not remain at a constant level and will decrease continuously until it discharges completely as shown in Fig. 2.13. In such a situation, the third harmonic voltage

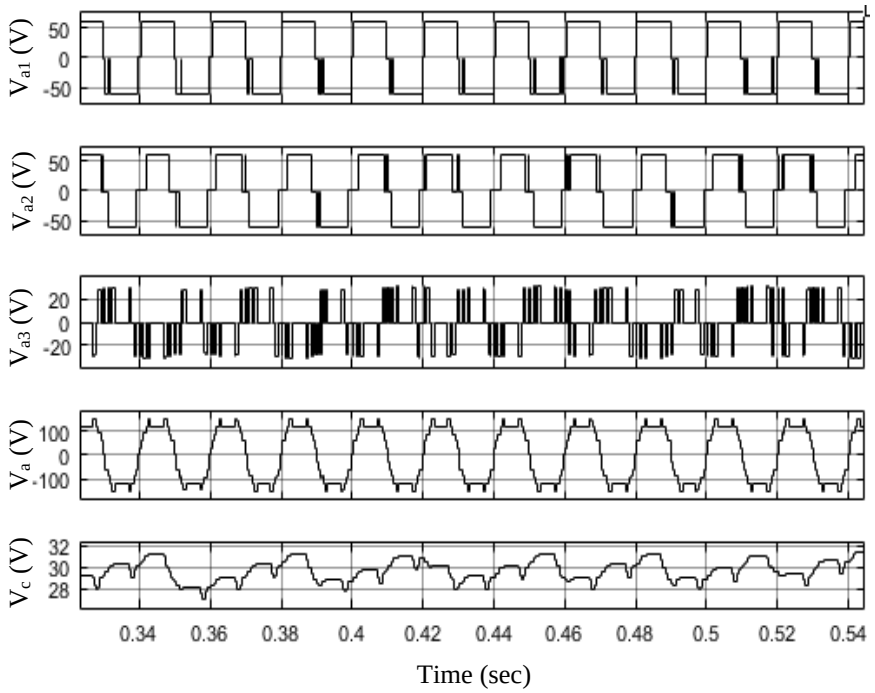
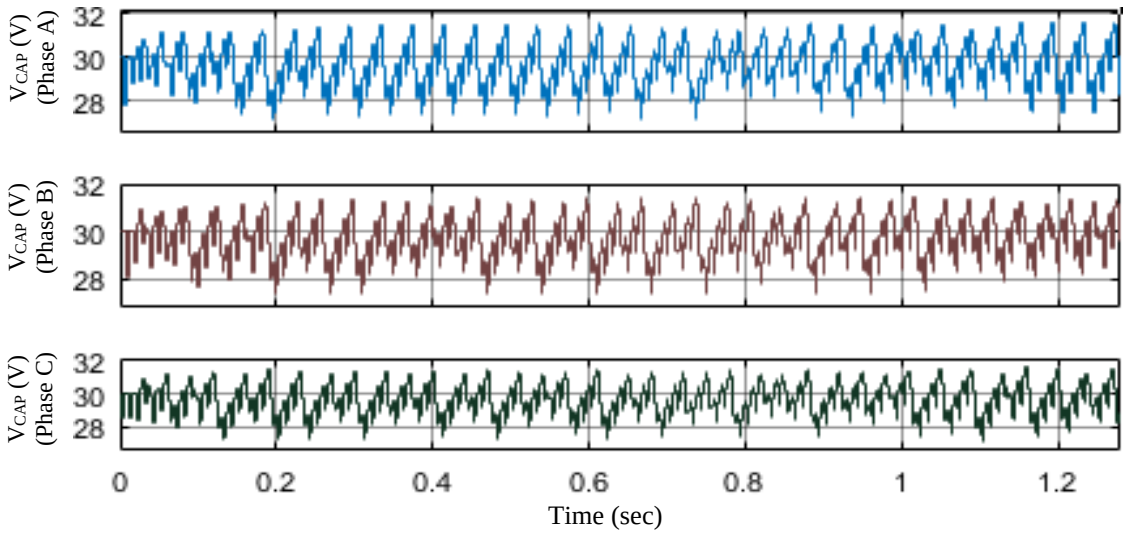
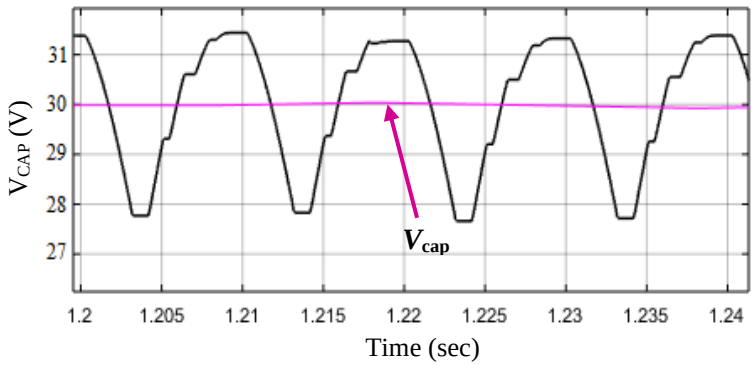


Fig. 2.14 Output voltages of each H-bridge cells with total output voltage at m_a =1.2 with capacitor voltage balance.

is injected to balance the capacitor voltage. The capacitor voltage balance at higher modulation index is shown in Fig. 2.14. The averge capacitor voltage is maintained constant at 30 V using capacitor voltage averaging technique. The simulated three-phase capacitor voltages are shown in Fig. 2.15(a) and average capacitor voltage is shown in Fig. 2.15(b).



(a)

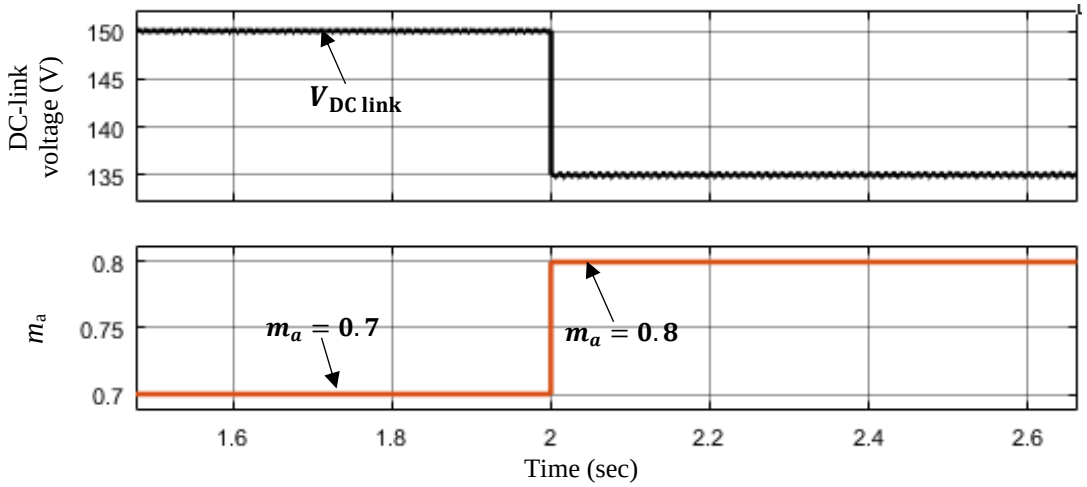


(b)

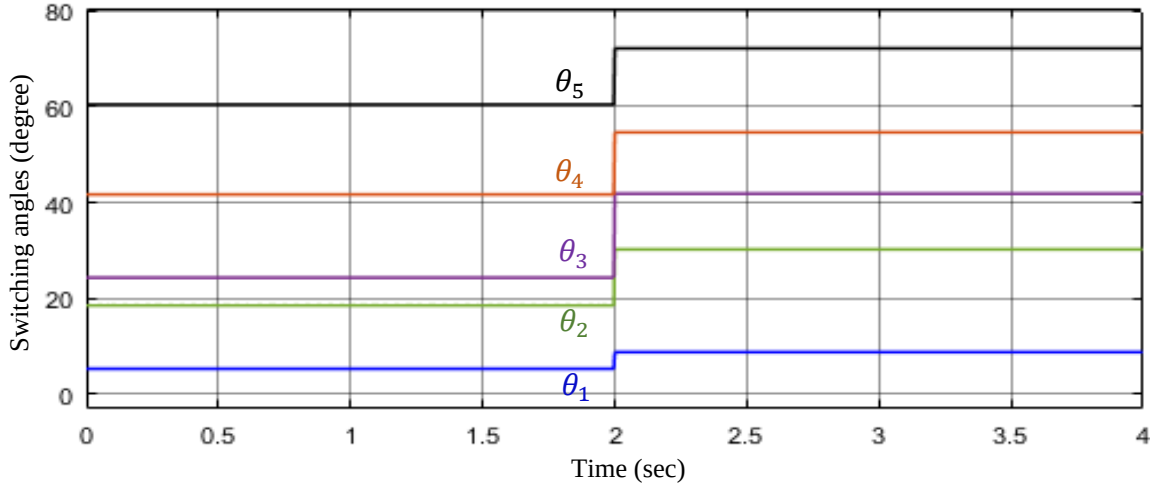
Fig. 2.15 Simulation results of three-phase capacitor voltages.
(a) Three-phase capacitor voltages with voltage averaging. (b) Capacitor voltage with voltage averaging (V_{CAP}).

2.9.3 Controller Performance During Change in DC-Link Voltage

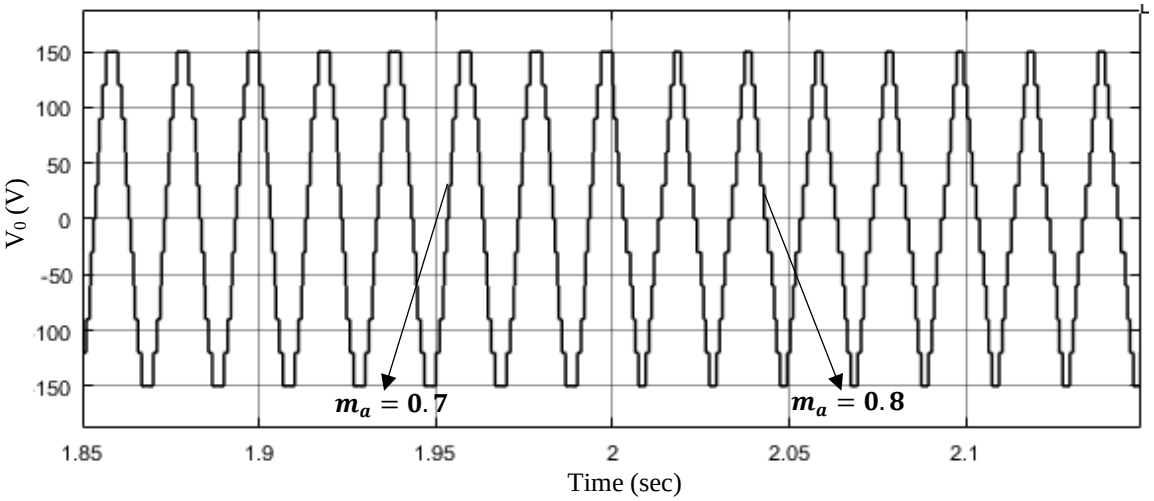
In closed loop control, the controller maintains the output voltage constant irrespective of the fluctuations in the DC-link voltage. During any fluctuations in the DC-link voltage, the modulation index (m_a) changes and the switching angle changes according to the corresponding modulation index. Please refer Fig. 2.11, where the AC voltage controller outputs are V_{md} and V_{mq} in *d-q* reference frame. The switching angles for different m_a values are stored in a look-up table. During fluctuations in DC-link voltage, m_a changes and the corresponding switching angles are obtained from the look-up table. Subsequently, the gate



(a)



(b)



(c)

Fig. 2.16 Simulation results of HC-MLI for change in DC-link voltage.
(a) Change in DC-link voltage due to change in m_a from 0.7 to 0.8. (b) Change in switching angles for change in m_a from 0.7 to 0.8. (c) Change in output voltage for change in m_a from 0.7 to 0.8.

control signals (S_1, S_2, S_3, ... S_n) are generated using the DSP which regulates the DC-link voltage. For verifying the control of DC-link voltage through simulation studies, a change in DC-link voltage from 150 V to 137 V is made. Consequently, the modulation index m_a changes from 0.7 to 0.8 to take care of the change in DC-link voltage as shown in Fig. 2.16(a). The change in corresponding switching angles due to change in m_a are shown in Fig. 2.16(b) and the generated output voltage is shown in Fig. 2.16(c).

2.9.4 Harmonic Analysis of Output Voltages at Different m_a

The output line voltage (V_{AB}) and its harmonic spectrum at m_a = 0.55 are shown in Figs. 2.17 and 18 respectively. Similarly, the output line voltage (V_{AB}) and its harmonic spectrum at m_a = 0.8 are shown in Figs. 2.19 and 2.20.

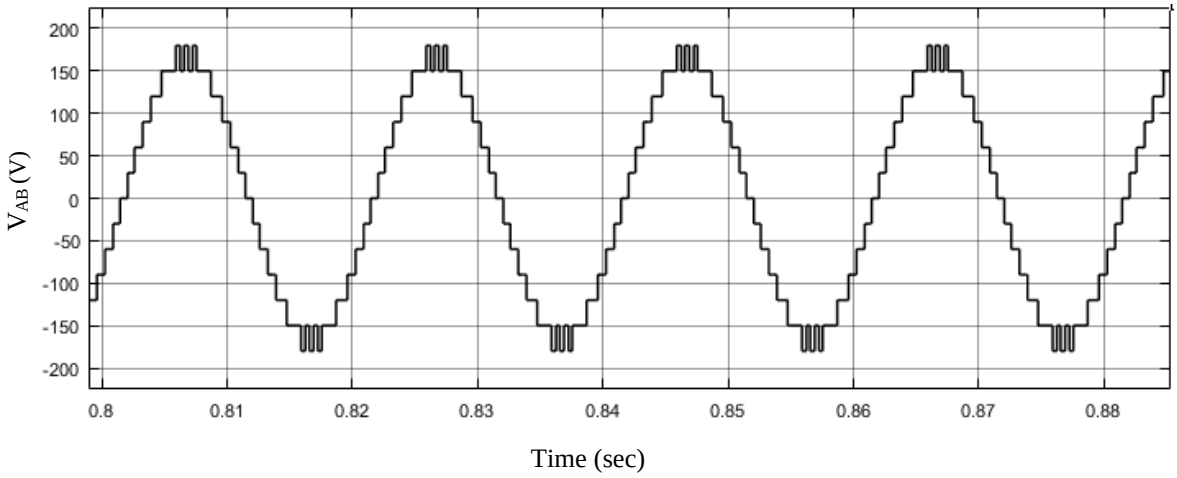


Fig. 2.17 Output voltage (V_{AB}) at m_a = 0.55.

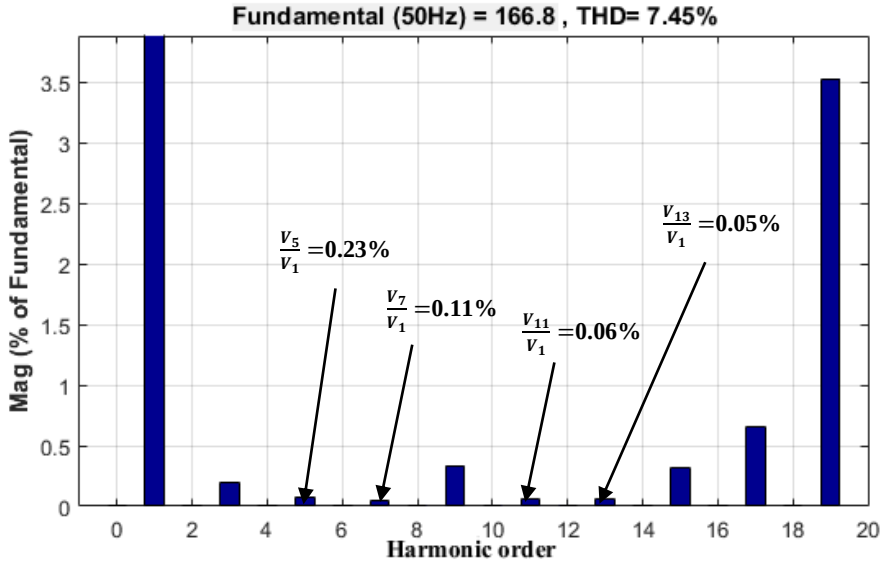


Fig. 2.18 Harmonic spectrum (V_{AB}) at m_a = 0.55.

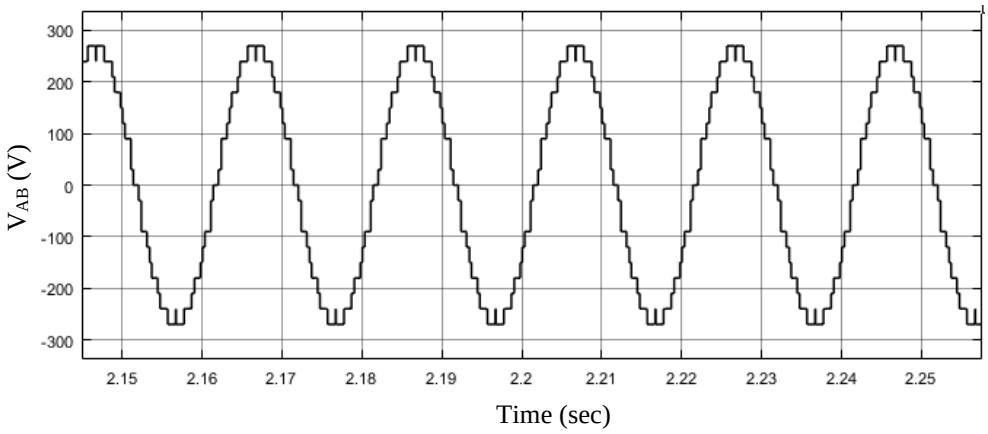


Fig. 2.19 Output voltage (V_{AB}) at $m_a = 0.8$.

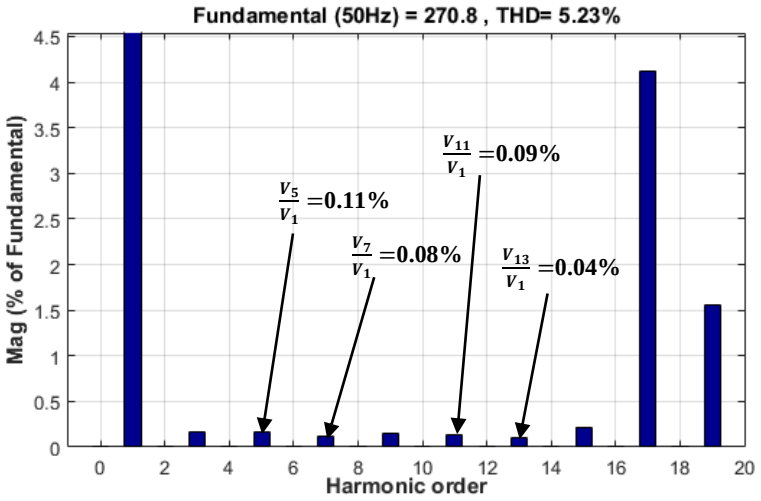


Fig. 2.20 Harmonic spectrum (V_{AB}) at $m_a = 0.8$.

2.9.5 Effects of Inductive Load on Capacitor Voltage Balancing at Higher Modulation Index

In (2.31), the load is assumed to be resistive. In HC-MLI, the maximum capacitor discharge occurs when the output voltage is at its maximum level. At this point, the current is also at its maximum level since the current is in phase with the voltage for resistive load. The capacitor discharges faster in case of resistive load in comparison to inductive and capacitive loads. In case of inductive and capacitive loads, the peak value of the output current does not coincide with the peak value of the output voltage. The phase shift between output voltage and load current of the inverter reduces the rate of discharging of the capacitor. It may be

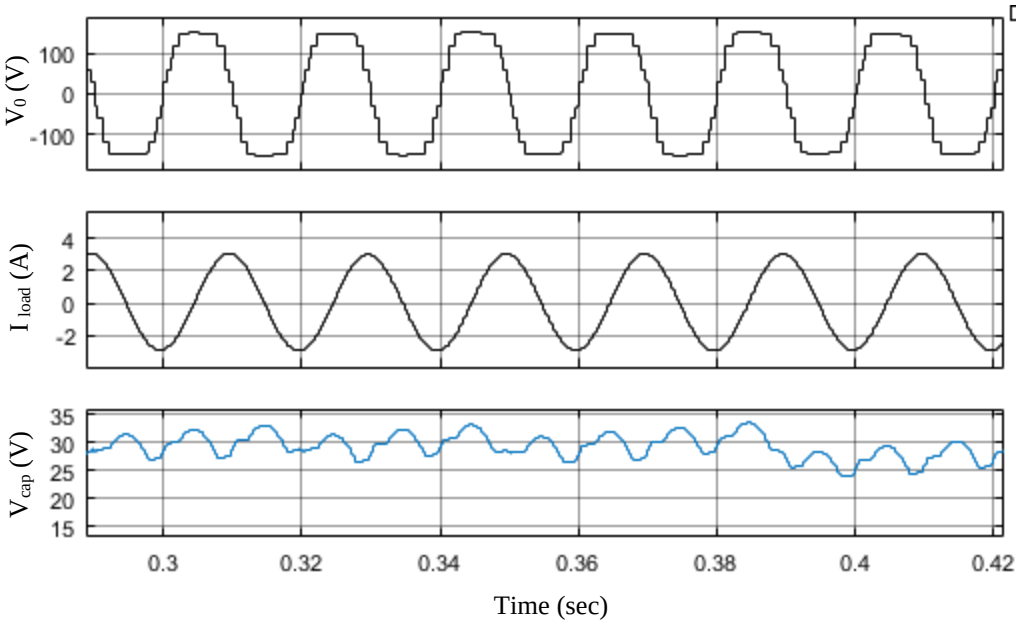


Fig. 2.21 Simulation results at m_a = 1.1 for inductive load.

concluded that if the constraint satisfies for resistive loads, it also satisfies for inductive and capacitive loads. In case of highly inductive loads, it is possible to keep the charge of the capacitor at the desired level even at higher modulation index, even if the constraint derived in (2.31) is not satisfied. The simulation is carried out for m_a = 1.1 for inductive load to observe the effects of regulation in capacitor voltage. The inductive load consists of (R=12 Ω and L=80 mH). Simulation results for the said load conditions are shown in Fig. 2.21. It can be observed from Fig. 2.21 that the capacitor voltage is regulated in this case. For resistive load, the same simulation results are shown in Fig. 2.22. It may be noted that the capacitor voltage regulation is not possible at m_a =1.1 in case of resistive load. Hence, it is always possible to balance the capacitor voltage in case of highly inductive loads even at higher values of m_a. For each individual value of power factor, the balancing of the capacitor is checked for the entire range of modulation indices and the maximum modulation index for each power factor is as shown in Fig. 2.23.

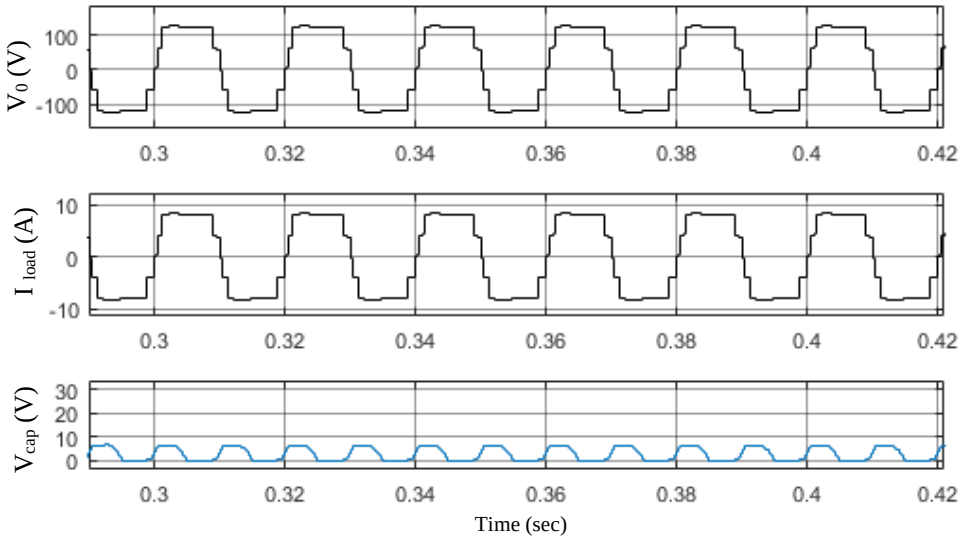


Fig. 2.22 Simulation results at m_a = 1.1 for resistive load.

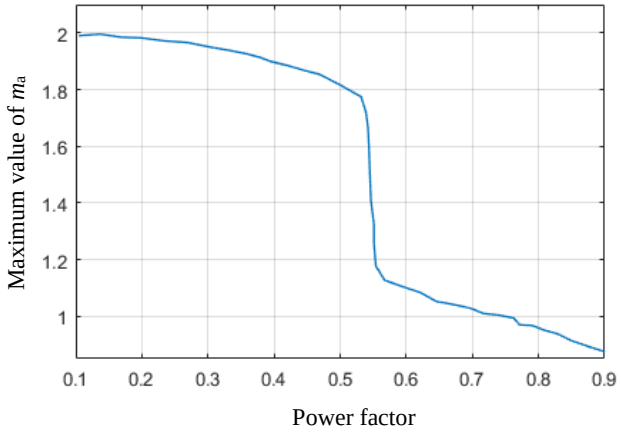


Fig. 2.23 Effect of power factor on capacitor voltage balancing.

Table 2.7
Components Used for Experiment

Components	Manufacturer
IGBT Modules	SK50GBO63D (Semikron)
IGBT Gate Driver	SKYPER 32R (Semikron)
Heat Sink	P3/250 mm
Optocoupler	FOD3182 (Fairchild)
Voltage Sensor	LV 55P (LEM)
Current Sensor	LA 25P (LEM)
OPAMP	LM3124n (IR Corporation)
DSP	TMS320F28335 (TI)

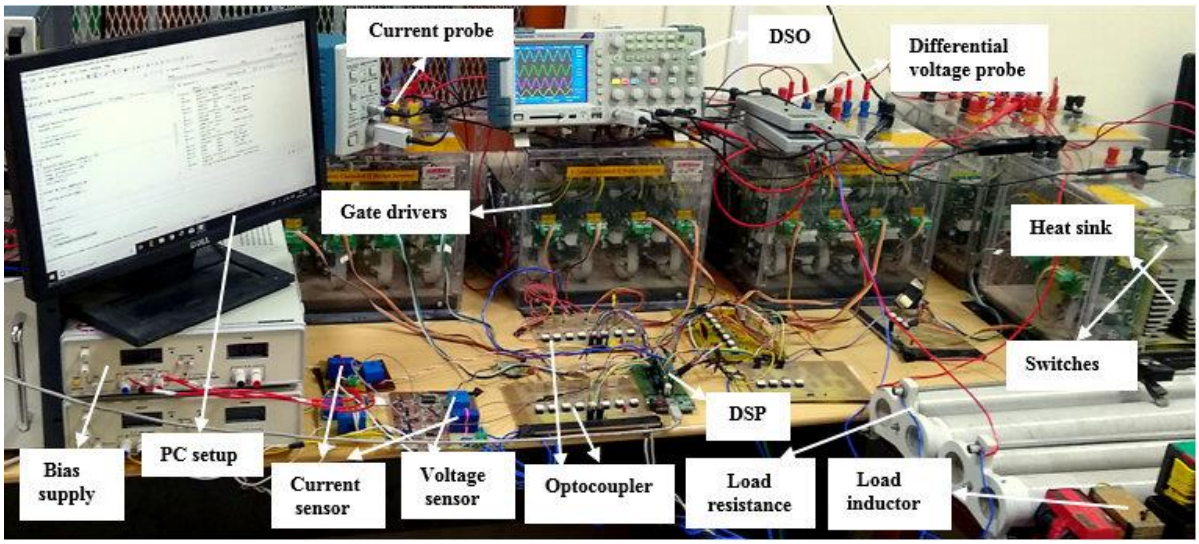


Fig. 2.24 Photograph of the experimental setup (11-level HC-MLI).

2.10 Experimental Verification

Fig. 2.24 shows the photograph of experimental setup. The control scheme has been implemented using a TI-TMS320F28335 DSP processor [109]. List of parameters used for experimentation are given in Table 2.7. In the experiments, the primary H-bridge cells (H_1, H_2) are fed by 60 V DC sources and 350 mF capacitor is connected to the supplementary H-bridge (H_3). The capacitor voltage (V_{CAP}) is 30 V. The sensed capacitor voltages (V_{CAP}) of the respective three-phases phase *A*, phase *B* and phase *C* are fed back to the ADC of DSP through a signal conditioning circuit. The sensed average capacitor voltage is compared with the reference value and given to the embedded code logic block of MATLAB/Simulink. The direction of the load current is sensed using a current sensor for capacitor voltage balancing at available redundancies. The capacitor voltage balancing is investigated experimentally for higher range of modulation indices. The output phase voltages (V_A, V_B, V_C) at $m_a = 0.55$ are shown in Fig. 2.25(a). The measured rms values of phase voltages (V_A, V_B, V_C) are 71.8 V. The performance of the HC-MLI has also been investigated for *R-L* load. The output voltage

V_A and output current I_L obtained through experiments for *R-L* load at m_a=0.55 is shown in Fig. 2.25(b). Fig. 2.25(c) and (d) shows the phase voltage (V_A) and phase voltages (V_A, V_B, V_C) at m_a = 1.2. The measured rms value of phase voltage (V_A) is 110.6 V. The experimental result confirms that capacitor voltage balancing is achieved at higher modulation index. It can be observed that capacitor voltage is maintained at 30 V. Table 2.8 shows the magnitudes of lower order harmonics at different modulation index. Harmonic magnitudes are within IEEE Std 519-2014 [110].

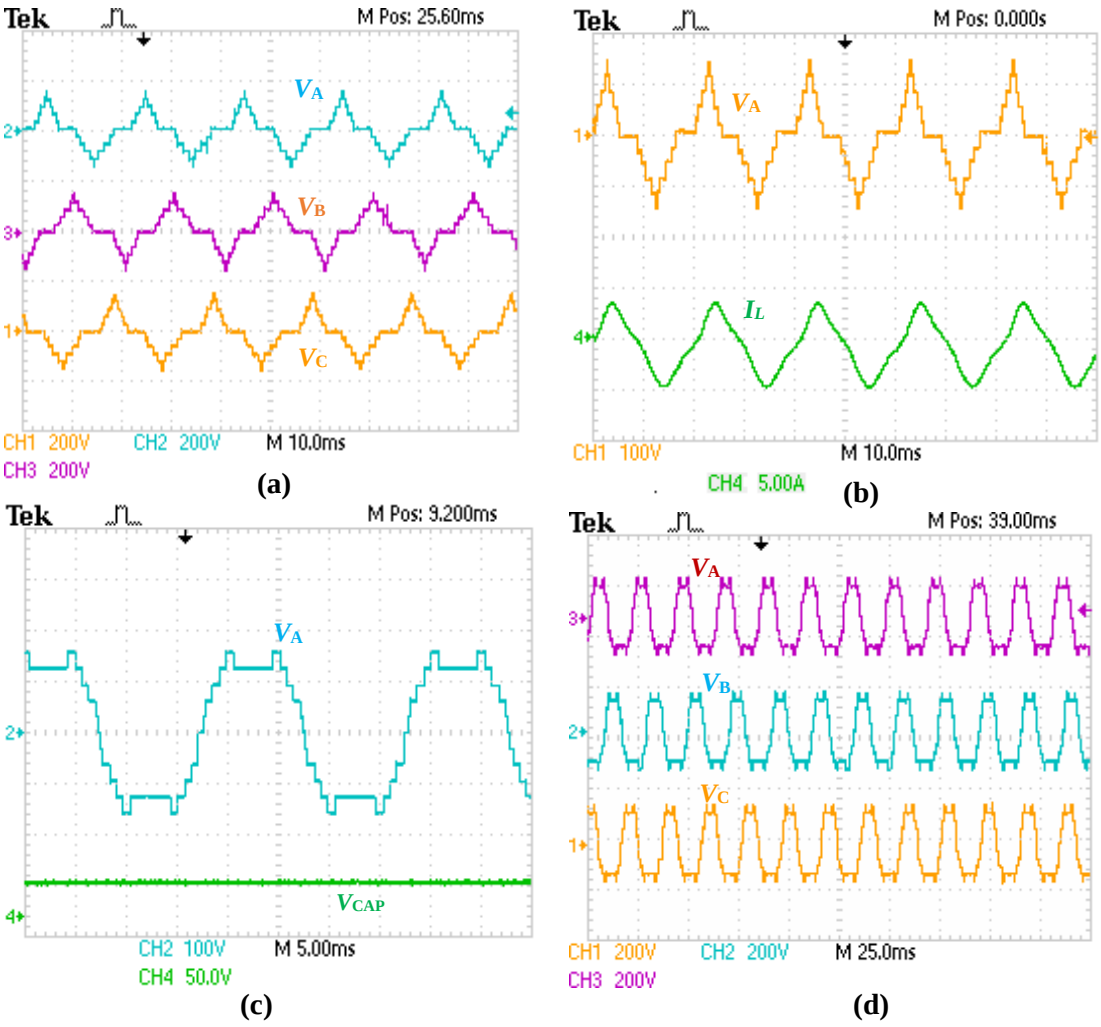


Fig. 2.25 Experimental results of the HC-MLI (Phase voltages).
(a) Phase voltages (V_A, V_B, V_C) at m_a = 0.55. (b) Phase voltage (V_A) for *R-L* load at m_a = 0.55. (c) Phase voltage (V_A) at m_a = 1.2 (3rd harmonic injected). (d) Phase voltages (V_A, V_B, V_C) at m_a = 1.2.

The experimental results of line voltage (V_{AB}) at m_a=0.55 and its harmonic spectrum are shown in Fig. 2.26(a) and (b). The measured rms value of line voltages is 118.5 V. It is observed from Fig. 2.26(b) that 5th,7th,11th and 13th order harmonics are eliminated from the output voltage of the HC-MLI. The experimental results of line-line voltages (V_{AB}, V_{BC}, V_{CA}) at m_a = 0.55 and m_a = 1.2 are shown in Fig. 2.26(c) and (d) respectively. Fig. 2.27(a) shows the steady state output voltage V_{AB} and load current I_L along with capacitor voltage V_{CAP}. The output voltage is maintained at 84.82 V for load current of 17 A by closed loop control. Fig. 2.27(b) shows the harmonic spectrum of V_{AB} at m_a = 0.55 after connecting LC filter. Table 2.9 shows the magnitudes of lower order harmonics at different modulation indices.

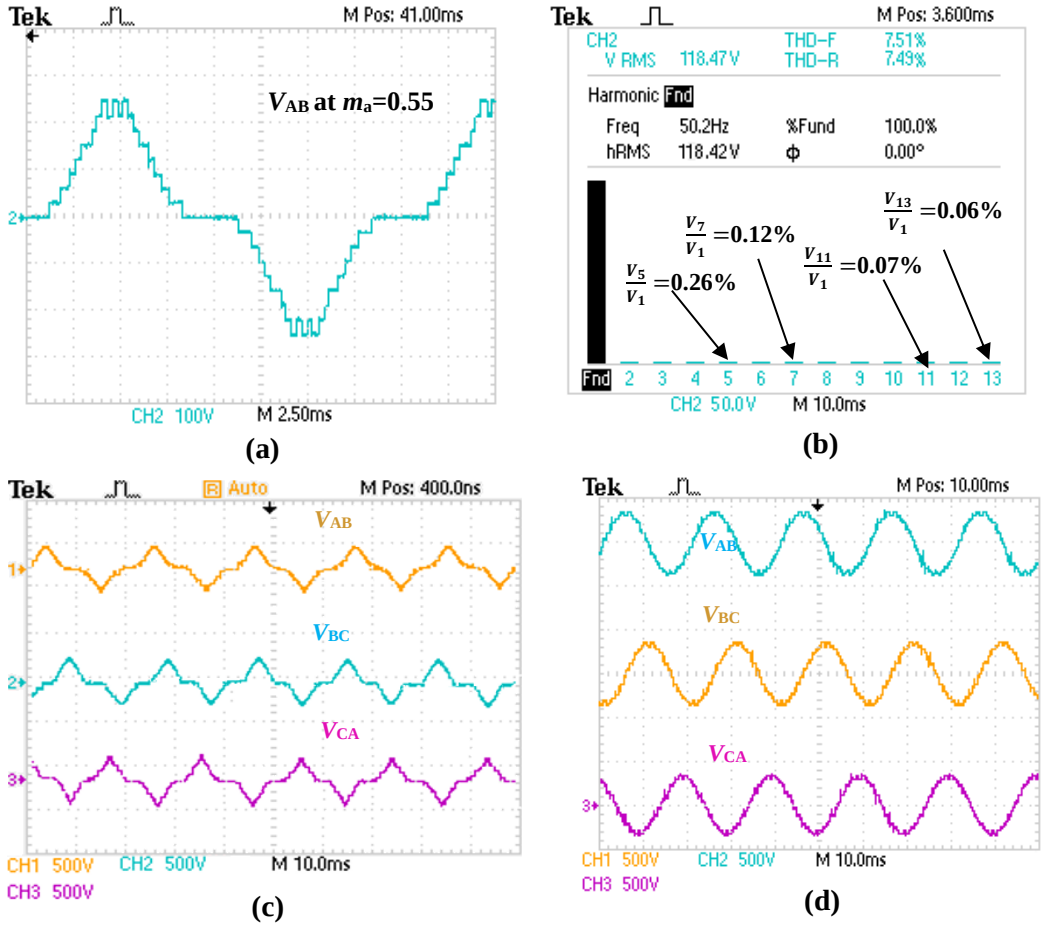


Fig. 2.26 Experimental results of the HC-MLI (Line voltages).
(a) Line voltage (V_{AB}) at m_a = 0.55. (b) Harmonic spectrum of V_{AB} at m_a = 0.55. (c) Line voltages (V_{AB}, V_{BC}, V_{CA}) at m_a = 0.55. (d) Line voltages (V_{AB}, V_{BC}, V_{CA}) at m_a = 1.2.

Table 2.8
Harmonic Magnitudes and % THD of V_{AB} Through Experiment at Different Modulation Indices

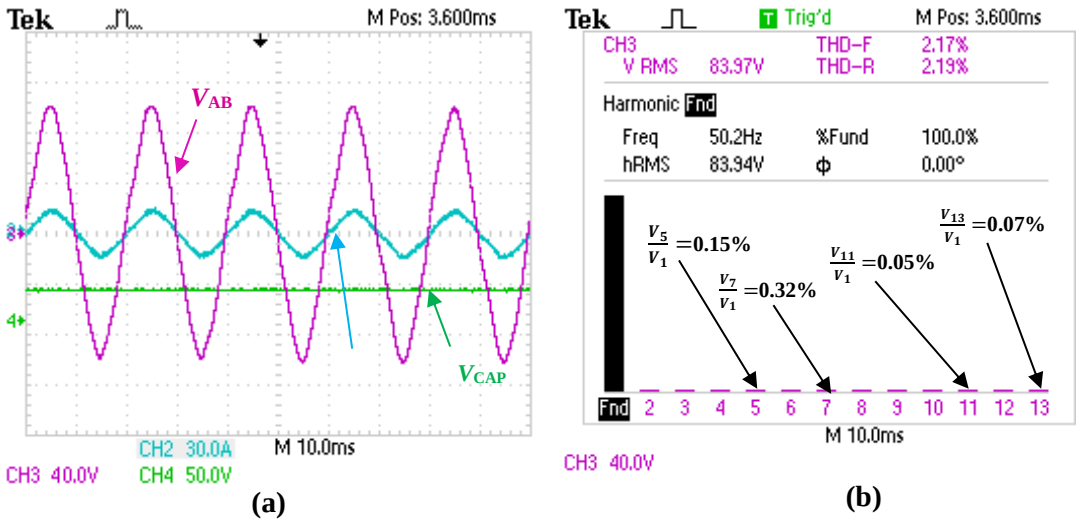
Modulation index	%h5	%h7	%h11	%h13	%THD
0.5	0.25	0.08	0.27	0.31	8.71
0.6	0.30	0.18	0.07	0.09	7.67
0.7	0.55	0.68	0.10	0.47	7.83
0.8	0.14	0.09	0.11	0.06	5.47
0.9	0.12	0.08	0.43	0.09	4.35
1	0.26	0.15	0.18	0.19	5.09
1.1	0.67	0.37	0.07	0.08	6.03
1.2	0.62	0.45	0.13	0.07	6.51

Table 2.9
Harmonic Magnitudes and %THD of line voltage V_{AB} at Different Modulation Indices

Modulation index	% h5	% h7	% h11	% h13	%THD
0.5	0.42	0.77	0.68	0.50	3.12
0.6	0.15	0.32	0.05	0.07	2.14
0.7	0.16	0.73	0.12	0.04	2.31
0.8	0.2	0.53	0.16	0.15	2.04
0.9	0.15	0.53	0.1	0.07	1.09
1	0.41	0.16	0.36	0.22	1.29
1.1	0.33	0.52	0.18	0.11	2.03
1.2	0.15	0.31	0.09	0.06	2.29

Table 2.10
Experimental %THD Comparison of Different Algorithms

Modulation index	%THD (MPSO)	%THD (PSO)	%THD (GA)
0.5	8.51	10.73	13.89
0.6	7.62	9.25	12.52
0.7	7.73	9.67	12.91
0.8	5.28	7.51	11.41
0.9	4.21	6.11	10.91
1	5.09	7.13	9.92
1.1	5.71	7.76	8.13
1.2	6.25	8.08	9.41



(a) (b)

Fig. 2.27 Experimental results of the HC-MLI after connecting LC filter.
(a) Line voltage (V_{AB}) with load current (I_L) and capacitor voltage (V_{CAP}) at m_a = 0.55.
(b) Harmonic spectrum of (V_{AB}) at m_a = 0.55.

It is worth mentioning that the harmonic magnitudes are well within IEEE Std 519-2014 [110]. Table 2.10 gives the comparison of experimentally obtained % THD at different modulation indices. The proposed MPSO gives improved result as compared to other reported algorithms. The output voltage and output current for *R-L* load (R=12 Ω and L= 37 mH) obtained through experiment are shown in Fig. 2.28. The algorithm has been experimentally verified in real time for step change in m_a from 0.5 to 0.6 as shown in Fig. 2.29.

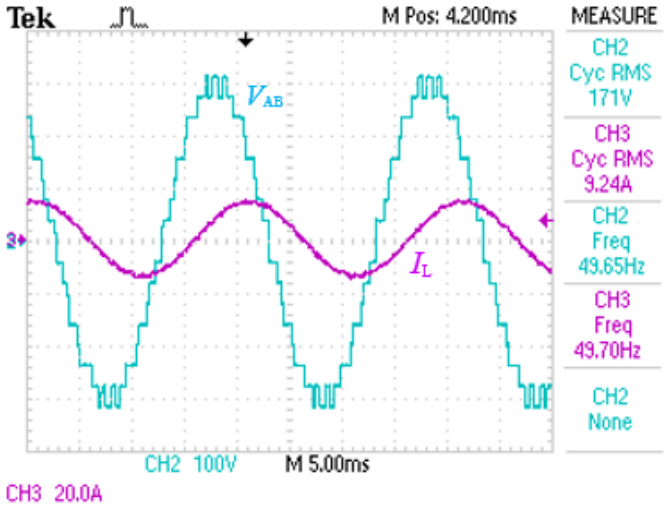


Fig. 2.28 Experimental result of HC-MLI of output line voltage versus load current for inductive load (R=12 Ω and L= 37 mH).

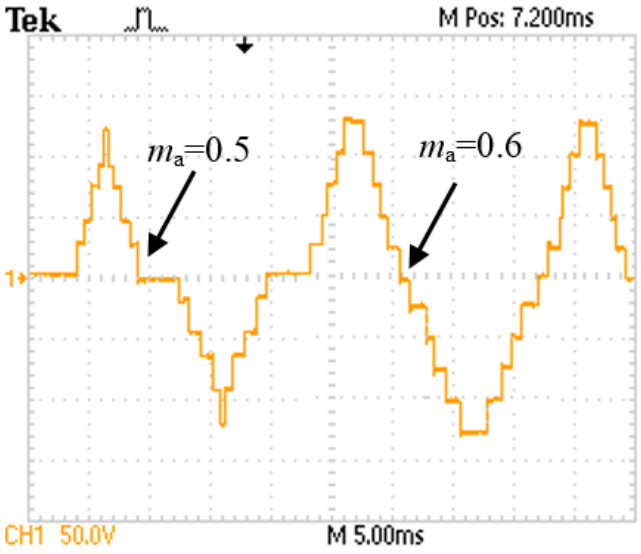


Fig. 2.29 Real time implementation of controller during step-change in m_a from 0.5 to 0.6.

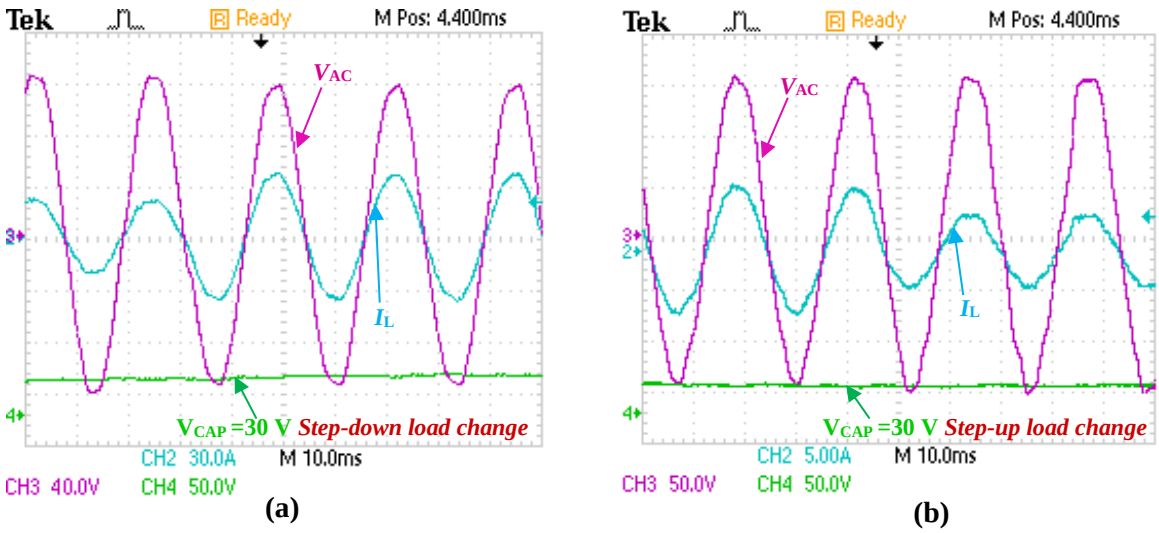


Fig. 2.30 Dynamic results of HC-MLI.
(a) 50% step-down change in load (b) 50% step-up change in load.

2.10.1 Dynamic Performance of HC-MLI

In order to validate the dynamic performance of the HC-MLI and capacitor voltage balance during load change, the output resistance is suddenly changed from 10 Ω to 5 Ω. It can be observed from Fig. 2.30(a) that after step-down change in load resistance, the load current increases from 9 A to 17 A but the output voltage (V_{AC}) and capacitor voltage (V_{CAP}) are maintained at 84.82 V and 30 V respectively. Similarly, Fig. 2.30(b) shows that during step-up load change and load current from decreases from 17 A to 9 A, output load voltage and capacitor voltage are also maintained constant.

2.11 Conclusion

This chapter presents MPSO optimized three-phase, 11-level HC-MLI using SHE-PWM technique. Improvements in weight and velocity factors in MPSO take care of local optima efficiently in this method leading to better convergence rate and reduced harmonic content. The proposed MPSO optimized HC-MLI ensures capacitor voltage balance even at higher modulation indices by utilizing the available redundancies of HC-MLI. It has been

demonstrated that the capacitor voltage balance in HC-MLI can be achieved even at higher modulation indices using harmonic injection method. Simulation and experimental studies are carried out to demonstrate steady state and dynamic performance of the proposed MPSO optimized three-phase HC-MLI. The proposed MPSO optimized SHE-PWM gives better results in terms harmonic content and convergence rate as compared to GA and PSO algorithms. In order to further improve the performance of HC-MLI, in terms of speed of convergence and harmonic content, a modified whale optimization (MWO) algorithm has been proposed in the next chapter.

Chapter 3

Harmonic Minimization in HC-MLI Using Modified Whale Optimization

3.1 Introduction

In this chapter, selective harmonics elimination pulse width modulation (SHE-PWM) technique has been employed through proposed modified whale optimization (MWO) for generating three phase, 11-level output voltage of hybrid cascaded hybrid multilevel inverter (HC-MLI) [111]. The MWO optimized three-phase HC-MLI enhances the performance in terms of harmonic content, rate of convergence and obtaining global optima quickly. In the proposed MWO optimized HC-MLI, capacitor voltage balance is made possible even at higher modulation indices using available redundant switching states of HC-MLI.

3.2 Mathematical Model of Whale Optimization Algorithm

Whale optimization (WO) algorithm is a naturally inspired meta-heuristic algorithm, which replicates the social behaviour of humpback whales [95], [96]. This algorithm is inspired by the bubble-net searching technique of humpback whales. The mathematical model of three main steps of hunting in WO; such as encircling prey, spiral bubble-net hunting and search for prey are discussed as follows:

3.2.1 Encircling Prey

The humpback whales encircle the prey and update their position towards the best search

agent. The humpback whales encircle the prey and update their position towards the best search agent using (3.1) and (3.2) are given as

$$D = \left|\vec{C} \cdot \vec{X}^*(j) - \vec{X}(j)\right| \tag{3.1}$$

$$\vec{X}(j+1) = \vec{X}^*(j) - \vec{A}.\vec{D} \tag{3.2}$$

where j is the current iteration, $\vec{X}$ indicates the position vector, $\vec{X}^*(j)$ is the position vector of the best solution till obtained, $\vec{A}$ and $\vec{C}$ are the coefficient vectors. The vector $\vec{A}$ is calculated as

$$\vec{A} = 2\vec{a} \cdot \vec{r} - \vec{a} \tag{3.3}$$

and vector $\vec{C}$ as

$$\vec{C} = 2.\vec{r} \tag{3.4}$$

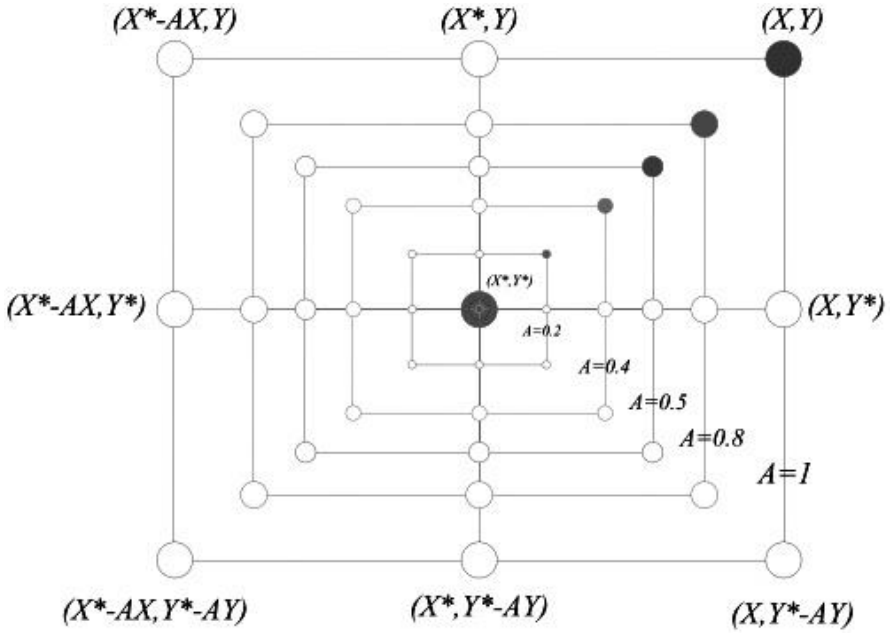
where the value of $\vec{a}$ linearly decreases from [2, 0] and $\vec{r}$ is random vector between [0, 1].

3.3 Bubble-Net Attacking Method (Exploitation Phase)

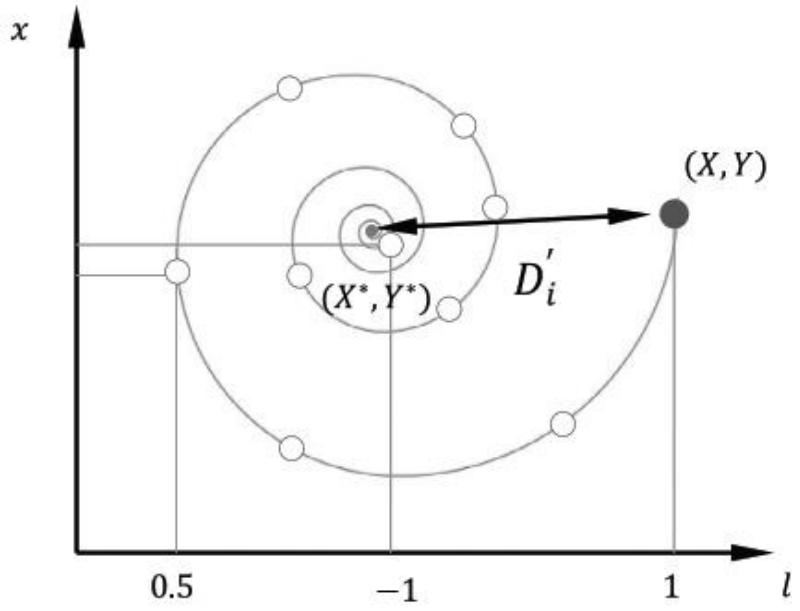
In order to mathematically model the bubble-net behavior of humpback whales, two approaches are designed as follows:

3.3.1 Shrinking Encircling Mechanism

It is achieved by decreasing the value of coefficient vector $\vec{a}$ from 2 to 0 in (3.3) over the course of iterations. The vector $\vec{A}$ becomes greater than 1 or less than −1 in due course of time. By setting the values $\vec{A}$ in the range [−1, 1], the position of search agent can be expounded in between the original and the current best position of search agent. Fig. 3.1(a) shows the positions of humpback whale from current co-ordinate (X, Y) to best optimum co-ordinate (X^*, Y^*) in 2D space.



(a)



(b)

Fig. 3.1 Bubble-net search mechanism in WOA (X^* is the best solution obtained so far) [95]. (a) shrinking encircling mechanism. (b) spiral updating position.

3.3.2 Spiral Updating Position Mechanism

The spiral updating position mechanism calculates the distance between the whale located at (X, Y) and prey located at (X^*, Y^*) as shown in Fig. 3.1(b). A spiral equation is created between the position of whale and prey to mimic the helix-shaped movement of humpback whales as follows:

$$\vec{X}(j+1) = \vec{D}' e^{pq} \cdot \cos(2\pi q) + \vec{X}^*(j) \tag{3.5}$$

where $\vec{D}' = \vec{X}^*(j) - \vec{X}(j)$ specifies the distance of the i^{th} humpback whale to the search prey, p is a constant which outlines the shape of the logarithmic spiral, q is a random number in the interval [−1, 1] and r denotes a random number in the interval [0, 1].

Assuming, 50% probability to select either the shrinking encircling or the spiral technique, the mathematical model for updating the position of humpback whale is given as

$$\vec{X}(j+1) = \begin{cases} \vec{X}_P(j) - \vec{A}.\vec{D} & if\ r \leq 0.5 \\ \vec{D}' \cdot e^{pq} \cdot \cos(2\pi q) + \vec{X}^*(j) & if\ r \geq 0.5 \end{cases} \tag{3.6}$$

where $\vec{D}' = \vec{X}^*(j) - \vec{X}(j)$ specifies the distance of the i^{th} humpback whale to the search prey, p is a constant which outlines the shape of the logarithmic spiral, q is a random number in the interval [−1, 1] and r denotes a random number in the interval [0, 1].

3.3.3 Search for prey

The adaptation of $\vec{A}$ vector is exploited to search the prey. $\vec{A}$ becomes greater than 1 or less than −1 in due course of time to emphasize exploration for achieving global search. The mathematical model for search of prey is given as

$$D = \left|\vec{C} \cdot \vec{X}_{rand} - \vec{X}\right| \tag{3.7}$$

$$\vec{X}(j+1) = \vec{X}_{rand} - \vec{A}.\vec{D} \tag{3.8}$$

where $\vec{X}_{rand}$ is a random whale position vector.

3.4 Merits of WO Algorithm

WO algorithm has better performance as compared to reported optimization algorithms in terms of exploitation, exploration ability and ability to get rid of the local minima. In the initial step of the algorithm, the whales try to move randomly around each other using (3.5). In the next step, the whales update their positions rapidly and move along a spiral shaped route in the direction of the best path that has been found so far using (3.6). Since these two stages are completed independently and in half iteration each, WOA has inherent property to get rid of the local minima.

3.5 Limitation of WO Algorithm

The encircling mechanism in WO algorithm mostly focuses on the exploration in the search space. As a result, WO has less capability to jump out from local optima, in case it falls in it. The convergence rate and speed depend only on one control parameter *a* and it has an excessive impact on the performance of WO [96]. Hence, WO has poor convergence speed in both exploration and exploitation phases. A balancing formulation mechanism between exploration and exploitation is required.

3.6 Proposed Modifications in WO Algorithm

To improve the convergence speed in both exploration and exploitation phase and to avoid possible local optima stagnation during encircling mechanism, a local search algorithm, called chaotic search mechanism is combined with WO to enhance the rate of convergence and avoid it from being stuck at local optima [112]. The evolved method is named as modified WO (MWO) in this work. A proper balance between exploration and exploitation is necessary in MWO due to its stochastic nature. MWO balances the exploration by

modifying the position co-efficient to an exponentially decaying function. Generally, higher exploration of search space results in lower probability of local optima stagnation. More exploration causes higher randomness and will probably not give good optimization results. Basic exploration and exploitation prevent the algorithm from finding global optima and results poor rate of convergence. Therefore, there must be a balance between exploration and exploitation. The proper balance between exploration and exploitation guarantees accurate estimation of the global optima. In MWO, the transition between them is obtained by the adaptive values of *A* and *a*. The function which gives the exponential decay for *a* during the iterations is given as

$$a = 2\left(1 - \frac{m}{n}\right) \tag{3.9}$$

where *m* indicates the maximum number of iterations and *n* is the current iteration. The numbers of iterations used for exploration and exploitation are 60% and 40% respectively.

The theory of nonlinear chaos has widely been used in different applications in last decade [112]. Dynamical chaotic systems are able to control unsteady intermittent gestures. In basic WOA, search agents are distributed irregularly in the search space because of their random initializations. The irregular distributions might provide a better start of the algorithm. However, the lack of ergodicity makes the algorithm trapped in local optimum. WOA with chaotic search technique has been applied in this work for the improvement of search efficiency and the reduction of the possibility of being trapped at the local optima. The chaotic equation used in MWO is defined as

$$x_{j+1} = \mu . x_j \left(1 - x_j\right) \tag{3.10}$$

where x_j is a variable ($j = 0,1,2\cdots$) and μ is the control parameter.

The procedure of chaotic local search is described as

$$cx_j^{n+1} = \mu . cx_j^n \left(1 - cx_j^n\right) \tag{3.11}$$

where cx_j^n represents the chaotic variable. *n* represents the iteration number.

The procedures of MWO is depicted in Fig. 3.2 and listed as follows:

Step 1: Set $n = 0$ and map the decision variables x_j^n from the interval ($x_{\min, j}, x_{\max, j}$) to chaotic variables cx_j^n using

$$cx_j^{n+1} = \frac{x_j^n - x_{min,\, j}}{x_{max,\, j} - x_{min,\, j}} \tag{3.12}$$

Step 2: Determine the chaotic variables cx_j^{n+1} for the next iteration using 3.9.

Step 3: Convert the chaotic variables cx_i^{n+1} to decision variables x_j^{n+1} using

$$x_j^{n+1} = x_{min,\, j} + cx_j^{n+1}(x_{max,\, j} - x_{min,\, j}) \tag{3.13}$$

Step 4: The new solutions are evaluated with variables x_j^{n+1}.

Step 5: If the new solution achieves better performance or the maximum number of iterations is reached, take the new solution as chaotic local search; or else, modify $n = n + 1$ and go back to Step 2.

The procedure for explaining the optimisation problem using MWO is as follows:

Step 1: Initialise MWO parameters between upper and lower limits.

Step 2: Generate initial population randomly.

Step 3: Calculate fitness value of each whale in the population and sort it according to their fitness values to choose best fit search agent.

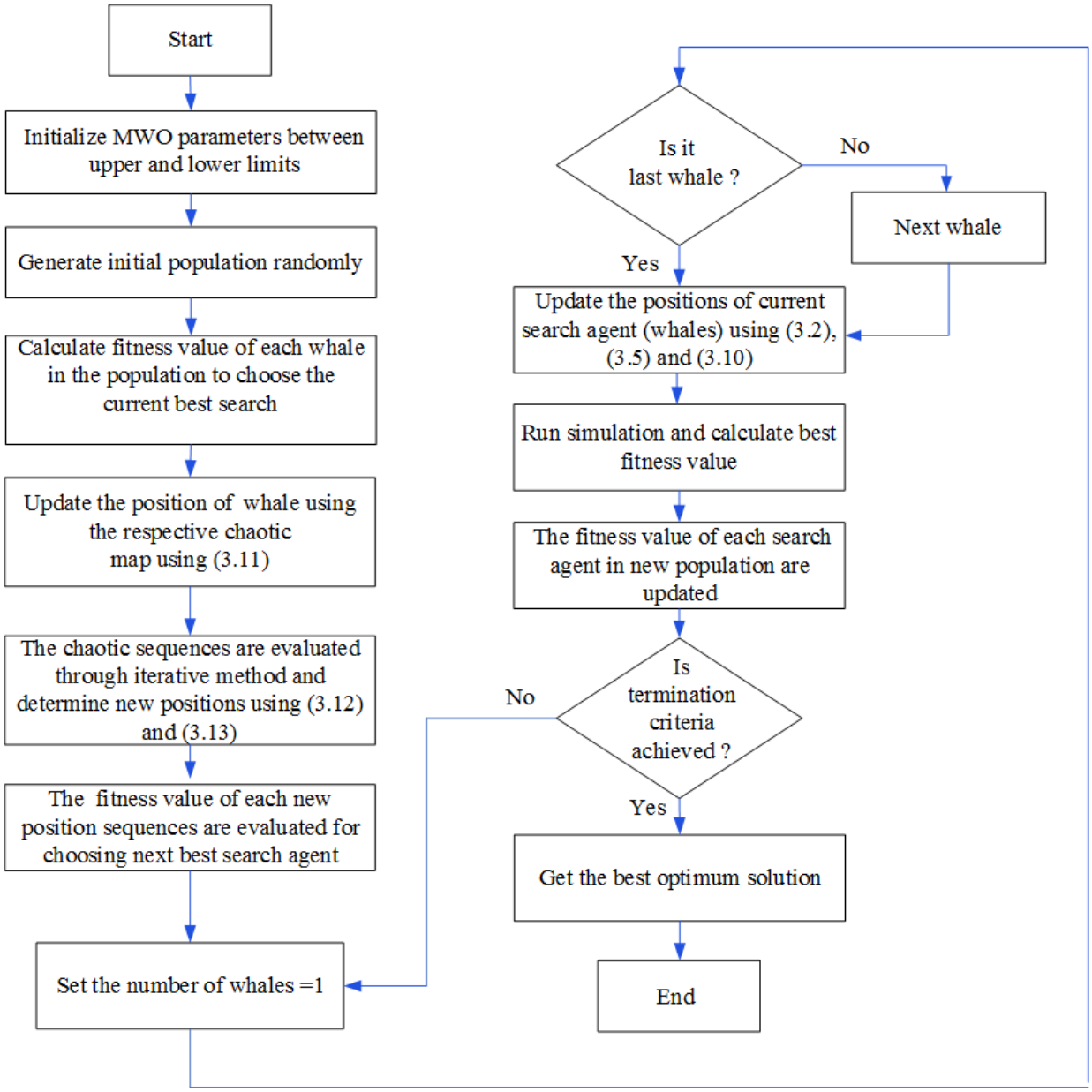


Fig. 3.2 Description of MWO algorithm.

Step 3: Calculate fitness value of each whale in the population and sort it according to their fitness values to choose best fit search agent.

Step 4: The position of whale is mapped into chaotic variables using (3.12).

Step 5: The chaotic sequences are evaluated through iterative technique and converted chaotic sequences represented as new positions using (3.11) and (3.13).

Step 6: The fitness of new position sequences is evaluated.

Step 7: Update co-efficient *A* and *C* in (3.3) and (3.4) and the parameter *a*, *q* and *r* in (3.7) and (3.6).

Step 8: For ($r < 0.5$)

If ($|A| < 1$), The position of the current search agent is updated using (3.2).

else ($|A| > 1$) Select a random search agent (X_{rand}) and the position of the current search agent is updated using (3.10).

Step 9: For ($r > 0.5$)

The position of the current search agent is updated by (3.5).

Step 10: Update the fitness values of each search agent till global optima is achieved.

Step 11: Check the boundary limit of the search agent.

3.7 Application of MWO Based SHE-PWM in HC-MLI

The proper objective function *f* is represented by the following mathematical equation

$$f = \min\left\{\left(100\frac{V_1^* - V_1}{V_1^*}\right)^4 + \frac{1}{5}\left(50 \times \frac{V_5}{V_1}\right)^2 + \frac{1}{7}\left(50 \times \frac{V_7}{V_1}\right)^2 + \frac{1}{11}\left(50 \times \frac{V_{11}}{V_1}\right)^2 + \frac{1}{13}\left(50 \times \frac{V_{13}}{V_1}\right)^2\right\} \quad (3.14)$$

subjected to

$$0 \leq \theta_1 \leq \theta_2 \ldots \theta_n < \frac{\pi}{2} \quad (3.15)$$

The main objective is to minimize (3.14) to maintain actual fundamental voltage component (V_1) close to the desired value (V_1^*) and to eliminate 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonic components from the output voltage. From (3.14), it can be observed that harmonic

components are reversely weighted to their harmonic orders (1/5, 1/7, 1/11 and 1/13) in the fitness function to give more importance to eliminate lower order harmonics. The number of iterations and population size in the algorithm are chosen as 200 and 150 respectively. The algorithm starts with the random initialization of whales (switching angles) and the fitness of each whale is evaluated. Exponentially decaying position co-efficient balances exploration versus exploitation. The algorithm is run for different modulation indices till the termination criteria is achieved. The plot of switching angles against modulation index (m_a) is shown in Fig. 3.3. The graph of the value of fitness function versus m_a is shown Fig. 3.4.

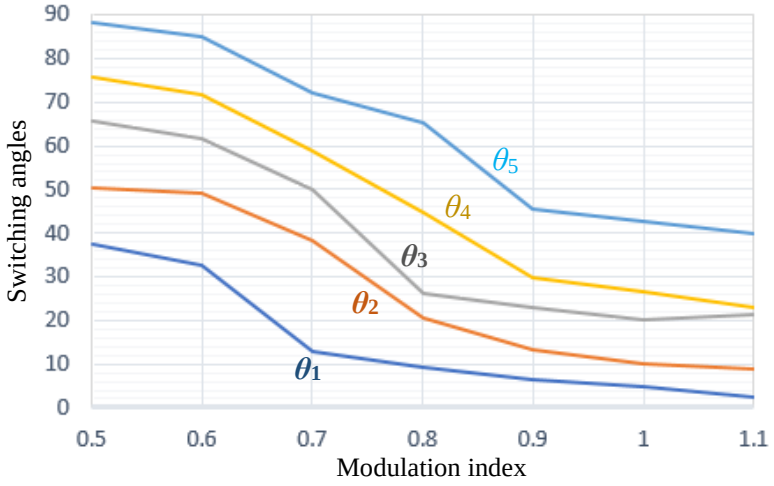


Fig. 3.3 Obtained switching angles at different m_a.

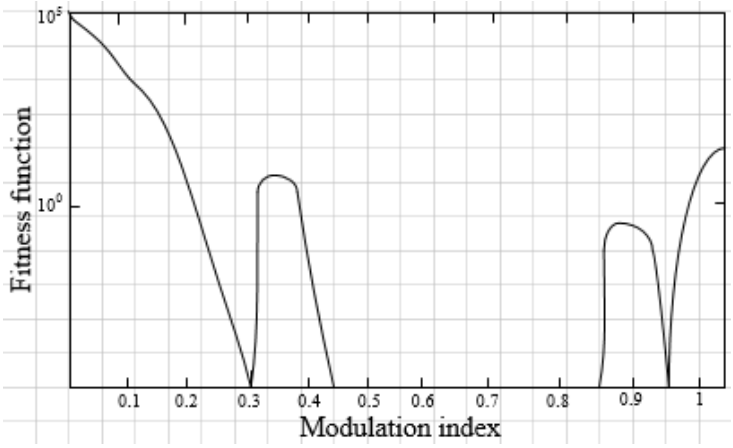


Fig. 3.4 Fitness function value versus m_a.

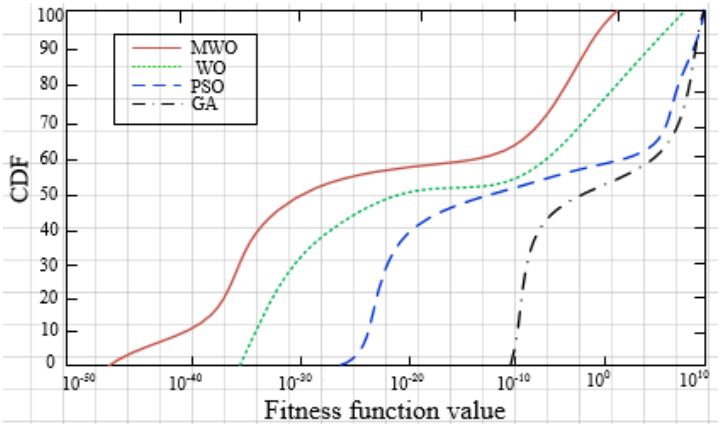
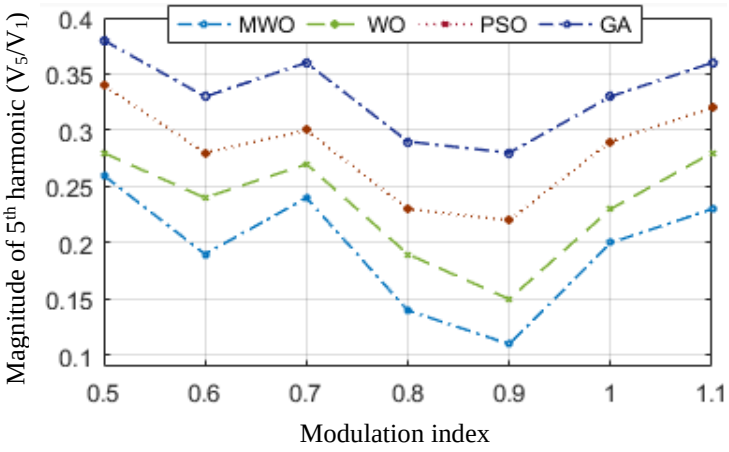
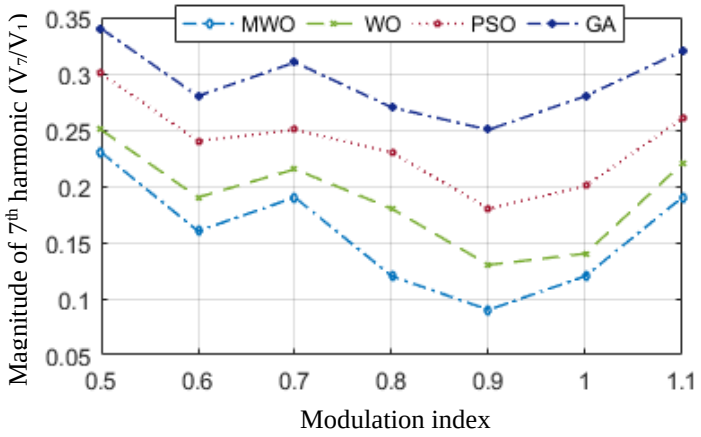


Fig. 3.5 Rate of convergence comparison of WO, PSO and GA algorithms.

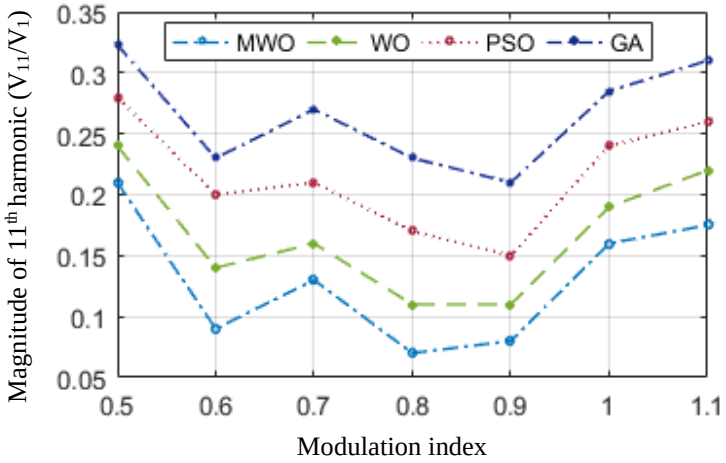
In order to compare the convergence rates, the comparison plot of cumulative distribution function (CDF) versus optimum fitness values for algorithms MWO, WO, PSO and GA are shown in Fig. 3.5. It can be observed from Fig. 3.5 that MWO has the highest CDF value, which confirms its higher probability of convergence as compared to other algorithms. Fig. 3.6(a)-10(d) show the magnitude of 5th, 7th, 11th and 13th harmonic components of the output line voltage with respect to fundamental component (V_5/V_1, V_7/V_1, V_{11}/V_1 and V_{13}/V_1) versus modulation index. It can be observed that 5th, 7th, 11th and 13th harmonic components are lowest for MWO and highest for GA.



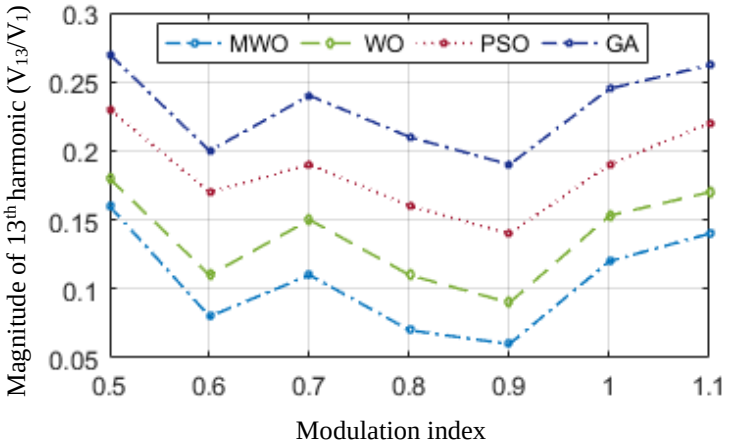
(a)


MWO
WO
PSO
GA
Magnitude of 7th harmonic (V7/V1)
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0.5
0.6
0.7
0.8
0.9
1
1.1
Modulation index

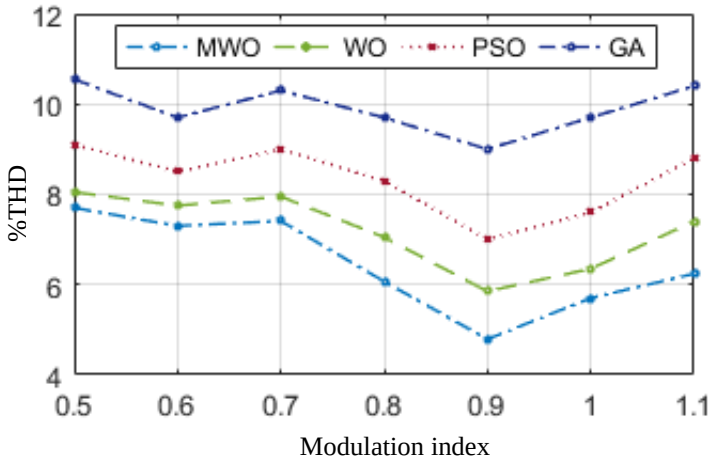
(b)


MWO
WO
PSO
GA
Magnitude of 11th harmonic (V11/V1)
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0.5
0.6
0.7
0.8
0.9
1
1.1
Modulation index

(c)


MWO
WO
PSO
GA
Magnitude of 13th harmonic (V13/V1)
0.3
0.25
0.2
0.15
0.1
0.05
0.5
0.6
0.7
0.8
0.9
1
1.1
Modulation index

(d)



(e)

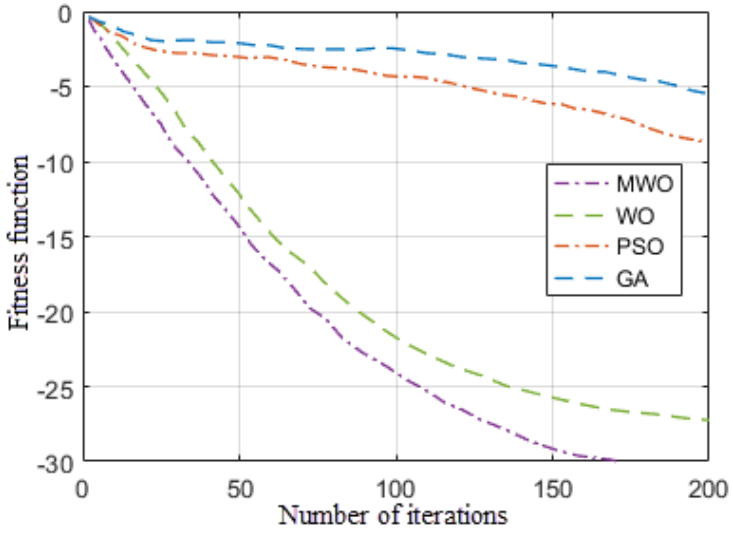
Fig. 3.6 Comparison between harmonics of different algorithms (GA, PSO, WO and MWO). (a) Magnitude of 5th harmonic. (b) Magnitude of 7th harmonic. (c) Magnitude of 11th harmonic. (d) Magnitude of 13th harmonic. (e) %THD of GA, PSO, WO and MWO.

Table 3.1
Parameters of MWO, WO, GA and PSO
No. of Iteration=200 and Population size =100 at (m_a=0.7)

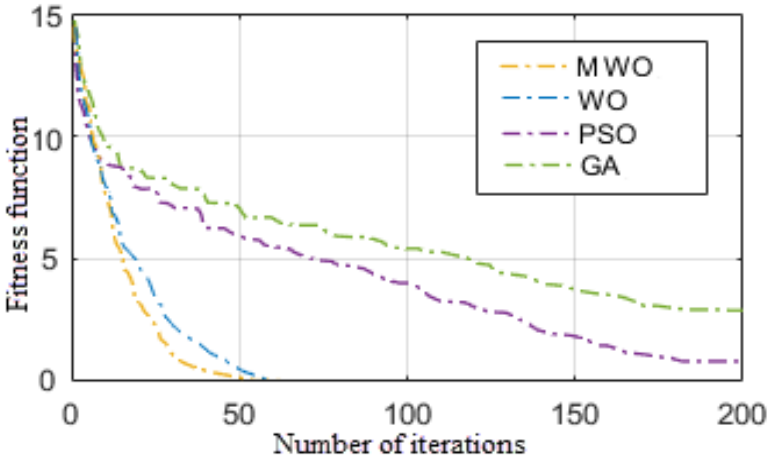
Parameters	MWO	WO	PSO	GA
Fitness value	$6.7X10^{-30}$	$4.7X10^{-10}$	$5.3X10^{-2}$	0.0624
Convergence rate	Very high	High	High	Low
Rank of convergence	1	2	3	4
Computational time (sec)	1.312	1.168	1.712	3.146

Fig. 3.6(e) shows the of % total harmonic distortion (THD) of output line voltage comparison of MWO, WO, PSO and GA at different modulation indices. It can be observed %THD is least in case MWO among the algorithms compared. The comparison of fitness values and convergence rate of different algorithms are given in Table 3.1. So, the computational time required for digital MWO is slightly complicated in comparison to WO because this

algorithm is a combination of global exploration and local exploitation. It can be inferred from Table 3.1 that the computational time for MWO is less as compared to GA and PSO algorithms. However, the proposed MWO gives improved results than WO, PSO and GA in terms of possibility of attaining global optima, higher rank of convergence, higher fitness value and harmonic content for the same population size and number of iterations.



(a)



(b)

Fig. 3.7 Convergence plots of MWO, WO, PSO and GA. (a) Sphere function. (b) Rosenbrock function.

In order to compare different algorithms, standard test functions are used to measure the convergence speed. The Sphere and Rosenbrock functions are used to measure the convergence speed or the number of iterations required for convergence [113]. For Sphere and Rosenbrock function dimension, range and minimum value of function ($f_{\min}$) are taken as 30, [-100, 100], 0 and 30, [-30, 30], 0 respectively. The plot of fitness function versus number of iterations required are shown in Fig. 3.7(a) and 11(b) respectively. It can be concluded from Fig. 3.7 that MWO finds global solution more effectively with lesser number of iterations as compared to WO, PSO and GA. Hence, the convergence speed of MWO is fastest among the different algorithms compared.

3.8 Simulation Studies

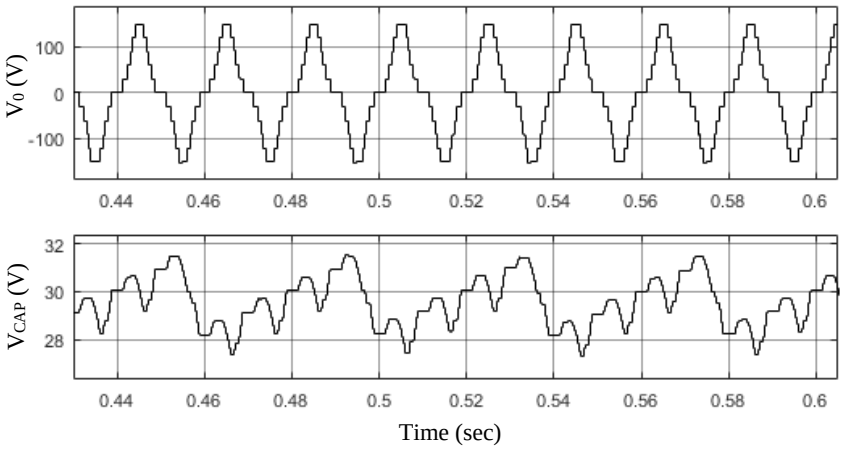
In order to verify the proposed work, three-phase, 11-level HC-MLI has been simulated in MATLAB/Simulink environment using proposed MWO algorithm.

3.8.1 Working at $m_a = 0.6$

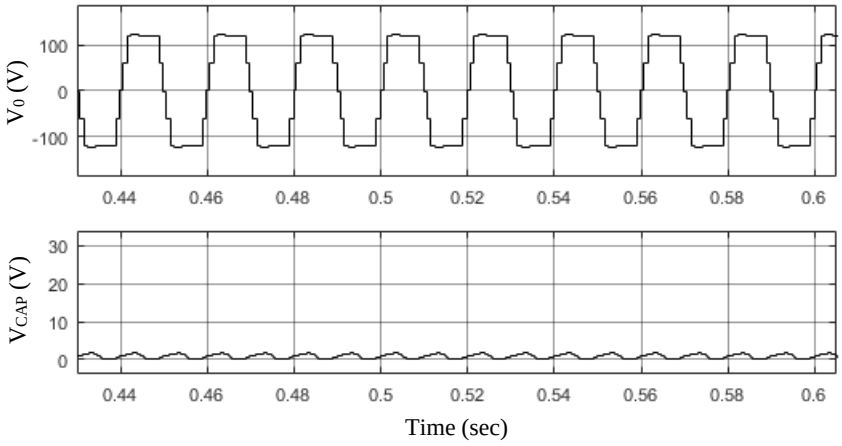
From Fig. 3.3, the switching angles that are obtained are $\theta_1 = 32.43$, $\theta_2 = 49.21$, $\theta_3 = 61.45$, $\theta_4 = 71.68$ and $\theta_5 = 85.31$. The output voltage waveform V_0 of HC-MLI and the waveform of capacitor voltage V_{cap} are shown in Fig. 3.8(a). The capacitor voltage is balanced at 30 V.

3.8.2 Working at $m_a = 1.1$

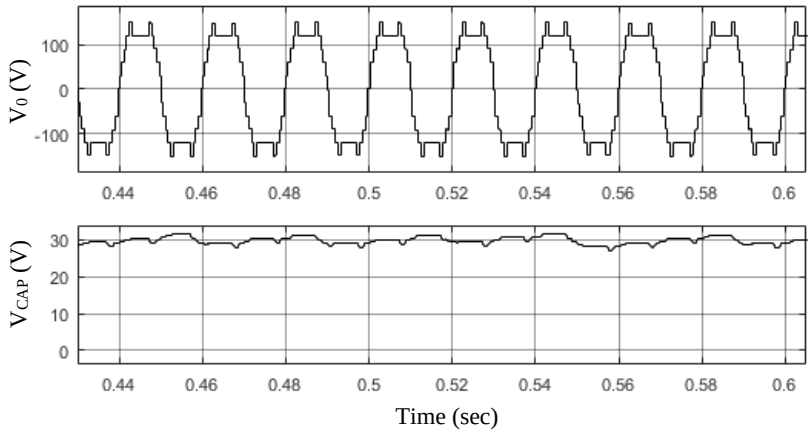
Similarly, for $m_a = 1.1$, the switching angles are obatained are $\theta_1 = 2.41$, $\theta_2 = 8.67$, $\theta_3 = 21.35$, $\theta_4 = 23.12$ and $\theta_5 = 39.84$. These switching angles will not satisfy the capacitor voltage criteria. Hence, in order to balance the capacitor, a third harmonic voltage is injected as discussed in section 2.6.2 of chapter 2. Output voltage V_0 and capacitor voltage V_{CAP} without and with capacitor balance are shown in Fig. 3.8(b) and 3.8(c) respectively. The average value of the capacitor voltage also gets balanced at 30 V for higher modulation index.



(a)

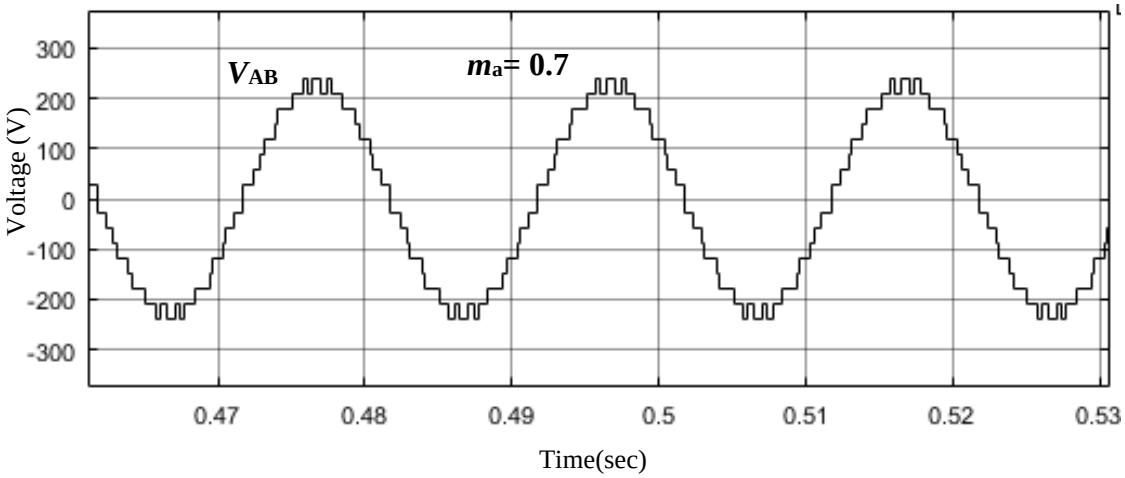


(b)

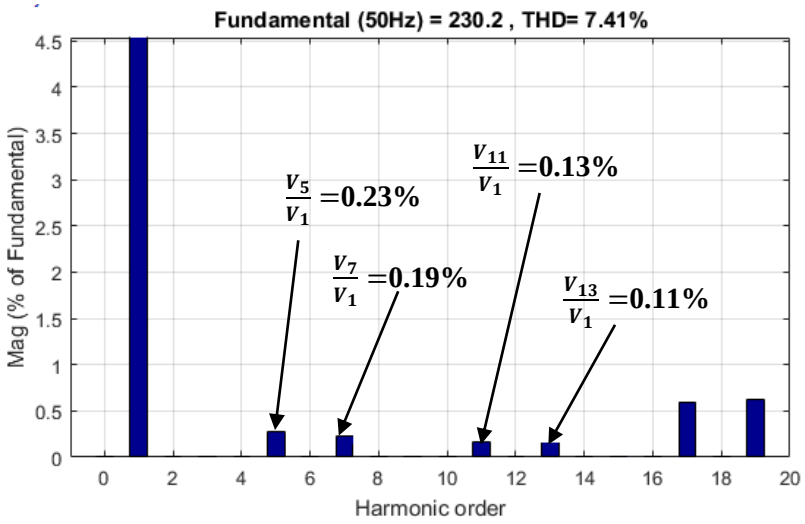


(c)

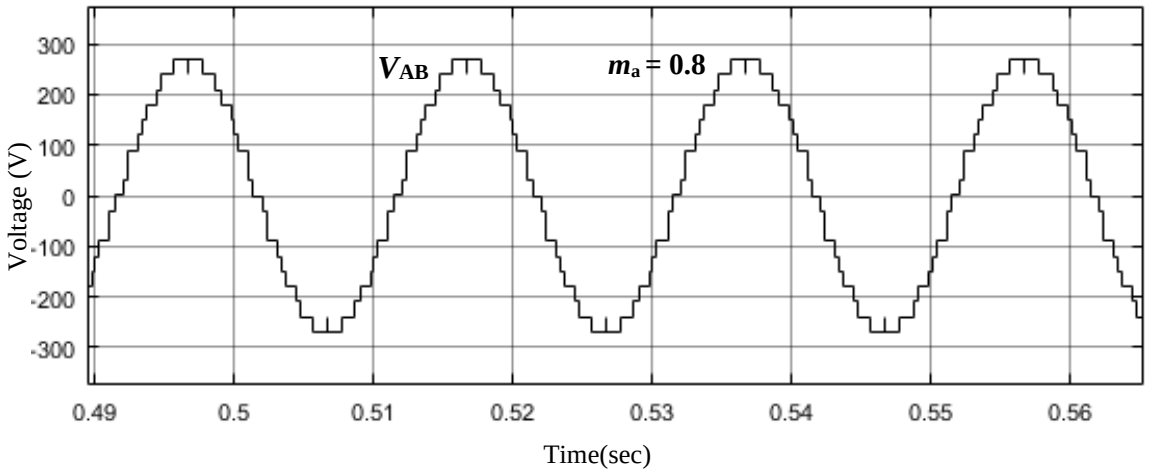
Fig. 3.8 Simulation results of MWO optimized HC-MLI for capacitor voltages. (a) V_0 and V_{CAP} for modulation index (m_a) = 0.6. (b) V_0 and V_{CAP} for m_a = 1.1 in case of unbalanced condition of capacitor. (c) V_0 and V_{CAP} for m_a = 1.1 at balanced capacitor voltage.


V_{AB}
m_a= 0.7
Voltage (V)
Time(sec)

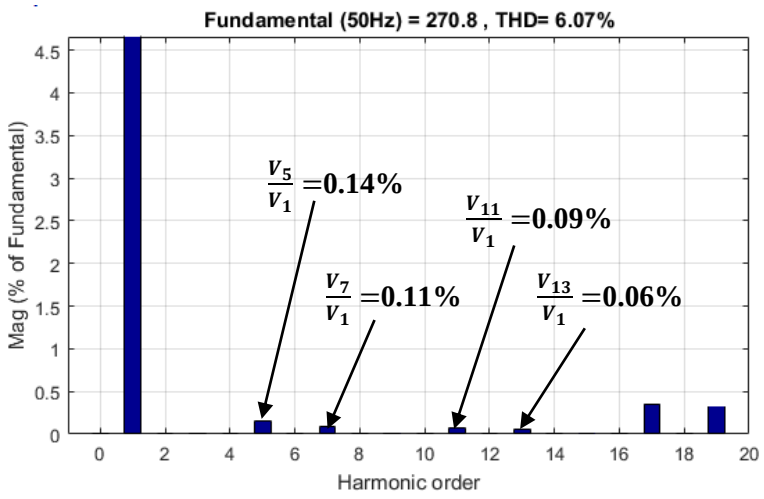
(a)


Fundamental (50Hz) = 230.2 , THD= 7.41%
Mag (% of Fundamental)
Harmonic order
$\frac{V_5}{V_1}$ =0.23%
$\frac{V_7}{V_1}$ =0.19%
$\frac{V_{11}}{V_1}$ =0.13%
$\frac{V_{13}}{V_1}$ =0.11%

(b)


V_{AB}
m_a = 0.8
Voltage (V)
Time(sec)

(c)



(d)

Fig. 3.9 Simulation results of HC-MLI (Line voltages and harmonic spectrum). (a) Output voltage V_{AB} at $m_a = 0.7$. (b) Harmonic spectrum at $m_a = 0.7$. (c) Output voltage V_{AB} at $m_a = 0.8$. (d) Harmonic spectrum at $m_a = 0.8$.

The output line voltage (V_{AB}) and their corresponding harmonic spectrums depicting magnitude of lower order harmonics (5^{th},7^{th}, 11^{th} and 13^{th}) are shown in Fig. 3.9. The simulation results of output line voltage and its harmonic analysis for $m_a = 0.7$ are shown in Fig. 3.9(a) and (b) and for $m_a = 0.8$ are shown in Fig. 3.9(c) and (d) respectively.

3.9 Experimental Verification

A 1.5 kW laboratory prototype is used to verify the performance of the proposed MWO optimized three-phase, 11-level HC-MLI, as shown in Fig. 2.24 of chapter 2. The phase voltages (V_A, V_B and V_C) of HC-MLI for resistive load at $m_a = 0.6$ are shown in Fig. 3.10(a) and measured as 88.52 V. The balancing of capacitor voltage at higher modulation index is investigated experimentally. The phase A voltage (V_A) at $m_a = 1.1$ is shown in Fig. 3.10(b) and three phase voltages (V_A, V_B and V_C) are shown in Fig. 3.10(c) and measured as 111.62 V. The capacitor voltage is balanced at 30 V. Hence, it confirms the balancing of capacitor voltage at higher m_a. For *R-L* load (R=12 Ω and L= 37 mH), the output voltage V_A and output

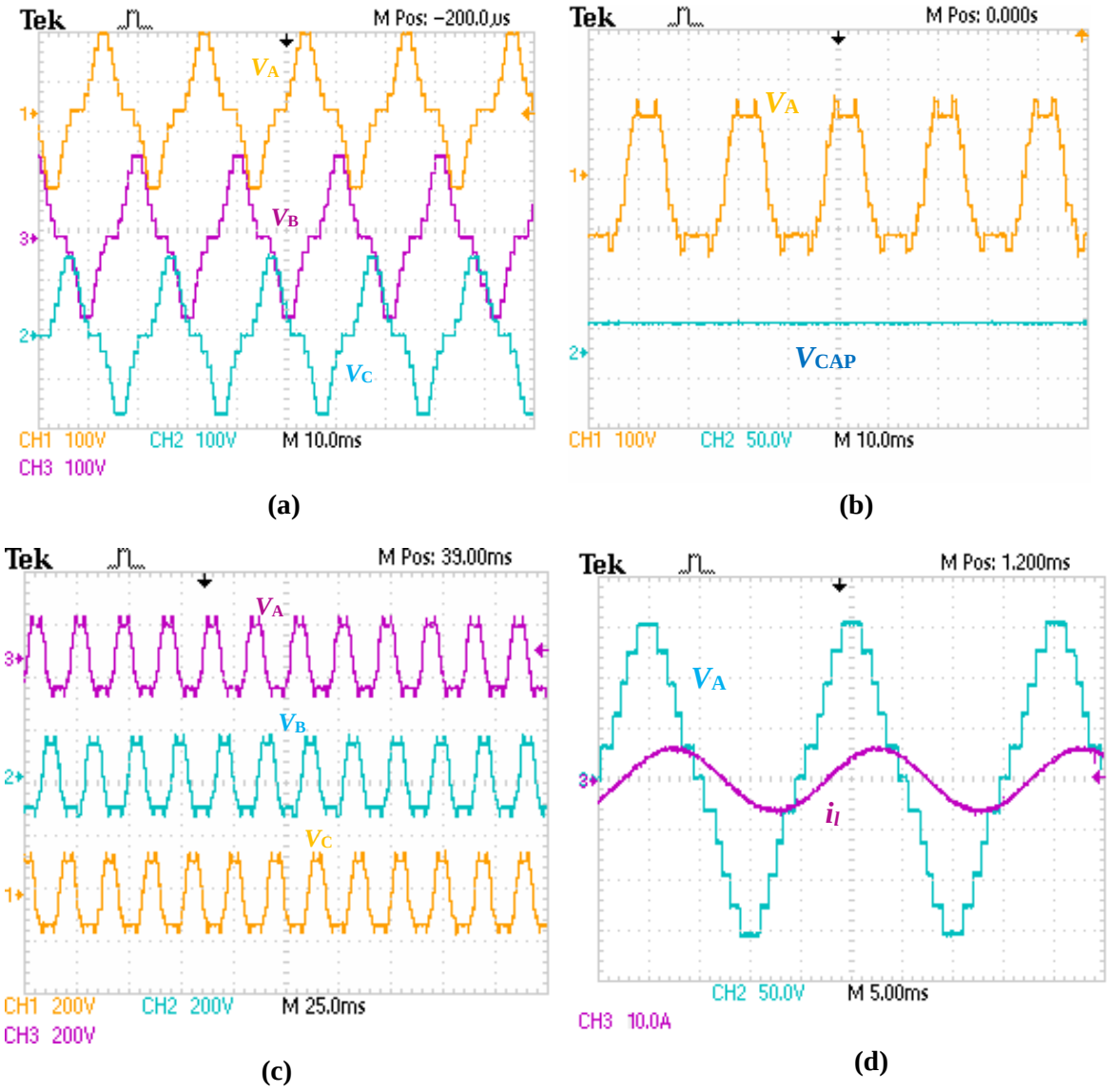


Fig. 3.10 Experimental results (Phase voltages).
(a) V_A, V_B and V_C for $m_a = 0.6$. (b) V_A for $m_a = 1.1$. (c) V_A, V_B and V_C for $m_a = 1.1$. (d) i_l for inductive load (R=12 Ω and L= 37 mH) for m_a = 0. 6.

current I_L are shown in Fig. 3.10(d). The line-line voltage (V_{AB}) of the MWO optimized HC-MLI at $m_a = 0.7$ is shown in Fig. 3.11(a) and measured as 174 V. The harmonic analysis of (V_{AB}) at $m_a = 0.7$ is shown in Fig. 3.11(b). It can be observed from Fig. 3.11(b) that the lower order harmonics such as 5^{th}, 7^{th},11^{th} and 13^{th} are reduced. Similarly, the line voltage (V_{AB}) for $m_a = 0.8$ is shown in Fig. 3.11(c) and its corresponding harmonic spectrum is shown in Fig. 3.11(d).

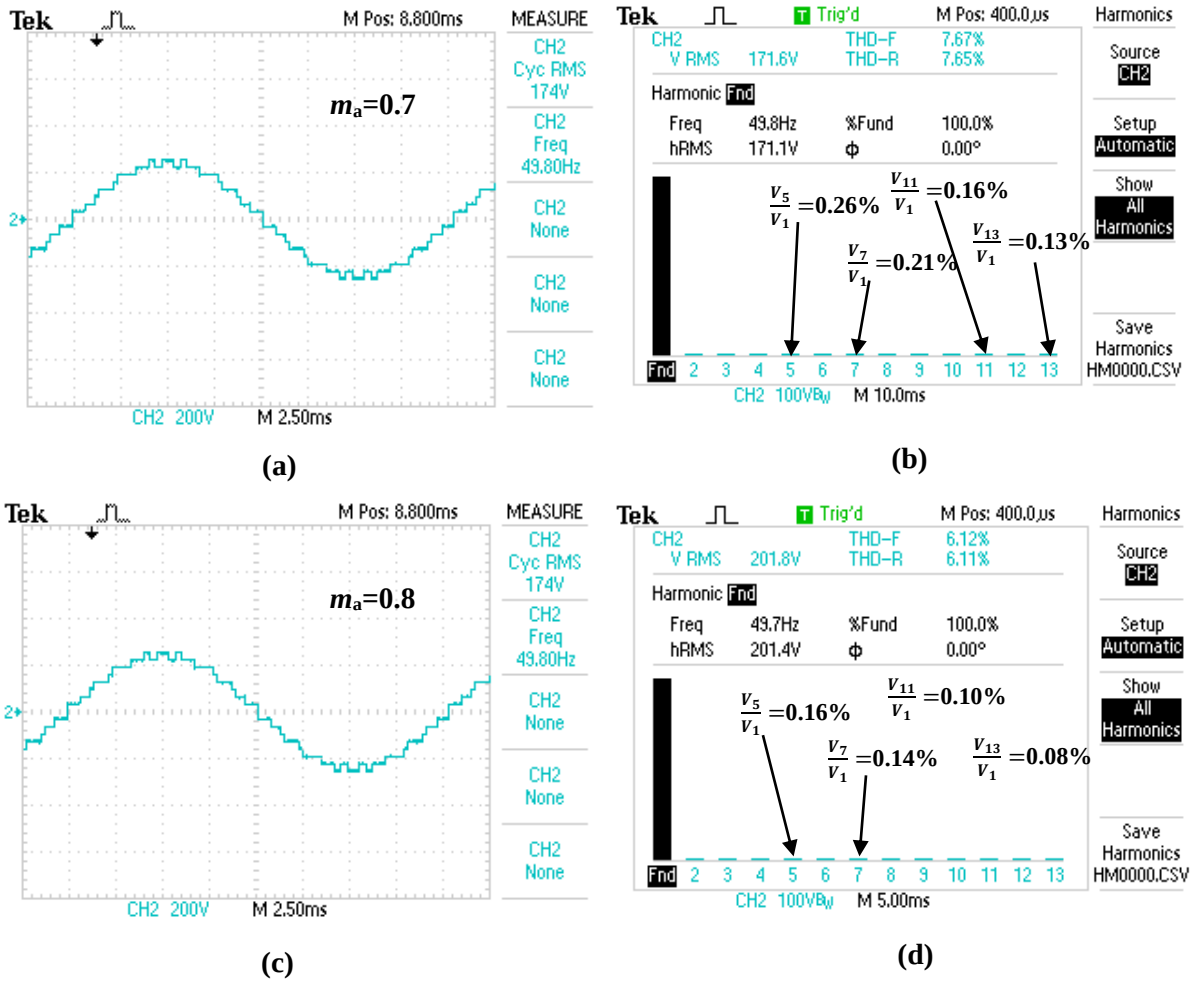
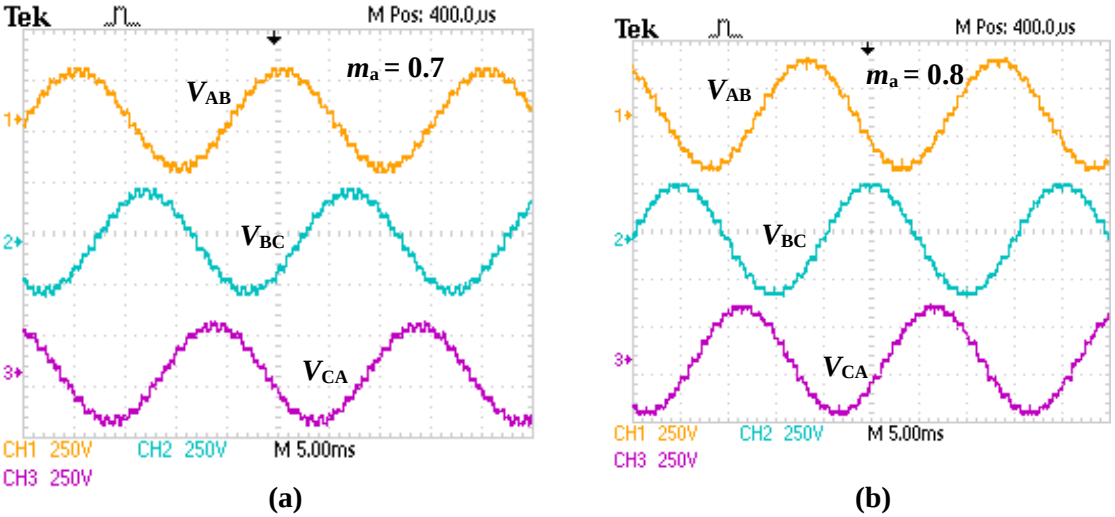
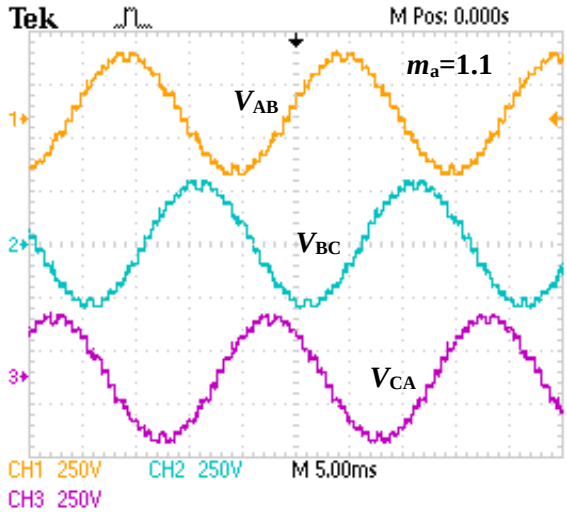


Fig. 3.11 Experimental results of HC-MLI (Line voltages and harmonic spectrums).
(a) Line-line voltage (V_{AB}) for m_a = 0.7. (b) Spectrum of harmonic analysis of V_{AB} for m_a 0.7 (c) Line-line voltage (V_{AB}) for m_a 0.8. (d) Spectrum of harmonic analysis of V_{AB} for m_a 0.8.





(c)

Fig. 3.12 Three-phase experimental results of HC-MLI.
(a) Line-line voltage (V_{AB}, V_{BC} and V_{CA}) for m_a = 0.7. (b) Voltage (V_{AB}, V_{BC} and V_{CA}) for m_a = 0.8. (c) Voltage (V_{AB}, V_{BC} and V_{CA}) for m_a = 1.1.

The harmonic magnitudes are within the IEEE Std 519-2014 [110]. Experimental results of line-line voltages (V_{AB}, V_{BC} and V_{CA}) at m_a = 0.7, 0.8 and 1.1 are shown in Fig. 3.12(a)-(c). The comparison of experimental %THD of proposed MWO with other reported optimization algorithms such as WO, PSO and GA is given in Table 3.2.

Table 3.2
Experimental %THD Comparison of Different Algorithms

Modulation index	%THD (MWO)	%THD (WO)	%THD (PSO)	%THD (GA)
0.5	7.41	8.57	10.27	13.87
0.6	6.53	7.12	9.21	12.35
0.7	6.69	7.53	9.73	12.86
0.8	6.05	6.98	7.42	11.32
0.9	4.81	5.18	6.05	10.85
1	5.83	6.17	7.09	9.87
1.1	6.24	7.71	7.71	8.05

3.10 Conclusion

In this chapter, MWO optimized three-phase, 11-level HC-MLI is presented using SHE-PWM. The use of adaptive position co-efficient vector and exponentially decaying function

in MWO gives improved results as compared to WO. In MWO, chaotic local search technique efficiently takes care of possible local optima strategy and enhances the convergence rate as compared to GA, PSO and WO. MWO also helps to obtain the global optima quickly as compared to other reported evolutionary algorithms and effectively eliminates lower order harmonics from the output voltage of HC-MLI. Moreover, the proposed MWO control strategy balances the capacitor voltage even at higher modulation index by exploiting the redundancies of HC-MLI. Simulation and experimental studies are carried out to demonstrate steady state and dynamic performance of the proposed MWO optimized three-phase HC-MLI. In order to further improve the performance in terms of speed of convergence and harmonic content, modified grey wolf optimization (MGWO) algorithm has been used in HC-MLI in the next chapter.

Chapter 4

Harmonic Minimization in HC-MLI Using Modified Grey Wolf Optimization

4.1 Introduction

In this chapter, selective harmonics elimination pulse width modulation (SHE-PWM) technique has been employed through modified grey wolf optimisation (MGWO). This optimization algorithm is then applied for the control of a three-phase, 11-level hybrid cascaded multilevel inverter (HC-MLI) [114]. SHE-PWM technique is implemented through MGWO which generates optimal switching angles for the HC-MLI, so as to eliminate lower order harmonics such as 5^{th}, 7^{th}, 11^{th} and 13^{th} from the output voltage. The capacitor voltage balance is achieved even at higher modulation indices by exploiting the redundant switching states of HC-MLI.

4.2 Mathematical Modelling of GWO Algorithm

GWO algorithm mimics the hunting mechanism and leadership hierarchy of grey wolves. GWO uses four main steps to achieve the best positions such as searching, encircling, hunting and attacking the prey [97], [98]. The algorithm consists of four types of grey wolves which are alpha (α), beta (β), delta (δ) and omega (ω). In this section, the mathematical models of the social hierarchy, encircling, search of prey, attacking prey and hunting mechanism are discussed. In order to mathematically model the social hierarchy of wolves, α is considered as the fittest solution. Consequently, the second and third best solutions are named β and δ respectively. The rest of the candidate solutions are assumed to be omega ω. In the GWO algorithm the hunting (optimization) is guided by α, β and δ.

4.2.1 Encircling Prey

The grey wolves update their positions around the prey using (4.1) and (4.2), given as

$$D = \left|\vec{C} \cdot \vec{X}_P(j) - \vec{X}(j)\right| \tag{4.1}$$

$$\vec{X}(j+1) = \vec{X}_P(j) - \vec{A}.\vec{D} \tag{4.2}$$

where j is the current iteration. X indicates the position vector of the grey wolf. X_p is the position vector of the prey. A and C are coefficient vectors. Vector A is expressed as

$$\vec{A} = 2\vec{a}.\vec{r}_1 - \vec{a} \tag{4.3}$$

and vector C as

$$\vec{C} = 2.\vec{r}_2 \tag{4.4}$$

where a is a coefficient vector. r_1 and r_2 are random vectors. The value of a linearly decreases from [2, 0] and r_1, r_2 are random vectors between [0, 1].

A two-dimensional position vector and some of the possible update co-ordinates are demonstrated in Fig. 4.1. The grey wolf in position (X, Y) can update its position according to the position of the prey (X^*, Y^*) as shown in Fig. 4.1. Different places around the best agent can be reached with respect to the current position by adjusting the value of A and C vectors.

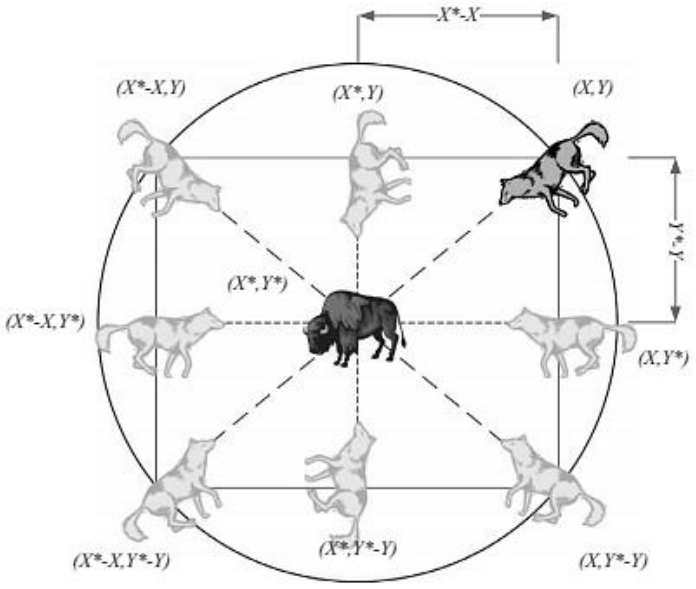


Fig. 4.1 2D vectors and their possible next locations in GWO [97].

4.2.2 Attacking Prey (Exploitation Phase)

In order to mathematically model the attacking the prey, the value of $\vec{a}$ decreased in due course iterations. The value of a linearly decreases from [2, 0] and r_1, r_2 are random vectors between [0, 1]. The value of a is within the range [1, 2] at early stage. A becomes greater than 1 or less than −1 in due course of time. This helps the grey wolves to diverge from the currently considered prey to find a better prey. When, a decreases and comes within the range [0,1], A lies in the range [−1, 1], which compels the grey wolves to move gradually towards the best position. With these operators, the GWO algorithm allows its search agents to update their position based on the location of the α, β and δ and attack towards the prey. However, the GWO algorithm is prone to stagnation in local solutions with these operators.

4.2.3 Search for Prey (Exploration Phase)

Grey wolves mostly search according to the position of the α, β and δ wolves. They diverge from each other to search for prey and converge to attack prey. In order to mathematically model exploration, the value of $\vec{A}$ is set at a value greater than 1 or less than -1. This emphasizes exploration and allows the GWO algorithm to search globally. Fig. 4.2(a) shows that $|\vec{A}| < 1$ forces the wolves to attack the prey and Fig. 4.2(b) shows that $|\vec{A}| > 1$ forces the grey wolves to diverge from the prey.

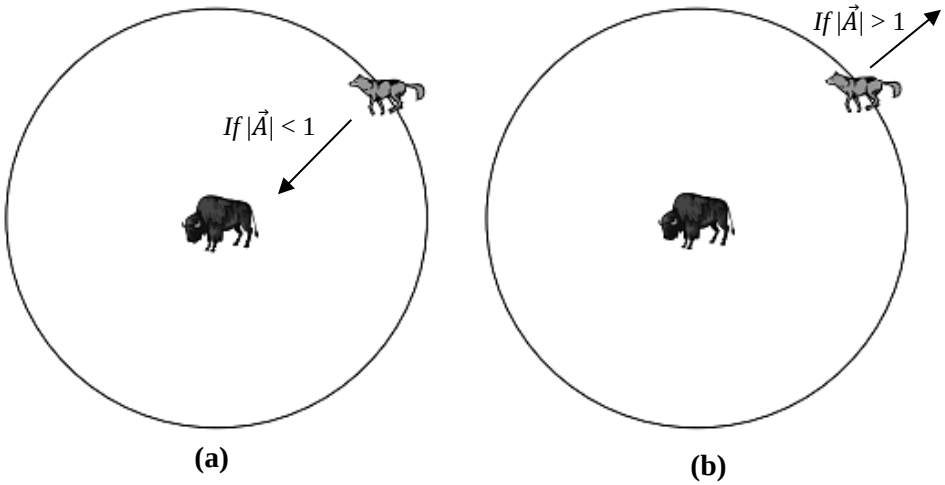


Fig. 4.2 Attacking prey versus searching for prey [98].

Hence, the optimal solution tends to diverge from the prey when, $\vec{A} > 1$ and converge towards the prey when $\vec{A} < 1$.

4.2.4 Hunting Mechanism

Grey wolves have the ability to recognize the location of prey and encircle them. The hunting is usually guided by α wolf. The β and δ wolves might also participate in hunting occasionally. In order to obtain the global optima more quickly, GWO improves the current best solution by using a weighting method. In GWO, the position update expression is weighted in every iteration as given in (4.7) and coefficient vectors are obtained using (4.5) and (4.6), where A_1, A_2 and A_3 are calculated using (4.3).

$$\begin{aligned} \overrightarrow{D}_\alpha &= \left|\vec{C}_1 \cdot \vec{X}_\alpha - \vec{X}\right| \\ \vec{D}_\beta &= \left|\vec{C}_2 \cdot \vec{X}_\beta - \vec{X}\right| \\ \vec{D}_\delta &= \left|\vec{C}_3 \cdot \vec{X}_\partial - \vec{X}\right| \end{aligned} \tag{4.5}$$

$$\begin{aligned} \vec{X}_1 &= \vec{X}_\alpha - \vec{A}_1 . \vec{D}_\alpha \\ \vec{X}_2 &= \vec{X}_\beta - \vec{A}_1 . \vec{D}_\beta \\ \vec{X}_3 &= \vec{X}_\delta - \vec{A}_1 . \vec{D}_\partial \end{aligned} \tag{4.6}$$

$$\vec{X}(j+1) = \frac{\vec{X}_1 + \vec{X}_2 + \vec{X}_3}{3} \tag{4.7}$$

4.3 Limitations of GWO

In case of conventional GWO, the location of the wolves within the entire community is updated by simple averaging of best locations. The GWO algorithm suffers from premature convergence and weak local searching ability. In order to take care this problem in the proposed work, a local search algorithm, called chaotic searching mechanism is combined with GWO to enhance the rate of convergence and avoid it from being stuck at local optima [112]. The evolved method is named as modified GWO

(MGWO) in this work. MGWO balances the exploration by modifying the position co-efficient to an exponentially decaying function. The convergence speed of the MGWO increases, when exploration is increased in comparison to exploitation. Moreover, this also avoids the local minima from being trapped. Weighted sum of best of the locations is taken instead of simple average of positions to achieve global optima.

4.4 Modified GWO Algorithm

The proper balance between exploration and exploitation guarantees accurate estimation of the global optima. Basic exploration and exploitation prevent the algorithm from finding global optima and also results into local optima stagnation. Generally, higher exploration of search space results in lower probability of local optima stagnation. Too much exploration is similar to too much randomness and will probably not give good optimization results. A right balance between these two exploration and exploitation can guarantee an accurate approximation of the global optimum. Thus, a balance between exploitation and exploration is a must. In MGWO, the transition between exploration and exploitation is generated by the adaptive values of a and A. In MGWO, half of the iterations are devoted to exploration ($|A| \geq 1$) and the other half are used for exploitation ($|A| < 1$). Exponential functions are used instead of linear function to decrease the value of a over the course of iterations. The function which gives the exponential decay for a during the iterations of MGWO is given as

$$a = 2\left(1 - \frac{m^2}{n^2}\right) \tag{4.8}$$

where m indicates the maximum number of iterations and n is the current iteration. The numbers of iterations used for exploration and exploitation are 60% and 40%, respectively.

GWO with chaotic search technique has been applied in this paper for the improvement of search efficiency and the reduction of the possibility of being trapped at the local optima [112]. The chaotic equation is defined as

$$x_{j+1} = \mu . x_j \left(1 - x_j\right) \tag{4.9}$$

where x_j is a variable ($j = 0,1,2 \cdots$) and μ is the control parameter. The procedure of chaotic local search is described as

$$cx_j^{n+1} = \mu . cx_j^n \left(1 - cx_j^n\right) \tag{4.10}$$

where cx_j^n represents the chaotic variable. *n* represents the iteration number.

The procedure of chaotic local search algorithm is as follows:

Step 1: Set *n* = 0 and map the decision variables x_j^n from the interval $(x_{min,\,j}, x_{max,\,j})$ to chaotic variables cx_j^n using

$$cx_j^n = \frac{x_j^n - x_{min,\,j}}{x_{max,\,j} - x_{min,\,j}} \tag{4.11}$$

Step 2: Determine the chaotic variables cx_j^{n+1} for the next iteration using (4.9).

Step 3: Convert the chaotic variables cx_i^{n+1} to decision variables x_j^{n+1} using

$$x_j^{n+1} = x_{min,\,j} + cx_j^{n+1}(x_{max,\,j} - x_{min,\,j}) \tag{4.12}$$

Step 4: The new solutions are evaluated with variables x_j^{n+1}.

Step 5: If the new solution achieves better performance or the maximum number of iterations is reached, take the new solution as chaotic local search; or else, modify *n* = *n*+ 1 and go back to Step 2.

4.4.1 Proposed Variable Weights in MGWO

In GWO, the searching and hunting process are governed by α wolf, whereas the β wolf plays less important role and the δ wolf plays lesser important role. During hunting process, α is nearest to the prey among three grey wolves; β and δ ranks second and third. So, the position of α wolf is mainly contributed in searching new individuals, while the importance of other wolves is ignored. This means that the weight of α should be near to 1 at the beginning, while the weights of the β and δ could be near zero. At the final state, the α, β and δ wolves should encircle the prey, which means that they have equal weights. So, the weight of the α is reduced and the weights of the β and δ arise in final stage of the algorithm. The previously described (4.7) is now modified in the proposed MGWO algorithm and given as

$$\vec{X}(j+1) = w_1.\vec{X}_1 + w_2.\vec{X}_2 + w_3.\vec{X}_3 \tag{4.13}$$

where w_1, w_2 and w_3 are the corresponding weights.

The weight of α, β and δ are denoted as w_1, w_2 and w_3. The weights should always satisfy $w_1 \geq w_2 \geq w_3$. Mathematically, the weight of α is changed from 1 to 1/3 during the searching procedure. At the same time, the weights of the β and δ is increased to 1/3 from 0.

The procedure for explaining the optimization problem using MGWO is as follows:

Step 1: Initialise MGWO parameters between upper and lower limits.

Step 2: Generate initial population randomly.

Step 3: Calculate fitness value of each grey wolf in the population and sort it according to fitness values.

Step 4: Select the first, second and third best fitness values as the positions of grey wolves α, β and ω respectively.

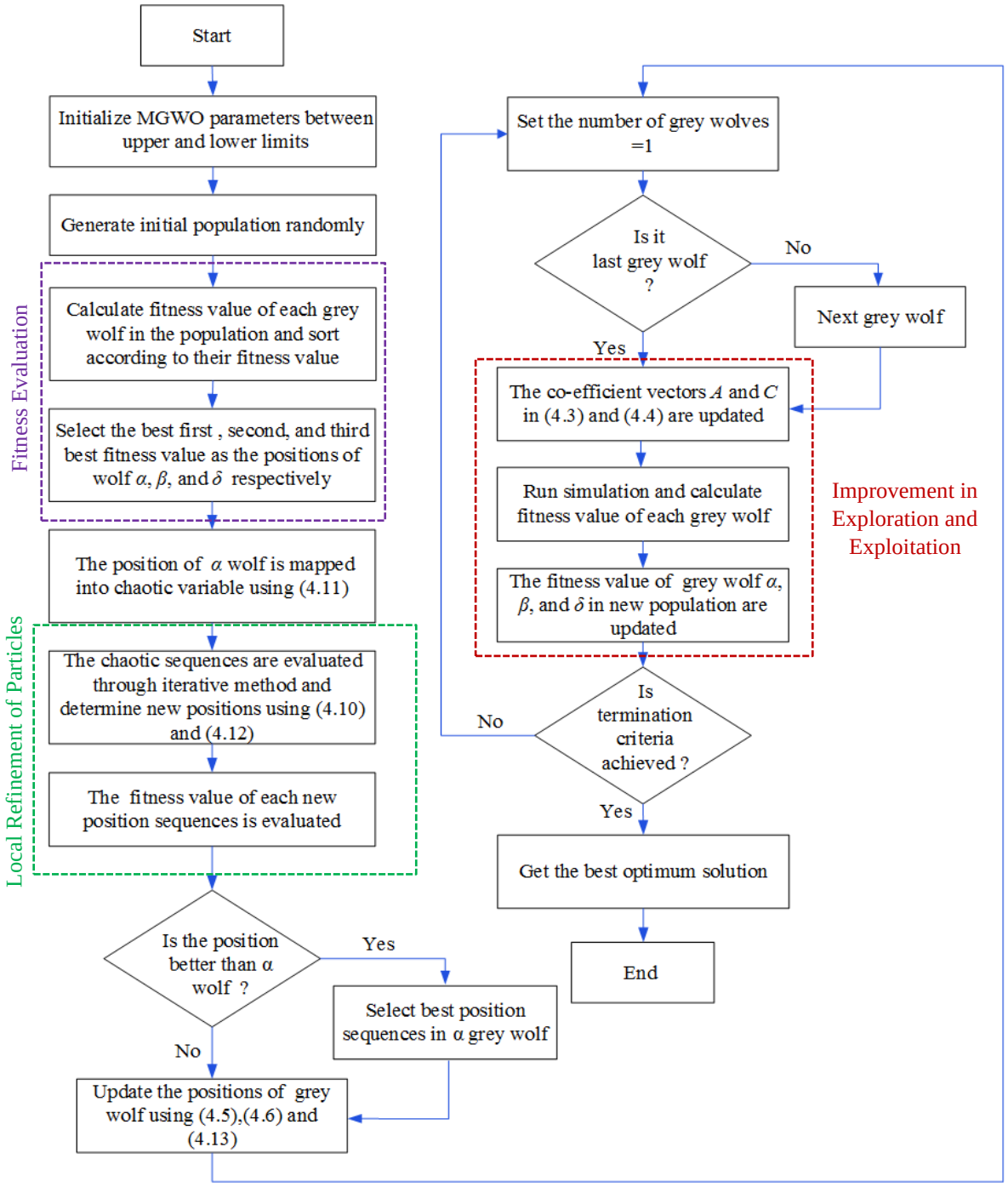


Fig. 4.3 Description of MGWO algorithm.

Step 5: The position of α wolf is mapped into chaotic variables using (4.11).

Step 6: The chaotic sequences are calculated through iterative technique and converted chaotic sequences are represented as new positions using (4.10) and (4.12).

Step 7: The fitness of new position sequences is evaluated.

Step 8: Update the positions of current grey wolves using (4.15) - (4.17).

Step 9: The co-efficient *A* and *C* in (4.5) and (4.6) and the parameter *a* in (4.13) are updated.

Step 10: The fitness values of grey wolves α, β and δ in new population are update till global optima is achieved.

Step 11: Repeat step 2 to 10, till the termination criteria is achieved.

The detailed flow chart of the optimization algorithm (MGWO) is shown in Fig. 4.3.

4.5 Implementation of SHE-PWM in MGWO Optimized HC-MLI

The proper objective function *f* is represented by the following mathematical equation

$$f = \min\left\{\left(100\frac{V_1^* - V_1}{V_1^*}\right)^4 + \sum_{s=2}^{S}\frac{1}{h_s}\left(50\frac{V_{h_s}}{V_1}\right)^2\right\} \tag{4.14}$$

subjected to

$$0 \le \theta_1 \le \theta_2 \ldots \theta_n < \frac{\pi}{2} \tag{4.15}$$

where h_s is the S_{th} harmonic order e.g., $h_2 = 5$, $h_3 = 7$, h_4=11 and h_5=15 and V_1^* represents the fundamental component of output voltage. The weighting factors $\left(\frac{1}{h_s}\right)$ defines the elimination in lower order harmonics. The number of iterations and population size in the algorithm are chosen as 200 and 100 respectively. The algorithm starts with the random initialization of wolves (switching angles) and the fitness of each wolf is then evaluated. In MGWO, chaotic iterative method is used for local refinement. Exponentially decaying position co-efficient stabilities exploration and exploitation mechanism. The algorithm is run for different modulation indices till the termination criteria is achieved. The plot of switching angles versus modulation index (m_a) is shown in Fig. 4.4. The graphs of fitness value versus modulation index for GA, PSO, GWO and MGWO are shown Fig. 4.5. The magnitude of lower order harmonics (5^{th}, 7^{th}, 11^{th} and 13^{th}) versus modulation index for the

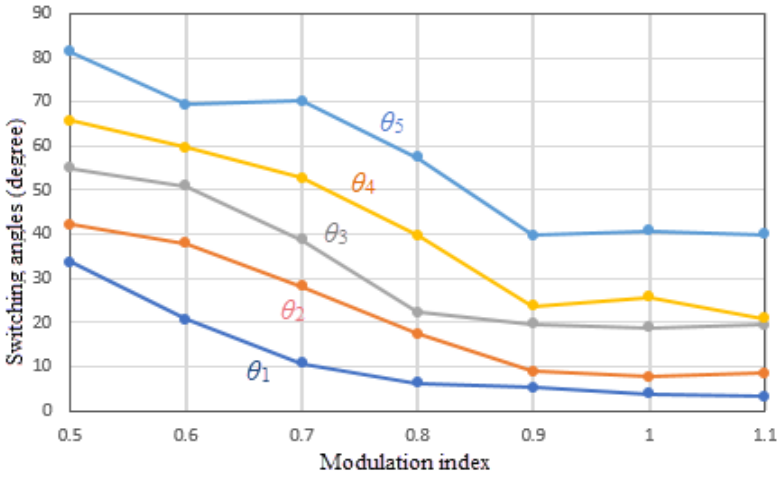


Fig. 4.4 Switching angles at different modulation index.

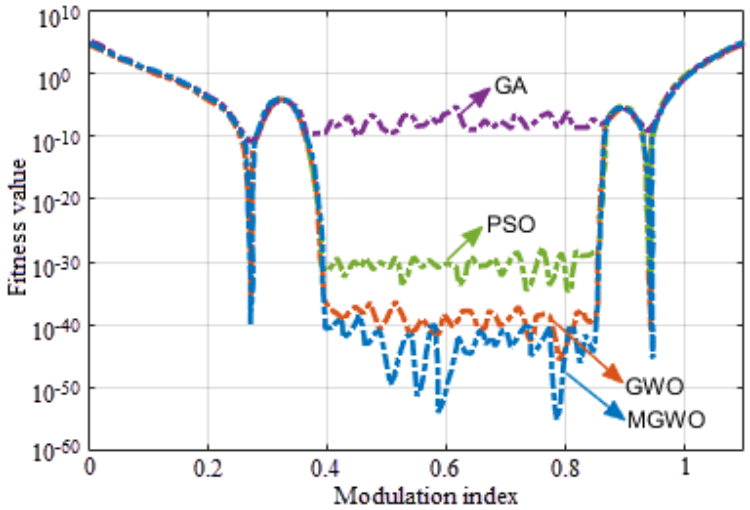


Fig. 4.5 Fitness value for MGWO, GWO, PSO and GA versus modulation index.

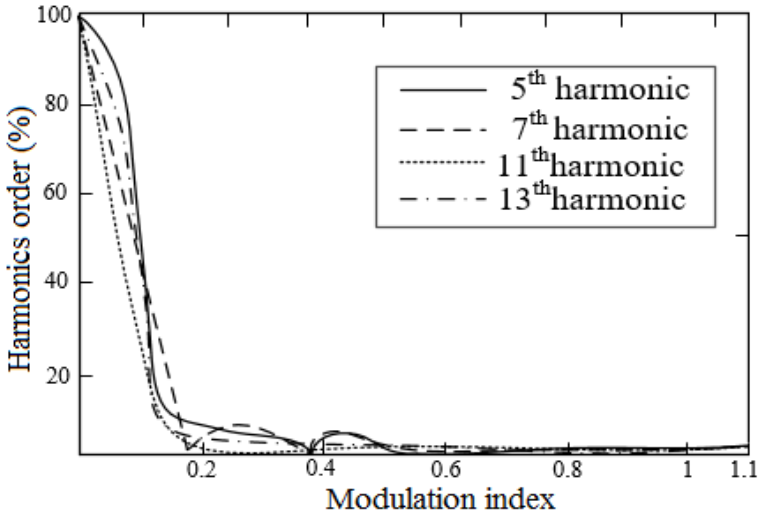


Fig. 4.6 The 5^{th},7^{th},11^{th} and 13^{th} harmonics versus modulation index.

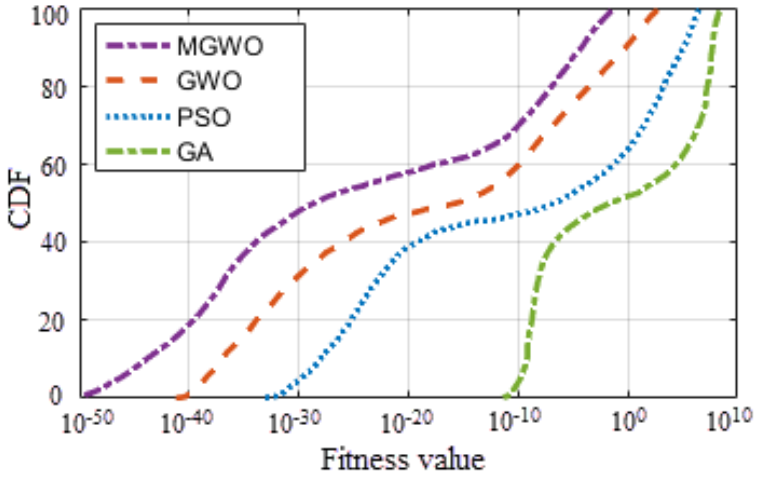


Fig. 4.7 Comparison of CDF versus fitness value for MGWO, GWO, PSO and GA.

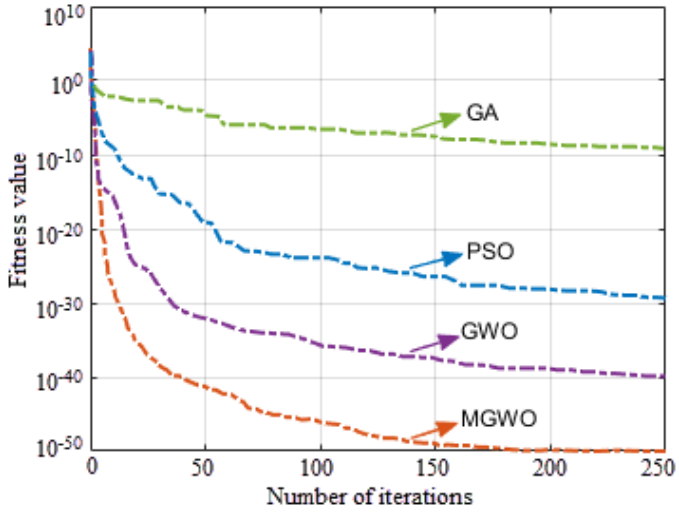


Fig. 4.8 Convergence plot of MGWO, GWO, PSO and GA versus number of iterations.

proposed MGWO are shown in Fig. 4.6. It can be observed from Fig. 4.6 that the lower order harmonics have decreased significantly. The cumulative distribution function (CDF) is evaluated to validate the usefulness of MGWO [114]. The comparison plots of CDF for GA, PSO and GWO with MGWO algorithm are shown in Fig. 4.7. The results obtained establish the superiority of MGWO in terms of rate of convergence as compared to GWO, PSO and GA. The convergence plots of fitness function versus number of iterations for MGWO, GWO, PSO and GA are shown in Fig. 4.8. It can be observed from Fig. 4.8 that the controller needs up to 200 iterations to obtain the optimal switching angle values in case of MGWO.

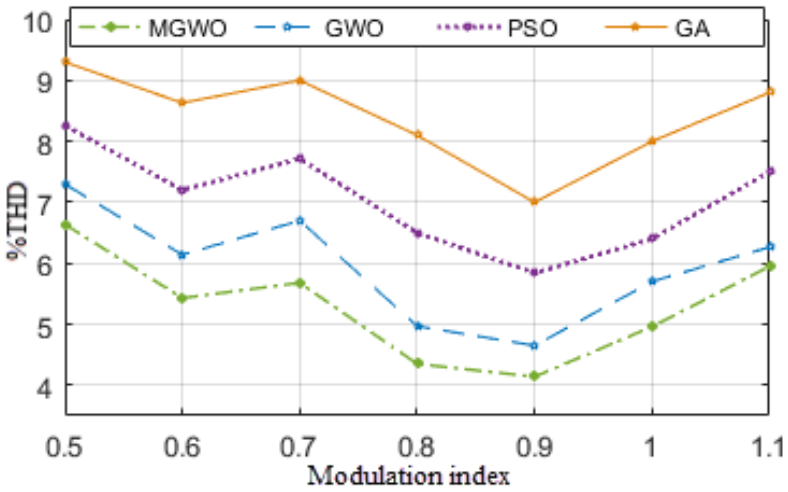


Fig. 4.9 Comparison of %THD for MGWO, GWO, PSO and GA at different modulation index.

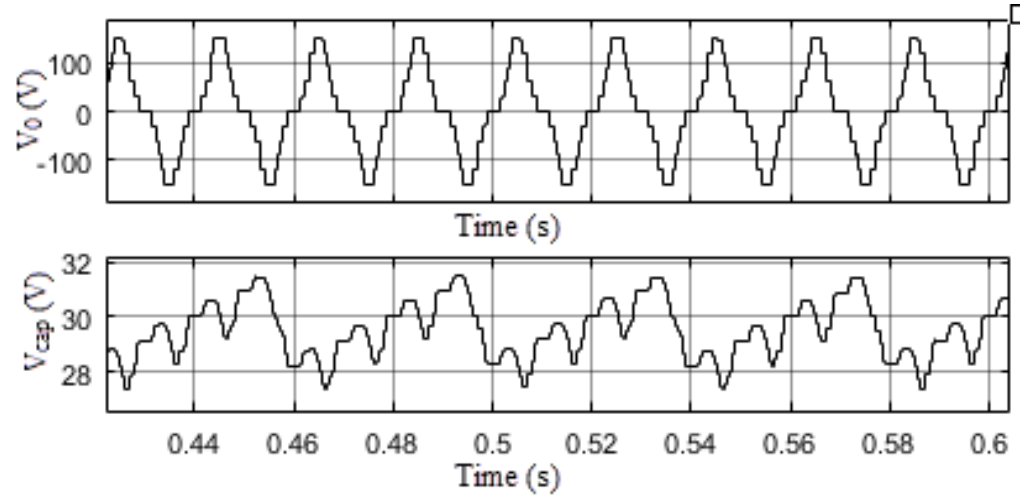
Table 4.1
Parameters of MGWO, GWO, PSO and GA
No. of iteration=200 and Population size =100 at (m_a = 0.5)

Parameters	MGWO	GWO	PSO	GA
Fitness value	$6.7X10^{-46}$	$4.5X10^{-38}$	$5.3X10^{-30}$	$6.2X10^{-10}$
Convergence rate to global optima	very high	high	high	low

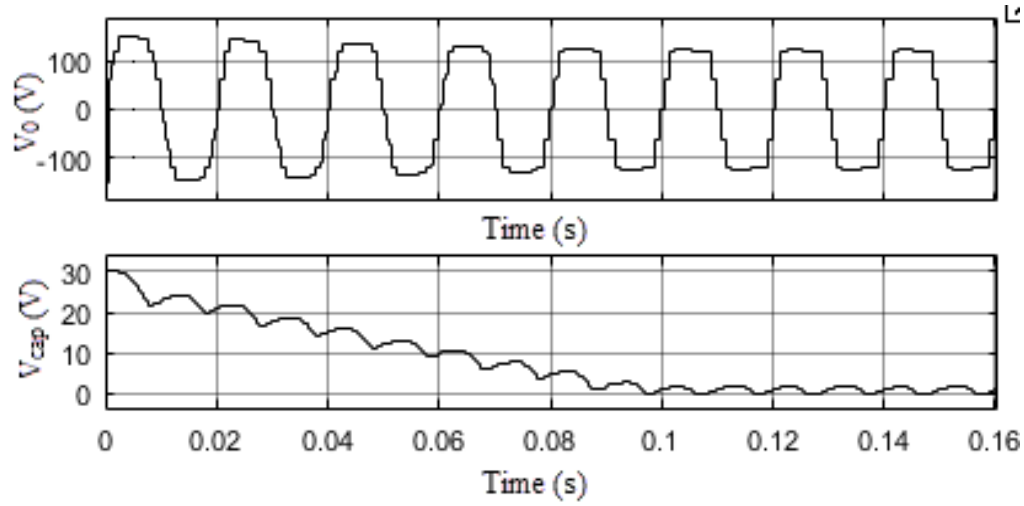
The %THD at different modulation indices for reported algorithms with proposed MGWO algorithm are shown in Fig. 4.9. The proposed MGWO optimized HC-MLI has better harmonic content than GA, PSO and GWO. The comparison of fitness values and convergence rate of different algorithms are given in Table 4.1. It can be concluded from Table 4.1 that the fitness value and convergence rate of MGWO is better than GA, PSO and GWO.

4.6 Simulation Verification

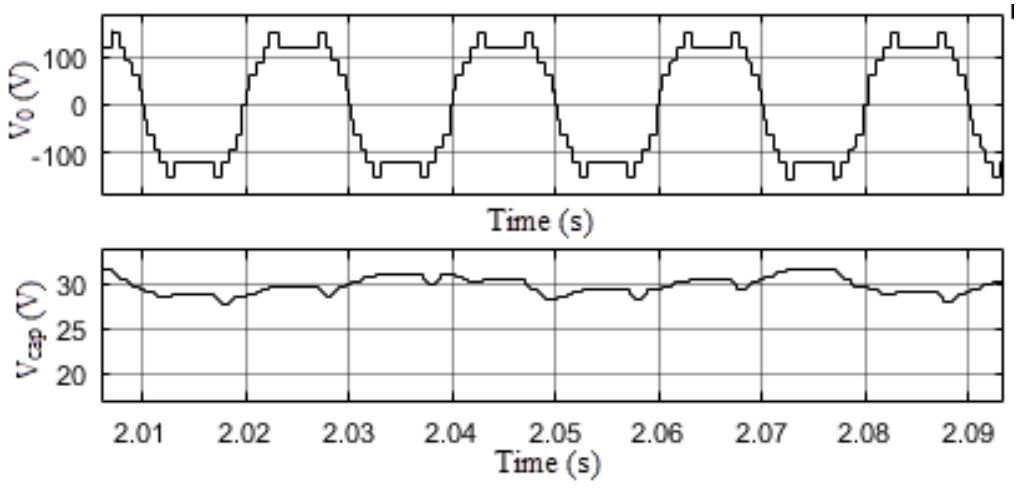
In order to verify the proposed work, a 1.5 kW three-phase, 11-level HC-MLI has been simulated in MATLAB/Simulink using proposed MGWO algorithm.



(a)



(b)



(c)

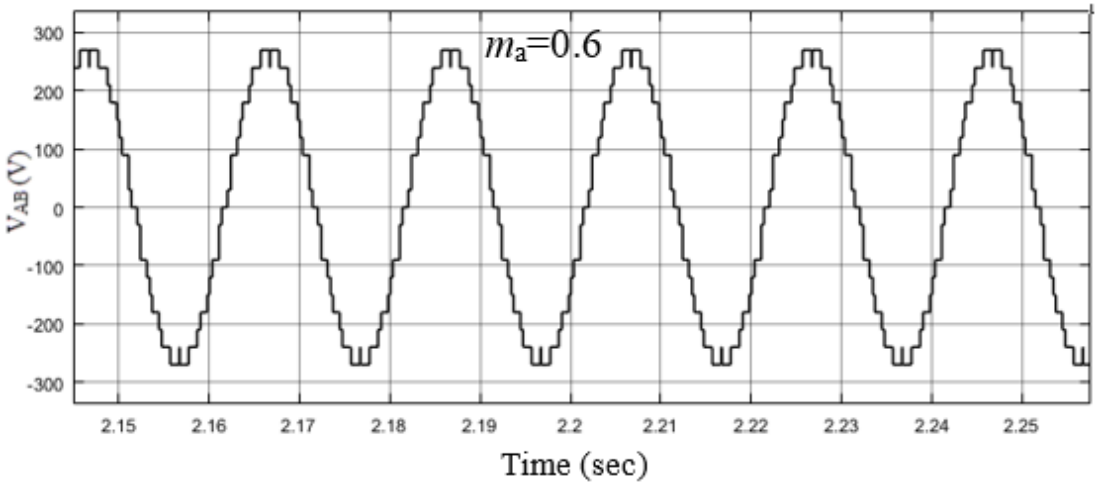
Fig. 4.10 Simulation results of MGWO optimized HC-MLI (Capacitor voltages). (a) V_0 and V_{cap} for modulation index (m_a) = 0.6. (b) V_0 and V_{cap} for m_a = 1.1 in case of unbalanced condition of capacitor. (c) V_0 and V_{cap} for m_a = 1.1 at balanced condition of capacitor voltage.

4.6.1 Operation at $m_a = 0.6$

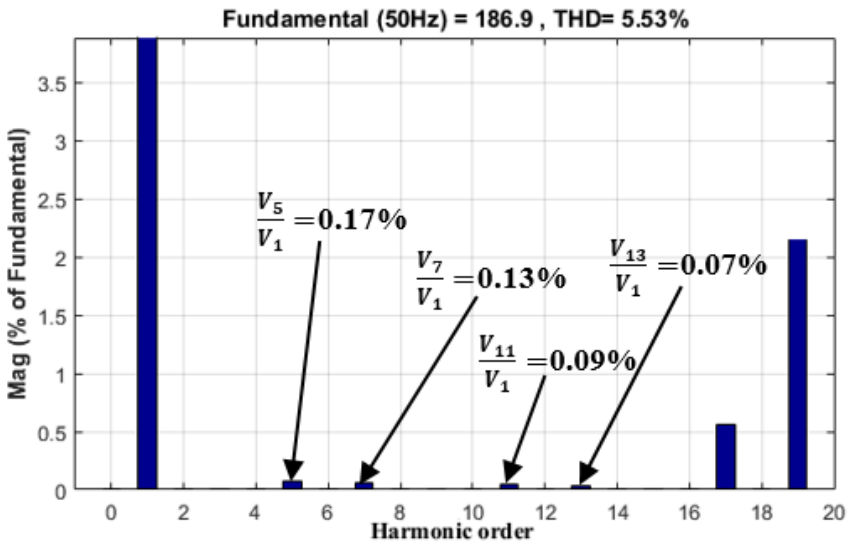
From Fig. 4.4, the switching angles are obtained as $\theta_1 = 31.75$, $\theta_2 = 45.96$, $\theta_3 = 57.54$, $\theta_4 = 68.54$ and $\theta_5 = 85.34$. The waveform of V_0 and capacitor voltage V_{cap} of the HC-MLI are shown in Fig. 4.10(a). The average voltage across the capacitor is balanced at 30 V.

4.6.2 Operation at $m_a = 1.1$

Similarly, for $m_a = 1.1$, the switching angles are obatained as $\theta_1 = 5.33$, $\theta_2 = 8.57$, $\theta_3 = 20.56$, $\theta_4 = 25.39$ and $\theta_5 = 41.58$.



(a)



(b)

Fig. 4.11 Simulation results of MGWO optimized HC-MLI (Line voltages and harmonic spectrums).
(a) Line-line voltage (V_{AB}) for m_a 0.6. (b) Spectrum of harmonic analysis of V_{AB} for m_a 0.6.

With these switching angles, it is unable balance the capacitor voltage. Hence, in order to balance the capacitor, a third harmonic voltage is injected as discussed in 2.6.2 of chapter 2. Output voltage V_0 and capacitor voltage V_{cap} without and with capacitor balance are shown in Fig. 4.10(b) and (c) respectively. The average value of the capacitor voltage also gets balanced at 30 V for higher modulation index.

The output line voltage (V_{AB}) and its harmonic spectrum at $m_a = 0.6$ are shown in Fig. 4.11(a) and (b). It can be observed from Fig. 4.11(b) that lower order dominant harmonics (5^{th},7^{th}, 11^{th} and 13^{th}) have been eliminated from the output voltage of HC-MLI.

4.7 Experimental Validation

A 1.5 kW laboratory prototype is used to verify the performance of the proposed MGWO optimized three-phase, 11-level HC-MLI, as shown in Fig. 2.24 of chapter 2. The phase voltages (V_A, V_B and V_C) for resistive load at $m_a = 0.6$ are shown in Fig. 4.12(a) and are measured as 72.5 V. For *R-L* load, the output voltage V_A and output current I_L at $m_a = 0.6$ are shown in Fig. 4.12(b). The balancing of capacitor voltage at higher modulation index is also investigated experimentally. Fig. 4.12(c) shows the output phase *A* voltage (V_A) at $m_a = 1.1$ and three phase voltages (V_A, V_B and V_C) are shown in Fig. 4.12(d) and are measured as 111.5 V. The voltage of capacitor is balanced at 30 V. Hence, it confirms the balancing of capacitor voltage at higher m_a. The line-line voltage V_{AB} of the MGWO optimized HC-MLI at m_a=0.6 is shown in Fig. 4.13(a) and measured as 168.53 V. The harmonic spectrum analysis of V_{AB} for m_a=0.6 is shown in Fig. 4.13(b). From Fig. 4.13(b), it can be observed that the lower order harmonics such as 5^{th}, 7^{th}, 11^{th} and 13^{th} are reduced. Experimental results of line-line voltages (V_{AB}, V_{BC} and V_{CA}) at higher $m_a = 1.1$ are shown in Fig. 4.14. The output voltage V_{AC} and load current I_L after connecting filter inductor is shown in Fig. 4.15(a).

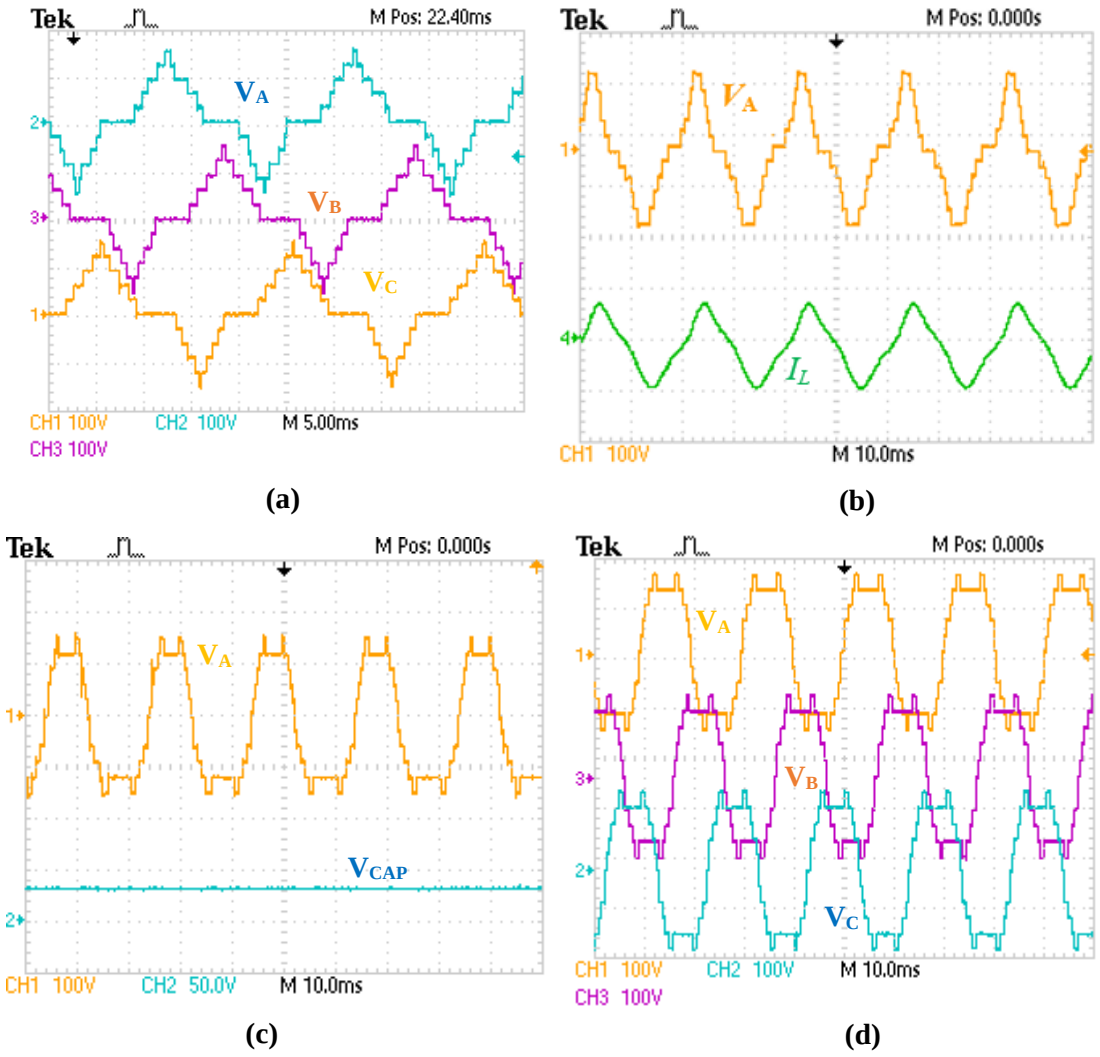


Fig. 4.12 Experimental results of MGWO optimized HC-MLI (Phase voltages).
(a) V_A, V_B and V_C for m_a 0.6. (b) V_A for inductive load for m_a 0.65. (c) V_A for m_a 1.1.(d) V_A, V_B and V_C for m_a 1.1.

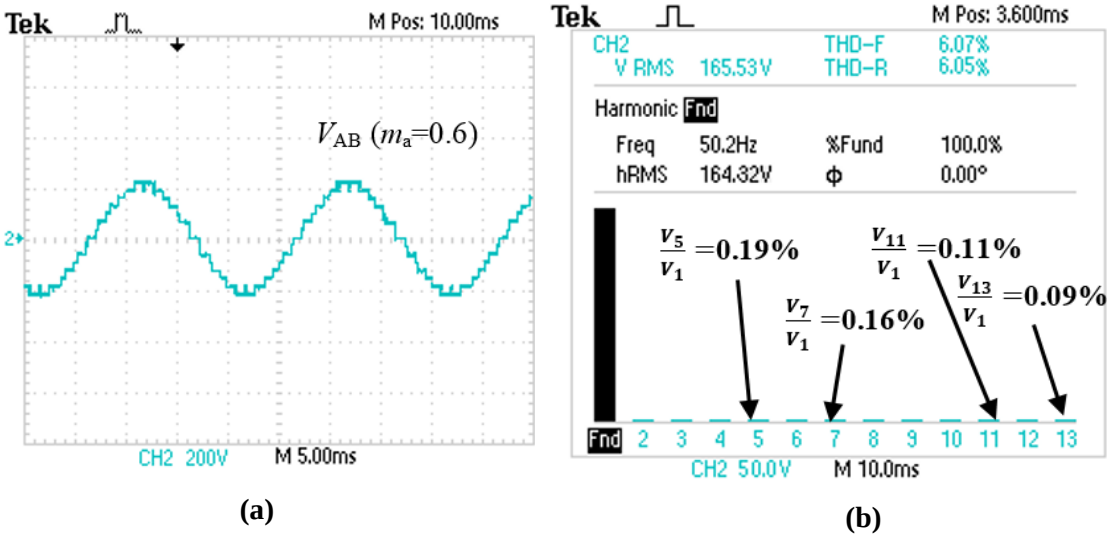


Fig. 4.13 Experimental result of line voltage at m_a 0.6.(a) Line -line voltage V_{AB} for m_a 0.6. (b) Spectrum of harmonic analysis of V_{AB} for m_a = 0.6.

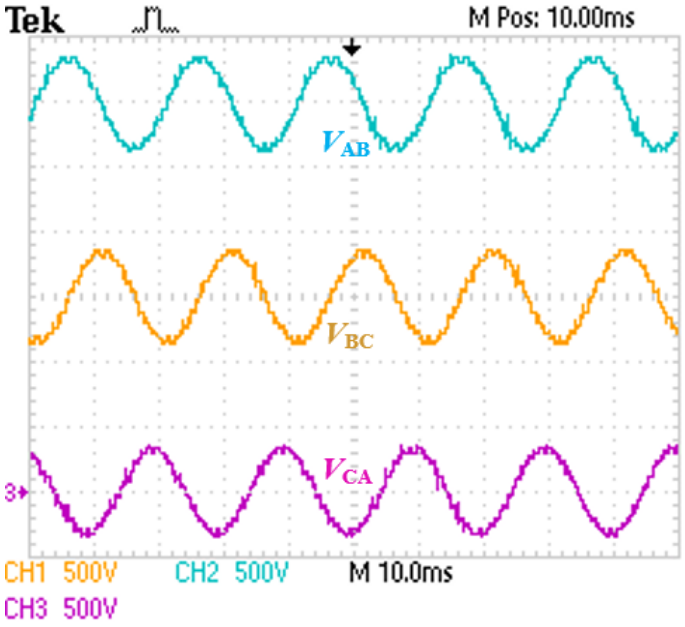
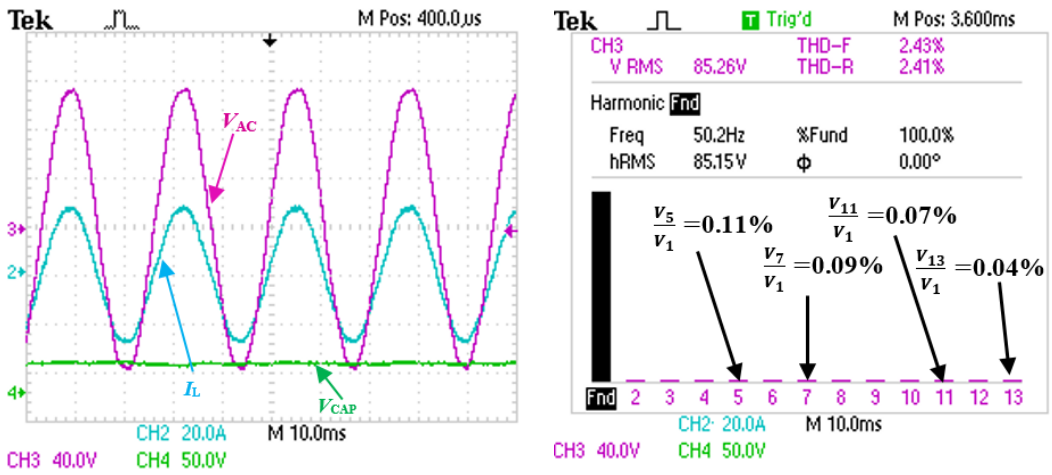


Fig. 4.14 Experimental results of MGWO optimized HC-MLI **(**Line-line voltage (V_{AB}) at m_a = 1.1).



(a) **(b)**

Fig. 4.15 Experimental result of line voltage after connecting LC filter.
(a) Line-line voltage V_{AB} and voltage of capacitor V_{CAP} for m_a = 0.6. (b) Spectrum of harmonic analysis of V_{AB} for m_a = 0.6.

The output voltage of the HC-MLI is maintained at 85.2 V using closed loop control as discussed earlier for a load current of 16.8 A. The detailed harmonic analysis of V_{AC} at m_a = 0.6 after connecting LC filter is shown in Fig. 4.15(b) and harmonic magnitudes are within the IEEE Std 519-2014 [110].

Table 4.2
Comparison Between GWO [97] and MGWO

Modulation index (m_a)	**m_a = 0.6**					**m_a = 1.1**				
Harmonic order (h_s)	5^{th}	7^{th}	11^{th}	13^{th}	% THD	5^{th}	7^{th}	11^{th}	13^{th}	% THD
GWO [97]	0.2478	0.2235	0.1526	0.1229	6.13	0.3754	0.3158	0.2613	0.2145	6.24
MGWO	0.1963	0.1642	0.1103	0.0876	5.54	0.3268	0.2416	0.2127	0.1763	6.03

4.8 Comparison Between GWO and MGWO

A comparison between GWO [97] and MGWO is made as shown in Table 4.2, containing magnitude of lower order harmonics (5^{th}, 7^{th}, 11^{th} and 13^{th}) and %THD obtained through experimentation for GWO and MGWO algorithms at modulation indices m_a = 0.6 and 1.1, respectively. It can be observed that the lower order harmonics and %THD are further reduced in MGWO in comparison to GWO.

4.9 Comparison Among MPSO, MWO and MGWO

From the results obtained in chapters 2, 3 and 4, a comparison is made among MPSO, MWO and MGWO optimized HC-MLI using SHE-PWM for the same number of iterations and population size. It has been found that the running time of MPSO is more than MWO and MGWO. MPSO is more complicated than MWO and MGWO because it is a combination of a global exploration and local exploitation, which uses a complicated differential evolution mutation strategy. In the proposed MWO, the code complexity is less and it uses leadership hierarchy mechanism to obtain better refined solution as compared MPSO. The convergence rate of MWO is better than MPSO. The computational time required for digital implementation of MWO is also less than MPSO. The proposed MGWO gives improved results than MPSO and MWO; in terms of possibility of attaining global optima, higher rank of convergence, higher fitness value and harmonic content for the same population size and number of iterations.

Table 4.3
Comparison of % THD Among Proposed MPSO, MWO and MGWO

Modulation index	MPSO (%THD)	MWO (%THD)	MGWO (%THD)
0.5	8.41	8.23	7.52
0.6	7.53	7.09	6.41
0.7	7.69	6.78	6.12
0.8	5.23	5.01	4.33
0.9	4.78	4.50	4.14
1	5.03	4.67	4.55
1.1	5.64	5.11	4.01

Table 4.4
Performance comparison of MGWO, MWO and MPSO
No. of Iteration=200 and Population size =100 at (m_a=0.7)

Parameters	MGWO	MWO	MPSO
Convergence rate	Very high	Medium	Low
Computational time (sec)	1.116	1.132	1.953

The %THD comparison among MPSO, MWO and MGWO is given in Table 4.3. Table 4.4 gives the comparison of convergence rate and computational time for MGWO, MWO and MPSO. It can be observed from Tables 4.3 and 4.4 that the proposed MGWO gives better result in terms of harmonic content, convergence rate, and computational time.

4.10 Conclusion

In this chapter, MGWO optimized three-phase, 11-level HC-MLI is presented using SHE-PWM. The use of adaptive position co-efficient vector and exponentially decaying

function in MGWO gives improved results as compared to GWO. In MGWO, chaotic local search technique efficiently takes care of local optima, while weighted position control strategy enhances the convergence rate as compared to GA, PSO and GWO. MGWO also helps to obtain the global optima quickly as compared to GA, PSO and GWO and effectively eliminates lower order harmonics from the output voltage. Moreover, the proposed MGWO control strategy balances the capacitor voltage even at higher modulation indices by exploiting the redundancies of HC-MLI. The steady state and dynamic performance of the proposed MGWO optimized HC-MLI has been validated through simulation and experimentation. Further, a comparison among MPSO, MWO and MGWO has been carried out, which confirms the superiority of MGWO in terms of harmonic minimization and convergence rate.

It has been found that balancing of capacitor voltage is an inherent challenge in HC-MLIs. Several control schemes have been reported in the literature to achieve capacitor voltage balance in HC-MLIs, which makes the overall control complicated. The control schemes become even more complicated with the increase in number of output voltage levels of the HC-MLIs, as the increase in output voltage levels require more active and passive components along with increased number of DC voltage sources. Switched-capacitor multilevel inverters (SC-MLIs) have emerged in recent years as a promising MLI to counter these problems. SC-MLIs use lesser active and passive components along with reduced number of DC voltage sources as compared to HC-MLI. Also, the capacitor voltage is balanced inherently in SC-MLIs, without using extra control circuits and therefore the switching scheme is simple as compared to HC-MLI. The SC-MLIs given in literature are explored and two new topologies of them, namely diode assisted switched-capacitor MLI (DASC-MLI) and reduced voltage stress switched capacitor MLI (RVSC-MLI) are proposed using MGWO in the next two chapters.

Chapter 5

A 17-Level Diode Assisted Switched Capacitor Multilevel Inverter

5.1 Introduction

In this chapter, a new 17-level diode assisted switched-capacitor MLI (DASC-MLI) is proposed. The proposed DASC-MLI generates output voltage using single DC voltage source and lower number of active and passive components, and has reduced total standing voltage (TSV) and peak inverse voltage (PIV) as compared to conventional SC-MLIs. The DASC-MLI possesses reverse current capability and can also be extended to obtain higher voltage levels through its extended structure. The capacitors are self-balanced in the proposed DASC-MLI without any additional voltage balancing mechanism. Output voltages higher than input voltage can be achieved through DASC-MLI, thus signifying its voltage boosting ability. The overall cost and volume of the proposed DASC-MLI, reduces considerably as compared to other reported SC-MLIs.

5.2 Proposed 17-level Diode Assisted Switched-Capacitor MLI

The basic module of diode assisted switched-capacitor MLI (DASC-MLI) is shown in Fig. 5.1. It uses series-parallel combinations of voltage source and capacitor to maintain the capacitor voltages at the desired levels. It can be observed from Fig. 5.1(a) that the capacitors are charged through parallelization by voltage source, when the switch S_w is turned ON. In this mode, both the diodes D_{Da} and D_{Db} are reverse biased. As can be seen in Fig. 5.1(b), the capacitor is discharged to obtain higher voltage levels by turning OFF the switch S_w, thus forcing the current to flow through forward biased diodes D_{Da} and D_{Db}. This module forms the basis of the proposed DASC-MLI and is connected to DASC-

MLI by four connection points α, β, γ and δ as highlighted in Fig. 5.1. The complete structure of proposed DASC-MLI and the connection with one of the modules is shown in Fig. 5.2. It consists of a single DC source, four capacitors C_1-C_4, five diodes D_1-D_5 and eleven switches S_1-S_{11}. The capacitor voltages of C_1, C_2 and C_3 are balanced at input voltage V_{DC} respectively, whereas the capacitor voltage of C_4 is balanced at $V_{DC}/2$. The mathematical derivation for voltage balancing of capacitor C_4 is explained below. Assuming that the output voltage and current waveforms possess half wave symmetry, the average current flowing through the capacitor (C_4) with R as the load resistance is given as

$$I_{C,\frac{7V_{dc}}{2}}^{+} = \frac{4V_{dc} - V_{C_4}}{R_L} \qquad I_{C,\frac{5V_{dc}}{2}}^{+} = \frac{3V_{dc} - V_{C_4}}{R_L} \qquad I_{C,\frac{3V_{dc}}{2}}^{+} = \frac{2V_{dc} - V_{C_4}}{R_L}$$

$$I_{C,\frac{V_{dc}}{2}}^{+} = \frac{V_{dc} - V_{C_4}}{R_L} \qquad I_{C,\frac{V_{dc}}{2}}^{-} = \frac{-V_{C_4}}{R_L} \qquad I_{C,\frac{3V_{dc}}{2}}^{-} = \frac{-V_{dc} - V_{C_4}}{R_L}$$

$$I_{C,\frac{5V_{dc}}{2}}^{-} = \frac{-2V_{dc} - V_{C_4}}{R_L} \qquad I_{C,\frac{7V_{dc}}{2}}^{-} = \frac{-3V_{dc} - V_{C_4}}{R_L} \tag{5.1}$$

where I_C^+ and I_C^- are currents through C_4 in positive and negative half cycle of output voltage V_0. The expression for net charge (Q) delivered/absorbed for a period T can be expressed as

$$\mathrm{Q} = I_{C,\frac{7V_{dc}}{2}}^{+} \cdot \left(\frac{\theta_8 - \theta_7}{\pi}\right).T + I_{C,\frac{5V_{dc}}{2}}^{+} \cdot \left(\frac{\theta_6 - \theta_5}{\pi}\right).T + I_{C,\frac{3V_{dc}}{2}}^{+} \cdot \left(\frac{\theta_4 - \theta_3}{\pi}\right).T +$$

$$I_{C,\frac{V_{dc}}{2}}^{+} \cdot \left(\frac{\theta_2 - \theta_1}{\pi}\right).T + I_{C,\frac{V_{dc}}{2}}^{-} \cdot \left(\frac{\theta_2 - \theta_1}{\pi}\right).T + I_{C,\frac{3V_{dc}}{2}}^{-} \cdot \left(\frac{\theta_4 - \theta_3}{\pi}\right).T +$$

$$I_{C,\frac{5V_{dc}}{2}}^{-} \cdot \left(\frac{\theta_6 - \theta_5}{\pi}\right).T + I_{C,\frac{7V_{dc}}{2}}^{-} \cdot \left(\frac{\theta_8 - \theta_7}{\pi}\right).T \tag{5.2}$$

$$Q = \left(\frac{V_{DC} - 2V_{C_4}}{R_L}\right) \cdot \left(\frac{\theta_8 - \theta_7 + \theta_6 - \theta_5 + \theta_4 - \theta_3 + \theta_2 - \theta_1}{\pi}\right) . T = 0$$

$$V_{DC} = \frac{V_{C_4}}{2} \tag{5.3}$$

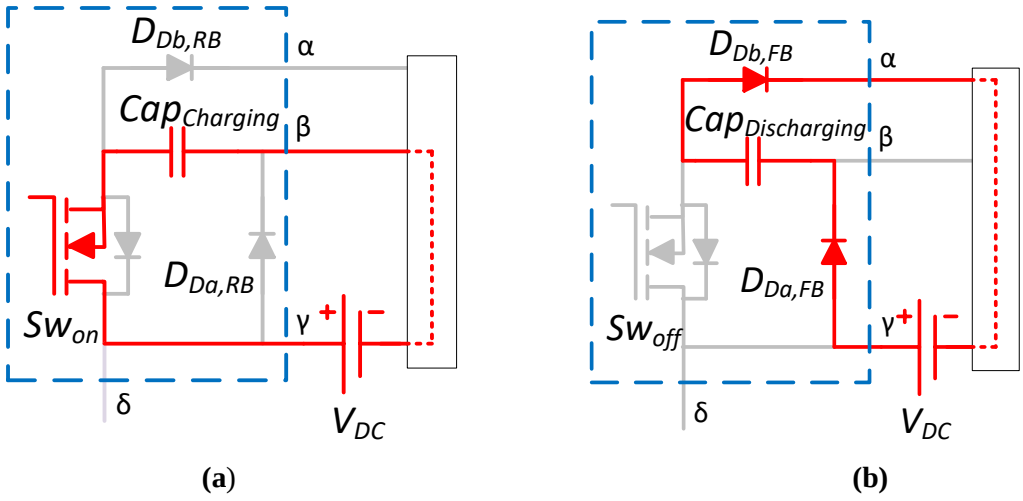


Fig. 5.1 Modes of DASC module (a) Charging (b) Discharging.

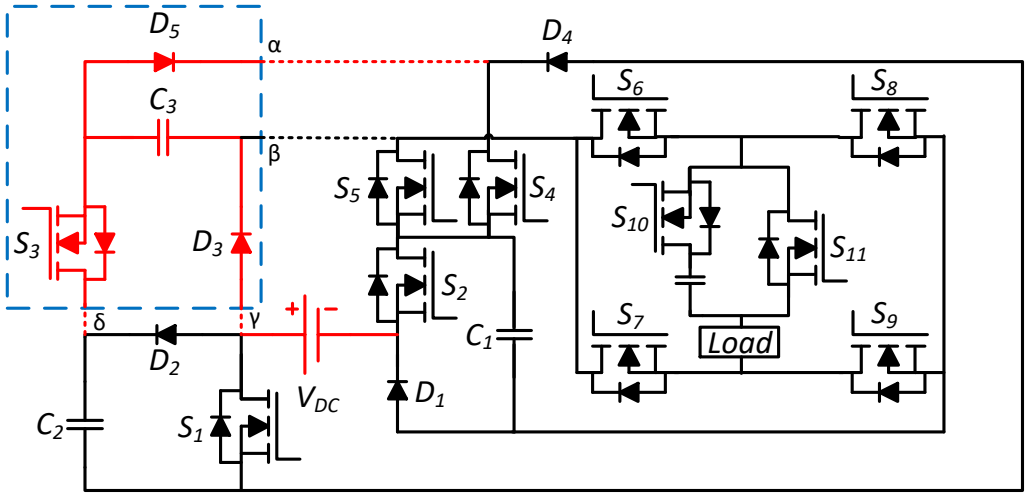


Fig. 5.2 Proposed 17-level DASC-MLI.

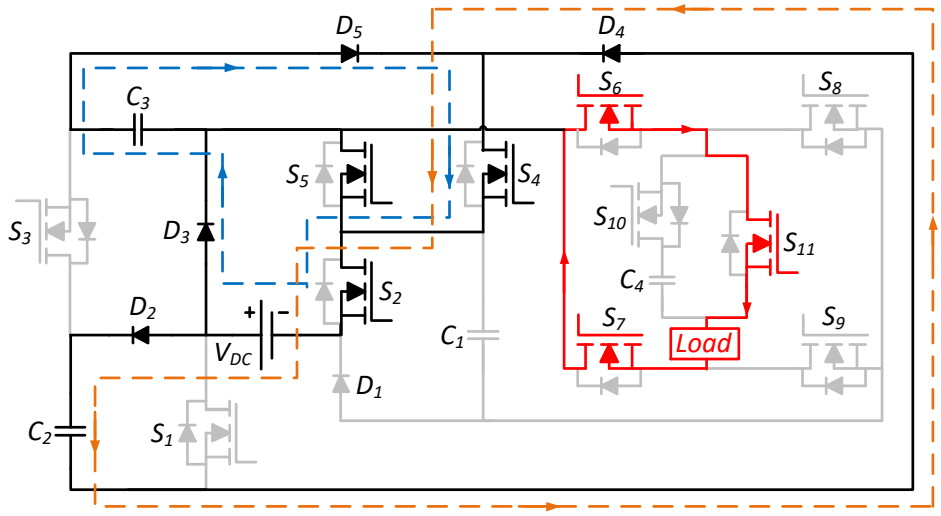
The switching patterns, diode behaviour and states of capacitors at each voltage level of the proposed DASC-MLI are shown in Table 5.1. The current paths of the proposed 17-level DASC-MLI for all positive levels are shown in Fig. 5.3(a)-(i). The dotted lines show

Table 5.1
Switching patterns, Diode behaviour and Capacitor states at each voltage level

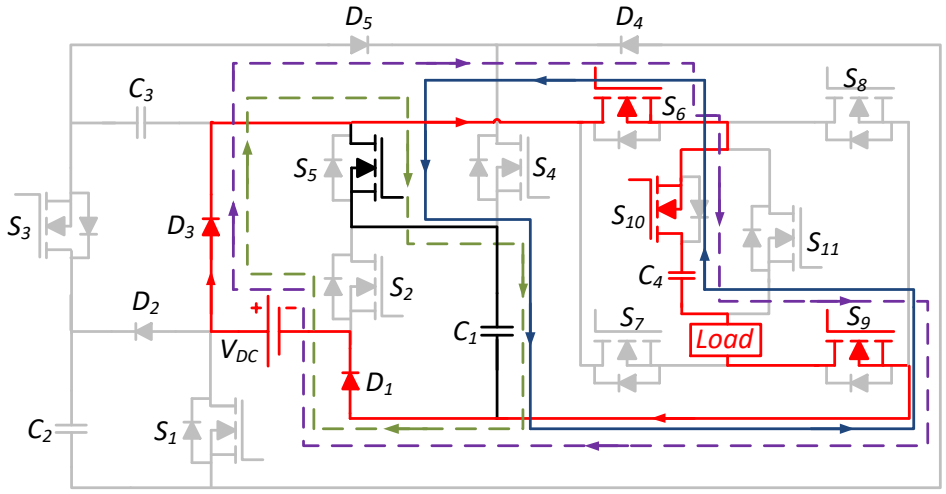
Output Voltage	$S_1 - S_{11}$	$D_1 - D_5$	$C_1 - C_4$
$+4V_{DC}$	1 1 1 0 0 1 0 0 1 0 1	0 0 0 0 0	DDDU
$+7V_{DC}/2$	1 1 1 0 0 1 0 0 1 1 0	0 0 0 0 0	DDDC
$+3V_{DC}$	1 0 1 0 0 1 0 0 1 0 1	1 0 0 0 0	UDDU
$+5V_{DC}/2$	1 0 1 0 0 1 0 0 1 1 0	1 0 0 0 0	UDDC
$+2V_{DC}$	0 1 0 1 0 1 0 0 1 0 1	0 1 1 1 1	DCCU
$+3V_{DC}/2$	0 1 0 1 0 1 0 0 1 1 0	0 1 1 1 1	DCCC
$+V_{DC}$	0 0 0 0 1 1 0 0 1 0 1	1 0 1 0 0	CUUU
$+V_{DC}/2$	0 0 0 0 1 1 0 0 1 1 0	1 0 1 0 0	CUUC
0	0 1 0 1 0 1 1 0 0 0 1	0 1 1 1 1	UCCU
$-V_{DC}/2$	0 0 0 1 1 1 1 0 0 1 0	0 1 1 1 1	UCCD
$-V_{DC}$	0 0 0 0 1 0 1 1 0 0 1	1 0 1 0 0	CUUU
$-3V_{DC}/2$	0 0 0 0 1 0 1 1 0 1 0	1 0 1 0 0	CUUD
$-2V_{DC}$	0 1 0 1 0 0 1 1 0 0 1	0 1 1 1 1	DCCU
$-5V_{DC}/2$	0 1 0 1 0 0 1 1 0 1 0	0 1 1 1 1	DCCD
$-3V_{DC}$	1 0 1 0 0 0 1 1 0 0 1	1 0 0 0 0	UDDU
$-7V_{DC}/2$	1 0 1 0 0 0 1 1 0 1 0	1 0 0 0 0	UDDD
$-4V_{DC}$	1 1 1 0 0 0 1 1 0 0 1	0 0 0 0 0	DDDU

In the column of switches, 1 and 0 represent turn ON and turn OFF. In the column of diode, 1 and 0 represent forward conduction and reverse blocking. The capacitor states are C for charging, D for discharging, and U for unchanged.

the charging path of the capacitors, the red (solid) lines show the current path through the load, and the blue (solid) lines show the reverse current path of the proposed DASC-MLI. All circuit configurations for voltage levels in one complete positive half cycle of output voltage are as follows:


D5
D4
C3
S6
S8
S5
S4
S10
S11
S3
D3
C4
S2
D2
+
-
C1
S7
Load
S9
VDC
D1
C2
S1

(a)


D5
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VDC
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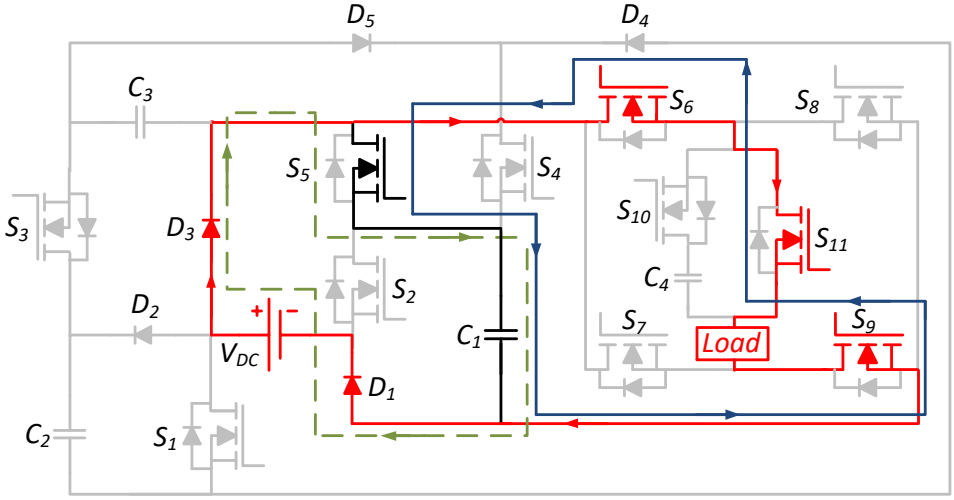
(b)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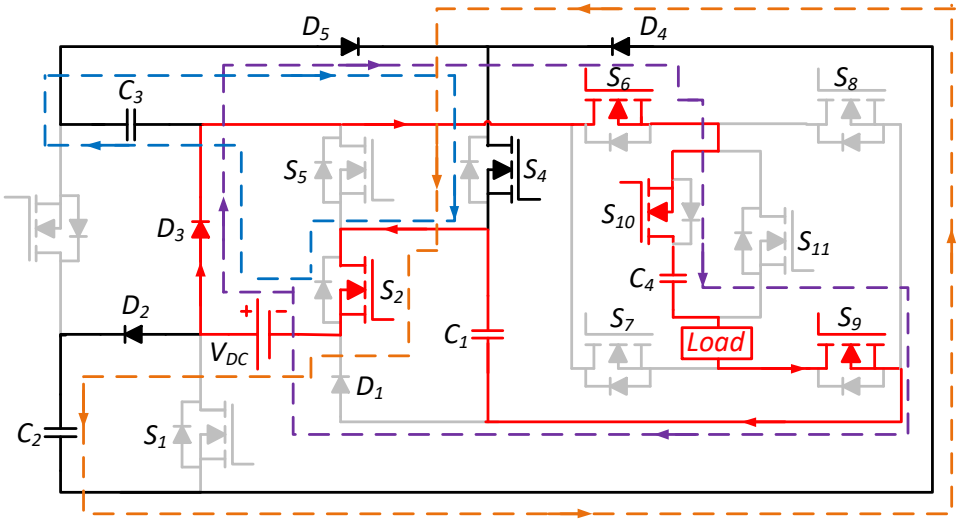
(c)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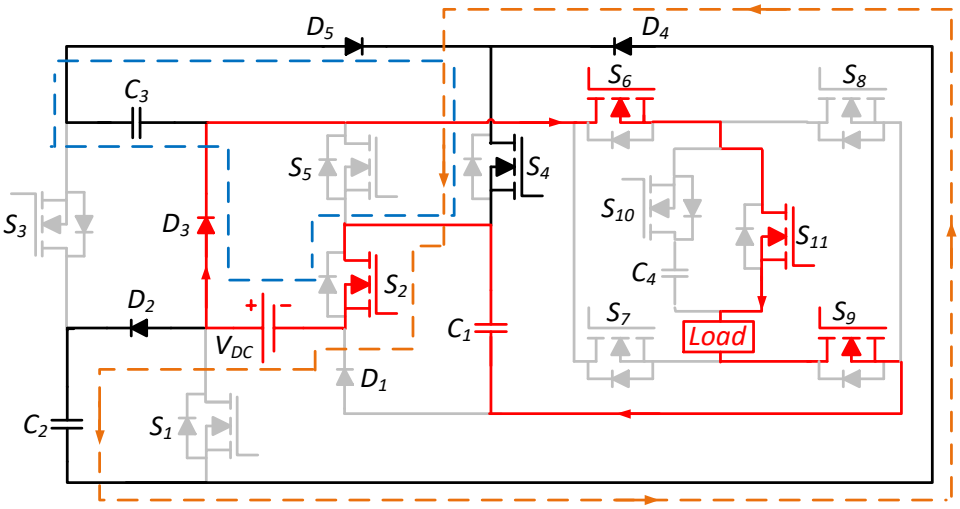
(d)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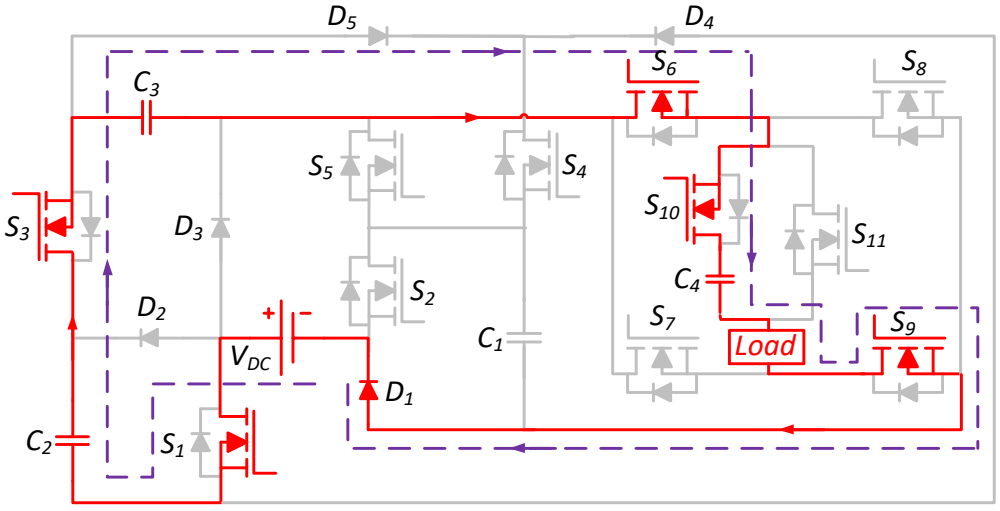
(e)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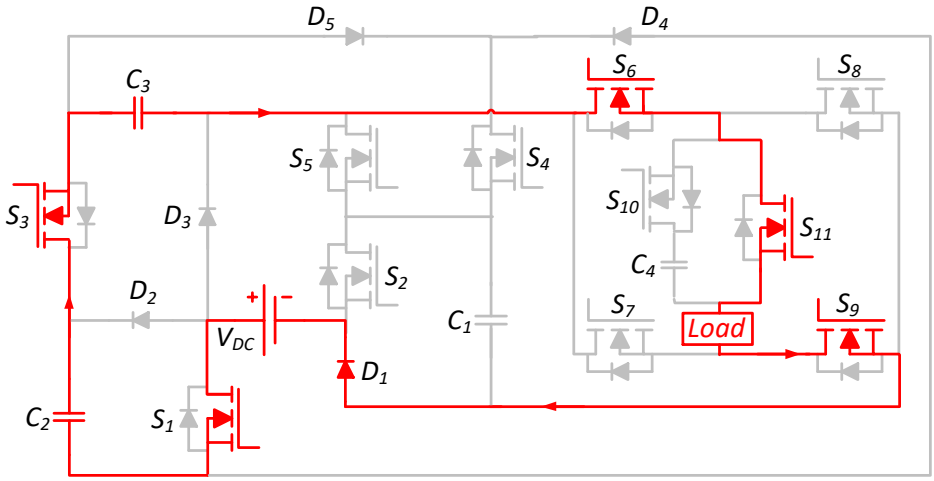
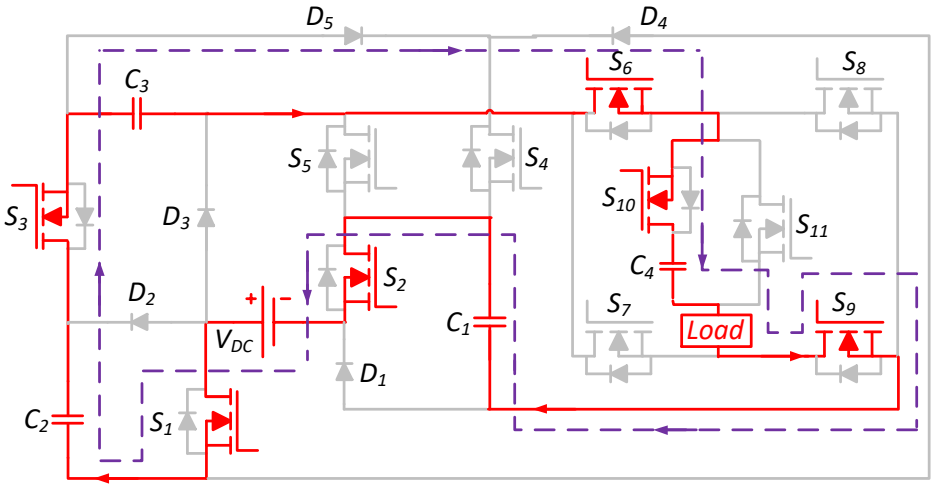
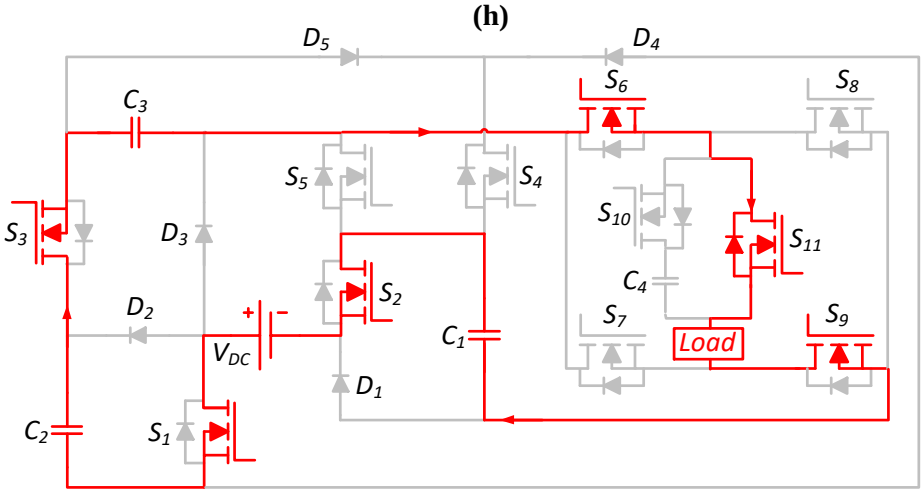
(f)



(g)



(h)



(i)

Fig. 5.3 Current flow for posituve voltage levels of the proposed 17-level DASC-MLI. (a) Current flow at voltage level zero. (b) Current flow at voltage level $V_{DC}/2$. (c) Current flow at voltage level V_{DC}. (d) Current flow at voltage level $3V_{DC}/2$. (e) Current flow at voltage level $2V_{DC}$. (f) Current flow at voltage level $5V_{DC}/2$. (g) Current flow at voltage level $3V_{DC}$. (h) Current flow at voltage level $V_{DC}/2$. (i) Current flow at voltage level $4V_{DC}$.

Level zero: Fig. 5.3(a) presents the current path for zero output voltage level. The capacitors C_2 and C_3 charge through D_2, D_4, S_4, S_2 and D_3, D_5, S_4, S_2 respectively in this interval.

Level $V_{DC}/2$: Fig. 5.3(b) shows the circuit configuration for generation of voltage level $V_{DC}/2$. The capacitors C_1 and C_4 charge through paths D_3, S_5, D_1 and D_3, S_6, S_{10}, S_9, D_1 respectively in this level. The reverse current passes through the switches S_{10}, S_6, S_5 and S_9.

Level V_{DC}: The circuit configuration for obtaining voltage V_{DC} across load is shown in Fig. 5.3(c). The capacitor C_1 charges in this interval through D_3, S_5 and D_1. The reverse current passes through the switches S_{11}, S_6, S_5 and S_9.

Level $3V_{DC}/2$: Fig. 5.3(d) shows the circuit configuration for voltage level $3V_{DC}/2$. All three capacitors C_2, C_3 and C_4 charge in this interval through charging paths D_2, D_4, S_4, S_2; D_3, D_5, S_4, S_2 and D_3, S_6, S_{10}, S_9, D_1 respectively. Capacitor C_1 discharges through D_3, S_6, S_{10}, S_9 and S_2 during this interval.

Level $2V_{DC}$: Fig. 5.3(e) shows the circuit configuration of voltage $2V_{DC}$. The capacitors C_2 and C_3 charge in this interval through D_2, D_4, S_4, S_2 and D_3, D_5, S_4, S_2. The capacitor C_1 discharges through D_3, S_6, S_{11}, S_9 and S_2.

Level $5V_{DC}/2$: Fig. 5.3(f) shows the circuit configuration for generation of voltage level $5V_{DC}/2$. The capacitors C_2 and C_3 are connected in series with the voltage source and discharge through S_1, S_3, S_6, S_{10}, S_9 and D_1. The capacitor C_4 is charged in this interval through the same path.

Level $3V_{DC}$: Fig. 5.3(g) shows the circuit configuration for output voltage $3V_{DC}$. The capacitors C_2 and C_3 are connected in series with the voltage source and discharge in this interval through path S_1, S_3, S_6, S_{11}, S_9 and D_1 to generate required output voltage.

Level $7V_{DC}/2$: Fig. 5.3(h) shows the circuit configuration of voltage level $7V_{DC}/2$. The capacitors C_1, C_2, and C_3 are connected in series with the voltage source and they discharge through S_1, S_3, S_6, S_{10}, S_9 and D_1 to generate $7V_{DC}/2$ output voltage. The capacitors C_4 charges in this interval through the same path.

Level $4V_{DC}$: Fig. 5.3(i) shows the circuit configuration for output voltage $4V_{DC}$. The capacitors C_1, C_2 and C_3 are connected in series with voltage source and they discharge through switches S_1, S_3, S_6, S_{11}, S_9 and S_2 to generate the required output voltage.

Similarly, output voltage levels for negative half cycle can be obtained through switching patterns given in Table 5.1.

PIV is a major factor in the selection of components for any MLI. In the proposed DASC-MLI, the switches S_6, S_7, S_8, S_9 suffer maximum stress, whereas the switches S_{10} and S_{11} suffer constant PIV of $V_{DC}/2$ irrespective of the number of levels. The PIV across the switches and diodes in the proposed for 17-level DASC-MLI is given in the Table 5.2.

Table 5.2
PIV across Switches for 17-level DASC-MLI

Device	PIV (×V_{DC})	Device	PIV (×V_{DC})
S_1, S_2	1	S_6, S_7, S_8, S_9	4
S_3	3/2	S_{10}, S_{11}	0.5
S_4	2	D_1, D_3, D_4, D_5	1
S_5	3	D_2	2

5.3 Extended Structure of Proposed 17-Level DASC-MLI

The extended structure of the proposed DASC-MLI can be obtained by adding a DASC unit consisting of one switch, one capacitor, and two diodes. Each such extended unit (m) adds 4 extra levels to the output voltage. The generalized (17+4m) level extended structure of the proposed DASC-MLI is shown in Fig. 5.4. One diode of each module is

connected through γ, while the other diode is connected through α. The switch and capacitors are connected through δ and β respectively as shown in Fig. 5.1. All the capacitor voltages in the proposed extended DASC-MLI are inherently self-balanced. For achieving higher voltage levels, the proposed DASC-MLI does not require any additional voltage source. Hence, the cost of the proposed DASC-MLI is considerably reduced for achieving higher voltage levels.

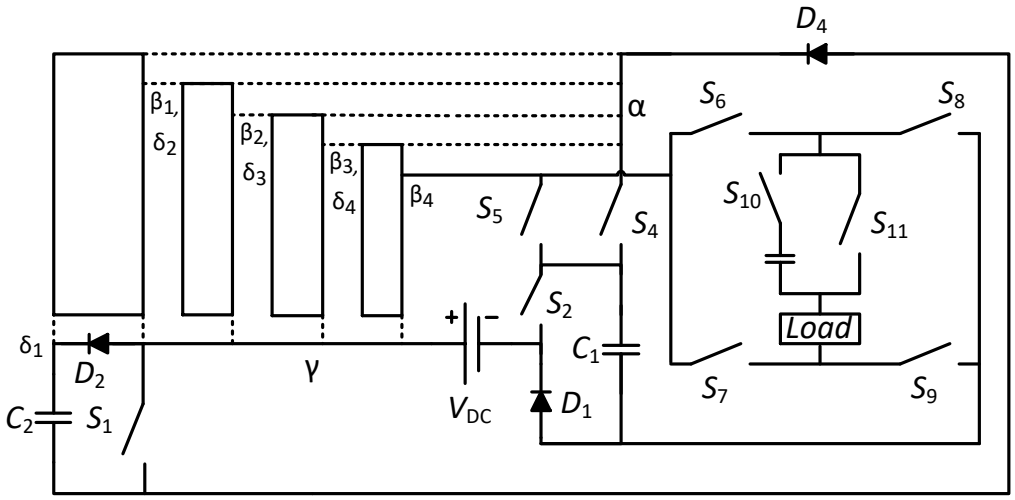


Fig. 5.4 Extension of proposed DASC-MLI.

5.3.1 Generalized Configuration of the Proposed DASC-MLI

The required number of active and passive components for generating $4n+1$ levels in the proposed generalized DASC-MLI (where n is the number of capacitors) can be calculated as:

$$\begin{cases} N_{\text{Switch}} = n+7 \\ N_{\text{Diode}} = 2n-3 \\ N_{\text{Source}} = 1 \end{cases} \tag{5.4}$$

where N_{Switch}, N_{Diode} and N_{Source} are the number of switches, diodes, and DC sources respectively. The TSV of the proposed DASC-MLI is calculated by adding the individual PIV of all switches. The TSV and TSV_{pu} of the generalized DASC-MLI are given as

$$\text{TSV} = \left(\frac{n^2 + 5n + 15}{2} \right) \cdot V_{\text{DC}} \tag{5.5}$$

$$\text{TSV}_{\text{pu}} = \left(\frac{n^2 + 5n + 15}{2n} \right) \cdot V_{\text{DC}} \tag{5.6}$$

5.4 Switching Scheme

Selective harmonic elimination technique using modified grew wolf optimization is used to generate the switching angles for the proposed DASC-MLI. The switching angles and output voltage levels of the proposed 17-level DASC-MLI are shown in Fig. 5.5. For proper operation of SC-MLI, the switching angles should satisfy the condition given as

$$0 < \theta_1 < \theta_2 < \theta_3 < \theta_4 < \theta_5 < \theta_6 < \theta_7 < \theta_8 < \theta_9 = \frac{\pi}{2} \tag{5.7}$$

The Fourier expansion of the quasi-square waveform of the output voltage for the proposed 17-level DASC-MLI is given as

$$V_0 = \frac{V_{\text{DC}}}{2\pi} \sum_{p=1,3,\cdots}^{\infty} \sum_{i=1}^{8} \frac{\cos(p\theta_i)}{p} \sin p\omega t \tag{5.8}$$

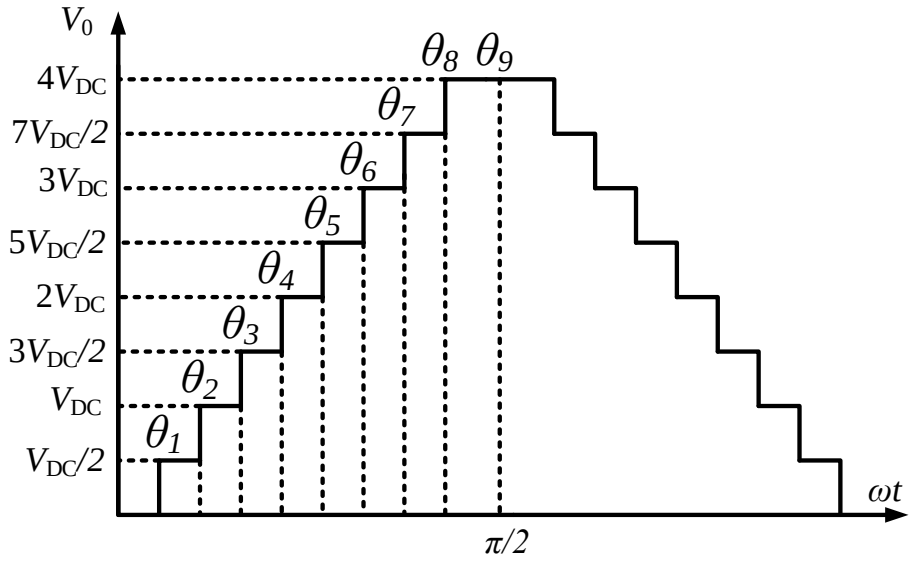


Fig. 5.5 Switching angles and output voltage levels of proposed 17-level DASC-MLI.

where ω is the angular frequency of the staircase output voltage waveform. The amplitude modulation index (M_{of}) of the fundamental output voltage waveform is expressed as:

$$M_{of} = \frac{1}{8}\sum_{i=1}^{8}\cos(\theta_i) \tag{5.9}$$

The switching angles for 17-level DASC-MLI θ_i (i = 1-8) are obtained using

$$\cos\theta_1 + \cos\theta_2 + \cos\theta_3 + \cos\theta_4 + \cos\theta_5 + \cos\theta_6 + \cos\theta_7 + \cos\theta_8 = 8M_{of}$$

$$\begin{aligned}&\cos(z\theta_1) + \cos(z\theta_2) + \cos(z\theta_3) + \cos(z\theta_4) + \cos(z\theta_5)\\ &+ \cos(z\theta_6) + \cos(z\theta_7) + \cos(z\theta_8) = 0\end{aligned} \tag{5.10}$$

where z is the number of harmonics. The harmonics such as 5th, 7th, 11th, 13th, 17th, 19th and 23rd are considered for obtaining the switching angles.

5.5 Capacitance Calculation

To calculate values of the capacitances, the charge-discharge cycle of each capacitor is considered [45]. For demonstration, the largest discharge period is calculated for C_1. The largest discharge interval and the corresponding currents through resistive load R_L for these intervals is calculated to define total charge and is shown in Table 5.3.

Table 5.3
Largest Discharge Interval for capacitor (C_1)

Interval	Current (i_0)
$\theta_3 \le \theta \le \theta_4$	$5V_{DC}/2R_L$
$\theta_4 \le \theta \le \theta_5$	$3V_{DC}/R_L$
$\theta_7 \le \theta \le \theta_8$	$7V_{DC}/2R_L$
$\theta_8 \le \theta \le \pi - \theta_8$	$4V_{DC}/R_L$

The maximum discharging value Q_{C_1} of the capacitor C_1 is calculated based on discharge cycles and is given as:

$$Q_{C_1} = \frac{1}{\omega}\left[\int_{\theta_3}^{\theta_4} i_o d\theta + \int_{\theta_4}^{\theta_5} i_o d\theta + \int_{\theta_7}^{\theta_8} i_o d\theta + \int_{\theta_8}^{\pi-\theta_8} i_o d\theta\right] \tag{5.11}$$

Similarly, maximum discharging values Q_{C_2}, Q_{C_3}, Q_{C_4} of the capacitors C_2, C_3, C_4 can be obtained. The maximum allowable voltage ripples across the capacitor C_i is kV_{C_i} (i=1, 2, 3 and 4), where k is the ripple factor. Using the derived values of Q_{C_1}, Q_{C_2}, Q_{C_3} and Q_{C_4} the values of capacitors C_1, C_2, C_3 and C_4 are obtained as:

$$C_1 \geq \frac{\left(4\pi - 3\theta_3 - \theta_4 + 4\theta_5 - 7\theta_7 - \theta_8\right)}{2\pi f_S k R_L} \tag{5.12}$$

$$C_2, C_3 \geq \frac{\left(4\pi - 5\theta_5 - \theta_6 - \theta_7 - \theta_8\right)}{2\pi f_S k R_L} \tag{5.13}$$

$$C_4 \geq \frac{\left(\theta_2 - \theta_1 - 3\theta_3 + 3\theta_4 - 5\theta_5 + 5\theta_6 - 7\theta_7 + 7\theta_8\right)}{2\pi f_S k R_L} \tag{5.14}$$

For the resistive-inductive loading condition, the function of load current, $I_L(t)$ can be derived as

$$I_L(t) = I_{max} \sin(\omega t - \phi) \tag{5.15}$$

here I_{max} is the maximum value of load current, and ϕ is the output phase difference. The net charge can then be obtained. Substituting the charge to obtain capacitance yields

$$C_1 \geq \frac{2I_{max}\begin{pmatrix}\cos(\theta_3 - \Phi) + \cos(\theta_7 - \Phi) \\ -\cos(\theta_5 - \Phi) - \sin(\Phi)\end{pmatrix}}{2\pi f_S k V_{DC}} \tag{5.16}$$

$$C_2, C_3 \geq \frac{2I_{max}\left(\cos(\theta_5 - \Phi) - \sin(\Phi)\right)}{2\pi f_S k V_{DC}} \tag{5.17}$$

$$C_4 \geq \frac{I_{max}\begin{pmatrix}\cos(\theta_4 - \Phi) - \cos(\theta_3 - \Phi) + \cos(\theta_2 - \Phi) \\ -\cos(\theta_1 - \Phi) + \cos(\theta_6 - \Phi) - \cos(\theta_5 - \Phi) \\ +\cos(1.5\pi) - \cos(\theta_7 - \Phi)\end{pmatrix}}{2\pi f_S k V_{DC}} \tag{5.18}$$

Assuming voltage ripple k = 0.05 and 0.1, the optimal capacitor values can be determined. From (5.16)-(5.18), it can be observed that the optimum values of capacitors inversely vary with the ripple factor, and output frequency. To demonstrate the effect of load resistance on the optimum capacitance values, the variations of C_1, C_2, C_3 and C_4 with different ranges of output load, R_L are shown in Fig. 5.6(a). The optimal values of capacitors are calculated for different values of phase angle and are shown in Fig. 5.6(b).

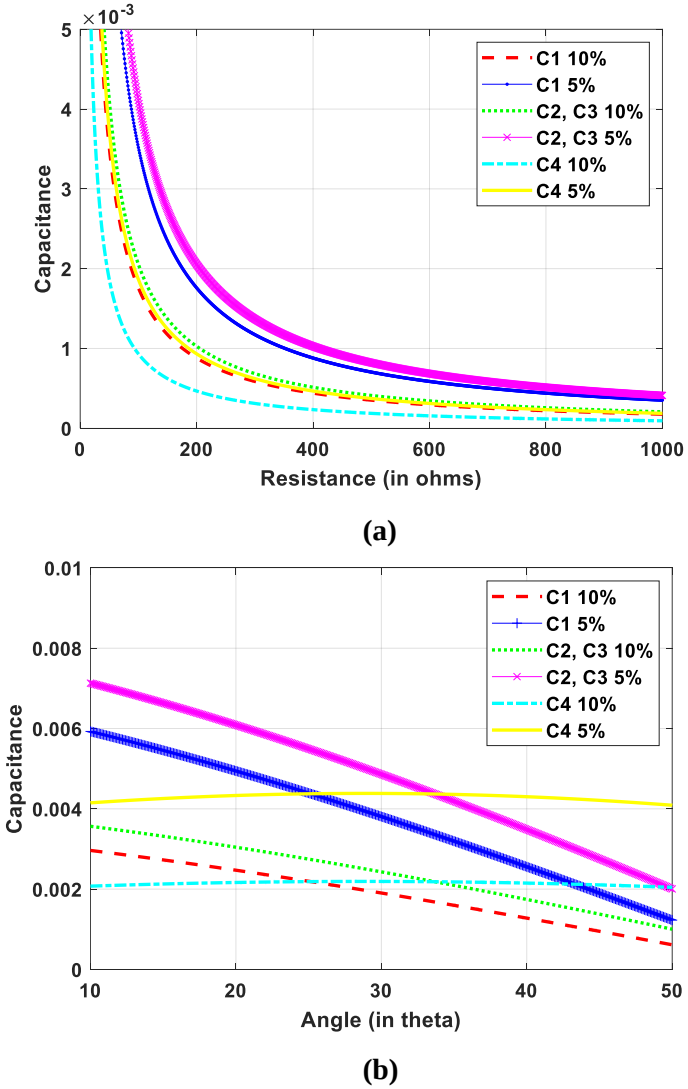


Fig. 5.6 Values of capacitance of all capacitors. (a) under different load resistance. (b) under different phase angles.

5.6 Conduction Loss of the Proposed DASC-MLI

The conduction losses, P_C in the proposed DASC-MLI can be attributed to two factors: steady state conduction losses and the charging state conduction losses. The steady state

conduction loss (CL), $P_{CL,SS}$ can be calculated by summing loss across each circuit element (diode, Switch, etc.) and $F_{j,}$ (j=1,.., J) incurred at each voltage level $U_{q,}$ (q=1,.., Q).

$$P_{CL,SS} = \sum_{q=1}^{Q}\sum_{j=1}^{J} P_{CL,SS,F_j,U_q} \tag{5.19}$$

here J and Q are the total number of elements and voltage levels respectively. The conduction loss, P_{CL,SS,F_j,U_q} at each level U_q for each element F_j can further be generalized as the sum of losses experienced due to on-state voltage drop at j^{th} component and their on-state resistances. This loss can be presented as

$$P_{CL,SS,F_j,U_q} = \begin{pmatrix} V_{on,F_j,U_q}.i_{load,avg,SS,F_j,U_q} \\ +R_{on,F_j,U_q}.i^2_{load,rms,SS,F_j,U_q} \end{pmatrix} \tag{5.20}$$

The charging state (CS) conduction losses (CL), $P_{CL,\,CS}$ occur due to charging currents superimposing the steady state current while charging capacitors. This charging current, $i_{CL,CS,F_j,U_q}(t)$ and its associated losses can be drastically reduced using a very small inductor (L_S) and a very small resistor (R_S) in series with the input source. The inclusion of this impedance at source side transforms the circuit into a series RLC circuit. Assuming series RLC circuit, the instantaneous current flowing through any element F_j, at any level U_q can be easily calculated as

$$i_{CL,CS,F_j,U_q}(t) = e^{\frac{-t.R_{eq,\,U_q}}{L_S}}.\left(I_{q-1}\cos(\lambda t) - \frac{I_{q-1}R_{eq,L_q}}{2.\lambda.L_S}\sin(\lambda t) - \frac{\Delta V}{\lambda.L_S}\sin(\lambda t) \right) \tag{5.21}$$

where

$$\lambda = \sqrt{\frac{1}{L_S.C_{\text{eq,U}_q}} - \left(\frac{R_{\text{eq,U}_q}}{2.L_S}\right)^2} \tag{5.22}$$

where $C_{\text{eq.}}$ and $R_{\text{eq.}}$ are the equivalent capacitance and resistance respectively in the charging loop including source resistance R_S. The ΔV is the difference between the capacitor voltage at beginning of level Uq. For each element F_j at level U_q, this current would generate conduction losses of magnitude:

$$P_{\text{CL,CS,F}_j,\text{ U}_q} = \left(\int_{t_{U_q,begin}}^{t_{U_q,end}} R_{\text{on, F}_j,\text{U}_q}.i^2_{\text{CL,CS, F}_j,\text{ U}_q}.dt + \int_{t_{U_q,begin}}^{t_{U_q,end}} V_{\text{on, F}_j,\text{U}_q}.i_{\text{CL,CS, F}_j,\text{ U}_q}.dt \right) \tag{5.23}$$

where, $t_{U_{q,begin}}$ and $t_{U_{q,end}}$ are the beginning and ending time of output voltage level Uq. The total CS-CL losses can be calculated like SS-CL by adding losses across each element:

$$P_{\text{CL,CS}} = \sum_{q=1}^{Q}\sum_{j=1}^{J} P_{CL,CS,F_j,U_q} \tag{5.24}$$

Since, it is mathematically difficult to accurately predict voltage at each instant of time due to several components involved, for ease in calculation of losses, ΔV is approximated to its maximum value of $0.1V_{\text{DC}}$.

5.7 Switching Loss Calculation

The switching loss occurs due to charging and discharging of parasitic capacitances of switches during the turn on and turn off of switches in a cycle [51]. The switching loss during turn on $P_{\text{sw, }i\text{(on)}}$ and turn off $P_{\text{sw, }i\text{(off)}}$ are given as

$$P_{\text{sw},\,i\,(\text{on})} = \frac{1}{6} f_{sw,i} V_{\text{sw},i} I_i t_{on} \tag{5.25}$$

$$P_{\text{sw},\,i\,(\text{off})} = \frac{1}{6} f_{sw,i} V_{\text{sw},i}\, I_i^{'} t_{off} \tag{5.26}$$

where $V_{\text{sw},\,i}$ is the off-state voltage of the i^{th} switch, I_{i} is the current of the i^{th} switch when the switch is turned on, I_{i}' is the current of the i^{th} switch before the turn off of the switch, t_{on} is the duration when the switch is turned on, t_{off} is the duration when the switch is turned off, and f_{sw} is the switching frequency. To calculate total switching loss, the number of N_{on} and the number of N_{off} switching states per one cycle is multiplied by (5.25) and (5.26). The total switching loss is calculated for each level and added as follows:

$$P_S = \sum_{i=1}^{17} \left(\sum_{j=1}^{N_{on}(i)} P_{\text{sw,on(ij)}} + \sum_{j=1}^{N_{off}(i)} P_{\text{sw,off(ij)}} \right) \tag{5.27}$$

Using (5.27), the total switching loss of the proposed 17-level DASC-MLI is obtained as:

$$P_{\text{S}} = \frac{54 V_{DC}^2}{R_L} f_S t_{on} + \frac{53.5 V_{DC}^2}{R_L} f_S t_{off} \tag{5.28}$$

5.8 Ripple Loss Analysis

The ripple loss occurs at the time of charging of capacitors at different switching instances. The voltage ripple of capacitors is obtained as

$$\Delta V_{Ci} = \frac{1}{C_i} \int_{t}^{t'} i_{c_i}(\text{t}).dt \tag{5.29}$$

where i_{c_i} is the capacitor current and $t - t'$ is the charging interval. The ripple voltages of capacitors C_1, C_2, C_3 and C_4 are given as

$$\Delta V_{C1} = \frac{V_{dc}}{2\pi f_S R_L C_1}\left(4\pi - 3\theta_3 - \theta_4 + 4\theta_5 - 7\theta_7 - \theta_8\right) \tag{5.30}$$

$$\Delta V_{C2}, \Delta V_{C3} = \frac{V_{dc}}{2\pi f_S R_L C_2}\left(4\pi - 5\theta_5 - \theta_6 - \theta_7 - \theta_8\right) \tag{5.31}$$

$$\Delta V_{C4} = \frac{V_{dc}}{2\pi f_S R_L C_4}\left(\theta_2 - \theta_1 - 3\theta_3 + 3\theta_4 - 5\theta_5 + 5\theta_6 - 7\theta_7 + 7\theta_8\right) \tag{5.32}$$

The ripple loss in one cycle operation of the output voltage is given as

$$P_{\mathrm{R}} = \frac{1}{2T}\sum_{i=1,2,3,4} C_i \Delta V_i^2 \tag{5.33}$$

where C_{i} and ΔV_i are the i^{th} capacitor and ripple voltage of it.

The efficiency of the proposed DASC-MLI can be written as:

$$\eta = \frac{P_0}{P_0 + P_C + P_S + P_R} \tag{5.34}$$

where P_0, P_{C}, P_{S} and P_{R} are the output power, conduction, switching and ripple losses respectively.

5.9 Comparison with Other Reported topologies

In this section, the proposed DASC-MLI is compared with other reported SC-MLIs in terms of used capacitors, switches, diodes, TSV, PIV, boosting factor and cost function (CF). It can be observed from Fig. 5.7(a) that the proposed DASC-MLI requires lesser number of capacitors to utilize the same levels as compared to other selected MLIs. The DASC-MLI uses lower number of switches compared to other recently proposed topologies like symmetric topology in [44] and switched-capacitor topology in [42] as

shown in Fig. 5.7(b). Topologies presented in [43] possess large TSV for higher levels, whereas topology [40] requires much more diodes to achieve same voltage levels. The topology given in [41] and [45] requires a greater number of switches as compared to proposed DASC-MLI. The TSV and number of capacitors required in [46] are also very high. Table 5.4 also gives the comparison of different reported SC-MLIs and the proposed DASC-MLI in for 17-level SC-MLI. The generalized graphical representations of TSV and number of diodes versus voltage levels for different SC-MLI topologies are shown in Fig. 5.7(c) and (d) respectively. A CF has been further used to demonstrate potentiality of proposed DASC-MLI compared to other reported SC-MLIs and is given as [54]

$$\mathrm{CF} = N_{\mathrm{switch}} + N_{\mathrm{cap}} + N_{\mathrm{diode}} + TSV_{\mathrm{pu}} \tag{5.35}$$

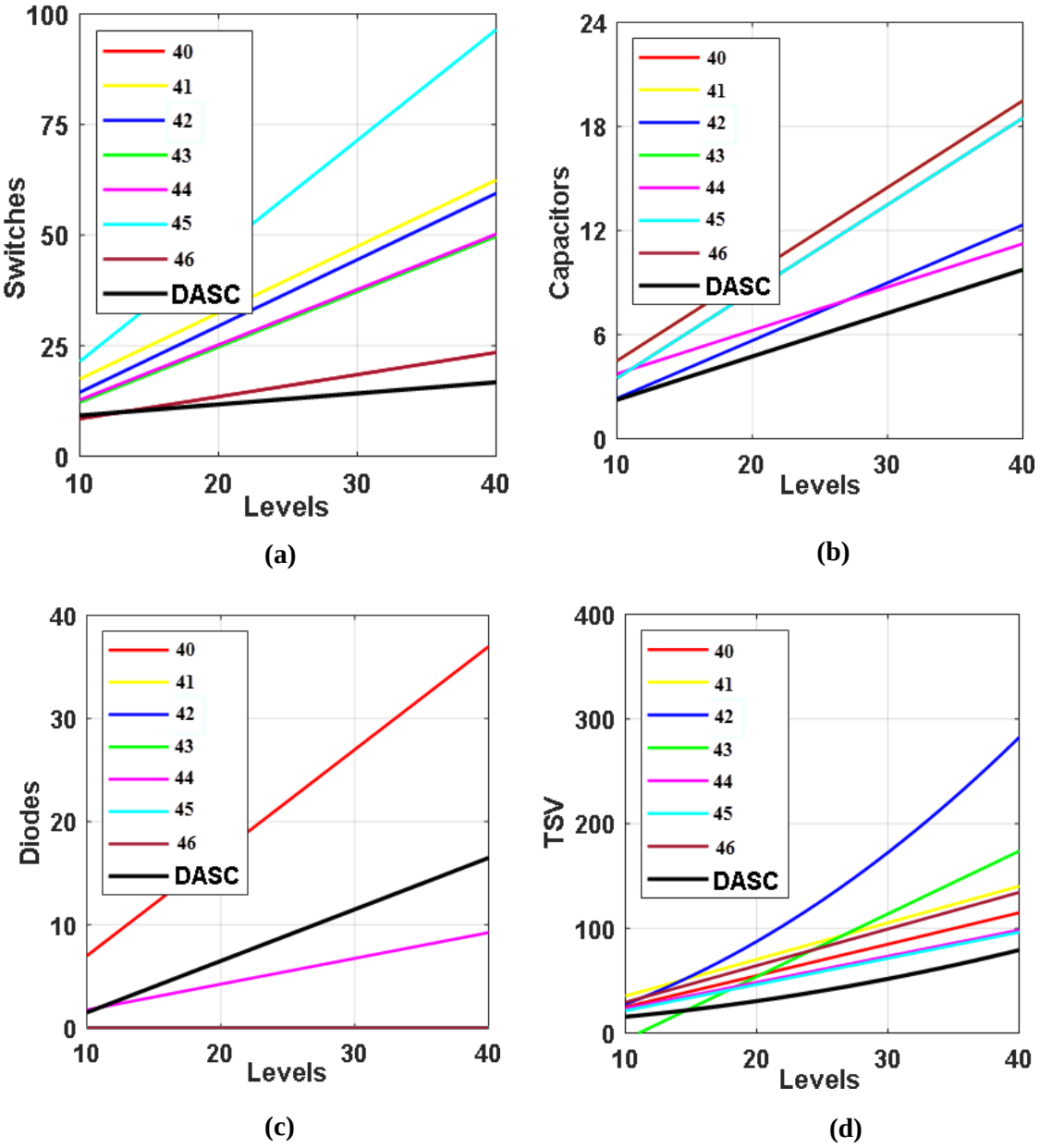
where N_{switch}, N_{cap} and N_{diode} are the number of switches, capacitors and diodes, respectively.

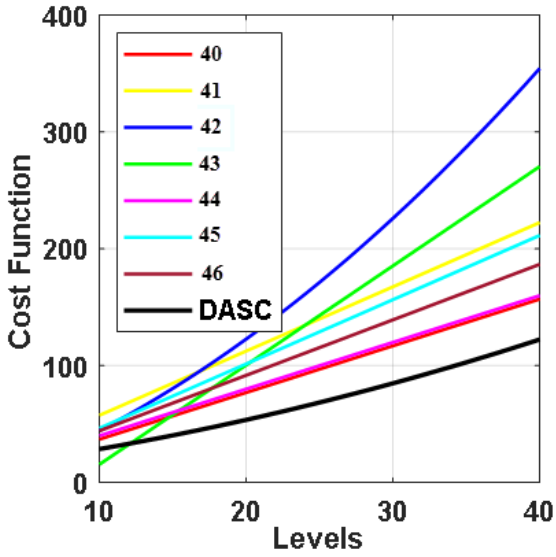
Table 5.4
Comparison of proposed 17-level DASC-MLI with Other Recent SC-MLI Topologies

Param.	**[45]**	**[42]**	**[40]**	**[41]**	**[46]**	**[43]**	**[44]**	**DASC-MLI**
N_{Switch}	39	25	12	25	12	23.5*	23.5*	11
N_{Cap}	7	7	7	7	8	4.5*	5.5*	4
N_{Diode}	0	0	14	0	0	0	3.5*	5
TSV_{sw}	39	72	96	53	54	48	41	25.5
TSV_{diode}	0	0	28	0	0	0	3.5	6
TSV_{total}	39	72	126	53	54	48	44.5	31.5
PIV	1	8	8	8	4	8	2	4
Boost factor	8	8	8	8	8	14	4	4
Extend-ability	Y	Y	Y	Y	Y	Y	Y	Y

* **as per the generalization provided in paper**

The generalized graphical representations of CF versus voltage levels for different SC-MLI topologies are shown in Fig. 5.7(e). It can be observed that the cost of the proposed DASC-MLI is reduced as compared to other reported SC-MLIs. When operated at same boosting factor, the proposed DASC-MLI requires lower number of switches at same number of voltage levels. If the proposed DASC-MLI has greater TSV at same boosting ratio, then the number of levels generated is almost twice those generated by other SC-MLI topologies, thus verifying the lower TSV and component count at higher voltage levels of the proposed DASC-MLI.





(e)

Fig. 5.7 Comparison of the proposed DASC-MLI with recent topologies. (a) Number of required sources versus levels. (b) Number of required switches versus levels. (c) TSV versus number of levels. (d) Diode versus number of levels CF. (e) Cost function versus number of levels of different topologies.

5.10 Simulation Studies

The performance of the proposed DASC-MLI is validated through a 550 W MATLAB/Simulink model. Modulation index is taken as 0.75 in this study. The output voltage V_0 and current I_0 waveforms of the proposed 17-level DASC-MLI for a resistive load (R = 40 Ω) are shown in Fig. 5.8(a). The measured rms values of voltage and current are 155.4 V and 3.42 A respectively at 50 Hz frequency. For R-L load (R = 40 Ω, L = 100 mH), output voltage V_0 and current I_0 are shown in Fig. 5.8(b) and measured as 155.4 V and 3.38 A respectively. The capacitor voltages are shown in Fig. 5.9. It can be observed that capacitor voltages V_{C1}, V_{C2}, V_{C3} and V_{C4} are balanced at 60 V, 60 V, 60 V and 30 V respectively. The voltage stresses across four switches (S_1, S_2, S_3 and S_4) of the proposed DASC-MLI are shown in Fig. 5.10(a) and are measured as 60 V, 60 V, 90 V and 120 V respectively. The voltage stresses across switches (S_5, S_{10} and S_{11}) are shown in Fig. 5.10(b) and are also measured as 180 V, 30 V and 30 V respectively. Similar, the voltage stresses across each switch (S_6, S_7, S_8 and S_9) of the H-bridge are 240 V respectively, as shown in Fig. 5.10(c).

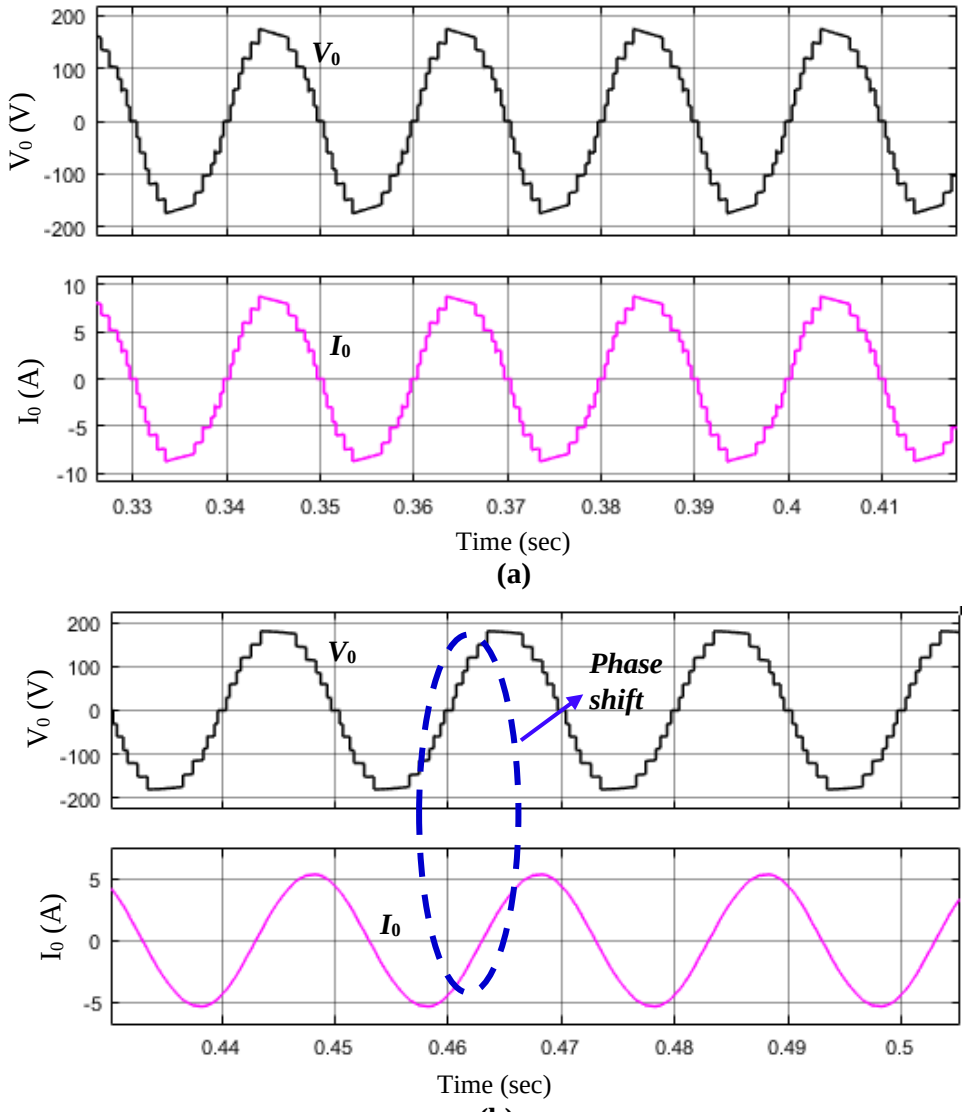


Fig. 5.8 Simulation results of the proposed DASC-MLI. (a) Output voltage (V_o) and current (I_o) for *R* load (R= 40 Ω). (b) Output voltage (V_o) and current (I_o) for *R-L* load (R= 40 Ω, L= 100 mH.

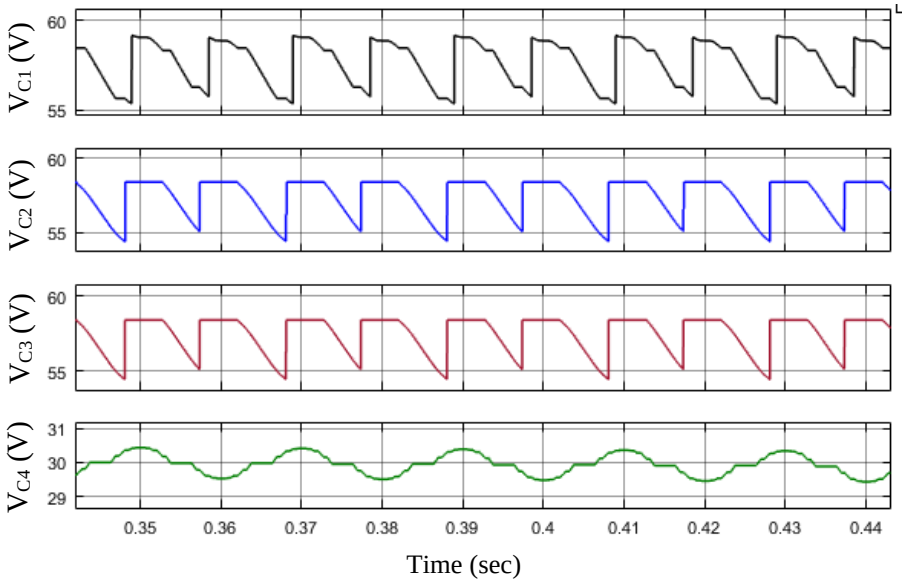


Fig. 5.9 Simulation results of capacitor voltages. (V_{C1}, V_{C2}, V_{C3}, V_{C4}).

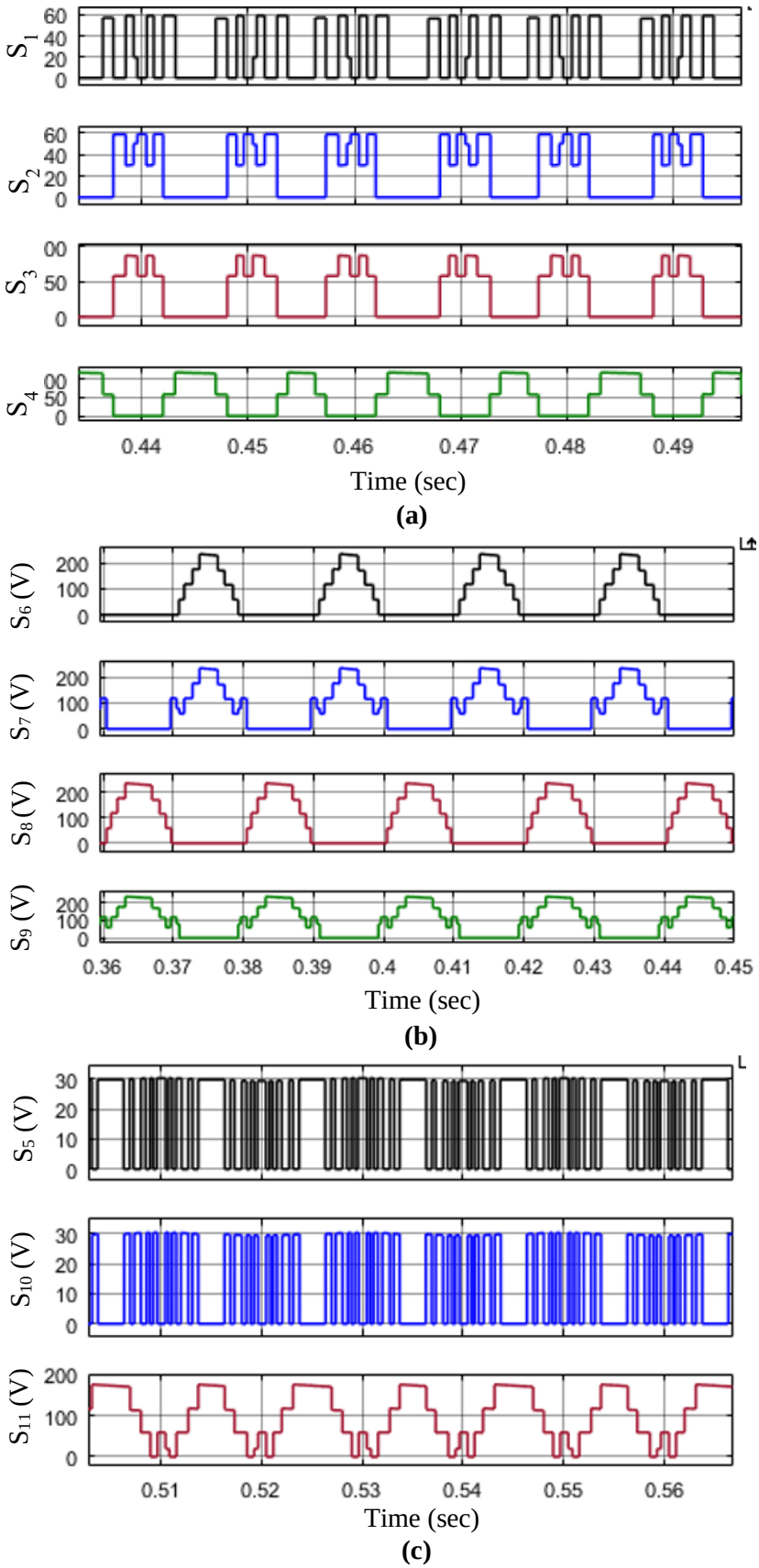


Fig. 5.10 Voltage stress of the proposed DASC-MLI. (a) Voltage stresses across switches (S_1, S_2, S_3, S_4). (b) Voltage stresses across switches (S_5, S_{10}, S_{11}). (c) Voltage stresses across switches (S_6, S_7, S_8, S_9).

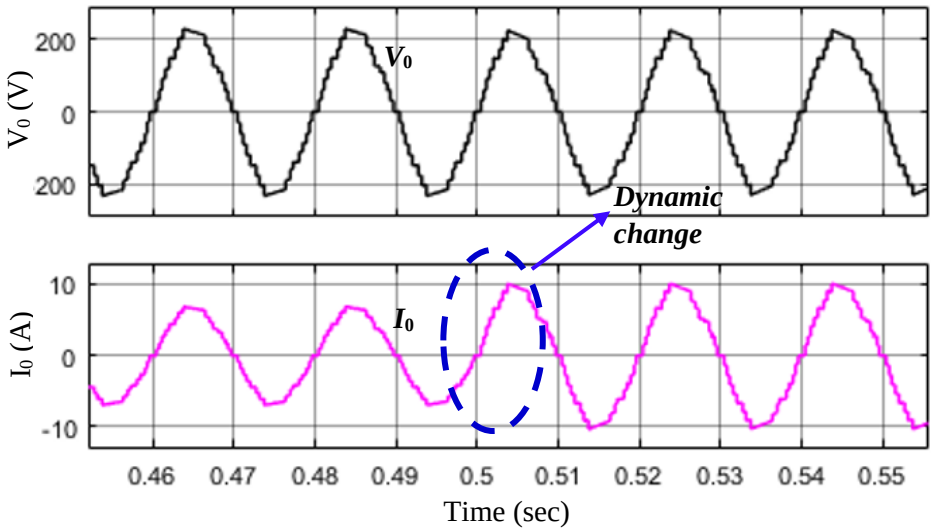


Fig. 5.11 Dynamic performance of the proposed SC-MLI for step-down change in load resistance.

The load resistance is step changed from 70 Ω to 35 Ω to observe the dynamic behaviour of the DASC-MLI. The load current is changed from 3.5 A to 7 A due to step change in resistance and is shown in Fig. 5.11. It can be observed that the load change does not have any effect on the output voltage waveform. Hence, it confirms the self-voltage balance of capacitors in the proposed DASC-MLI.

5.11 Experimental Validation of DASC-MLI

The performance of the proposed DASC-MLI is validated through a 570 W experimental prototype as shown in Fig. 5.12. The parameters used in experiment are listed in Table 5.5.

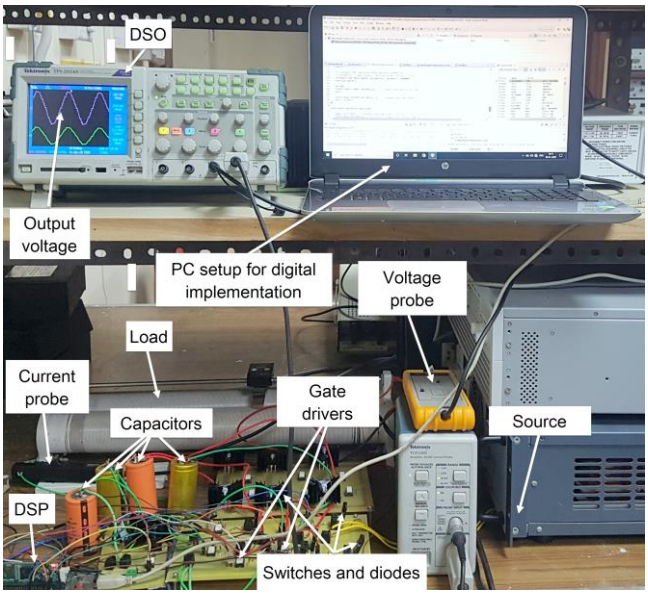


Fig. 5.12 Photograph of experimental prototype of 17-level DASC-MLI.

Table 5.5
Devices and Parameters Used for Experimentation

Microcontroller	TI-TMS320F28335
IGBT	HGTG12N60A4D
Gate Driver	FOD3184
Diode	STP516150
Electrolytic Capacitors	2200µF (C_1, C_2) and 1800 µF (C_3, C_4)

5.11.1 Steady State Performance

The steady state performance of DASC-MLI is investigated in this section. The DC source voltage V_{dc} is taken as 60 V and the experimentation has been carried out using TI-TMS320F28335 DSP processor.

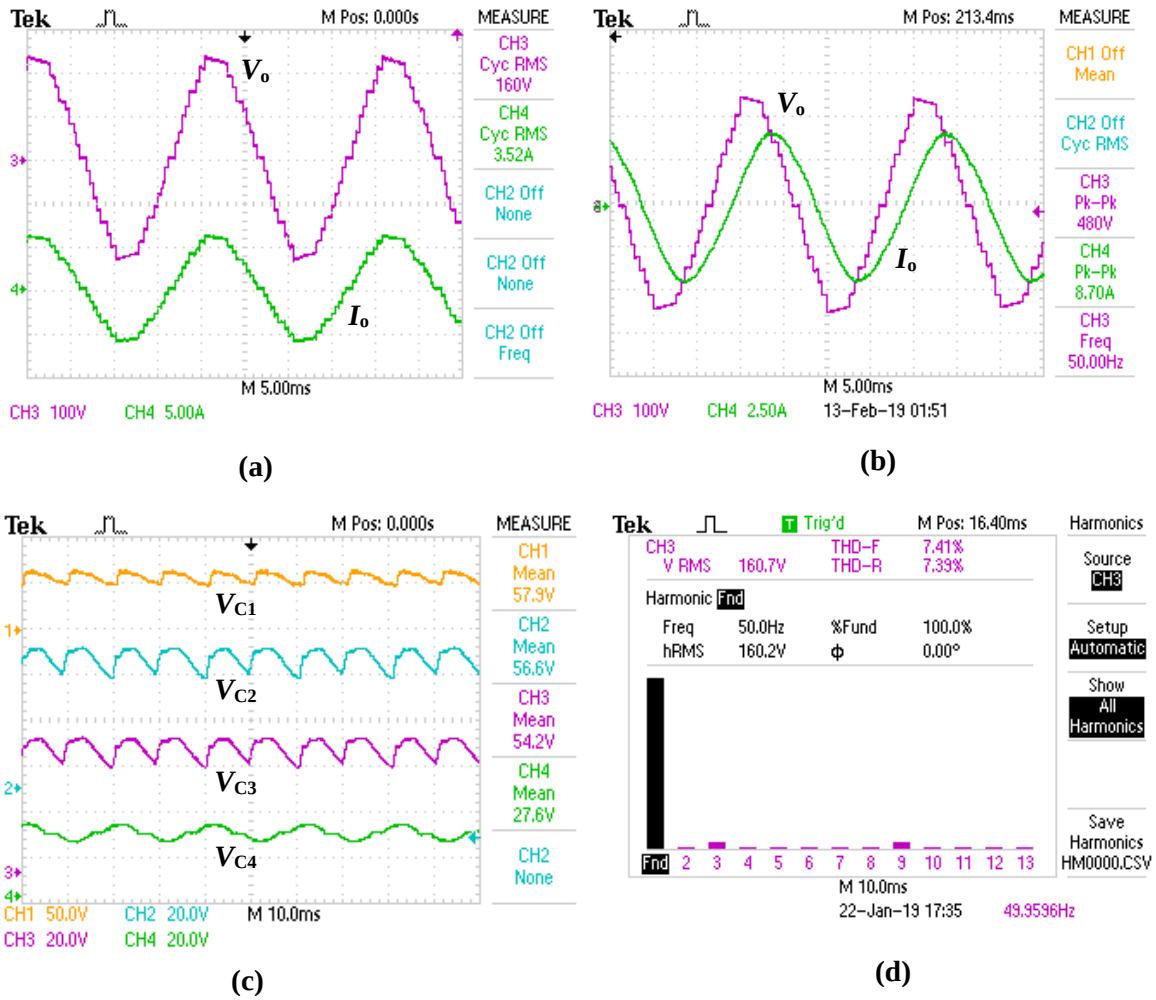


Fig. 5.13 Experimental results of the proposed DASC-MLI. (a) Output voltage (V_o) and current (I_o) for R load (R= 40 Ω). (b) Output voltage (V_o) and current (I_o) for R-L load (R= 40 Ω, L= 100 mH). (c) Capacitor voltages (V_{C1}, V_{C2}, V_{C3}, V_{C4}). (d) Harmonic spectrum of V_o.

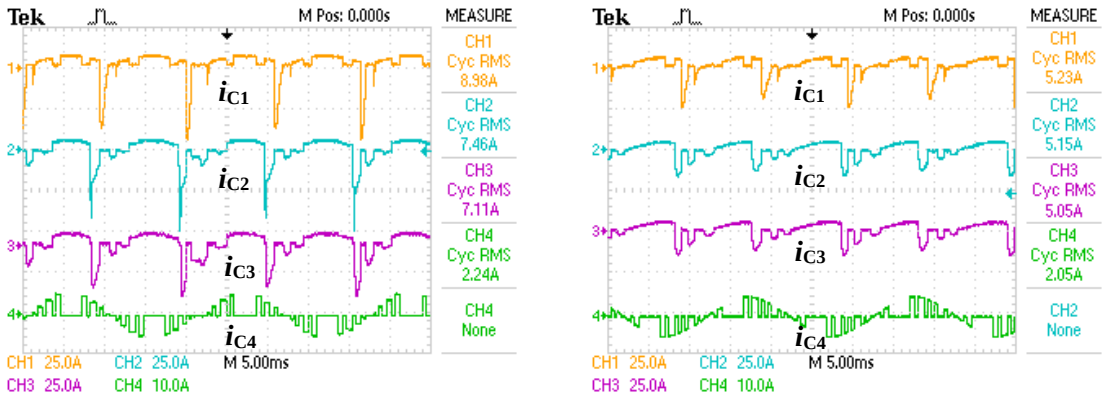


Fig. 5.14 Experimentally results of capacitor currents of DASC-MLI. (a) Capacitor currents i_{C1}, i_{C2}, i_{C3}, and i_{C4} for $R = 40\ \Omega$. (b) Capacitor currents i_{C1}, i_{C2}, i_{C3} and i_{C4} for $R = 40\ \Omega$, $L = 100$ mH.

Fundamental switching strategy (50 Hz) is used and the value of M_{of} is taken as 0.75. The output voltage V_0 and current I_0 waveforms for a resistive load ($R = 40\ \Omega$) are shown in Fig. 5.13(a). The measured rms values of voltage and current are 154.7 V and 3.38 A at 50 Hz frequency respectively. For *R-L* load ($R = 40\ \Omega$, $L = 100$ mH), output voltage V_0 and current I_0 are shown in Fig. 5.13(b) and measured as 154.1 V and 3.17 A respectively. The capacitor voltages are shown in Fig. 5.13(c). It can be observed that capacitor voltages V_{C1}, V_{C2}, V_{C3} and V_{C4} are balance at 56.5 V, 56 V, 54.2 V and 27 V respectively. The ripples voltage ΔV_{C1}, ΔV_{C2}, ΔV_{C3} and ΔV_{C4} of capacitors are 4 V, 4.4 V, 5.9 V and 2.3 V respectively. The harmonic spectrum of the output voltage V_0 is shown in Fig. 5.13(d) and output voltage THD is measured as 7.41%. To verify the proper charge balance in capacitors, the respective capacitor currents for *R* and *R-L* load are shown in Fig. 5.14(a)-(b). The measured rms values of current in case of *R* load ($R = 40\ \Omega$) for capacitors C_1, C_2, C_3 and C_4 are 4.27 A, 4.10 A, 4.25 A and 2.64 A respectively as shown in Fig. 5.14(a). Similarly, for *R-L* load ($R = 40\ \Omega$ and $L = 100$ mH), the measured rms value of capacitors are 4.35 A, 3.31 A, 3.58 A and 2.63 A respectively as shown in Fig. 5.14(b). The voltage stresses across four switches (S_1, S_2, S_3 and S_4) of the proposed DASC-MLI are shown in Fig. 5.15(a) and are measured as 60 V, 60 V, 92 V and 120 V

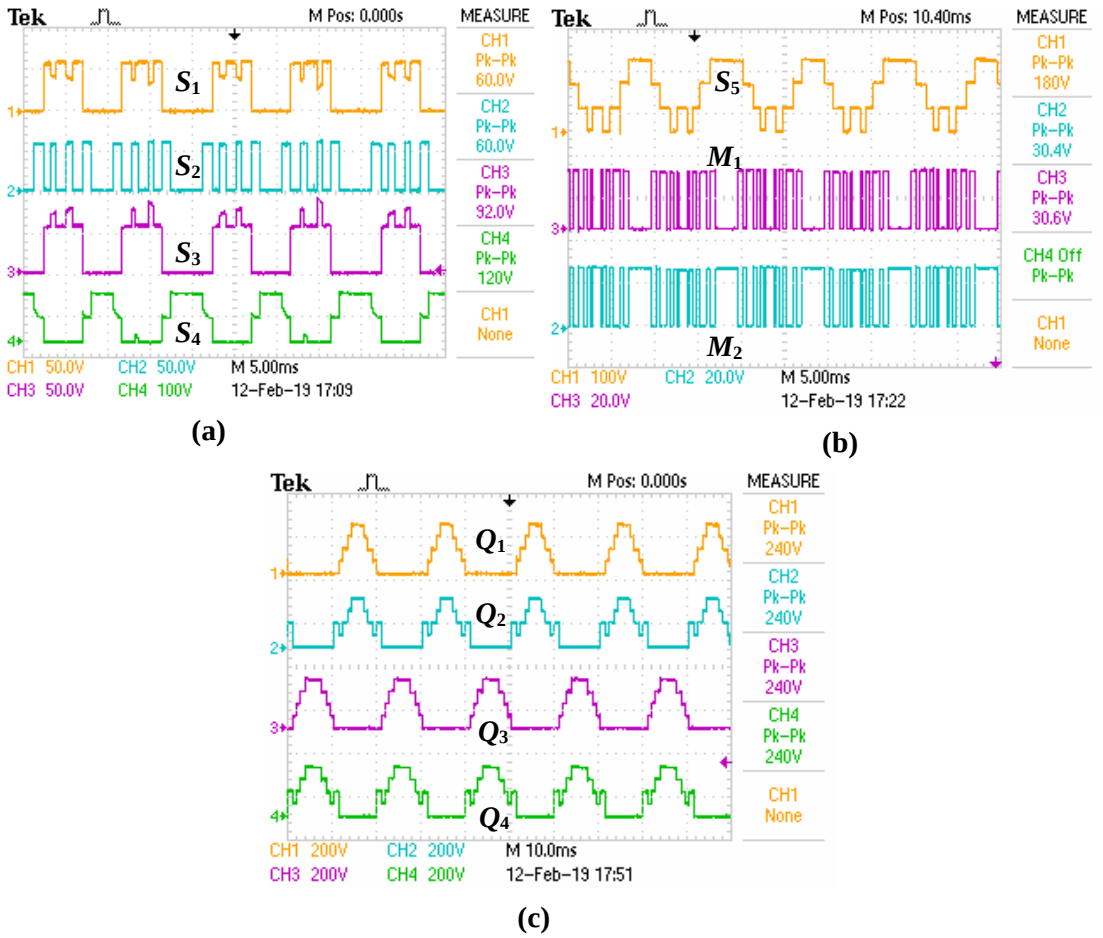


Fig. 5.15 Experimental results of voltage stress of DASC-MLI. (a) Voltage stresses across switches (S_1, S_2, S_3, S_4). (b) Voltage stresses across switches (S_5, M_1, M_2). (c) Voltage stresses across switches (Q_1, Q_2, Q_3, Q_4).

respectively. The voltage stresses across switches (S_5, M_1 and M_2) are shown in Fig. 5.15(b) and are measured as 180 V, 30.4 V and 30.6 V respectively. Similarly, the voltage stresses across switches (Q_1, Q_2, Q_3 and Q_4) of the H-bridge are 240 V, as shown in Fig. 5.15(c). Peak charging current is common in DASC-MLIs and to alleviate the current spikes, and reduce the device stresses, several strategies are discussed in literatures [47], [48] and [52]. Reducing spikes by increasing switching frequency is given in [47]. Literature [48] discusses the alleviation of spikes by increasing capacitance value. Using resistors [52] or inductors at source also reduces the spikes. In the proposed work, a small inductor and a small resistor at the source is used to reduce the current spikes. The switch and device current stress analysis is carried out for load resistance R= 40 Ω, input resistor R= 0.15 Ω and input inductor L=35 µH.

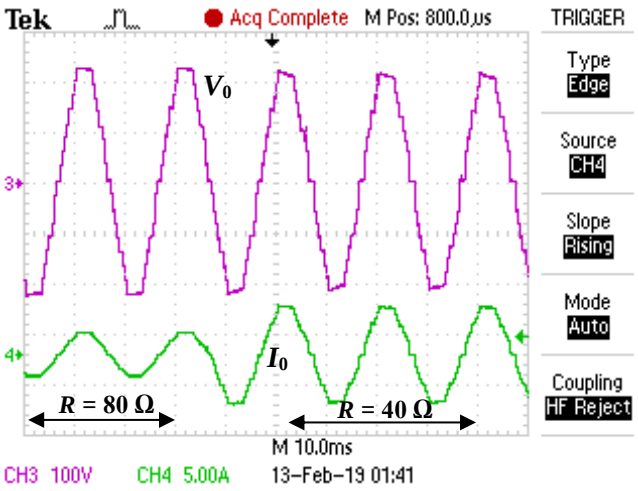


Fig. 5.16 Experimental verification of dynamic performance of DASC-MLI for step-up change in load resistance.

5.11.2 Dynamic Performance

The dynamic performance of the proposed RV-SCMLI is investigated in this section. The load resistance is step changed from 80 Ω to 40 Ω to observe the dynamic performance of the DASC-MLI. The load current is changed from 1.8 A to 3.6 A due to step change in resistance and is shown in Fig. 5.16. From Fig. 5.16, it can also be observed that the load change has no effect on the output voltage waveform, which confirms the self-voltage balancing of capacitors in DASC-MLI.

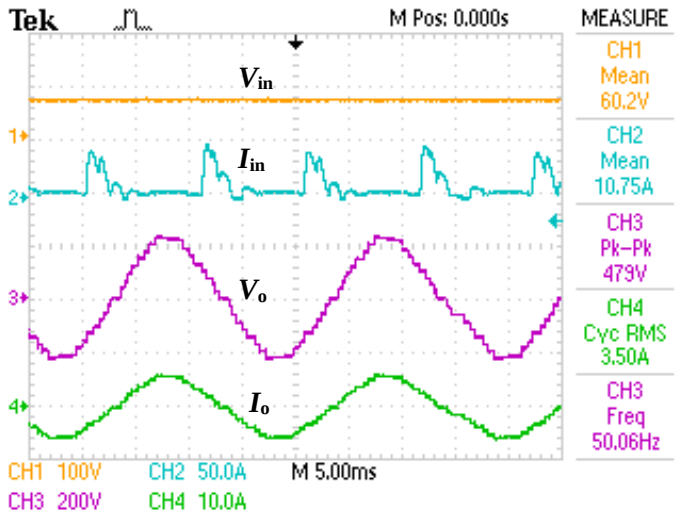


Fig. 5. 17 Input voltage, current and output voltage, current for *R* load (*R* = 40Ω) of DASC-MLI.

5.11.3 Calculation of Efficiency

The conduction loss, switching loss and ripple loss are calculated using (5.24), (5.28) and (5.33) and are 16.75 W, 5.37 W and 6.23 W respectively. The experimental efficiency of the proposed DASC-MLI is also calculated. To determine the efficiency (η) of the proposed DASC-MLI; input voltage V_{in}, input current I_{in}, output voltage V_o and output current I_o are measured experimentally for R load from Fig. 5.17. For R load (R= 40 Ω), the measured input power, output power and loss are P_{in} = 580.15 W, P_{out} =543.47 W and P_{loss} = 37.49 W, respectively. The experimentally calculated efficiency (η) for 580 W DASC-MLI is 93.54%.

5.12 Conclusion

A new 17-level DASC-MLI using reduced number of active and passive components is proposed in this chapter. TSV of the proposed DASC-MLI is low, thus facilitating utilization of lower-rated semiconductor devices for higher power applications. The DASC-MLI possesses reverse current carrying capability and higher output voltage levels using only one DC voltage source. Output voltage levels, higher than 17-level can also be achieved using the extended structure of proposed DASC-MLI. The potentiality of proposed DASC-MLI is verified through a cost function. Capacitor voltages are inherently balanced utilizing a combination of switches and diodes, thus completely eliminating the necessity of any external balancing circuit or algorithm in DASC-MLI. The number of capacitors and switches required in DASC-MLI are lower than reported SC-MLIs and thus its cost is lesser than reported SC-MLIs. The performance of the proposed DASC-MLI has been validated through a 580 W experimental prototype in this chapter. In order to further reduce the PIV, a new self-voltage balanced 17-level reduced voltage switched-capacitor MLI (RVSC-MLI) is proposed in the next chapter.

Chapter 6

A 17-Level Reduced Voltage Stress Switched Capacitor Multilevel Inverter

6.1 Introduction

In this chapter, a new 17-level reduced voltage switched-capacitor MLI (RVSC-MLI) is proposed. The peak inverse voltage (PIV) of the switches and diodes are within the input DC source voltage level in RVSC-MLI. The proposed RVSC-MLI can generate 17-level output voltage using a single DC voltage source with lesser number of circuit components. The TSV of the proposed RVSC-MLI is comparatively lower than existing SC-MLIs and diode assisted switched-capacitor MLI (DASC-MLI), which makes it suitable for higher voltage applications with low rated power devices. Higher voltage levels (more than 17-levels) can also be achieved using the extended structure of the proposed RVSC-MLI with only one DC voltage source. The output voltage of the proposed RVSC-MLI is more than the input voltage, which signifies its boosting capability. A voltage gain of two can be achieved using the proposed RVSC-MLI and the voltage gain can be further increased using the extended structure of it. In the proposed RVSC-MLI, the capacitors are periodically charged and discharged without using any voltage balancing mechanism.

6.2 Proposed Reduced Voltage Stress Switched-Capacitor MLI

The circuit configuration of the proposed RVSC-MLI is shown in Fig 6.1. It consists of thirteen unidirectional switches (S_1-S_5), (T_1-T_4), (Q_A-Q_D); four bidirectional switches (S_a-S_d); four diodes (D_A-D_D) and two floating capacitors (C_A and C_B). The PIV across all

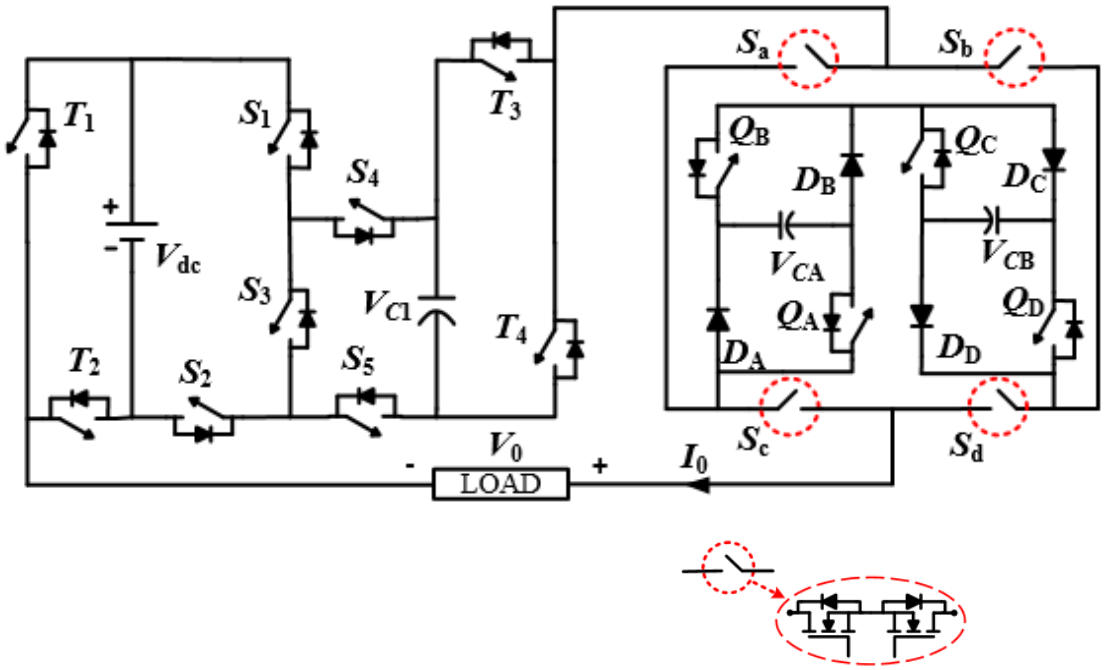


Fig. 6.1 Circuit configuration of the proposed 17-level RVSC-MLI.

switches and diodes are within supply voltage V_{dc} in the proposed RVSC-MLI. Different voltage levels can be generated by series and parallel combinations of voltage source and capacitors in the proposed circuit.

6.3 Generation of Voltage Levels

The switching patterns of different voltage levels for (left and right half) of both half cycles of the proposed 17-level RVSC-MLI are given in Table 6.1. The current path for different left half of positive voltage levels are shown in Fig. 6.2(a)-(i). In these figures, the blue colour indicates the current flowing path in the circuit. It can be observed from Table 6.1 that to maintain the voltages of the floating capacitors C_A and C_B at $V_{dc}/2$ and $V_{dc}/4$ respectively, their charging and discharging time intervals are kept identical. To verify the charge balance of capacitors C_A and C_B, the net charge Q_A and Q_B for a complete cycle are given as ($< >$ represents average current flowing through the capacitors for load impedance Z)

$$Q_A = \left[\langle i^{+L}_{C_A,\frac{V_{dc}}{4}}\rangle - \langle i^{+L}_{C_A,\frac{V_{dc}}{2}}\rangle + \langle i^{+L}_{C_A,\frac{3V_{dc}}{4}}\rangle - \langle i^{+L}_{C_A,\frac{5V_{dc}}{4}}\rangle + \langle i^{+L}_{C_A,\frac{3V_{dc}}{2}}\rangle - \langle i^{+L}_{C_A,\frac{7V_{dc}}{4}}\rangle + \right.$$

$$\langle i^{+R}_{C_A,\frac{3V_{dc}}{2}}\rangle - \langle i^{+R}_{C_A,\frac{V_{dc}}{2}}\rangle - \langle i^{-L}_{C_A,\frac{V_{dc}}{4}}\rangle + \langle i^{-L}_{C_A,\frac{V_{dc}}{2}}\rangle - \langle i^{-L}_{C_A,\frac{3V_{dc}}{4}}\rangle + \langle i^{-L}_{C_A,\frac{5V_{dc}}{4}}\rangle - \langle i^{-L}_{C_A,\frac{3V_{dc}}{2}}\rangle +$$

$$\left.\langle i^{-L}_{C_A,\frac{7V_{dc}}{4}}\rangle - \langle i^{-R}_{C_A,\frac{3V_{dc}}{2}}\rangle + \langle i^{-R}_{C_A,\frac{V_{dc}}{2}}\rangle\right] \cdot T$$

$$= \frac{1}{Z}\{(V_{dc} - V_{C_A} - V_{dc}/4) - V_{C_A} + (V_{dc} - V_{C_A} + V_{dc}/4) - (V_{dc} + V_{C_A} - V_{dc}/4) +$$

$$(2V_{dc} - V_{C_A}) - (V_{dc} + V_{C_A} + V_{dc}/4) + (2V_{dc} - V_{C_A}) - V_{C_A} - (V_{C_A} - V_{dc}/4) +$$

$$(V_{dc} - V_{C_A}) - (V_{C_A} + V_{dc}/4) + (2V_{dc} - V_{C_A} - V_{dc}/4) - (V_{dc} + V_{C_A}) + (2V_{dc} -$$

$$V_{C_A} + V_{dc}/4) - (V_{dc} + V_{C_A}) + (V_{dc} - V_{C_A})\}$$

$$= 8V_{dc} - 16V_{dc} \qquad (6.1)$$

$$Q_B = \left[\langle i^{+L}_{C_B,\frac{V_{dc}}{4}}\rangle - \langle i^{+L}_{C_B,\frac{3V_{dc}}{4}}\rangle + \langle i^{+L}_{C_B,\frac{5V_{dc}}{4}}\rangle - \langle i^{+L}_{C_B,\frac{7V_{dc}}{4}}\rangle + \langle i^{+R}_{C_B,\frac{7V_{dc}}{4}}\rangle - \langle i^{+R}_{C_B,\frac{5V_{dc}}{4}}\rangle \right.$$

$$+ \langle i^{+R}_{C_B,\frac{3V_{dc}}{4}}\rangle - \langle i^{+R}_{C_B,\frac{V_{dc}}{4}}\rangle + \langle i^{-L}_{C_B,\frac{V_{dc}}{4}}\rangle - \langle i^{-L}_{C_B,\frac{3V_{dc}}{4}}\rangle + \langle i^{-L}_{C_B,\frac{5V_{dc}}{4}}\rangle - \langle i^{-L}_{C_B,\frac{7V_{dc}}{4}}\rangle$$

$$\left. + \langle i^{-R}_{C_B,\frac{7V_{dc}}{4}}\rangle - \langle i^{-R}_{C_B,\frac{5V_{dc}}{4}}\rangle + \langle i^{-R}_{C_B,\frac{3V_{dc}}{4}}\rangle - \langle i^{-R}_{C_B,\frac{V_{dc}}{4}}\rangle\right] \cdot T$$

$$= \frac{1}{Z}\{(V_{dc} - V_{C_B} - V_{dc}/2) - (V_{dc} + V_{C_B} - V_{dc}/2) + (V_{dc} - V_{C_B} + V_{dc}/2) - (V_{dc} +$$

$$V_{C_B} + V_{dc}/2) + (2V_{dc} - V_{C_B}) + (V_{dc} - V_{C_B}) - V_{C_B} + (V_{dc}/2 - V_{C_B}) - (V_{C_B} +$$

$$V_{dc}/2) + (V_{dc} - V_{C_B}) + (2V_{dc} - V_{C_B} - V_{dc}/2) - (2V_{dc} + V_{C_B} - V_{dc}/2) + (2V_{dc} -$$

$$V_{C_B}) - (V_{dc} + V_{C_B}) + (V_{dc} - V_{C_B}) - V_{C_B}\}$$

$$= 4V_{dc} - 16V_{C_B} \qquad (6.2)$$

where $i^{+L}_{C_{A(B)},v_0}$, $i^{+R}_{C_{A(B)},v_0}$ are the currents through $C_{A(B)}$ in left and right half of positive

voltage level v_0, $i_{C_{A(B)},v_0}^{-L}$, $i_{C_{A(B)},v_0}^{-R}$ are the currents through $C_{A(B)}$ in left and right half of negative voltage level v_0, and T is the total time period of the output voltage.

At steady state, due to the symmetric nature of the output current and considering $Q_A = 0$ and $Q_B = 0$ in (6.1) and (6.2), it can be observed that the voltage across C_A and C_B are $V_{dc}/2$ and $V_{dc}/4$ respectively. As the capacitors are self-balanced and do not require additional circuit, the overall size, cost and complexity of the RVSC-MLI reduces.

The different voltage levels (left half) of positive half cycle are achieved in the proposed 17-level RVSC-MLI through Table 6.1 and Fig. 6.2 are given as

Level zero: Fig. 6.2(a) shows the circuit configuration of the zero-voltage level. It is achieved using switches T_2, S_2, S_3, S_4, T_3, S_a, Q_A, Q_C, S_d and diodes D_B, D_D.

Level $+V_{dc}/4$: Fig. 6.2(b) shows the circuit configuration of voltage level $+V_{dc}/4$. The voltage source V_{dc} charges the capacitors C_1 through the switches S_1, diodes of S_4, S_5 and S_2. The capacitor C_A charges through the diodes D_A and D_B, whereas C_B charges through diodes D_C and D_D. The switches T_2, T_3, S_a, S_d ensure positive voltage level across the load. The voltage of $+V_{dc}/4$ is obtained as ($+V_{dc}$ - $V_{dc}/2$ - $V_{dc}/4$).

Level $+V_{dc}/2$: Fig. Fig. 6.1(c) shows the circuit configuration of voltage level $+V_{dc}/2$. The capacitor C_A feeds the load to achieve the voltage level and it discharges through the switches Q_A and Q_B. The capacitor C_B is bypassed through the switch Q_C and diode D_D. The capacitor C_1 remains unaffected while the current flows using switches S_2, S_3 and S_4.

Level $+3V_{dc}/4$: Fig. 6.2(d) shows the circuit configuration for generation of voltage level $+3V_{dc}/4$. The voltage source V_{dc} charges the capacitors C_1 and C_A (as explained in level $V_{dc}/4$). The capacitor C_B discharges through the switches Q_C and Q_D. The voltage level $+3V_{dc}/4$ is obtained as (V_{dc} - $V_{dc}/2$ + $V_{dc}/4$).

Table 6.1
Switching Patterns and States of Capacitors of the Proposed 17-level RVSC-MLI

Output voltage levels	Switches	Capacitor states		
		C_1	C_A	C_B
$+2V_{dc}$	T_2, S_1, S_3, S_5, T_3, S_a, Q_A, Q_C, S_d	D	U	U
(+L) $+7V_{dc}/4$	T_2, S_1, S_4, S_2, S_5, T_3, S_a, Q_A, Q_B, Q_C, Q_D, S_d	C	D	D
(+R)	T_2, S_1, S_3, S_5, T_3, S_a, Q_A, S_d	D	U	C
$+3V_{dc}/2$	T_2, S_1, S_3, S_5, T_3, S_a, Q_C, S_d	D	C	U
(+L) $+5V_{dc}/4$	T_2, S_1, S_4, S_2, S_5, T_3, S_a, Q_A, Q_B, S_d	C	D	C
(+R)	T_2, S_1, S_4, S_2, S_5, T_3, S_a, Q_A, Q_C, Q_D, S_d	C	U	D
$+V_{dc}$	T_2, S_1, S_4, S_2, S_5, T_3, S_a, Q_A, Q_C, S_d	C	U	U
(+L) $+3V_{dc}/4$	T_2, S_1, S_4, S_2, S_5, T_3, S_a, Q_C, Q_D, S_d	C	C	D
(+R)	T_2, S_1, S_4, S_2, S_5, T_3, S_a, Q_A, S_d	C	U	C
$+V_{dc}/2$	T_2, S_2, S_3, S_4, T_3, S_a, Q_A, Q_B, Q_C, S_d	U	D	U
(+L) $+V_{dc}/4$	T_2, S_1, S_4, S_2, S_5, T_3, S_a, S_d	C	C	C
(+R)	T_2, S_2, S_3, S_4, T_3, S_a, Q_A, Q_C, Q_D, S_d	U	U	D
0	T_2, S_2, S_3, S_4, T_3, S_a, Q_A, Q_C, S_d	U	U	U

Output voltage levels	Switches	Capacitor states		
		C_1	C_A	C_B
$-2V_{dc}$	S_c, Q_B, Q_D, S_b, T_4, S_4, S_3, S_2, T_1	D	U	U
(-L) $-7V_{dc}/4$	S_c, Q_C, Q_D, S_b, T_4, S_4, S_3, S_2, T_1	D	C	D
(-R)	S_c, Q_A, S_b, T_4, S_4, S_3, S_2, T_1	D	U	C
$-3V_{dc}/2$	S_c, Q_A, Q_B, Q_C, S_b, T_4, S_1, S_4, S_5, S_2, T_1	C	D	U
(-L) $-5V_{dc}/4$	S_c, S_b, T_4, S_4, S_3, S_2, T_1	D	C	C
(-R)	S_c, Q_A, Q_C, Q_D, S_b, T_4, S_5, S_2, S_1, S_4, T_1	C	U	D
$-V_{dc}$	S_c, Q_B, Q_D, S_b, T_4, S_5, S_2, S_1, S_4, T_1	C	U	U
(-L) $-3V_{dc}/4$	S_c, Q_A, Q_B, Q_C, Q_D, S_b, T_4, S_5, S_3, S_1, T_1	U	D	D
(-R)	S_c, Q_A, S_b, T_4, S_5, S_2, S_1, S_4, T_1	C	U	C
$-V_{dc}/2$	S_c, Q_C, S_b, T_4, S_5, S_2, S_1, S_4, T_1	C	C	U
(-L) $-V_{dc}/4$	S_c, Q_A, Q_B, S_b, T_4, S_5, S_3, S_1, T_1	U	D	C
(-R)	S_c, Q_A, Q_C, Q_D, S_b, T_4, S_5, S_3, S_1, T_1	U	U	D
0	S_c, Q_B, Q_D, S_b, T_3, S_4, S_1, T_1	U	U	U

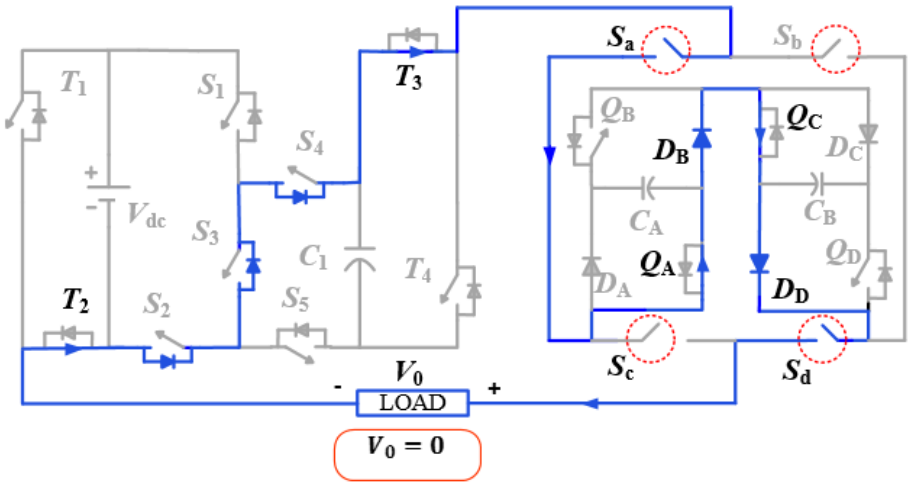
The column ON Switches represents the switches carrying load current. The capacitor states C is for charging, D for discharging, and U for unchanged. +L, +R are left and right half voltage levels of positive half cycle; -L, -R are left and right half voltage levels of negative half cycle.

Level $+V_{dc}$: Fig. 6.2(e) shows the circuit configuration of voltage level $+V_{dc}$. The voltage source feeds the load directly without involving any capacitor to generate the voltage level. C_1 is charged in this interval (as explained in level $V_{dc}/4$). The capacitors C_A and C_B remain unaffected and are bypassed through switches Q_A, Q_C and diodes D_B, D_D.

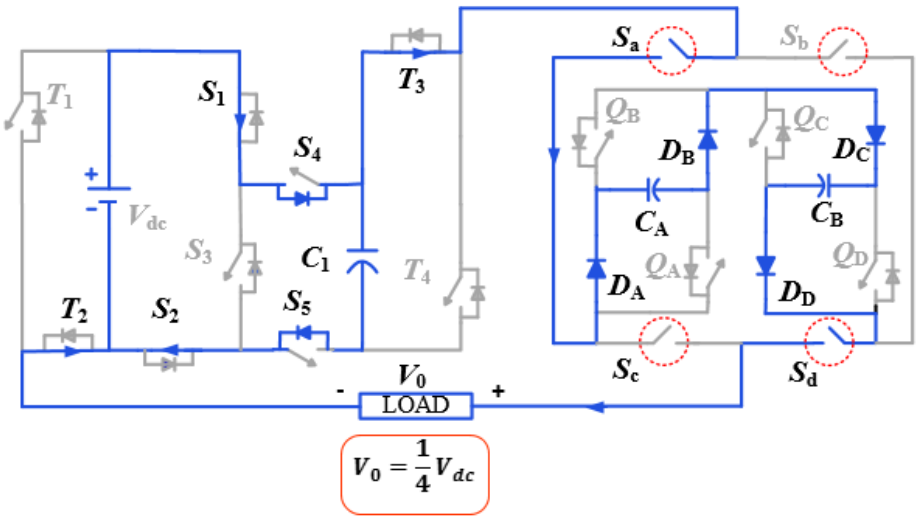
Level $+5V_{dc}/4$: Fig. 6.2(f) shows the circuit configuration for generation of voltage level $+5V_{dc}/4$. The switches T_2, S_1, S_4, S_2, S_5, T_3, S_a, Q_A, Q_B and S_d are turned on in this interval. The capacitors C_1 and C_B get charged in this interval. The capacitor C_A discharges through the switches Q_A and Q_B.

Level +3V_{dc}/2: Fig. 6.2(g) shows the circuit configuration of voltage level +3V_{dc}/2. The switches T_2, S_1, S_3, S_5, T_3, S_a, Q_C and S_d are turned on in this interval. The capacitors C_A get charged through the charging loop. The capacitor C_1 discharges in this interval through switches S_1, S_3 and S_5. The capacitor C_B remain unaffected and are bypassed through switches Q_A, Q_C and diodes D_B, D_D.

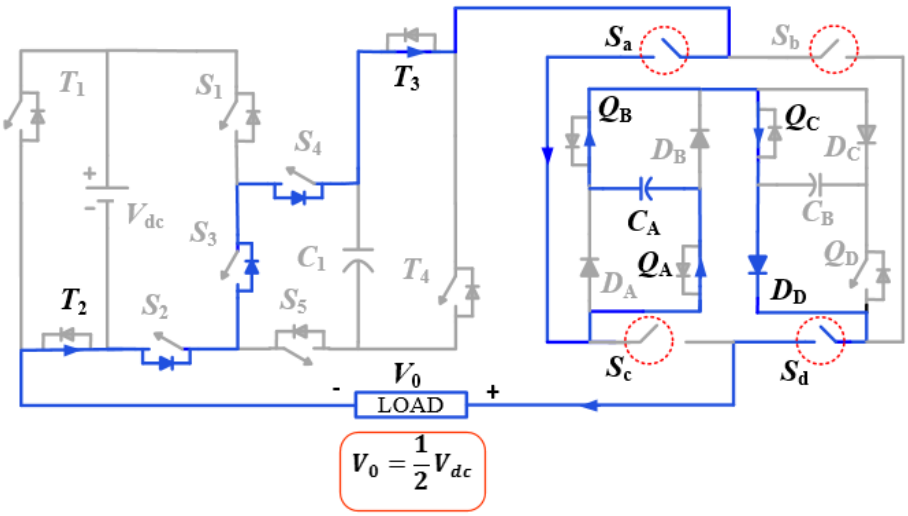
Level +7V_{dc}/4: Fig. 6.2(h) shows the circuit configuration for generation of voltage level +7V_{dc}/4. The voltage source V_{dc} charges the capacitors C_1 (as explained in level V_{dc}/4). The capacitor C_A and C_B discharges through the switches Q_A, Q_B, Q_C and Q_D. The voltage level +7V_{dc}/4 is obtained as (V_{dc} +V_{dc}/2 + V_{dc}/4).



(a)

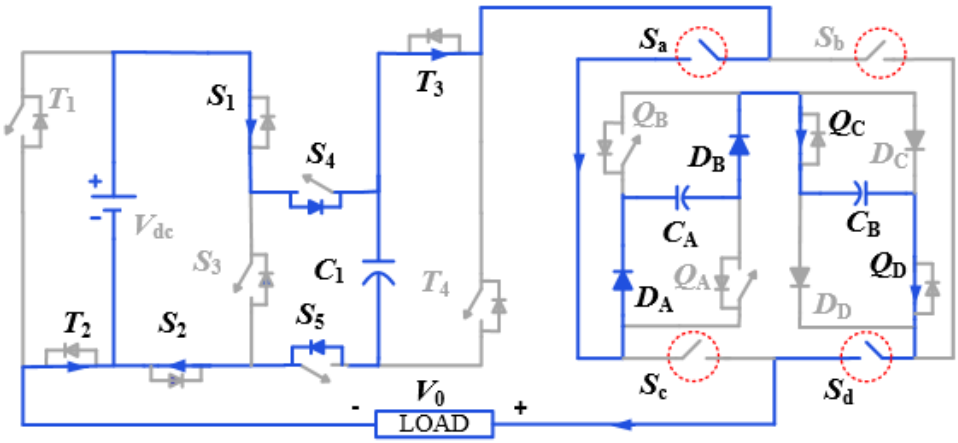


(b)



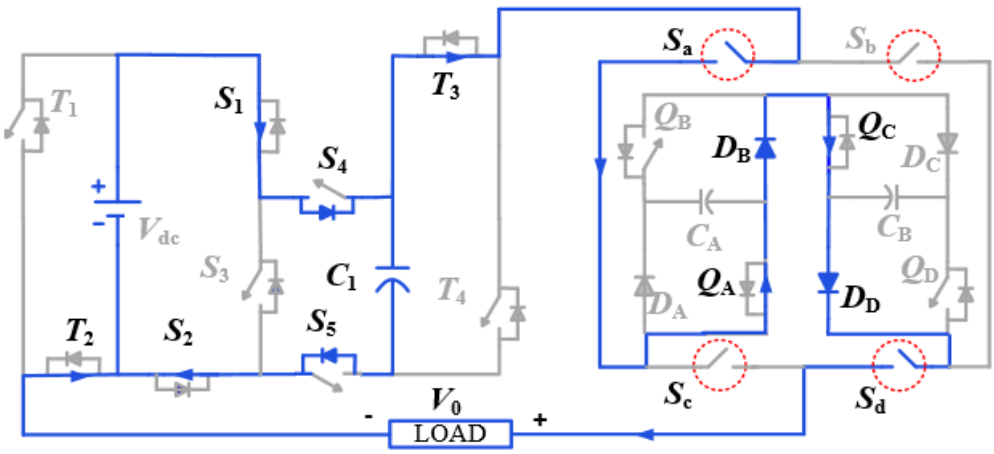
$$V_0 = \frac{1}{2}V_{dc}$$

(c)



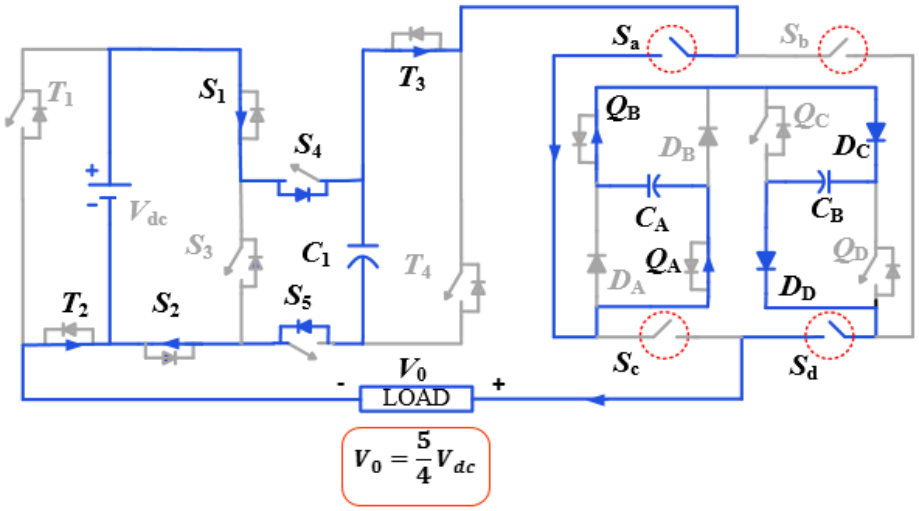
$$V_0 = \frac{3}{4}V_{dc}$$

(d)

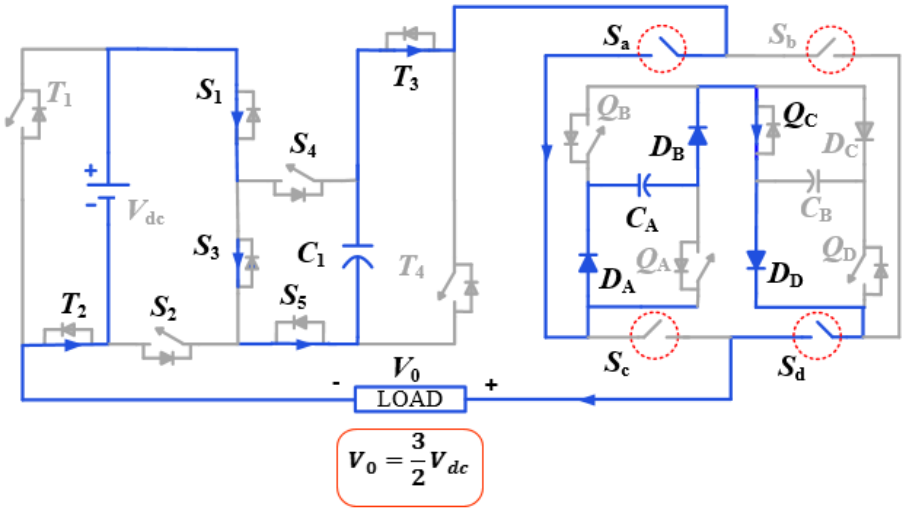


$$V_0 = V_{dc}$$

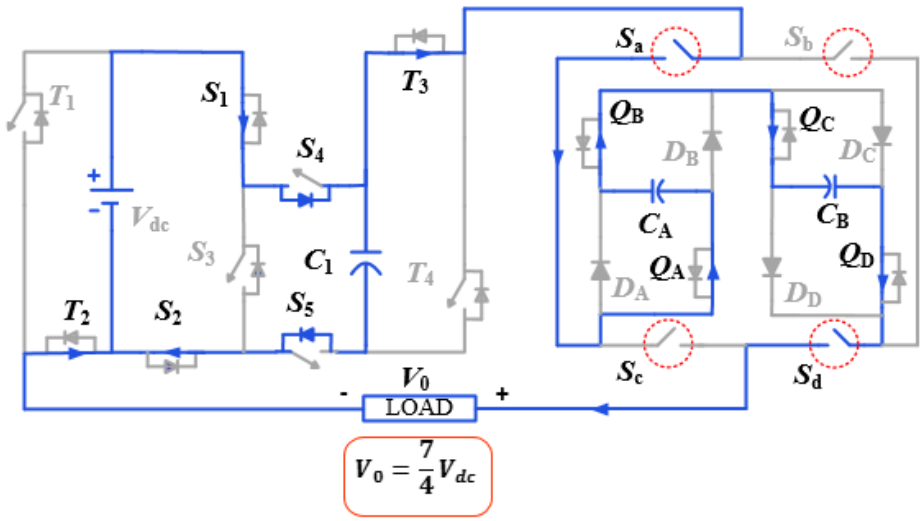
(e)


T_1
S_1
T_3
S_a
S_b
Q_B
D_B
Q_C
D_C
S_4
V_{dc}
C_A
C_B
S_3
C_1
T_4
Q_A
Q_D
D_A
D_D
T_2
S_2
S_5
S_c
S_d
V_0
LOAD
$V_0 = \frac{5}{4} V_{dc}$

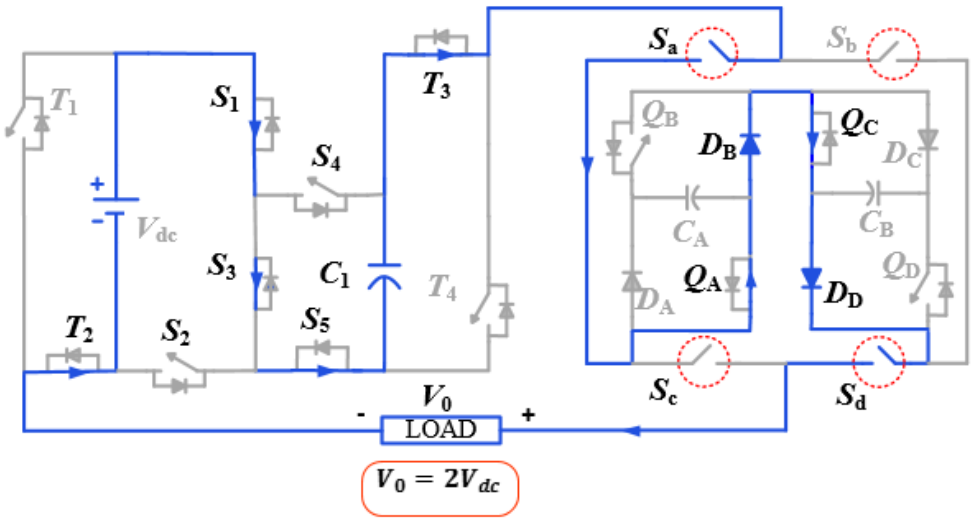
(f)


T_1
S_1
T_3
S_a
S_b
Q_B
D_B
Q_C
D_C
S_4
V_{dc}
C_A
C_B
S_3
C_1
T_4
Q_A
Q_D
D_A
D_D
T_2
S_2
S_5
S_c
S_d
V_0
LOAD
$V_0 = \frac{3}{2} V_{dc}$

(g)


T_1
S_1
T_3
S_a
S_b
Q_B
D_B
Q_C
D_C
S_4
V_{dc}
C_A
C_B
S_3
C_1
T_4
Q_A
Q_D
D_A
D_D
T_2
S_2
S_5
S_c
S_d
V_0
LOAD
$V_0 = \frac{7}{4} V_{dc}$

(h)



(i)

Fig. 6.2 Current flow for posituve voltage levels of the proposed 17-level RVSC-MLI. (a) Current flow at voltage level zero. (b) Current flow at voltage level $V_{DC}/4$. (c) Current flow at voltage level $V_{DC}/2$. (d) Current flow at voltage level $3V_{DC}/4$. (e) Current flow at voltage level V_{DC}. (f) Current flow at voltage level $5V_{DC}/4$. (g) Current flow at voltage level $3V_{DC}/2$. (h) Current flow at voltage level $7V_{DC}/4$. (i) Current flow at voltage level $2V_{DC}$.

Level $+2V_{dc}$: Fig. 6.2(i) shows the circuit configuration of voltage level $+2V_{dc}$. The voltage source and the capacitor C_1 feeds the load directly without involving any capacitor to generate the voltage level. C_1 is discharged in this interval thorough switches S_1, S_3 and S_5. The capacitors C_A and C_B remains unchanged in this interval. The voltage level $+2V_{dc}$ is obtained as (V_{dc} +V_{dc}).

6.4 Generalized Structure of the Proposed 17-level RVSC-MLI

For achieving higher voltage levels, the proposed RVSC-MLI structure can be extended by cascading the (switches $S_{1,i}$-$S_{5,i}$ and capacitors $C_{1,i}$), where i is the number of units are connected in cascade as shown in Fig. 6.3. The generalized structure of the proposed RVSC-MLI does not require any additional voltage source to achieve higher voltage levels.

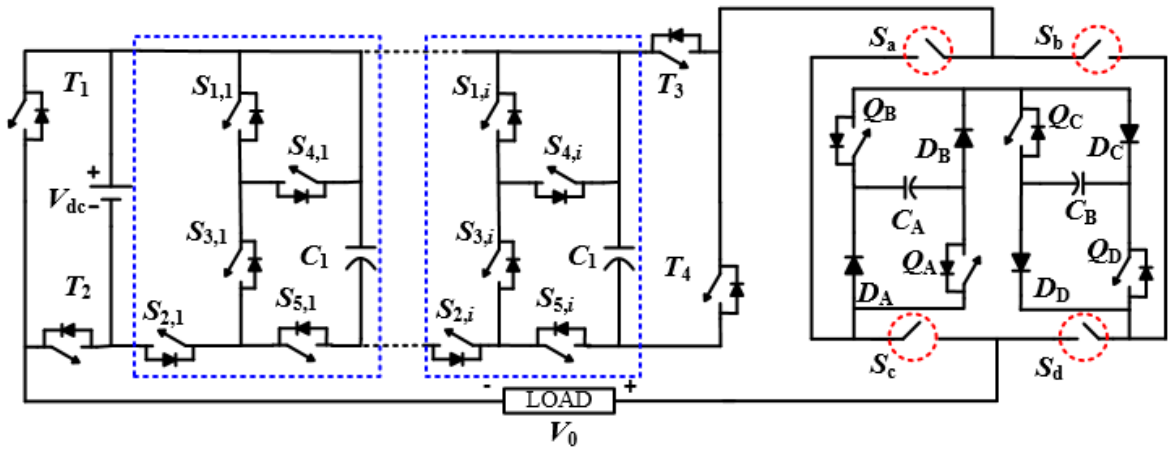


Fig. 6.3 Extended structure of the proposed 17-level RVSC-MLI.

Table 6.2
Maximum Blocking Voltage Across Switches of 17-level RV-SCMLI

Switches	Maximum voltage stress($\times V_{dc}$)	Switches	Maximum voltage stress($\times V_{dc}$)
S_1	1	T_4	1
S_2	1	S_a	$\frac{3}{4}$
S_3	1	S_b	$\frac{3}{4}$
S_4	1	S_c	$\frac{3}{4}$
S_5	1	S_d	$\frac{3}{4}$
T_1	1	Q_A	$\frac{1}{2}$
T_2	1	Q_B	$\frac{1}{2}$
T_3	1	Q_C, Q_D	$\frac{1}{4}$, $\frac{1}{4}$

The maximum blocking voltages of all switches are given in Table 6.2. The PIV across all switches are within input DC source voltage V_{dc}. From Table 6.2, the TSV of the 17-level RVSC-MLI is calculated by adding the individual PIV of all switches and is obtained as

$$\begin{cases} \text{TSV} = 16.5V_{dc} \\ \text{PIV} = 1V_{dc} \end{cases} \tag{6.3}$$

The PIV of switches and diodes in the generalized structure of the proposed RVSC-MLI are within V_{dc}. The number of active and passive elements for generating $8n-7$ voltage levels in the proposed generalized RVSC-MLI (where n is the number of capacitors) can be expressed as

$$\begin{cases} N_{switch} = 5n+6 \\ N_{diode} = 4 \\ N_{source} = 1 \end{cases} \tag{6.4}$$

where N_{switch}, N_{diode} and N_{source} are the number of switches, diodes and DC sources respectively.

6.5 Switching Scheme

Selective harmonic elimination technique using modified grey wolf optimization is used to generate the switching angles of the proposed RVSC-MLI. The switching angles and output voltage levels of the proposed 17-level RVSC-MLI is shown in Fig. 6.4, where the amplitude of each step voltage and switching angle are taken as $\pm V_{dc}/4$ and θ_i (i=1-8) respectively. Fourier expansion of the quasi-square waveform of the output voltage for the proposed 17-level RVSC-MLI is given as

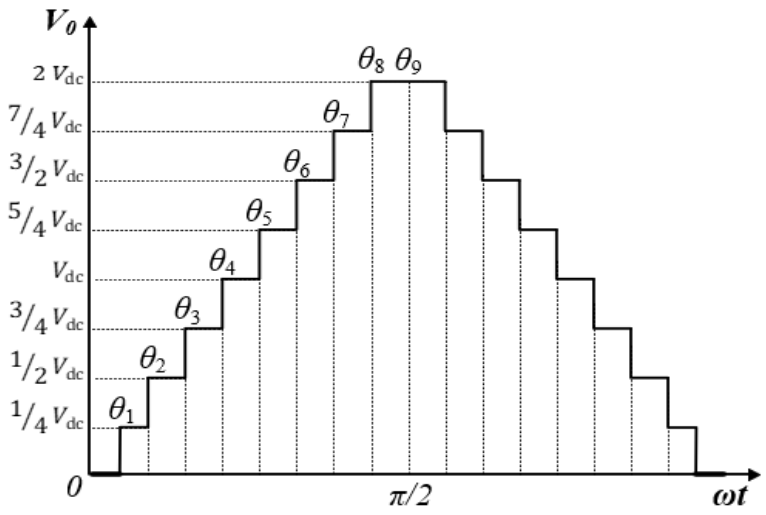


Fig. 6.4 Switching angles and output voltage levels of the proposed 17-level RVSC-MLI.

$$V_0 = \frac{V_{dc}}{2\pi} \sum_{k=1,3,\cdots}^{\infty} \sum_{i=1}^{8} \frac{\cos(k\theta_i)}{k} \sin k\omega t \tag{6.5}$$

where ω is the angular frequency of the staircase output voltage waveform. The amplitude modulation index (M_{of}) of the fundamental output voltage waveform is expressed as:

$$M_{of} = \frac{1}{8} \sum_{i=1}^{8} \cos(\theta_i) \tag{6.6}$$

The switching angles for 17-level RVSC-MLI θ_i (i = 1-8) are obtained using

$$\begin{cases} \cos\theta_1 + \cos\theta_2 + \cos\theta_3 + \cos\theta_4 + \cos\theta_5 + \cos\theta_6 + \cos\theta_7 + \cos\theta_8 = 8M_{of} \\ \cos(m\theta_1) + \cos(m\theta_2) + \cos(m\theta_3) + \cos(m\theta_4) + \cos(m\theta_5) \\ + \cos(m\theta_6) + \cos(m\theta_7) + \cos(m\theta_8) = 0 \end{cases} \tag{6.7}$$

where m is the number of harmonics. The harmonics such as 5th, 7th, 11th, 13th, 17th, 19th and 23rd are considered for obtaining the switching angles.

6.6 Capacitance Calculation

To calculate the values of the capacitances, the longest discharging cycles of the capacitors are considered. It can be observed from Table 6.1 that the capacitor C_1 has the longest discharging cycle in the interval θ_8 to $\pi - \theta_6$. The capacitor C_A has the longest discharging period from $\pi - \theta_6$ to $\pi + \theta_8$, which consists of a few small charging intervals also. The discharging intervals are $\pi - \theta_7$ to $\pi - \theta_6$, $\pi + \theta_2$ to $\pi + \theta_3$, $\pi + \theta_5$ to $\pi + \theta_6$ and $\pi + \theta_7$ to $\pi + \theta_8$, whereas the charging intervals are $\pi - \theta_3$ to $\pi - \theta_2$, $\pi + \theta_1$ to $\pi + \theta_2$, $\pi + \theta_3$ to $\pi + \theta_4$ and $\pi + \theta_6$ to $\pi + \theta_7$. The capacitor C_B has the longest discharging period from θ_7 to θ_8. The maximum discharging values Q_{C1}, Q_A and Q_B of the capacitors C_1, C_A and C_B are given as

$$Q_{C_1} = \frac{1}{\omega}\left[\int_{\theta_8}^{\pi-\theta_8} i_o d\theta + \int_{\pi-\theta_8}^{\pi-\theta_7} i_o d\theta + \int_{\pi-\theta_7}^{\pi-\theta_6} i_o d\theta\right] \tag{6.8}$$

$$Q_{C_A} = \frac{1}{\omega}\left[\int_{\pi-\theta_7}^{\pi-\theta_6} i_o d\theta - \int_{\pi-\theta_3}^{\pi-\theta_2} i_o d\theta - \int_{\pi+\theta_1}^{\pi+\theta_2} i_o d\theta + \int_{\pi+\theta_2}^{\pi+\theta_3} i_o d\theta\right.$$

$$\left. - \int_{\pi+\theta_3}^{\pi+\theta_4} i_o d\theta + \int_{\pi+\theta_5}^{\pi+\theta_6} i_o d\theta - \int_{\pi+\theta_6}^{\pi+\theta_7} i_o d\theta + \int_{\pi+\theta_7}^{\pi+\theta_8} i_o d\theta\right] \tag{6.9}$$

$$Q_{C_B} = \frac{1}{\omega}\left[\int_{\theta_7}^{\theta_8} i_o d\theta\right] \tag{6.10}$$

where $i_0=\frac{v_0}{R_L}$, v_0 is output voltage at the respective intervals (given in Table 6.1) and R_L is load resistance. The maximum allowable voltage ripples across the capacitor C_i is kV_{Ci} (i=1, A, B), where k is the ripple factor. The optimal value of the capacitance (C_i) is given as

$$C_i \geq \frac{Q_{Ci}}{kV_{Ci}} \text{ for } i = 1, \text{A, B} \tag{6.11}$$

Substituting the values of i_0 into (6.8), (6.9) and (6.10) and from (6.11), the values of capacitors (C_1, C_A and C_B) are obtained as

$$C_{1\min} = \frac{1}{8\pi f_S R_L k}\left(8\pi - 6\theta_6 - \theta_7 - 9\theta_8\right) \tag{6.12}$$

$$C_{A\min} = \frac{1}{4\pi f_S R_L k}\left(\theta_1 - \theta_2 + 3\theta_3 - 3\theta_4 - 5\theta_5 + 5\theta_6 - 7\theta_7 + 7\theta_8\right) \tag{6.13}$$

$$C_{B\min} = \frac{1}{2\pi f_S R_L k}\left(-7\theta_7 + 7\theta_8\right) \tag{6.14}$$

6.7 Switching Loss Calculation

The switching loss occurs due to charging and discharging of parasitic capacitances of switches. Switching loss occurs during the turn on and turn off of switches in a cycle [51]. The switching loss during turn on $P_{\mathrm{sw},i(\mathrm{on})}$ and turn off $P_{\mathrm{sw},i(\mathrm{off})}$ are given as

$$\begin{aligned} P_{\mathrm{sw},i\,(\mathrm{on})} &= f_{\mathrm{sw}} \int_0^{t_{on}} V_{\mathrm{sw},i}(\mathrm{t}).i(t)dt \\ &= f_{sw} \int_0^{t_{on}} \left(\frac{V_{sw,i}}{t_{on}} \cdot t \right) \left(-\frac{I_i}{t_{on}} (t - t_{on}) \right) dt \\ &= \frac{1}{6} f_{sw,i} V_{\mathrm{sw},i} I_i t_{on} \end{aligned} \tag{6.15}$$

$$\begin{aligned} P_{\mathrm{sw},i\,(\mathrm{off})} &= f_{\mathrm{sw}} \int_0^{t_{off}} V_{\mathrm{sw},i}(\mathrm{t}).i(t)dt \\ &= f_{sw} \int_0^{t_{off}} \left(\frac{V_{\mathrm{sw},i}}{t_{off}} \cdot t \right) \left(-\frac{I_i^{'}}{t_{off}} (t - t_{off}) \right) dt \\ &= \frac{1}{6} f_{sw} V_{\mathrm{sw},i}\, I_i^{'} t_{off} \end{aligned} \tag{6.16}$$

where $V_{\mathrm{sw,i}}$ is the off-state voltage of the i^{th} switch, I_{i} is the current of the i^{th} switch when the switch is turned on, I_{i}' is the current of the i^{th} switch before the turn off of the switch, t_{on} is the duration when the switch is turned on, t_{off} is the duration when the switch is turned off and f_{sw} is the switching frequency. To calculate total switching loss, the number of N_{on} and the number of N_{off} switching states per one cycle is multiplied by (6.15) and (6.16). The total switching loss is calculated as

$$P_{\mathrm{S}} = \sum_{i=1}^{17} \left(\sum_{j=1}^{N_{on(i)}} P_{\mathrm{sw,on(ij)}} + \sum_{j=1}^{N_{off\,(i)}} P_{\mathrm{sw,off(ij)}} \right) \tag{6.17}$$

Using (6.17), the total switching loss of the proposed 17-level RVSC-MLI is obtained as

$$P_{\mathrm{S}} = \frac{14.65 {V_{dc}}^2}{R_L} f_s t_{on} + \frac{13.76 {V_{dc}}^2}{R_L} f_s t_{off} \tag{6.18}$$

6.8 Conduction Loss Analysis

Conducting loss is caused by the parasitic parameters such as on-state resistances of switches, voltage drops of diodes, and the currents in the circuits. The diodes (including the body diodes of switches) are assumed to have the same voltage drop V_D and resistance r_d. All the switches are assumed to have the same on-state resistance r_s. The conduction loss of the proposed 17-level RVSC-MLI is given as

$$P_{con} = \frac{2}{\pi}\sum_{i=1}^{8}\left\{\frac{V_0 - V_{Deq}}{r_{eq} + R_L}\right\} \times r_{eq}.\left(\theta_{i+1} - \theta_i\right) \tag{6.19}$$

where V_0, V_{Deq}, r_{eq} and R_L are the output voltage, the equivalent voltage drops of diodes, the equivalent parasitic resistance and the load resistance respectively.

6.9 Ripple Loss Analysis

The ripple loss occurs at the time of charging of capacitors at different switching instances. The voltage ripple of capacitors is obtained as

$$\Delta V_{Ci} = \frac{1}{C_i}\int_{t}^{t'} i_{c_i}(t).dt \tag{6.20}$$

where i_{c_i} is the capacitor current and $t - t'$ is the charging interval. The ripple voltages of capacitors (C_1, C_A and C_B) are given as:

$$\Delta V_{C1} = \frac{1}{8\pi f_S R_L C_1}\left(8\pi - 6\theta_6 - \theta_7 - 9\theta_8\right) \tag{6.21}$$

$$\Delta V_{CA} = \frac{1}{4\pi f_S R_L C_2}\left(\theta_1 - \theta_2 + 3\theta_3 - 3\theta_4 - 5\theta_5 + 5\theta_6 - 7\theta_7 + 7\theta_8\right) \tag{6.22}$$

$$\Delta V_{CB} = \frac{1}{2\pi f_S R_L C_B}\left(-7\theta_7 + 7\theta_8\right) \tag{6.23}$$

The ripple loss in one cycle operation of the output voltage is given as

$$P_{\mathrm{R}} = \frac{1}{2T} \sum_{i=1,\mathrm{A},\mathrm{B}} C_i \Delta V_i^2 \tag{6.24}$$

where C_{i} and ΔV_i are the i^{th} capacitor and ripple voltage of it.

The efficiency of the proposed 17-level RVSC-MLI can be written as

$$\eta = \frac{P_0}{P_0 + P_C + P_S + P_R} \tag{6.25}$$

where P_0, P_{C}, P_{S} and P_{R} are the output power, conduction, switching and ripple losses.

6.10 Comparison with Other Reported SC-MLI Topologies

In this section, the proposed RVSC-MLI is compared with other reported SC-MLIs in terms of active and passive components, TSV, PIV and cost as given in Table 6.3. The proposed SC-MLI requires one DC voltage source, PIV and TSV is reduced as compared to the reported SC-MLIs. In [59] and [60] number of sources increases linearly with the output voltage level. In [38], [40], [47] and [56] to generate 17-level output voltage, seven capacitors are required and TSV and PIV are also relatively higher as compared to proposed RVSC-MLI. The topology presented in [40] and [47] requires thirty-nine and twenty-five switches to generate a 17-level output voltage with higher TSV and PIV as compared to proposed topology. The TSV and PIV of the topologies [12-18] and DASC-MLI are much higher than the proposed RVSC-MLI. The generalized graphical representation of PIV and TSV versus output voltage levels for different topologies are shown in Fig. 6.5(a) and (b).

A cost function (CF) has been used to compare the proposed RVSC-MLI with the reported SC-MLIs and is given as [54]

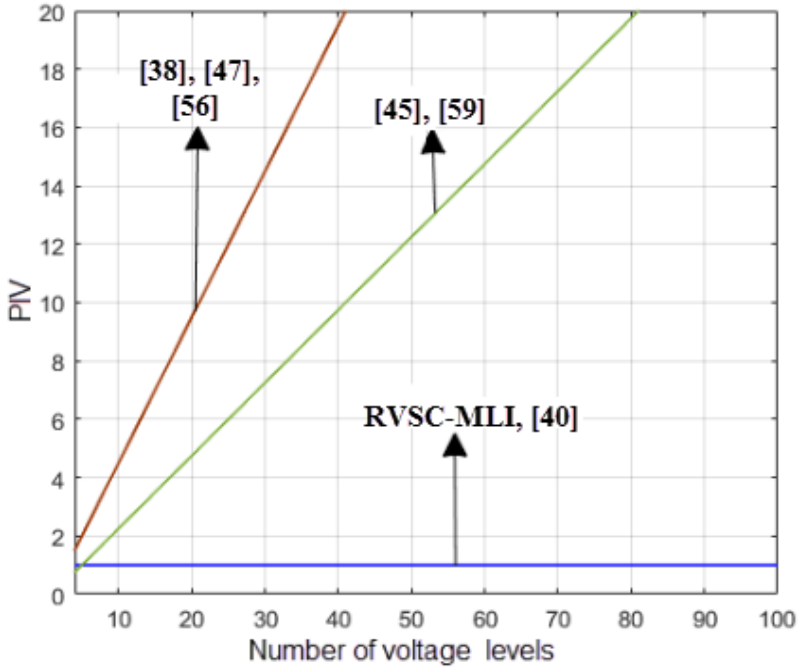
$$\mathrm{CF} = \left(N_{\mathrm{switch}} + N_{\mathrm{cap}} + N_{\mathrm{diode}} + \lambda TSV_{\mathrm{pu}} + \delta PIV_{\mathrm{pu}} \right) N_{\mathrm{source}} \tag{6.26}$$

Table 6.3
Comparison of proposed 17-level RVSC-MLI with Reported 17-level SC-MLI Topologies

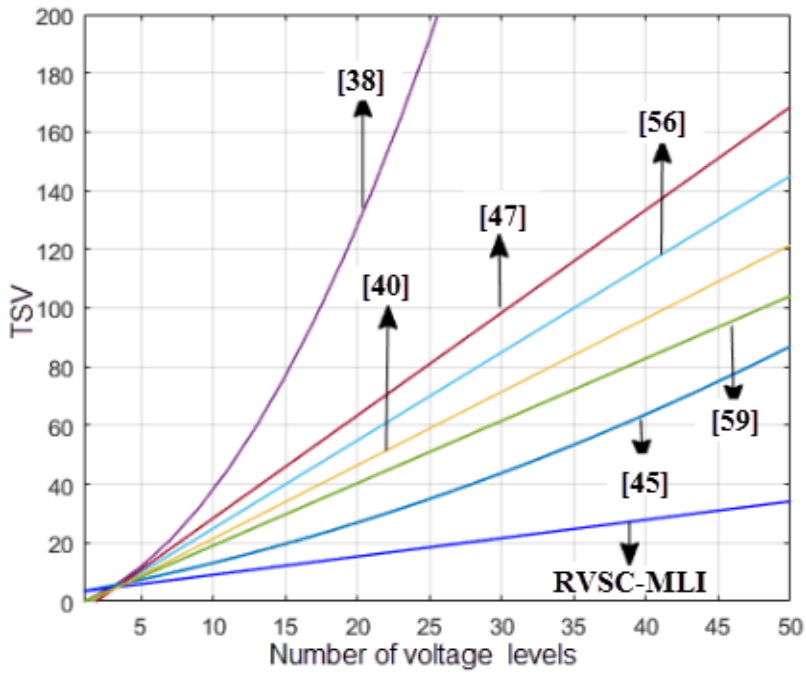
Parameters	[60]	[47]	[40]	[59]	[56]	[38]	[45]	DASC-MLI	RVSC-MLI
N_{Source}	8	1	1	4	1	1	1	1	1
N_{Switch}	18	25	39	14	18	12	17	11	21
N_{Cap}	0	7	7	4	7	7	4	4	3
N_{Diode}	0	0	0	20	7	14	4	5	4
TSV($\times V_{dc}$)	32	53	39	34	46	96	29	25.5	16.5
PIV($\times V_{dc}$)	8	8	1	4	8	8	4	4	1
CF (λ=0.5, δ=0.5)	304	62.5	66	228	59	85	41.5	34.75	36.75
CF (λ=1.5, δ=0.5)	560	115.5	105	364	105	181	70.5	60.25	53.25
CF (λ=0.5, δ=1.5)	368	70.5	67	244	67	93	45.5	38.75	37.75
CF (λ=1.5, δ=1.5)	624	123.5	106	380	113	189	74.5	64.25	54.25
Boosting Feature and Extendibility	No	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes

where N_{switch}, N_{cap}, N_{diode} and N_{source} are the number of switches, capacitors, diodes, DC source and λ, δ are the importance factors of TSV_{pu} and PIV_{pu}. The active/passive components such as the number DC voltage sources, number of switches, capacitors and diodes are considered in the cost calculation. To explain the effects of TSV and PIV in the proposed CF, weight coefficients λ and δ are multiplied in per unit scales. The values of λ and δ mentioned in Table 3 are: λ=0.5, δ=0.5; λ=1.5, δ=0.5; λ=0.5, δ=1.5 and λ=1.5, δ=1.5. It is important to note that if λ and δ are less than one, the required number of passive components are given more importance in the cost calculation. However, if λ and δ are more than one, TSV and PIV are given more importance in the cost calculation. Referring Table 6.3, when λ=0.5 and δ=0.5, the required number of passive components are given more importance; for λ=1.5 and δ=0.5, TSV is given more importance; for λ=0.5 and δ=1.5, PIV is given more importance; for λ=1.5 and δ=1.5, both TSV and PIV are given importance in the cost calculation. Thus, the cost calculated using four different

values of λ and δ shows the merits of the proposed RVSC-MLI for all cases, whether passive components or TSV and/or PIV are given more importance.



(a)



(b)

Fig. 6.5 Comparison of the proposed 17-level RVSC-MLI with reported SC-MLIs. (a) PIV versus number of voltage levels. (b) TSV with number of voltage levels.

6.11 Simulation Studies

The performance of the proposed RVSC-MLI is simulated in MATLAB/Simulink. The DC source voltage V_{DC} is taken as 100 V. Fundamental switching strategy (50 Hz) is used and the value of modulation index is taken as 0.75. Considering 10% voltage ripple, the values of capacitors C_1, C_A and C_B obtained using (6.12)-(6.14) are approximately 1470 µF, 660 µF and 800 µF respectively. The output voltage V_0 and current I_0 waveforms of the proposed 17-level RVSC-MLI for a resistive load (R = 40 Ω) are shown in Fig. 6.6(a). The measured rms values of voltage and current are 135.5 V and 3.42 A respectively.

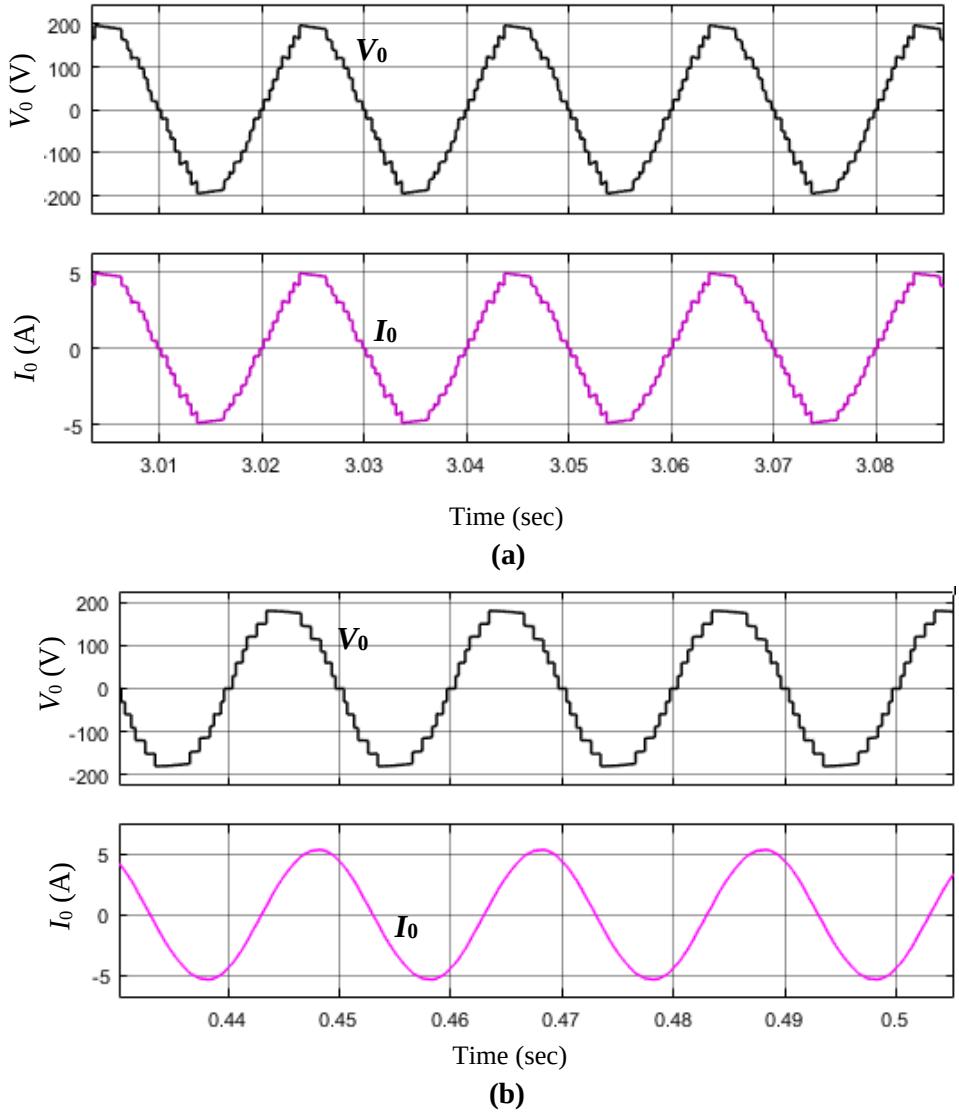


Fig. 6.6 Simulation results of the proposed 17-level RVSC-MLI. (a) Output voltage (V_o) and current (I_o) for R load (R= 40 Ω). (b) Output voltage (V_o) and current (I_o) for R-L load (R= 40 Ω, L= 60 mH).

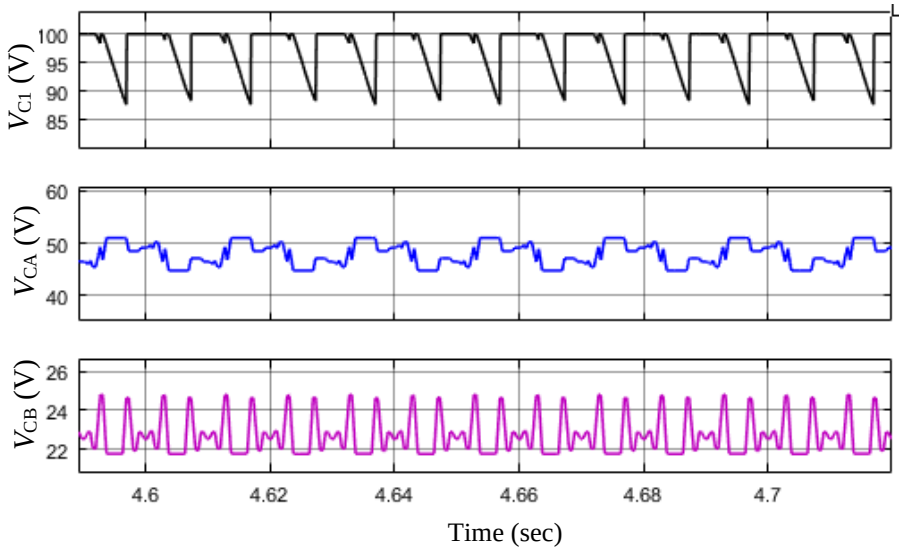
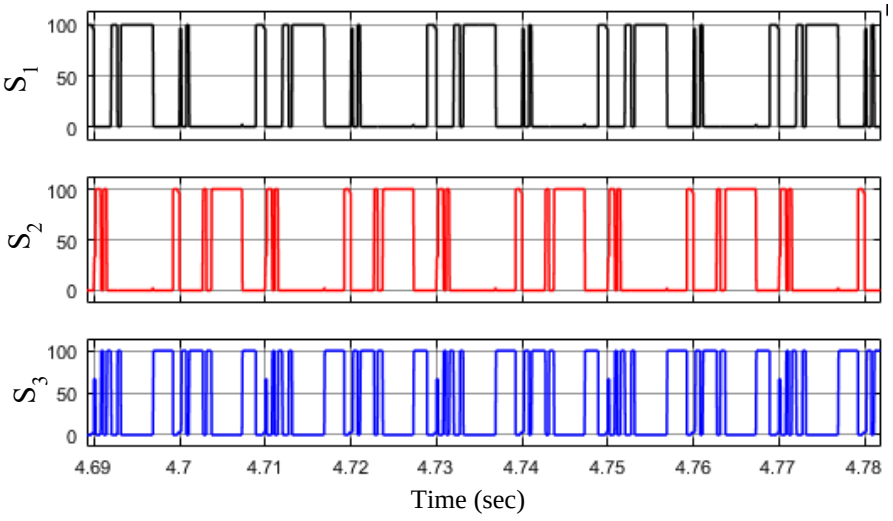


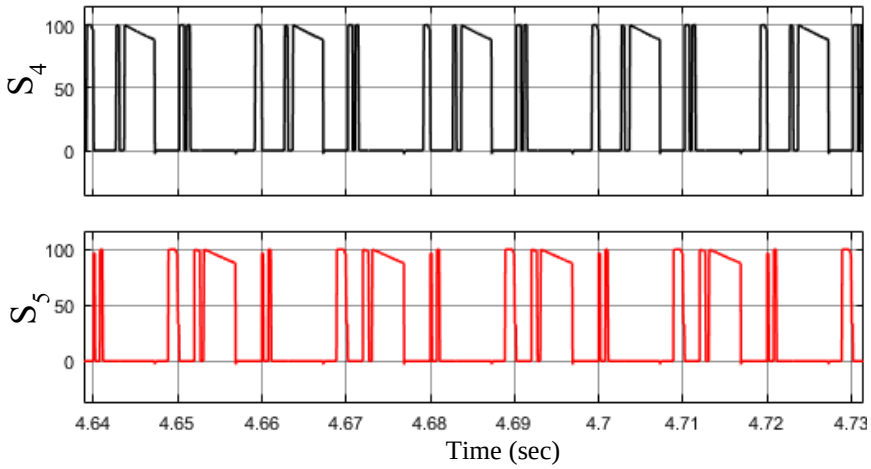
Fig. 6.7 Simulation results of capacitor voltages of RV-SCMLI. (V_{C1}, V_{CA} and V_{CB}).

The output voltage V_0 and current I_0 waveforms for *R-L* (40 Ω and 60 mH) condition loading condition is shown in Fig. 6.6(b). The three capacitor voltages are shown in Fig. 6.7. It can be observed from Fig. 6.7 that capacitor voltages V_{C1}, V_{CA} and V_{CB} are self-balanced at voltages V_{C1} = 100 V, V_{CA} = 50 V and V_{CB} = 25 V respectively. The voltage stresses across switches of (S_1, S_2, S_3, S_4 and S_5) of the proposed RVSC-MLI are shown in Fig. 6.8(a) and (b) respectively. The voltage stresses across switches (S_1, S_2, S_3 S_4 and S_5) are measured as 100 V respectively. The voltage stresses across switches (S_a, S_b, S_c and S_d) are shown in Fig. 6.8(c). It can be observed from Fig.6.8(c) that the voltage measured across switches (S_a, S_b, S_c and S_d) are 75 V respectively.

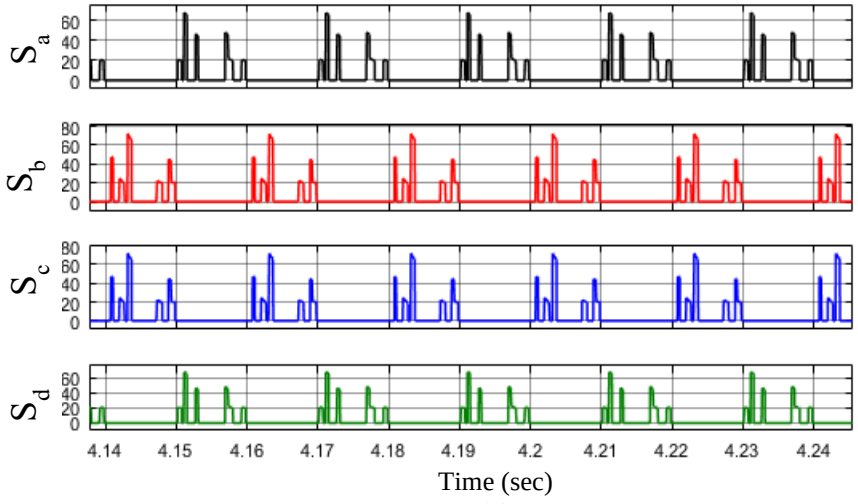


(a)

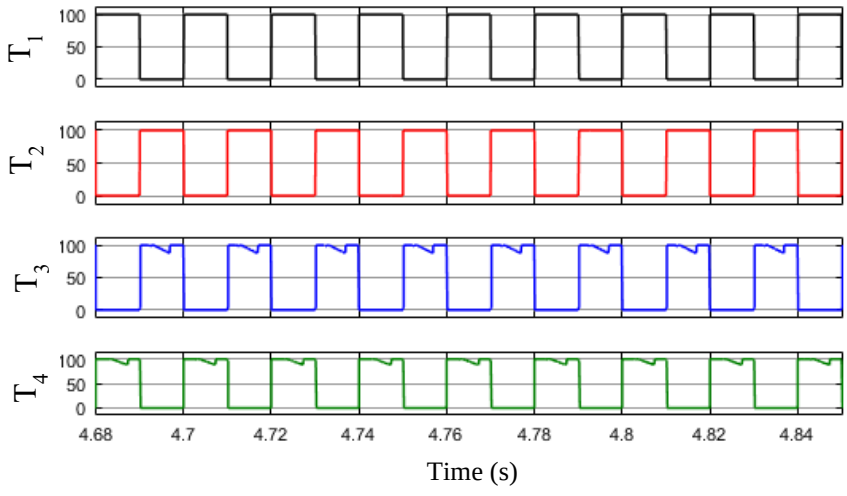
The voltage stresses across switches T_1, T_2, T_3 and T_4 are shown in Fig. 6.8(d) and are measured as 100 V respectively. Similarly, the voltage stresses across switches (Q_A, Q_B, Q_C and Q_D) are shown in Fig. 6.8(e) and measured as 50 V, 50 V, 25 V and 25 V respectively.



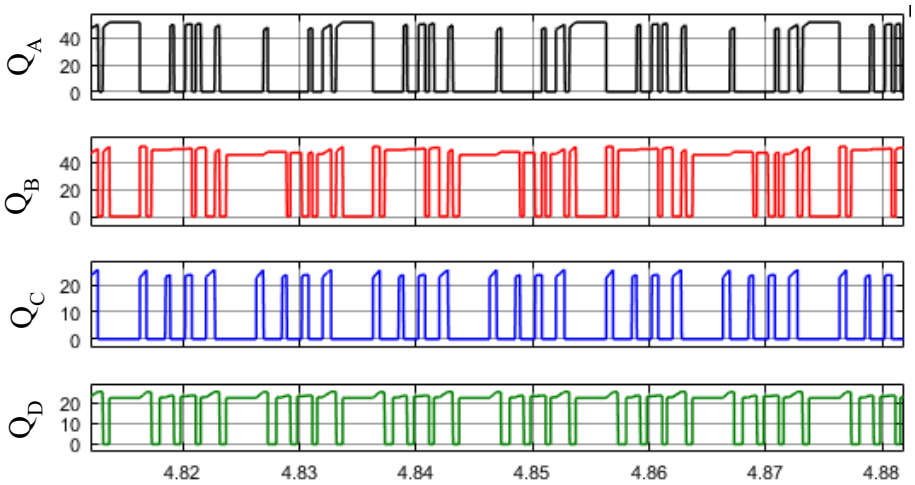
(b)



(c)



(d)



(e)

Fig. 6.8 Simulation results of voltage stress of the proposed RVSC-MLI. (a) Voltage stresses across switches (S_1, S_2 and S_3). (b) Voltage stresses across switches (S_4 and S_5). (c) Voltage stresses across switches (S_a, S_b, S_c and S_d). (d) Voltage stresses across switches (T_1, T_2, T_3 and T_4). (e) Voltage stresses across switches (Q_A, Q_B, Q_C and Q_D).

The dynamic performance of the proposed RVSC-MLI is verified through simulation in this work. The load resistance is step changed from 80 Ω to 40 Ω to observe the dynamic behaviour of the RV-SCMLI. The load current is changed from 1.8 A to 3.53 A due to step change in resistance and is shown in Fig. 6.9. From Fig. 6.9, it can be noticed that the load change does not any effect on output voltage waveform. Hence, it confirms the inherent voltage balance of capacitors in the proposed RVSC-MLI.

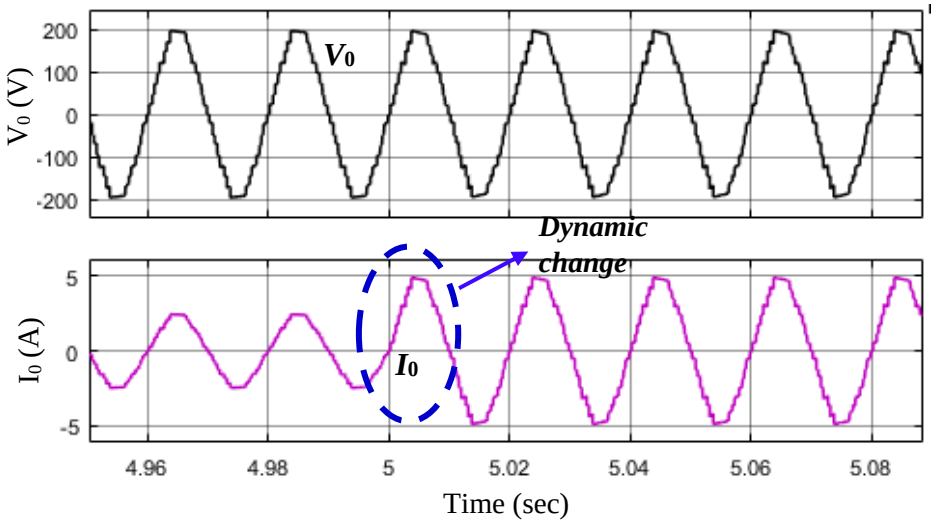


Fig. 6.9 Dynamic performance of the proposed RVSC-MLI for step-down change in load resistance.

6.12 Experimental Validation

The performance of the proposed RVSC-MLI is validated through a 550 W experimental prototype, as shown in Fig. 6.10. The parameters used in experiment are listed in Table 6.4.

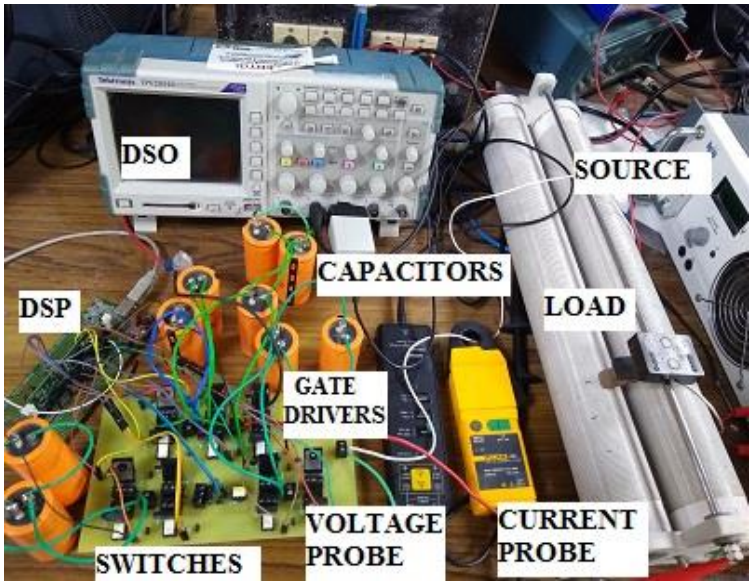


Fig. 6.10 Photograph of experimental prototype (17-level RV-SCMLI).

Table 6.4
Devices and Parameters Used for Experimentation

Microcontroller	TI-TMS320F28335
IGBT	HGTG12N60A4D
Gate Drivers	FOD-3184
Electrolytic Capacitors	1470µF (C_1), 660 µF (C_A) and 800 (C_B)

6.12.1 Steady State Performance

The steady state performance of the proposed RV-SCMLI is investigated in this section. The input DC source voltage V_{dc} is as taken 100 V. Fundamental switching strategy (50 Hz) is used and the value of M_{of} is taken as 0.75 in this study. The input voltage V_{dc}, input current $I_{in,}$ voltage V_0 and output current I_0 waveforms of the proposed 17-level RVSC-MLI for a resistive load ($R = 40\ \Omega$) are shown in Fig. 6.11(a) and the rms values of V_0 and I_0 are 134.8 V and 3.37 A respectively. The measured frequency of V_0 and I_0 is 50 Hz.

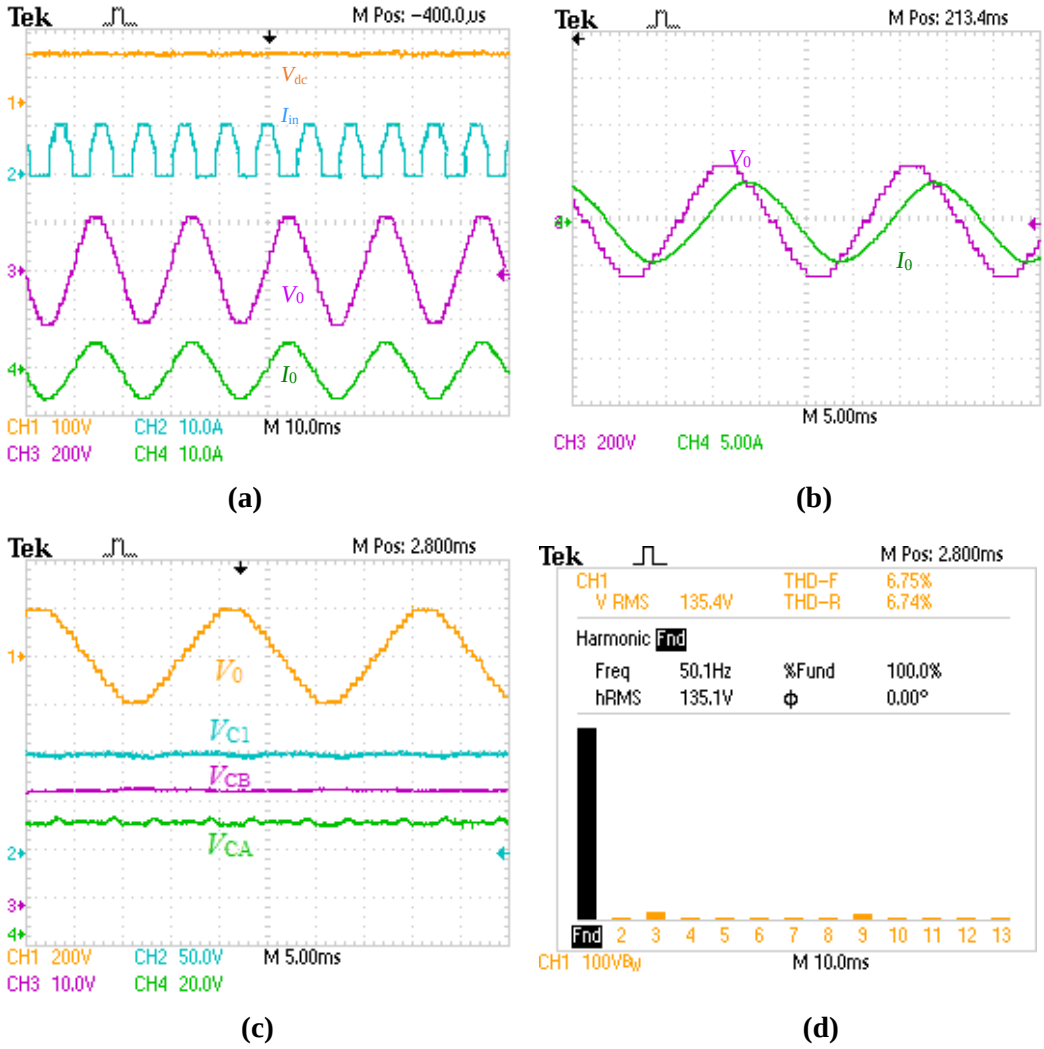


Fig. 6.11 Experimental results of the proposed RVSC-MLI. (a) Input voltage (V_{dc}), Input current (I_{in}), Output voltage (V_o) and current (I_o) for *R* load. (b) Output voltage (V_o) and current (I_o) for *R-L* load. (c) Capacitor voltages (V_{C1}, V_{CA}, V_{CB}). (d) Harmonic spectrum of V_o.

For *R-L* load (R = 40 Ω, L = 60 mH), output voltage V_0 and current I_0 are shown in Fig. 6.11(b). It can be observed from Fig. 6.11(c) that capacitor voltages (V_{C1}, V_{CA} and V_{CB}) are balanced at 100 V, 50 V and 25 V respectively. The ripples voltage ΔV_{C1}, ΔV_{CA} and ΔV_{CB} of capacitors are 9 V, 4.5 V and 2.5 V respectively. The harmonic spectrum of the output voltage V_0 is shown in Fig. 6.11(d) and THD is measured as 6.75%. The voltage stresses across switches of (S_1, S_2, S_3, S_4 and S_5) are shown in Fig. 6.12(a) and (b) and measured as 100 V respectively. Similarly, the voltage stresses across switches (T_1, T_2, S_c and S_d) and (T_3, T_4, S_a and S_b) are shown in Fig. 6.12(c) and (d) respectively.

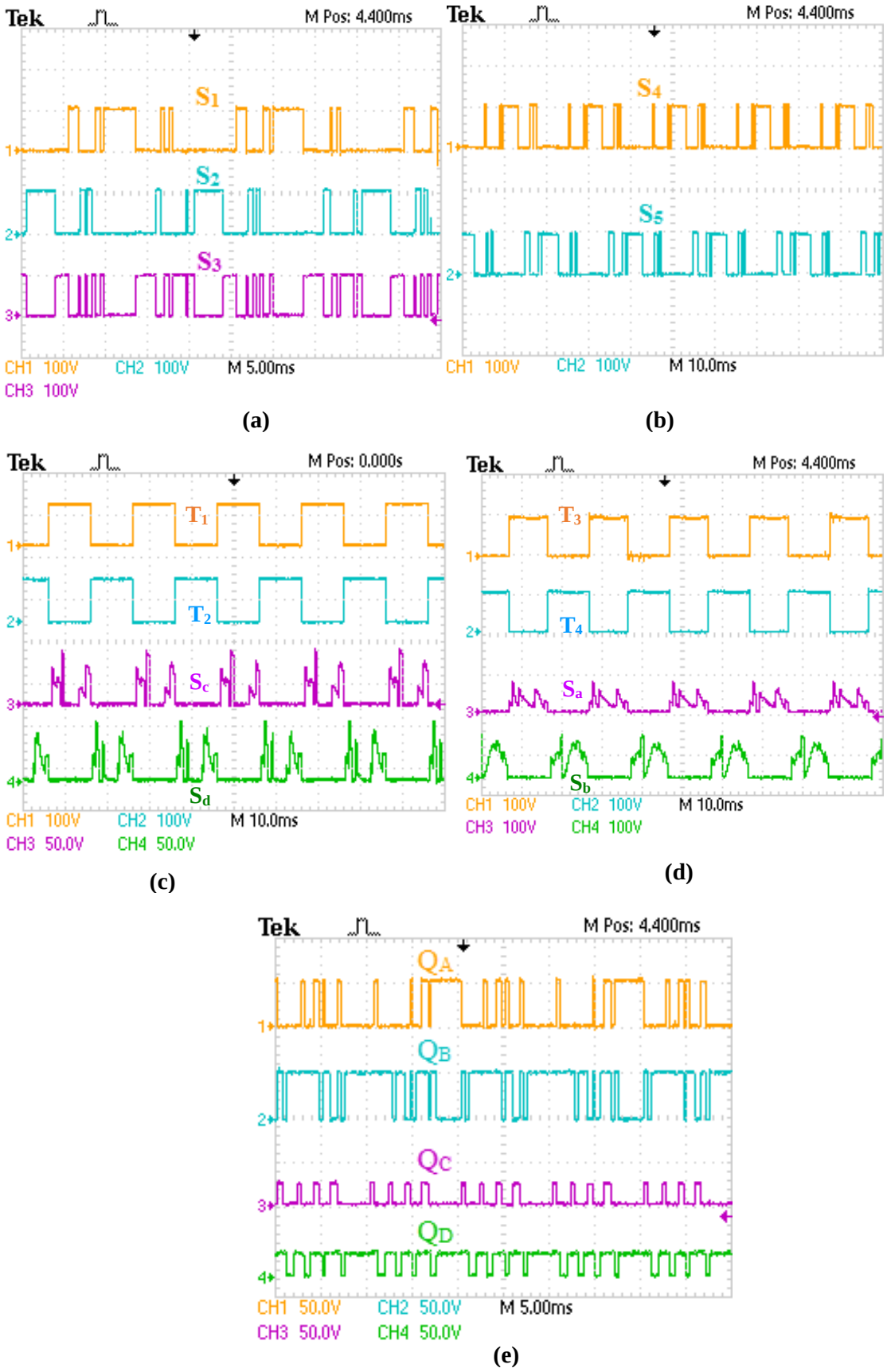
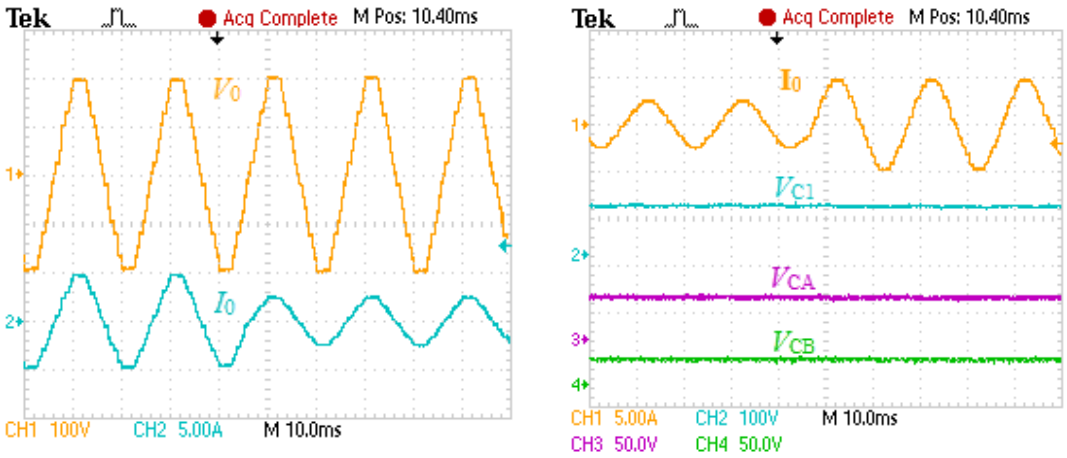


Fig. 6.12 Experimental results of voltage stresses of the proposed RVSC-MLI. (a) Voltage stresses across switches (S_1, S_2, S_3). (b) Voltage stresses across switches (S_4, S_5). (c) Voltage stresses across switches (T_1, T_2, S_c, S_d). (d) Voltage stresses across switches (T_3, T_4, S_a, S_b). (e) Voltage stresses across switches (Q_A, Q_B, Q_C, Q_D).

It can be observed that the voltage stress across the switches T_1, T_2, S_c and S_d are 100 V, 100 V, 75 V and 75 V respectively and the voltage stresses across switches T_3, T_4, S_a and S_b are 100 V, 100 V, 75 V and 75 V respectively. The voltage stresses across switches (Q_A, Q_B, Q_C and Q_D) are shown in 6.12(e) and are measured as Q_A, Q_B, Q_C and Q_D are 50 V, 50 V, 25 V and 25 V respectively.

The voltage stresses across diodes of the proposed SC-MLI are also within input DC voltage V_{dc}. From the experimental results, it is verified that the PIV of all switches of the proposed RVSC-MLI are within input DC voltage V_{dc}. The voltage stresses across diodes of the proposed RVSC-MLI are also within V_{dc}.

The switching loss, conduction loss and ripple loss are calculated using (6.18), (6.19) and (6.24) and are given as 8.51 W, 20.78 W and 9.67 W respectively. From Fig. 6.11(a), the measured input power P_{in} = 500 W, output power P_{out} = 456 W and loss P_{loss} = 44 W, which gives efficiency η = 91.2%.



(a) **(b)**

Fig. 6.13 Dynamic performance of the proposed RVSC-MLI. (a) Step-down change in load current. (b) Step-up change in load current.

6.12.2 Dynamic Performance

The dynamic performance of the proposed RV-SCMLI is investigated in this section. The load resistance is changed to observe the dynamic response of the proposed RVSC-MLI.

The dynamic response for step-down change in load current 5 A (peak) to 2.5 A (peak) and step-up change in load current 2.5 A (peak) to 5 A (peak) are shown in Fig. 6.13(a) and (b) respectively. From Fig. 6.13(a) it can be observed that the load change does not have any considerably effect on the output voltage waveform and Fig. Fig. 6.13(b) confirms the self-voltage balance of capacitors in the proposed RVSC-MLI.

6.13 Conclusion

An extendable 17-level RVSC-MLI with reduced voltage stress and lesser number of active and passive components using a single DC voltage source is presented in this chapter. It has been observed that the PIV across all the switches and diodes are within the input DC voltage in proposed RVSC-MLI. Higher voltage levels than 17 can also be achieved through the extended structure of the proposed RVSC-MLI. The proposed RVSC-MLI requires lower rated power switches as compared to existing SC-MLIs due to reduction in PIV. Moreover, a voltage gain of two is achieved through the proposed 17-level RVSC-MLI which can be further increased through the extended structure of it. Comparative analysis with the reported SC-MLIs validates its merits in terms of PIV, TSV and active/passive components. Capacitor voltage balance has been achieved in the proposed RVSC-MLI without using any additional circuit. The performance of the proposed RVSC-MLI has been validated through experimental prototype.

Chapter 7

Conclusion and Future Scope

7.1 Conclusion

This work presents modified particle optimization (MPSO), modified whale optimization (MWO) and modified grey wolf optimization (MGWO) for harmonic minimization of hybrid cascaded multilevel inverter (HC-MLI) using SHE-PWM. The results obtained through MPSO, MWO and MGWO are compared in terms of harmonic minimization in HC-MLI as compared to genetic algorithm (GA), particle swarm optimization (PSO), whale optimization (WO) and grey wolf optimization (GWO).

It has been observed that at higher number of output voltage levels, the number of active and passive components are very high in HC-MLI and complicated voltage balancing mechanism is required in them, which makes the overall system bulkier and complex. The problem can be reduced using switched capacitor based MLIs (SC-MLIs), where the number of active and passive components are less as compared to HC-MLI. In SC-MLIs, the capacitors are self-balanced, and therefore the switching scheme is simplified. Two new topologies of SC-MLI, named as diode assisted switched-capacitor MLI (DASC-MLI) and reduced voltage stress switched capacitor MLI (RVSC-MLI) are proposed in this work using MGWO, wherein the number of active and passive components are further reduced. Moreover, the peak inverse voltage (PIV) and total standing voltage (TSV) are also reduced in DASC-MLI and RVSC-MLI as compared to reported SC-MLIs.

In chapter 2, an MPSO optimized three-phase, 11-level HC-MLI using SHE-PWM technique is explored. Improvements in weight and velocity features in MPSO take care of local optima efficiently, leading to better convergence rate and lower harmonic content as compared to GA and PSO. The proposed MPSO optimized HC-MLI ensures capacitor voltage balance, even at higher modulation indices by utilizing the available redundancies of HC-MLI. The capacitor voltage balance in HC-MLI is also achieved at higher modulation indices using harmonic injection method in this work. In chapter 3, MWO optimized three-phase, 11-level HC-MLI is presented. The adaptive position co-efficient vector and exponentially decaying function in MWO gives improved results as compared to conventional WO. In MWO, the chaotic local search technique efficiently takes care of possible local optima and enhances its convergence rate. Moreover, the proposed MWO balances the capacitor voltage even at higher modulation indices, exploiting the redundancies of HC-MLI. In chapter 4, MGWO optimized SHE-PWM has been used for harmonic minimization in HC-MLI. The use of adaptive position co-efficient vector and exponentially decaying function gives improved results as compared to GWO in MGWO. The chaotic local search technique in MGWO avoids local optima stagnation, while weighted position method enhances the convergence rate**.** The MGWO reaches global optima faster than other reported algorithms discussed in this work and effectively eliminates selected lower order harmonics from the output voltage. Some of the applications of the proposed work are medium and high-power motor drives, static synchronous compensators and active power filters. The work has been validated though theoretical findings and simulations. A 1.5-kW prototype is developed to demonstrate the steady state and dynamic performance of the proposed MPSO, MWO and MGWO optimized three-phase HC-MLIs.

Two new topologies of SC-MLIs, 17-level DASC-MLI and RVSC-MLI using reduced active and passive components are presented in chapters 5 and 6. The basic unit of DASC-MLI and RVSC-MLI require only one DC voltage source to generate output voltage levels using lesser number of active and passive components as compared to existing SC-MLIs. Also, TSV and PIV of DASC-MLI and RVSC-MLI are reduced as compared to reported SC-MLIs. Also, they have improved reverse current carrying capability as compared to existing SC-MLIs. Higher output voltage levels than 17-level can also be achieved using extended structure of DASC-MLI and RVSC-MLI. Capacitor voltage balance has been achieved without using any additional circuit in DASC-MLI and RVSC-MLI. The proposed circuits have been verified through extensive simulation and scale down experimentation.

7.2 Future Scope

- Other reported advanced PWM techniques (other than SHE-PWM) such as selective harmonic mitigation PWM (SHM-PWM) and selective harmonic elimination pulse amplitude modulation (SHE-PAM) can also be applied to the proposed MPSO, MWO and MGWO optimized HC-MLI to further reduce the harmonics in the output voltage waveform.
- SHM-PWM and SHE-PAM methods can also be explored in DASC-MLI and RVSC-MLI.
- Advanced digital processors such as field programmable gate array (FPGA), real-time laboratory (RT-LAB), dSPACE, etc. can be used to in place of DSP to achieve improved results.
- Applications of proposed HC-MLI, DASC-MLI and RVSC-MLI can be investigated in the area of renewable energy.

- Grid integration of proposed MLIs is another area which can also investigated. During grid integration modes, the power quality issues are required to be addressed by designing efficient switching techniques and robust controllers.

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List of Publications

Journals:

1. **Abhinandan Routray**, R. K. Singh and R. Mahanty, "Harmonic Minimization in Three-Phase Hybrid Cascaded Multilevel Inverter Using Modified Particle Swarm Optimization," **IEEE Transactions on Industrial Informatics**, **vol. 15, no. 8, pp. 4407-4417, Aug. 2019.**

2. **Abhinandan Routray**, R. K. Singh and R. Mahanty, "Harmonic Reduction in Hybrid Cascaded Multilevel Inverter Using Modified Grey Wolf Optimization," **IEEE Transactions on Industry Applications, vol. 56, no. 2, pp. 1827-1838, Mar/Apr, 2020.**

3. **Abhinandan Routray**, R. K. Singh and R. Mahanty, "Selective Harmonic Elimination in Hybrid Cascaded Multilevel Inverter Using Modified Whale Optimisation," **International Transactions on Electrical Energy Systems, vol 30, no.4, Mar, 2020, DOI:10.1002/2050-7038.12298.**

4. Y. Khandelwal, **Abhinandan Routray,** R. K. Singh and R. Mahanty, "Reduced voltage stress hybrid multilevel inverter using optimised predictive control," **IET Power Electronics (Accepted) DOI:10.1049/iet-pel.2019.1314.**

5. **Abhinandan Routray,** J. Motawani, R. K. Singh and R. Mahanty, "Seventeen-Level Extendable Switched Capacitor Multilevel Inverter Using One Voltage Source and Reduced Components," **IET Power Electronics (first revision submitted).**

6. **Abhinandan Routray,** R. K. Singh and R. Mahanty, "Modified Grey Wolf Optimization Based Hybrid Multilevel Inverter Using Reduced Components," **IET Power Electronics (in review).**

7. **Abhinandan Routray**, R. K. Singh and R. Mahanty, "Quasi-resonant hybrid multilevel inverter for suppressed peak capacitor current spikes," **IET Power Electronics (in review).**

International Conferences:

1. **Abhinandan Routray**, R. K. Singh and R. Mahanty, "Selective Harmonic Elimination and Balancing of Capacitor Voltage in Hybrid Cascaded Multilevel Inverter Using Model Predictive Control," 2019 IEEE Energy Conversion Congress and Exposition **(ECCE), Baltimore**, MD, USA, 2019, pp. 2597-2602.

2. **Abhinandan Routray**, K. Shiluveru, Akash Singh, R. K. Singh and R. Mahanty, "Reduced Voltage Stress Thirteen-Level Extendable Switched Capacitor Multilevel Inverter," 2019 IEEE Energy Conversion Congress and Exposition **(ECCE), Baltimore**, MD, USA, 2019, pp. 6224-6230.

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4. **Abhinandan Routray**, R. K. Singh and R. Mahanty, "Capacitor Voltage Balancing in Hybrid Cascaded Multilevel Inverter Using Genetic Algorithm at Higher Modulation Indices," 2018 IEEE Energy Conversion Congress and Exposition **(ECCE), Portland**, OR, USA, 2018, pp. 3688-3693.

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6. **Abhinandan Routray**, R. K. Singh and R. Mahanty, "Scalable Thirteen-Level Hybrid Multilevel Inverter Using Reduced Components," 2020 IEEE Energy Conversion Congress and Exposition **(ECCE), Detroit,** Michigan, USA. (**Accepted**).

7. J.K. Motwani, **Abhinandan Routray,** R. K. Singh and R. Mahanty, "Optimized Predictive Control of Hybrid Multilevel PV Inverter with Reduced Leakage Current," 2020 IEEE Energy Conversion Congress and Exposition **(ECCE), Detroit,** Michigan, USA. (**Accepted**).

8. **Abhinandan Routray**, A. Singh, R. K. Singh and R. Mahanty, "Reduced voltage stress extendable seventeen-level multilevel inverter using single voltage source," 2019, 10th Power Electronics and Machine Drives **(PEMD), University of Nottingham, UK**, 2019. (**Accepted**).

9. **Abhinandan Routray**, V. Patel, R. Mahanty and R. K. Singh, "A novel GA optimized SHE PWM hybrid cascaded H-bridge multilevel inverter with Capacitor Voltage Averaging for motor drive applications," 2016 IEEE International Conference on Power Electronics, Drives and Energy Systems **(PEDES),** Trivandrum, 2016, pp. 1-5.

10. **Abhinandan Routray**, R. K. Singh and R. Mahanty, "Capacitor Voltage Balancing in Hybrid Cascaded Multilevel Inverter Using Modified Model Predictive Control," 2020 IEEE International Conference on Emerging Trends in Communication, Control and Computing (**ICONC3**), Lakshmangarh, Sikar, India, 2020, pp. 1-5, DOI: 10.1109/ICONC345789.2020.9117356.