Chapter 3

A Current Driven Fractional Power Processor for Ultra-Fast Charging

3.1 Introduction

Ultra-fast charging (UFC) is the most recent technology marching towards making the battery charging time comparable to refueling time. It refers to charging the battery at very high power, of the order of 350 kW to replenish the battery state-of-charge quickly within few minutes [127]. However, this reduced time comes at the cost of high current, likely up to 400 A which brings the disadvantage of high conduction losses across converter components, eventually requiring large heat sink and thermal management, thereby degrading the power density. In addition, the component cost, availability, and essential battery current control becomes challenging for designing converter of such high-power rating. The existing literature reported many approaches to mitigate the current and voltage stress including thew use of GaN and SiC switches, interleaving multiple stages, multi-level topologies to reduce size of passive component, etc. However, the converter still needs to be designed at maximum deliverable power that keeps the major UFC challenges persistent.

3.2 The Concept of Fractional Power Processing

An interesting approach to eliminate these challenges associated with high power processing is the fractional power processing approach, where converter only processes a fraction of total power [128] A Review of DC-DC Resonant Converter Topologies and Control Techniques for Electric Vehicle Applications. This is achieved by interconnecting the source to load through two channels, one being the converter that processes a part of power and other being a series path that directly transfers the bulk power from source to load. The power which is processed through converter is subjected to various losses such as conduction loss occurring in switches and conducting path, switching loss during turn-on and turn-off of the switches, and magnetic losses due to

inductors and transformers in its path. Thus, a part of power is lost during this processing. However, the rest of the power that is being directly transferred through the series path results in negligible losses. Therefore, it may be concluded that there is a two-fold reduction in loss, one due to theoretically loss-less transfer through series path, and secondly due to reduced loss in converter as a result of reduced power being processed. This leads to a significant reduction in the over-all loss component and therefore substantial improvement in overall system efficiency [129].

Further, one of the most attractive features identified out of the fractional power processing concept-based architecture is its application to utilize the conventional full-rated converters as a fractional power processing unit and making it suitable for UFC application. The reported FPP topologies for battery charging application were widely explored for unidirectional phase shifted full bridge converters however, their application remains limited with V2G demands gaining pace in modern EV ecosystem. Further, the existing approaches did not take into account the performance degradation due to lower light-load efficiency and loss of soft-switching. Swift and precise battery current control is another major challenges that typically required dedicated PI controllers to implement fast and robust current control.

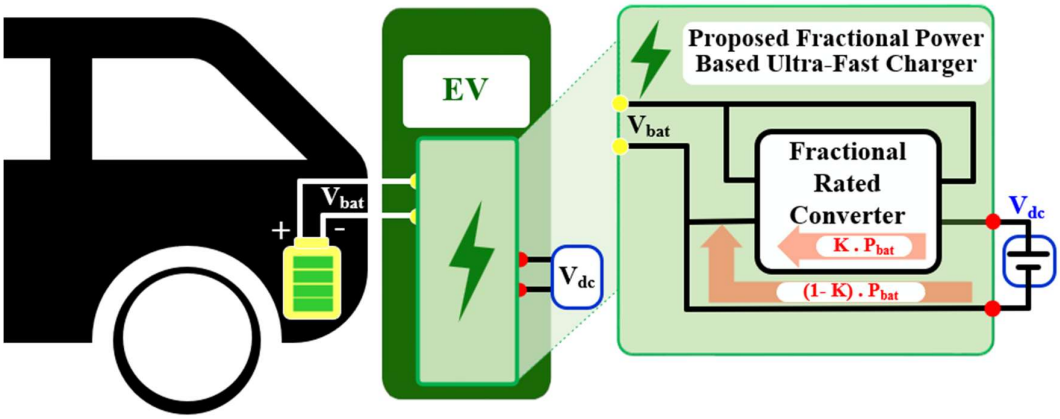


Fig. 3.1 Block Diagram Representation of the proposed charger.

To address the existing challenges associated with both conventional full power processing and existing fractional power processing chargers, this chapter presents a novel current-driven fractional power processor based on resonant dual active bridge converter for UFC applications. A representative block diagram of the novel charger is

shown in Fig. 3.1. This configuration is suitable for the present application as it can step-up the dc link voltage to charge high voltage-high power batteries and support bidirectional power flow to cater to the futuristic UFC applications. Further, the architecture offers significant reduction in the size of input inductor compared to full power processing approach because of the differential current $(I_{dc} - I_{bat})$ at the input.

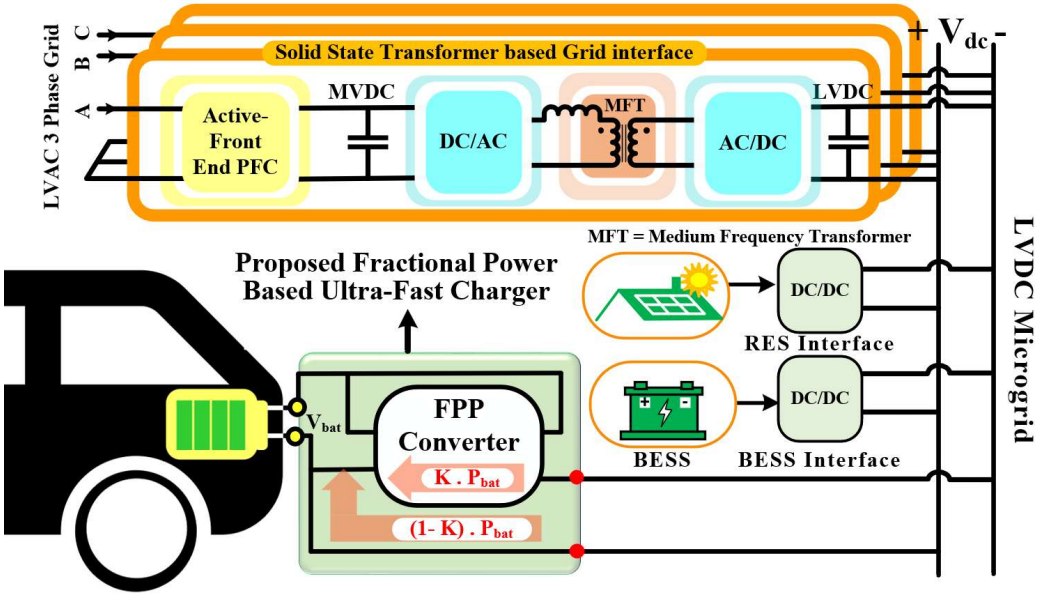


Fig. 3.2 The solid-state transformer based proposed UFCs architecture.

Here, it is worth mentioning that although the proposed converter works as step-up charger, it can feed the lower voltage batteries by regulating the LVDC-link voltage, by controlling the grid-side power electronic interface, shown in Fig. 3.2. Similarly, for catering to higher voltage batteries the control signal of the dc/dc stage of grid side interface are generated in accordance to the requirement of the load voltage.

The circuit configuration, detailed operation along with the parameter matrices are presented in this chapter. The performance of a 350 kW ultra-fast charger is analyzed and converter performance is validated and compared with the conventional full-power processing converter experimentally, through a scaled down laboratory prototype.

3.3 The proposed FPP based Current Driven Ultra-Fast Charger

3.3.1 Configuration of the Proposed Charger

In the proposed charger configuration, the battery to be charged is connected in series with the input inductor L_{in}, which is then connected across the input capacitor C_r as shown in Fig. 3.3. The charger further consists of a MOSFET-based inverter bridge connected to a high-frequency transformer, further connected to a MOSFET-based rectifier bridge. The DC source is connected across the negative terminal of converter output and negative of converter input. The input capacitor C_r forms a parallel resonant tank with the leakage inductance L_r of the transformer. Further, the positive terminal of converter output is connected to battery positive terminal. This results in a differential voltage ($V_{bat} - V_{dc}$) to appear across the converter output V_{out}. Similarly, a differential current $I_{out} - I_{bat}$ flows through converter input I_{in}.

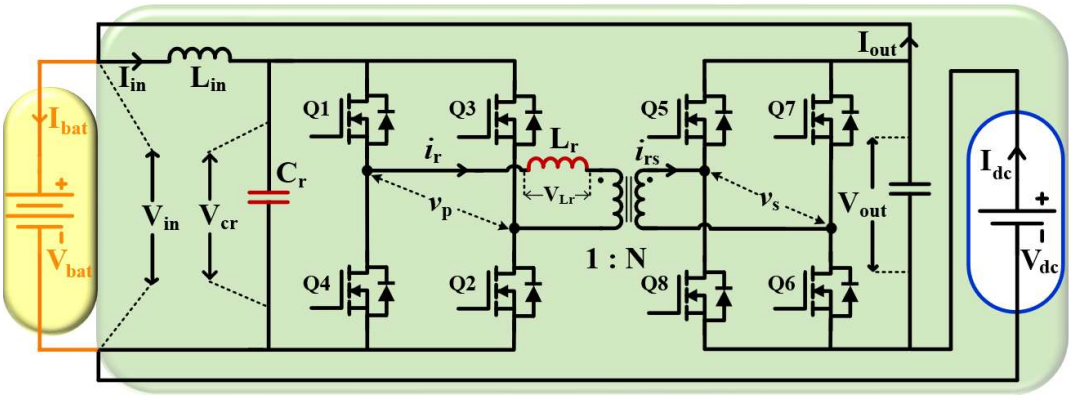


Fig. 3.3 The circuit of proposed fractional-power processing based UF charger.

3.3.2 Operation of the Proposed Charger

The operation of the proposed charger is divided into four intervals depending on the switching scheme. The key waveforms and circuit in each of the switching interval of the proposed charger are shown in Fig. 3.4 and Fig. 3.5 to Fig. 3.8, respectively. V_{GS} (Q1 Q2, Q3 Q4) and V_{GS} (Q5 Q6 Q7 Q8) represents the corresponding MOSFET gate signal. v_{cr} is the resonant capacitor voltage. v_p, v'_s represents the transformer primary and secondary voltage reflected to primary side, respectively. $v_{Lr} = v_p - v'_s$ is the resonant

inductor voltage and i_r represents the resonant inductor current. The switching strategy is such that each of the diagonal switch pair operates for 50% duty, and the rectifier bridge switching signal lags the inverter bridge switches by a phase shift ϕ. This phase shift governs the amount and direction of power flow and hence, the current fed to the battery. Notably, the converter input voltage V_{in} is equal to the battery voltage V_{bat}, which is also the average voltage across resonant capacitor v_{cr}, as shown in Fig. 3.4.

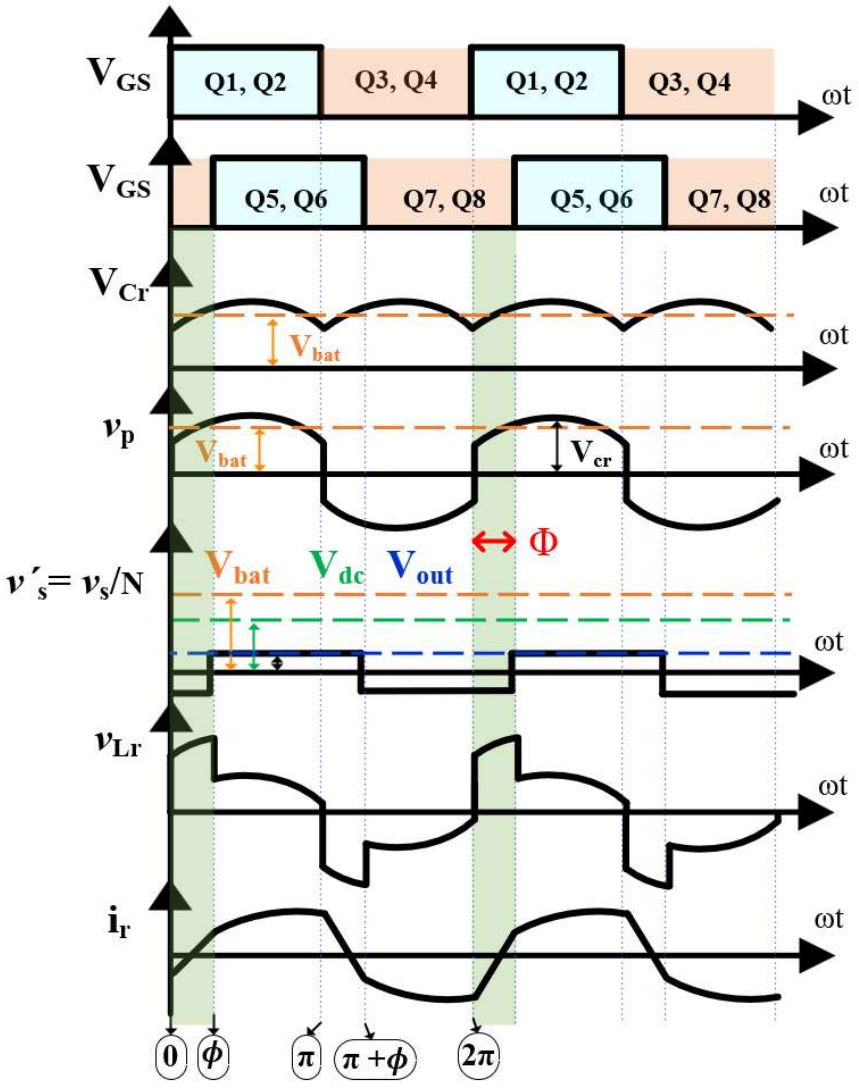
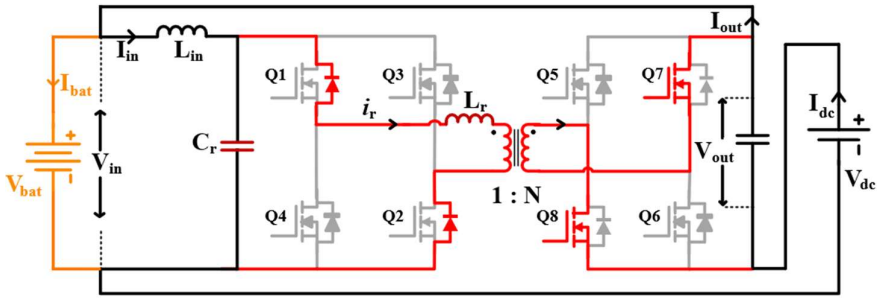


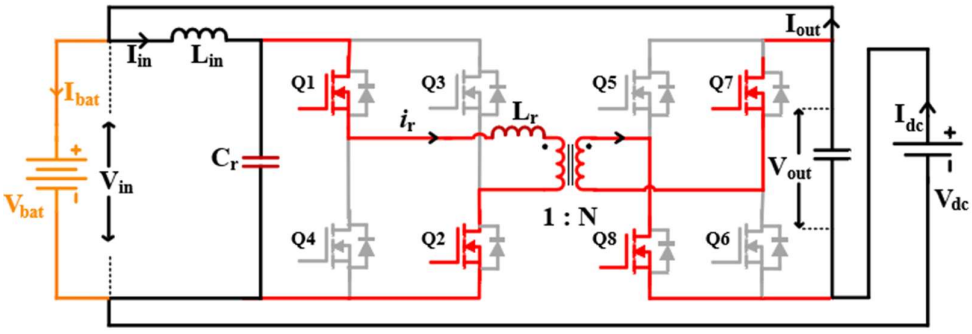
Fig. 3.4 Key waveforms of the proposed charger.

Interval I [$0 < \omega t \leq \phi$]: The operation of the converter begins at $\omega t = 0$ when Q3 Q4 are turned off and Q1 Q2 are given pulses, with Q7 Q8 already in conduction. This results in resonant inductor voltage $v_{Lr} = v_p + v'_s$ to be positive. Assuming the inductor current i_r to be lagging, the current at $\omega t = 0$ is negative, and begins to rise with a positive

slope, until it reaches zero. At the instant of switching $i_r < 0$, the current flows through body diode of Q1 Q2 as shown in Fig. 3.5 (a). When the gatepulse is applied and switch is turned on, the current starts to flow through switch Q1 Q2, Fig. 3.5 (b). It is to be noted the conduction of diode results in zero voltage across the switch, thus, ensuring zero-voltage switching (ZVS) turn-on of Q1 Q2. Similarly, the secondary bridge switches Q7 Q8 also achieve ZVS. This mode continues until Q7 Q8 is conducting, i.e., $\omega t = \phi$.

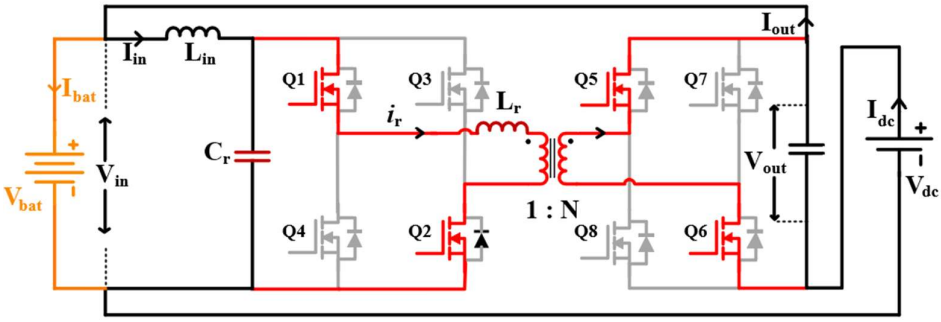


(a) During deadband



(b) During interval I

Fig. 3.5 Operation on proposed charger in interval I: $0 < \omega t \leq \phi$.

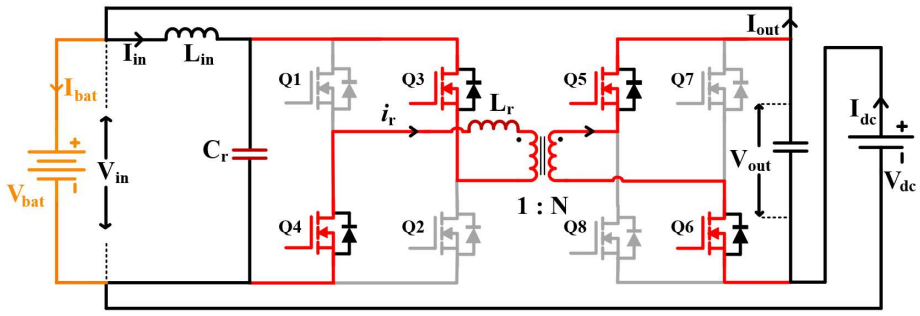


Interval II: $\phi < \omega t \leq \pi$

Fig. 3.6 Operation on proposed charger in interval II.

Interval II [$\phi < \omega t \leq \pi$]: At $\omega t = \phi$, Q7 Q8 is turned off and Q5 Q6 are triggered while Q1 Q2 remains in conduction as shown in Fig. 3.6. As $i_r > 0$, the current through Q7 Q8 shifts and now flows through the body diode of Q5 and Q6. The resonant inductor voltage $v_{Lr} = v_p - v'_s$ is still positive. Thus, the inductor current i_r continues to rise but with reduced slope. This mode continues until $\omega t = \pi$.

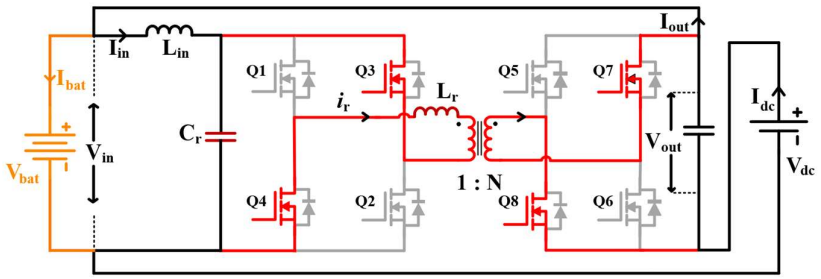
Interval III [$\pi < \omega t \leq \pi+\phi$]: At $\omega t = \pi$, Q1 Q2 is turned off and Q3 Q4 is triggered. This results in resonant inductor voltage $v_{Lr} = -v_p - v'_s$ to be negative. Thus, the inductor current slope is now negative and current decays sharply from its initial positive value. During the deadband, the current flows through the body diode of Q3 Q4 maintaining zero voltage across switch. As soon as gate pulse is applied and switch turns on i_r builds in negative direction, switches Q3 Q4 begins to conduct. Thus, Q3 Q4 turns on at ZVS, as in Fig. 3.7. The secondary current also shifts from body diode of Q5 Q6 to switch Q5 Q6, ensuring secondary bridge switch ZVS turn-on. This mode ends at $\omega t = \pi + \phi$.



Interval III: $\pi < \omega t \leq \pi+\phi$;

Fig. 3.7 Operation on proposed charger in interval III.

Interval IV [$\pi + \phi < \omega t \leq 2\pi$]: At $\omega t = \pi + \phi$, the switches Q5 and Q6 are turned off and Q7 Q8 are triggered, while Q3 Q4 continue to conduct as shown in Fig. 3.8. This results in $v_{Lr} = -v_p + v'_s$. The current i_r due to its lagging nature cannot change instantly and therefore flows through the body diode of Q5 Q6, and continues to decay with a reduced slope, until the cycle repeats and Q1 Q2 are turned on.



Interval IV: $\pi + \phi < \omega t \leq 2\pi$

Fig. 3.8 Operation on proposed charger in interval IV.

3.3.3 Current and Voltage Matrices of the Proposed Charger

The performance of the proposed charger can be compared and evaluated by establishing the mathematical model of the charger. Let V_{dc} and I_{dc} denote the charger source voltage and source current, and V_{bat} and I_{bat} denotes the load i.e., the battery voltage and current, respectively. Further, V_{in} and I_{in} represents the converter input voltage and current, and V_{out}, I_{out} represents the converter output voltage and current, respectively. The subscript 'fractional' and 'full' represent the corresponding parameter for fractional power processing converter and full power processing converter, respectively.

As discussed earlier, the proposed configuration allows only a fraction of total charger power to be processed by the converter. Thus, the configuration governs the terminal voltage and current of the converter. In the proposed charger, the battery is connected directly across converter input hence, $V_{in-fractional} = V_{bat}$ and the differential voltage appearing across the output results in $V_{out-fractional} = V_{bat} - V_{dc}$. Whereas, conventional full power converter case, the converter is directly connected across source and load resulting in $V_{in-fu} = V_{dc}$ and $V_{out-full} = V_{bat}$.

Evidently, one of the constraints imposed by the proposed charger configuration is the selection of input voltage given by (1) to ensure positive voltage at V_{out}, as

$$V_{bat,min} > V_{dc,max} \tag{3.1}$$

Where, $V_{bat,min}$ is the minimum discharge voltage of the battery and $V_{dc,max}$ is the maximum DC source voltage. Further, the converter output current of the proposed

charger is same as the dc source current, i.e., $I_{out-fractional} = I_{dc}$, and the converter input current can be calculated by applying KCL at the input node, which gives,

$$I_{in-fractional} = I_{out-fractional} - I_{bat} = I_{dc} - I_{bat} \tag{3.2}$$

Also, by invoking power balance on the converter, i.e.,

$$\eta\, V_{in}\, I_{in} = V_{out}\, I_{out} \tag{3.3}$$

Where η represents the converter efficiency. The above expression can be solved to determine the converter input and output current of fractional power processing case in terms of source and load parameters.

$$I_{in-fractional} = \frac{(V_{bat} - V_{dc})I_{bat}}{(\eta - 1)V_{bat} + V_{dc}} \tag{3.4}$$

$$I_{out-fractional} = \frac{\eta\, V_{bat} I_{bat}}{(\eta - 1)V_{bat} + V_{dc}} \tag{3.5}$$

A comparison of different system parameters for the proposed fractional power-based charger and conventional charger is given in Table 3.1.

Table 3.1 Ultra-Fast Charging System Comparison

Parameter	Full Power Processing Converter	Fractional Power Processing Converter
Converter Output Voltage V_{out}	V_{bat}	$V_{bat} - V_{dc}$
Converter Input Voltage V_{in}	V_{dc}	V_{bat}
Converter Output Current I_{out}	I_{bat}	$\frac{\eta\, V_{bat} I_{bat}}{(\eta - 1)V_{bat} + V_{dc}}$
Converter Input Current I_{in}	$\frac{V_{bat} I_{bat}}{\eta V_{dc}}$	$\frac{(V_{bat} - V_{dc})I_{bat}}{(\eta - 1)V_{bat} + V_{dc}}$
Fractionality Ratio $K = P_{in}/P_{bat}$	1	$\frac{(V_{bat} - V_{dc})}{(\eta - 1)V_{bat} + V_{dc}}$

System Efficiency η_{sys}	η	$\frac{(\eta-1)V_{bat}+V_{dc}}{\eta\, V_{dc}}$

3.4 Performance Analysis of Proposed Ultra-Fast Charger

The criticality of performance and loss reduction for any charger increases with the increase in its charging power level. When handling large power of order of 350 kW, as in the case of an ultra-fast charger, even a percent of increase in efficiency would mean significant saving of up to 3.5 kW. Hence, to analyze the system level benefits of the proposed fractional power-based UFC, this section explores its performance for the rated application in terms of converter characteristics, parameter variation, component selection, and control behavior. Further, the design and component selection of the proposed converter is discussed.

3.4.1 Effect of Fractionality Ratio, K

The fractionality ratio, K is defined as the ratio of fraction of power processed by the converter to the power supplied to the battery. The fractionality ratio, for the proposed charger may be calculated as

$$K_{i-Fractional} = \frac{(V_{bat} - V_{dc})}{(\eta - 1)V_{bat} + V_{dc}} \tag{3.6}$$

Evidently, processing only a part of power through the converter imparts the main advantage of the proposed charger, i.e., lower the power processed through converter, lower the losses, higher is the overall charging efficiency. Thus, fractionality ratio is the key parameter that defines the system behavior and is critical to system design. K can be controlled by selecting the source voltage V_{dc}. Fig. 3.9 shows the performance of FPP configured charger for the entire range of K to give designer with idea of the criticality of selection of source voltage, voltage conversion gain and fractionality ratio and their effect on the overall charging efficiency, for an 800 V battery charging system delivering 350 kW of battery power. Further, the current stress over switches of the primary bridge decreases, allowing for selection of low current rated switches. Fig. 3.10 (a) shows the effect on converter parameters with the selection of source voltage. As V_{dc} increases the

differential voltage decreases reducing the converter output voltage, allowing for selection of low-voltage rating switches.

$$\eta_{sys} = \frac{(V_{bat} - V_{dc})}{K\, V_{dc}\, \eta} \tag{3.7}$$

It can be inferred that as K decreases, i.e., amount of power processed through converter decreases, the current flowing through converter decreases and the charging efficiency increases. Fig. 3.10 (b) shows the relationship between K, V_{bat}, V_{dc} and the converter efficiency η, with each plane representing a converter efficiency value.

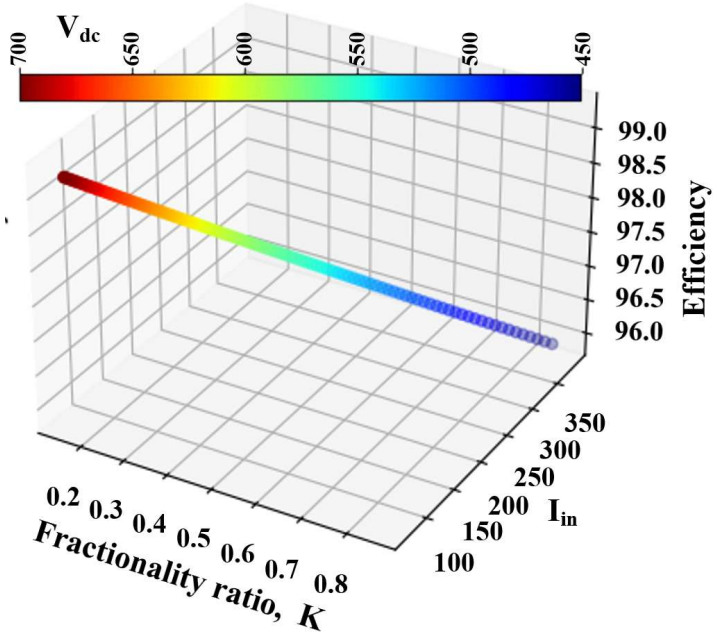
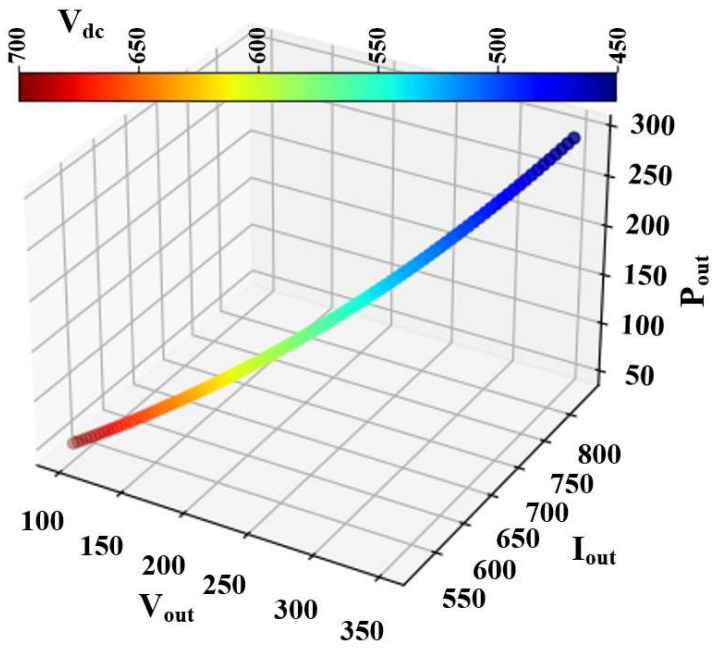


Fig. 3.9 Efficiency curve plotted against fractionality ratio K.



(a)

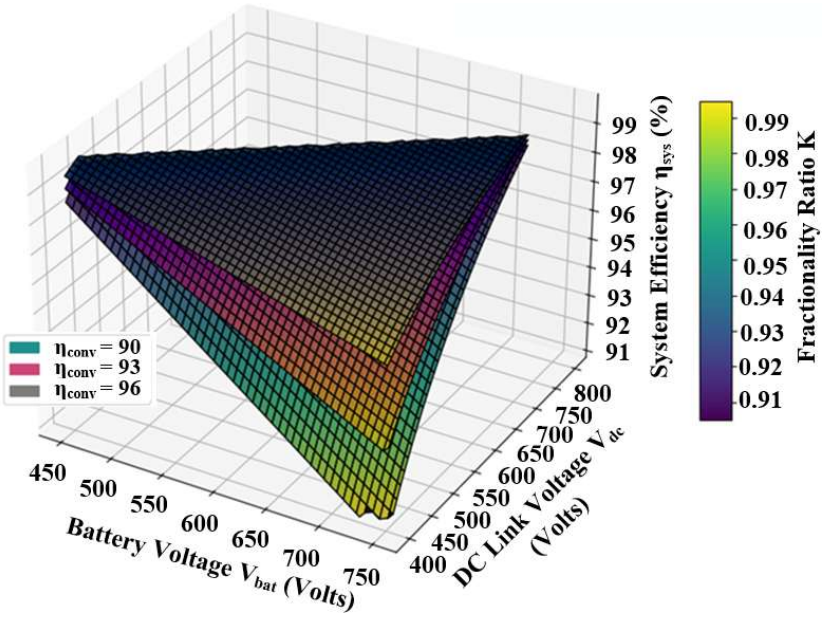


Fig. 3.10 (a) Converter parameters plotted against Vdc. (b) Variation of system efficiency with battery voltage, dc source voltage, and converter efficiency.

3.4.2 Effect of Phase Shift Control

UFC targets high current charging that predominantly demands constant current (CC) operation. The proposed UFC system, due to it parallel resonance feature can inherently behaves as a current source at the output, when operated at the resonant frequency. This

capability of proposed converter assists in minimizing the control requirement for CC ultra-fast charging. The load current of the system varies as a sine of phase shift, as defined by the relationship

$$I_{out} = \frac{V_{bat}}{N\, Z_o} \sin \phi \tag{3.8}$$

$$I_{bat} = \frac{[(\eta - 1)\, V_{bat} - V_{dc}]}{N\, \eta\, Z_o} \sin \phi \tag{3.9}$$

Where 1/N is the transformer turn ratio, Z_o is the characteristic impedance of the parallel resonant tank formed by L_r and C_r and η represents the converter efficiency.

Fig. 3.11 shows the variation of battery current with the converter phase-shift ϕ, keeping other parameters constant. It shows that battery current can be directly controlled by varying the phase-shift. Further, although the ratio of power handled by converter, K, is independent of ϕ, power handled by converter, P_{conv}, is governed by phase shift, as I_{out} is controlled by ϕ. Therefore, as the battery voltage rises, the K value would go up that would inflict additional power on the converter, but at each step the current can be reduced by reducing the phase shift, thus resulting in ultimately lower power handled by the converter, further improving the performance of the converter.

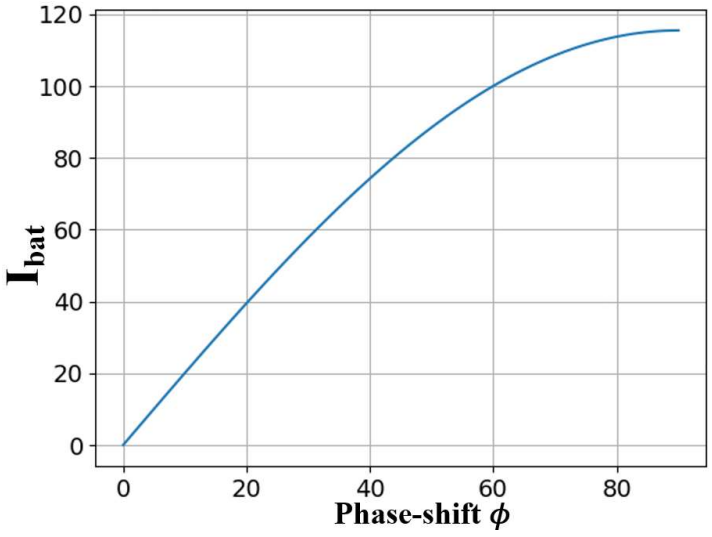


Fig. 3.11 Variation of I_{bat} with phase demonstrating CC behavior.

3.4.3 Effect of Fractionality on Component Selection and Loss Reduction

MOSFETs are subjected to two types of losses, the conduction loss and the switching loss, as shown in Fig. 3.12. The conduction losses are governed by both voltage and current rating of the switch. MOSFETs with high V_{ds} rating tends to have larger on-state resistance, R_{ds-on}, which results in higher conduction losses during on-state [13]. The effect further becomes pre-dominant in case of high current application such as UFC.

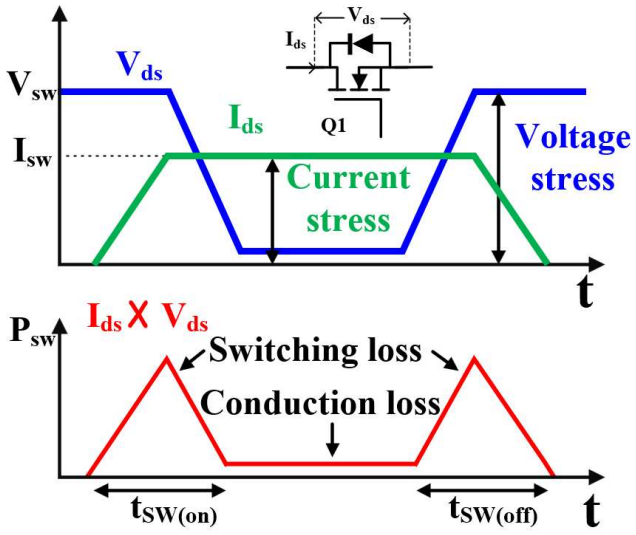


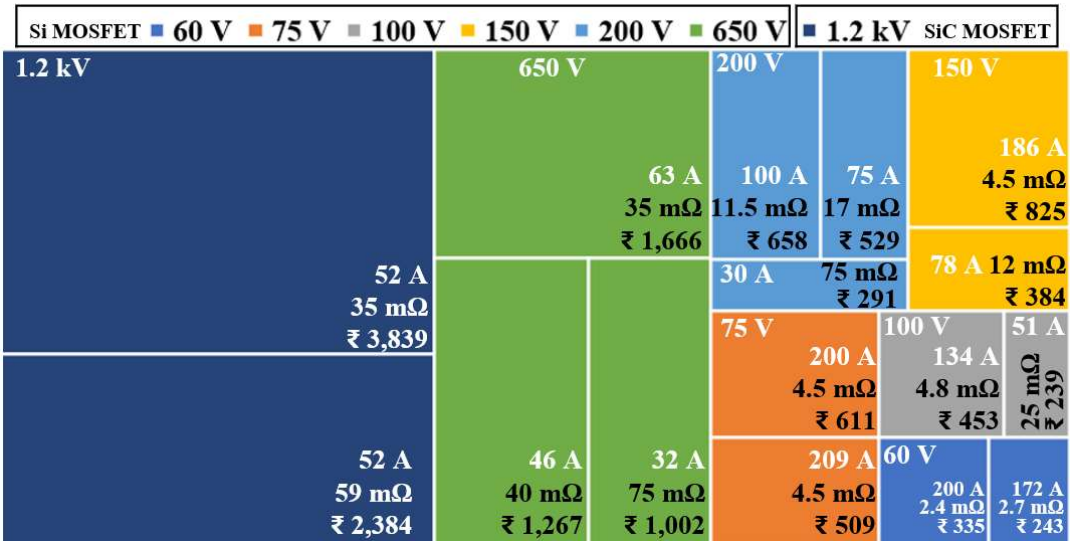
Fig. 3.12 Effect of current and voltage stress on losses.

However, in the proposed UFC charger, the high current side, i.e., the secondary bridge switches only have a differential voltage appearing across its switch, resulting in significantly lower voltage stress. This allows for selection of lower voltage and thus, low R_{ds-on} value switches, resulting in decrease in conduction losses, cost and improved efficiency. Additionally, only the difference current appears across primary bridge switches, this allows for selection of low current rated switches as well as lower conduction losses. Further, all the switches undergo soft-switching operation which eliminates the turn-on losses completely and minimizes the turn off losses due to reduced voltage and current level, thus ensuring overall reduction in loss and improved efficiency.

3.4.4 Effect of Fractionality on Charger Cost

As discussed, the proposed charger allows for selection of low rated components, presenting significant cost-benefits in component selection. Fig. 3.13 shows a cost

comparison of MOSFET from Infineon Technologies listed on Mouser Electronics; based on their voltage, current ratings and their R_{ds-} value to present an estimate of the cost cutting due to proposed work.



*Data based on Mouser Electronics website as on May 2024

Fig. 3.13 Cost comparison of MOSFET in terms of voltage, current, and R_{ds-on} rating.

The area covered on plot gives visual comparison of the cost of each MOSFET. It may be observed that there is a multi-fold increase in the switch cost as the voltage rating increases. Further, switches with same voltage and current rating but less R_{ds-on} has higher cost, as it has direct impact on the conduction losses and hence, the efficiency of the charger. It may also be concluded that the differential voltage obtained on the secondary side will bring considerable cumulative cost reduction even with high current ratings.

3.4.5 Simultaneous Charging and Vehicle Isolation Monitoring

The proposed ultra-fast charger can also be utilized for simultaneous charging of multiple EVs by interfacing multiple units of proposed charger directly to the dc link at LVDC bus, similar to the conventional approach presented in [86]. In this approach, the grid side isolation prevents the fault current and ground loops from propagating between grid and the battery. Further, the proposed charger meets out the safety requirement laid out

by the vehicle isolation monitoring device as in [130] which would generate warning/alarm in case of fault or allow charging as per normal operating condition.

3.5 Experimental Validation of Proposed Charger

The proposed concept of current driven fractional power processor for ultra-fast charging is verified at a scaled down level through a laboratory developed 1.3 kW power processor, shown in Fig. 3.14. The PWM signals are generated using digital signal processor (TMS320F28335). The design and operating parameters of the developed charger are given in Table 3.2. ITECH IT6006C battery emulator is used to validate the battery charging using proposed charger at 120 V to match the commercially available battery standards.

Table 3.2 Design Parameters and Operating Conditions of the Proposed Charger

Symbol	Quantity	Value	Symbol	Quantity	Value
L_{in}	Input inductor	2.5 mH	C_r	Resonant capacitor	202 nF
C_{out}	Output capacitor	94 µF	f_r	Resonant frequency	89 kHz
1/N	Transformer turn ratio	16:10	f_s	Switching frequency	89 kHz
L_r	Leakage inductance	16.1 µH	$Z_o = \sqrt{L_r/C_r}$	Characteristics impedance	8.89 Ω
V_{bat}	Battery voltage	120 V	V_{dc}	Source voltage	65-95 V
	P_{bat}		Battery power delivered		1.3 kW

3.5.1 Steady State Behavior of the Proposed Charger

The steady state waveforms of the proposed charger are shown in Fig. 3.15 to Fig. 3.17. v_p and v_s represents the primary and secondary transformer voltage, respectively.

V_{bat}, I_{bat} represents the battery voltage and current, respectively. i_{rs} is the transformer secondary current.

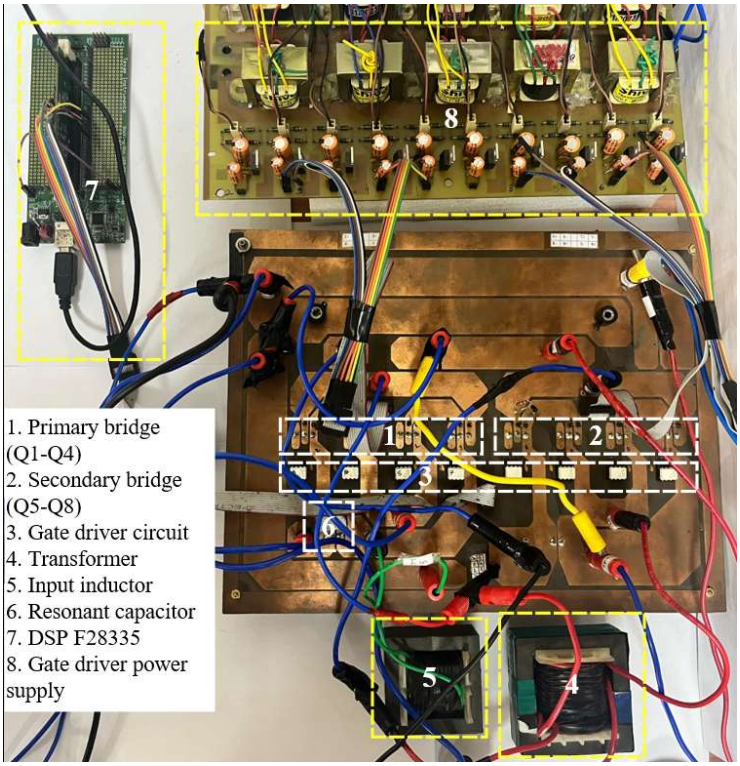


Fig. 3.14 Photograph of the laboratory developed 1.3 kW prototype of proposed fractional power processing-based charger.

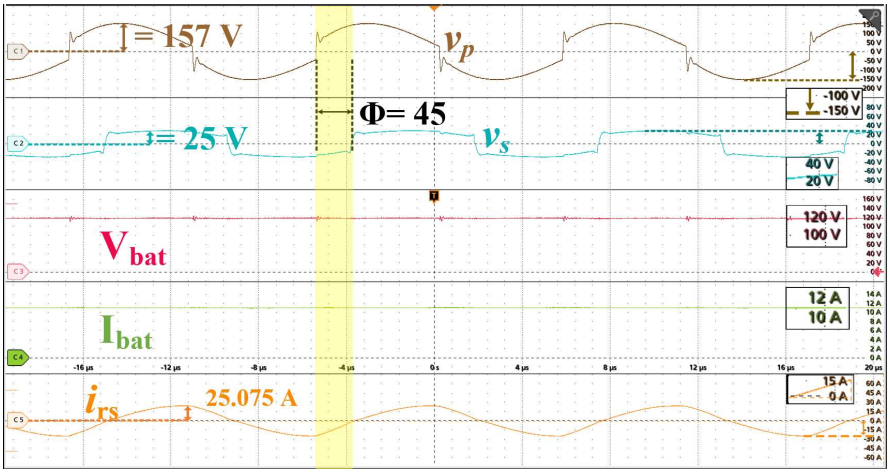


Fig. 3.15 Experimental results of proposed charger for battery charging of $V_{bat} = 120\,V$ with $P_{bat} = 1.32\,kW$, $V_{dc} = 95\,V$.

Fig. 3.15 represents the charger waveforms at $P_{bat} = 1.32\,kW$, for $v_{bat} = 120\,V$. Here, primary voltage v_p lags secondary voltage v_s by phase shift of 45°. It may be observed

that the RMS value of v_p and hence the input voltage is equal to the battery voltage i.e., 120 V, as also shown in Fig. 3.4. The peak value of v_p represents the voltage stress which is 157 V in this case. Further, the secondary voltage stress (v_{s-pe}) is only 25 V, which is due to the difference voltage $V_{bat} - V_{dc} = (120 - 95)$, reflecting on the benefit of the proposed charger. The RMS secondary current is $i_{rs} = 17.11\,A$ and secondary current stress is 25.07 A. It may also be observed that the inductor current at the beginning of yellow strip, i.e., at $\omega t = 0$ is negative which shows the primary bridge switches are turned on with ZVS and at $\omega t = 45°$ is positive representing ZVS turn on of secondary switches.

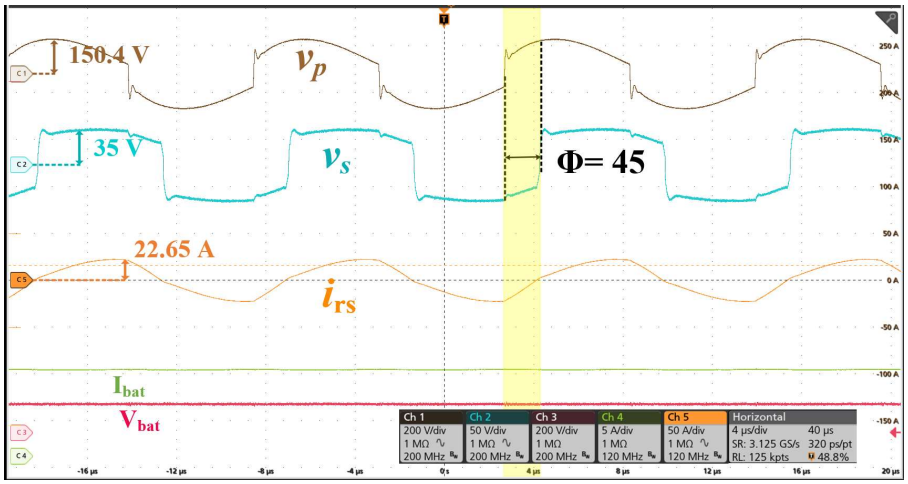


Fig. 3.16 Experimental results of proposed charger for battery charging of $V_{bat} = 120\,V$ *with* $P_{bat} = 1.105\,kW$, $V_{dc} = 85\,V$.

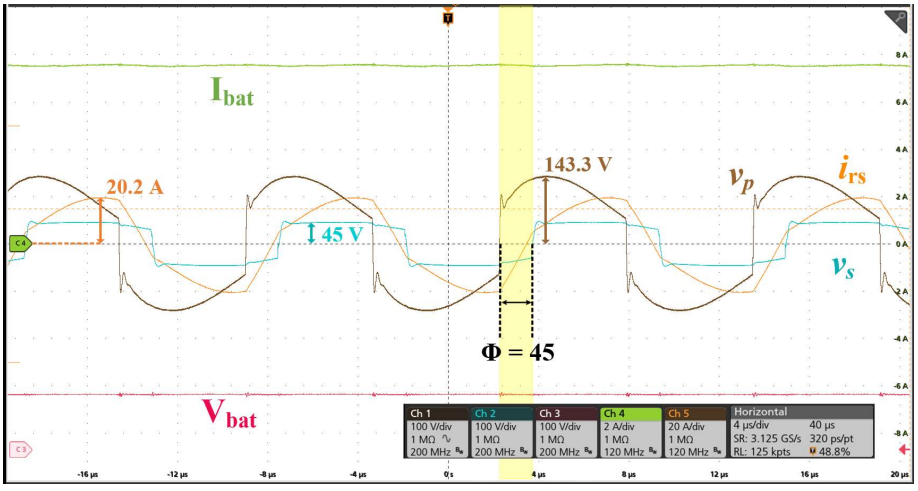
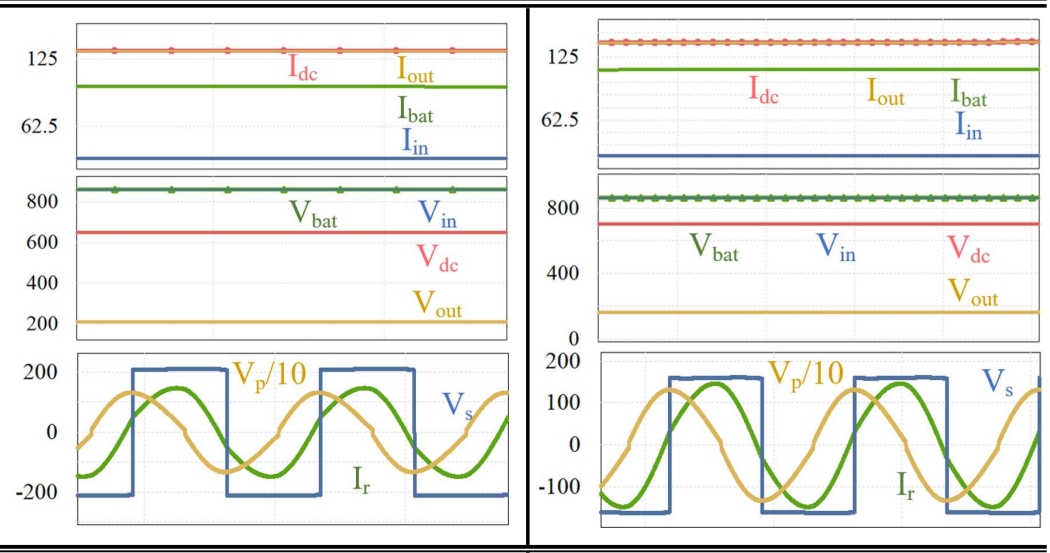


Fig. 3.17 Experimental results of proposed charger for battery charging of $V_{bat} = 120\,V$ *with* $P_{bat} = 900\,W$, $V_{dc} = 75\,V$.

Table 3.3 Simulation Study for 800 V Battery Charging System



	K = 0.23				K = 0.33			
	V_{dc}	V_{bat}	V_{in}	V_{out}	V_{dc}	V_{bat}	V_{in}	V_{out}
Voltage	700	860	860	160	650 V	860 V	860	210 V
	I_{dc}	I_{bat}	I_{in}	I_{out}	I_{dc}	I_{bat}	I_{in}	I_{out}
Current	140.1	113.1	27	140	132 A	99.16 A	32.89 A	132 A
Power	P_{dc}	P_{bat}	P_{in}	P_{out}	P_{dc}	P_{bat}	P_{in}	P_{out}
(kW)	98	97.18	23.22	22.40	85.8	85.27	28.28	27.72
	η_{sys}		η		η_{sys}		η	
Efficiency	99.16 %		96.46 %		99.3 %		98.01 %	

Fig. 3.16 and Fig. 3.17 shows the steady state results for $P_{bat} = 1.105\ kW$ and $900\ W$ with $V_{dc} = 85\ V$ and $75\ V$, respectively. This is also reflected on the secondary voltage $v_s = 120 - V_{dc} = 35\ V$ and $45\ V$ for each case. Further, the peak of v_p (primary voltage stress) decreases with decrease in delivered power. Additionally, it may be observed that the primary and secondary bridge switches achieve ZVS turn-on in both the cases.

The above results show that despite the battery voltage is 120 V and source voltage being 75 V, 85 V or 95 V, the effective voltage appearing at the converter terminal is 45 V, 35 V and 25 V, respectively. This also means a reduction of 40%, 58.8 % and 73.68% in voltage stress at the converter output. From this discussion it can be inferred that the power that flows through the converter is reduced i.e., only a fraction, compared to the power supplied to the battery. Further, the proposed concept can similarly be applied to UFC level (800V, 350 kW) to achieve significant reduction of converter processed

power. Also, the simulation results of this analysis and comparison are presented in Table 3.3. In addition, this analysis is critical to the system design and reflects on the suitability of proposed charger for wide range of input as available in modern DC micro-grid integrated UFC facilities.

3.5.2 Phase Control Behavior of the Proposed Charger

Ultra-fast charging in its literal meaning refers to charging the battery quickly at large current. Generally, this would mean charging the battery from an initial discharge state to 80-85 % of its state-of-charge (SOC). It has been explored and well established that the constant current charging and multi-stage constant current charging is the most optimal strategy for applications requiring quick charging [131]. Therefore, it is a notable advantage that the proposed charger can inherently acts as a constant current source when operated at a switching frequency equals to the resonant frequency of the parallel resonant tank, wherein the resonant tank is formed by the input capacitor C_r and the transformer's leakage inductance L_r. Consequently, the proposed charger can supply constant current which can be controlled by varying the phase shift ϕ, between the primary and secondary bridge. In this sub-section, the same is experimentally verified by charging the battery of $V_{bat} = 120\ V$ with $V_{dc} = 65\ V$. Fig. 3.18 shows the results for $\phi = 30°$, where $I_{bat} = 5.1\ A$. Transformer primary rms voltage is 120 V and primary switch stress is 133.4 V. The secondary voltage is 55 V. Secondary RMS current is 11.23 A and current stress is 15 A.

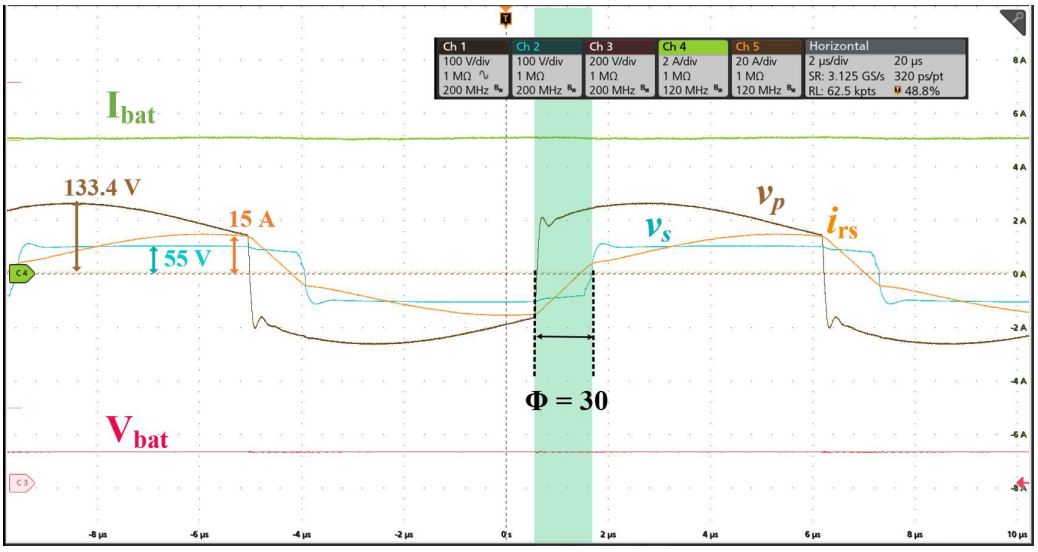


Fig. 3.18 Steady state results showing the effect of variation of phase shift and stable constant current operation for $V_{bat} = 120\ V, V_{dc} = 65\ V\ \phi = 30°$.

Both primary and secondary bridge switches attain ZVS turn-on for all the switches due to body diode conduction at turn-on instants, as also discussed in previous section.

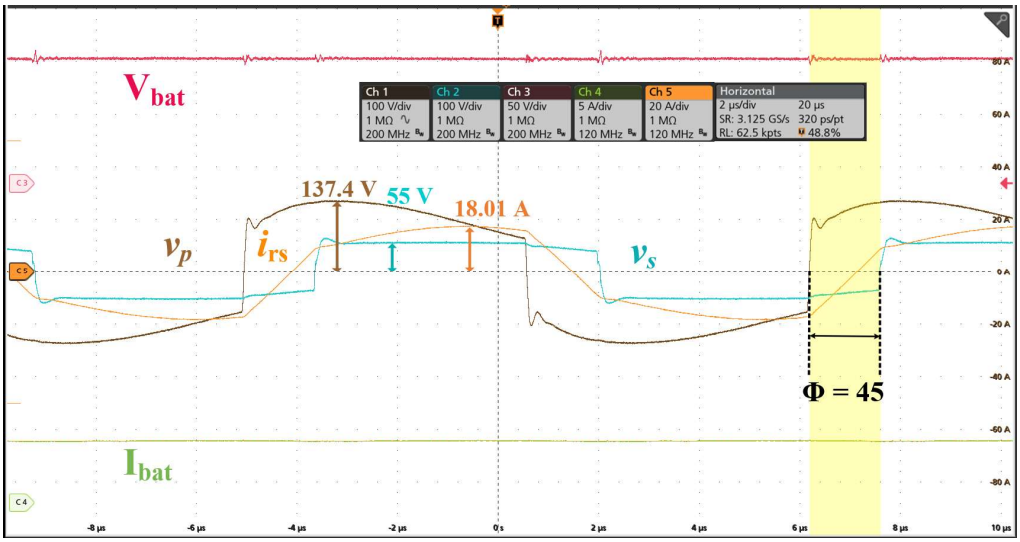


Fig. 3.19 Steady state results showing the effect of variation of phase shift and stable constant current operation for $V_{bat} = 120\ V, V_{dc} = 65\ V\ \phi = 45°$.

Fig. 3.19 further shows the effect of variation in phase shift with $\phi = 45°$, while keeping other parameters constant. It may be observed that v_s is 55 V, whereas, I_{bat} is 5.85 A. The same is reflected in i_{rs} with rms of 14.16 A. The secondary current stress obtained is 18.01 A for 45°. The rms voltage remains 120 V whereas the primary switch stress obtained is 137.4 V due to increase in the battery current and the output current.

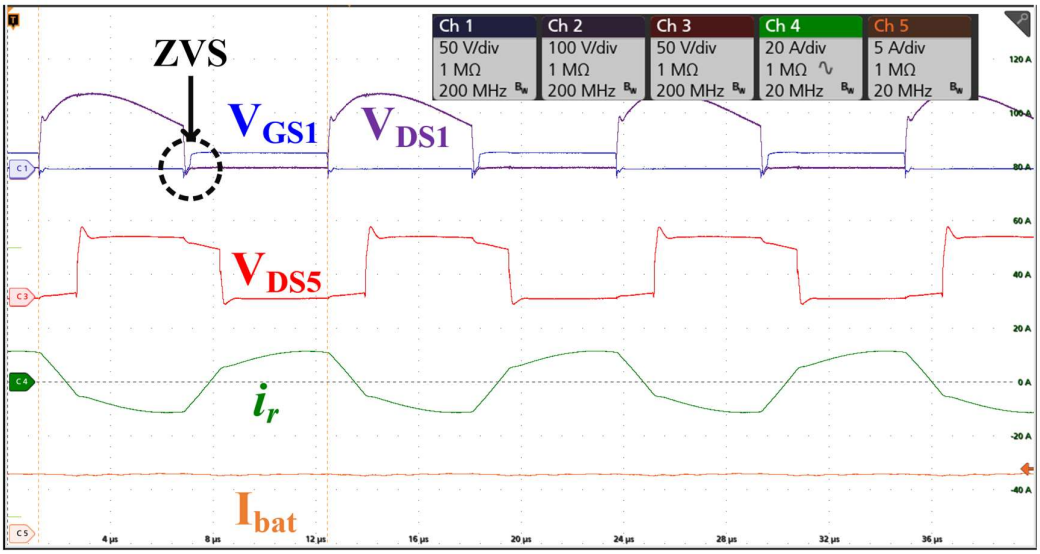


Fig. 3.20 Switching state of primary and secondary bridge switches during steady state operation at $\phi = 45°$.

Fig. 3.20 represents the switch waveforms of primary and secondary switches with respect to the gating signal at $\phi = 45°$. $V_{gs1}, V_{ds1}, V_{ds5}$ represents the gate pulse of Q1, switch stress of Q1 and switch stress of Q5 respectively. It may be observed that when Q1 is turning on, V_{ds1} has already reduced to zero, thus confirming ZVS turn-on of the switch.

3.5.3 Dynamic Response of the Converter

To observe the behavior of the converter in the presence of dynamics when operating in open loop, the converter is operated with sudden change in phase shift and the response were observed. Fig. 3.21 represents the dynamic response of the converter. Initially the converter is operating $\phi = 20°$, the battery current is 4 A and after the application of dynamics the battery current settles to 5.85 A, for $\phi = 45°$. The settling time is 1.9 ms. Further, the converter parameters have settled immediately after 9 switching cycles.

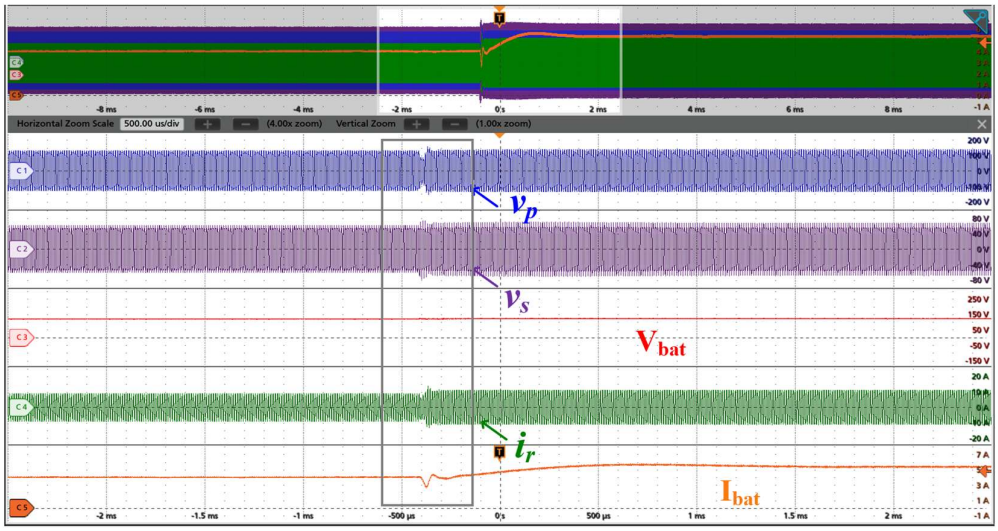


Fig. 3.21 Transient state result displaying the stable operation of converter in open loop dynamics for $\phi = 20°$ to $45°$

From the above results it may be concluded that by controlling the single control variable ϕ, the proposed charger can perform constant current charging for wide variation of load. This also implies that the proposed charger is robust with simple control strategy and reduced controller dependency.

3.5.4 Comparison with Full-Power Processing Charger

This section aims at establishing a performance comparison between the proposed FPP and the conventional full power processing charging system while delivering the same load conditions, utilizing the same converter components by configuring it as the proposed fractional power processor and the conventional full power processor. The findings are graphically represented in Fig. 3.22 to Fig. 3.25.

Fig. 3.22 represents the required dc voltage at input to deliver same battery power for $V_{bat} = 120\ V$, while keeping phase shift constant at $\phi = 45°$ in both cases. Further, for delivering 700 W in the proposed converter the required source voltage is $V_{dc-FP} = 65\ V$ while for conventional case $V_{dc-Fu} = 88\ V$. Similarly, in another scenario the charging is done at 1.3 kW, with $V_{dc-} = 95\ V$ and $V_{dc-Full} = 136\ V$, respectively.

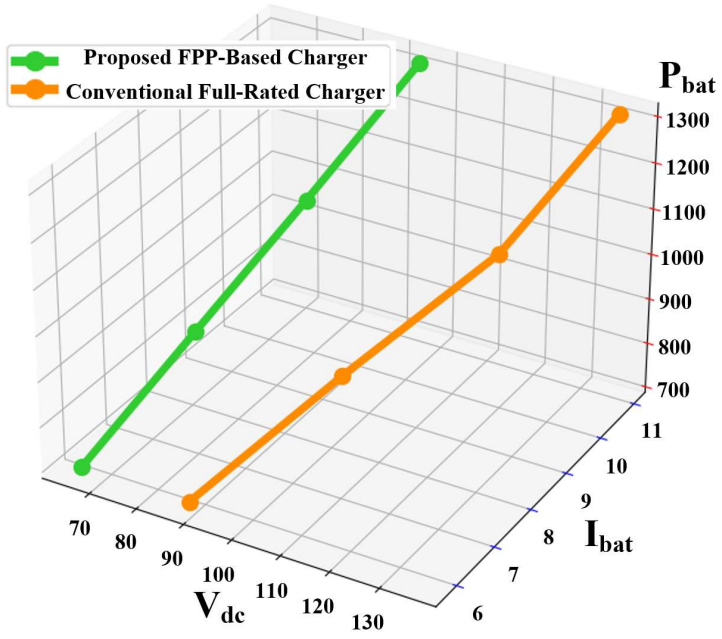


Fig. 3.22 Performance comparison based on experimental results for 120 V battery with battery power, battery current plotted against source voltage.

These two considered cases of proposed charger represent fractionality ratio K_{FPP} of 0.93 and 0.28, each, whereas for conventional case it remains $K_{Full} = 1$. Here, it may be inferred that there is a reduction in required source voltage to deliver same battery power in case of FPP compared to conventional analyzed for two extreme cases of K. Alternatively, the converter designed as full power processor can be configured as proposed charger to deliver higher power.

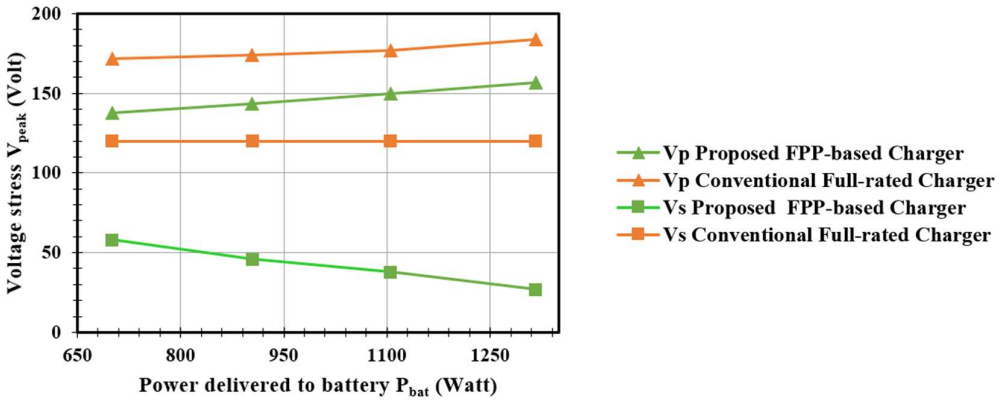


Fig. 3.23 Voltage stress of primary and secondary bridge plotted against delivered power.

Fig. 3.23 shows the voltage stress for different value of P_{bat} (or K_{FPP}) for proposed and conventional converter. Considering operation at $700\ W$, the conventional charger has $25.5\ \%$ higher voltage stress for primary switch and $106.8\ \%$ higher voltage stress for secondary switch. Similarly, when considering $K_{FPP} = 0.28$ the primary switches undergo $17.19\ \%$ higher voltage stress, whereas the secondary has $344.4\ \%$ of higher voltage stress, for conventional compared to the proposed charger. This analysis shows that as fractionality ratio increases there is a marginal increase in primary switch voltage stress but exceptional reduction in secondary bridge stress. It also reflects on the flexibility of selection of switch of much lower voltage rating for the proposed FPP charger compared to the conventional charger which ultimately results in selection of cheaper components that have low $R_{ds\text{-}on}$ and associated advantages as previously discussed in section 3.4.

Further, Fig. 3.24 represents the current stress on primary and secondary switches for the proposed and conventional charger, respectively. It may be observed that there is reduction in current stress of both primary and secondary bridge switches for the case of proposed charger compared to the that of conventional full power processing charger. It may further be observed that for a scenario of $P_{bat} = 700\ W, K_{FPP} = 0.93$ the conventional converter has 119.1% higher current stress over primary bridge switches and $141.6\ \%$ higher current stress on secondary bridge switches. Whereas, for $K_{FPP} = 0.28$, the conventional converter has 5.8% higher stress on primary and $16.2\ \%$ higher stress on secondary switches. This analysis highlights the reduction in current stress and hence the increase in required switch current rating for conventional charger compared

to proposed charger. Moreover, with increase in the fractionality ratio K, the impact of the proposed approach further increases.

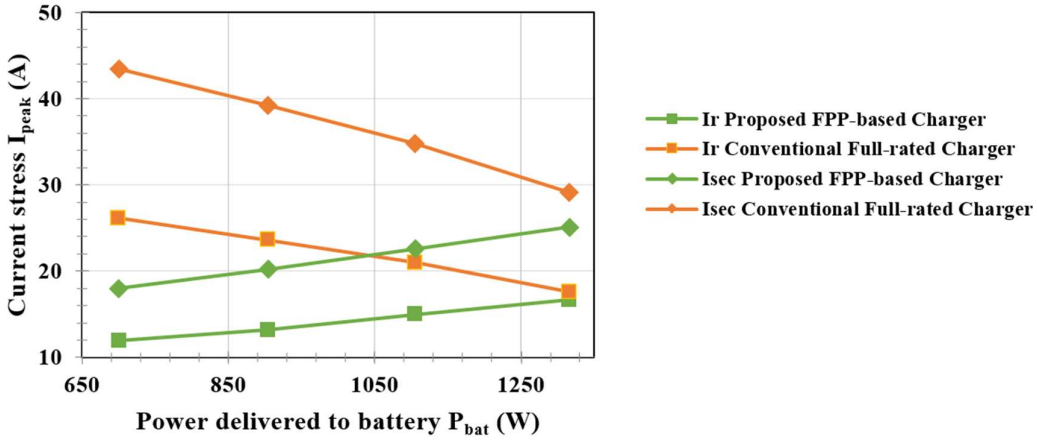


Fig. 3.24 Current stress of primary and secondary bridge vs delivered power.

In addition to the stress, the rms current sees an increase of 69.5 % for conventional charger while supplying 700 W, $K_{FPP} = 0.93$ and, it sees an increase of 22.86 % in conventional charger compared to proposed charger when delivering 1.3 kW at $K_{FPP} = 0.28$. It is known that the conduction losses for a converter varies as a square of the rms current through it. Thus, the conventional converter suffers from much higher conduction losses compared to the proposed converter at the same charging power, resulting in higher efficiency of proposed charger. Fig. 3.25 represents the efficiency analysis of proposed FPP based charger in comparison with conventional charger, along with the power processed by converter in each case.

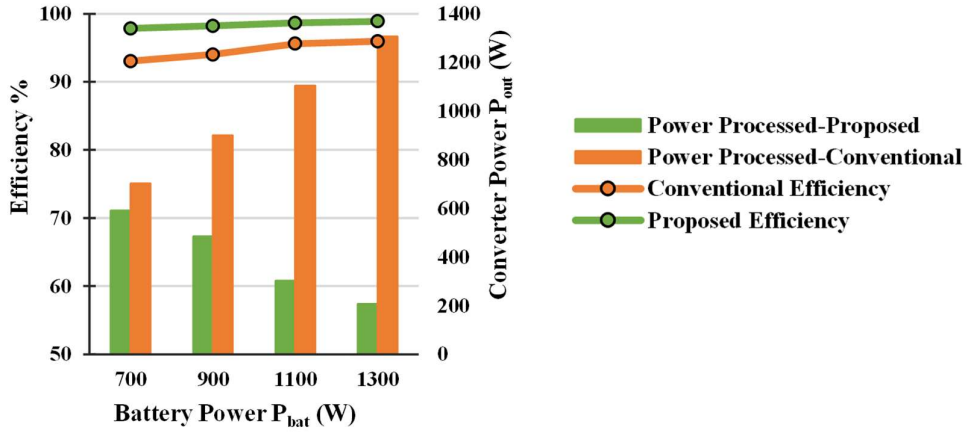


Fig. 3.25 Efficiency analysis of charging system.

The significant increment in efficiency for the proposed FPP based charger can be clearly concluded from the graph. Further, as the fraction of power processed by the converter (K_{FPP}) for proposed case reduces, the efficiency increases. Peak efficiency of 98.33 % is achieved for proposed charger at 1.32 kW, showing a significant increase from 95.96 % compared to conventional charger at 1.3 kW. The above analysis is critical to application in ultra-fast charger design where efficiency is of prime importance and selection of lower rated components can give significant cost cutting. As well as, the loss reduction can effectively reduce the heat sink size and thus, facilitate economic and compact charger design that can perform efficient high power charging operation.

3.5.5 Comparison with Other FPP Literature

Considering the recent literature on FPP as the state-of-the art in applications relating to EV battery charging, a comparative analysis is presented in Table 3.4. The review compares the proposed charger with recent literature in different aspects such as quantitatively in terms of FPP architecture, the dc/dc converter topology, the system key characteristics governing the overall performance, and the potential application, then quantitatively based on its experimental validation and efficiency.

From Table 3.4, it may be concluded that there is a dearth of step-up fractional power processors for EV charging application. Additionally, the proposed charger is superior from other counterparts in terms of bi-directional power flow, soft switching of primary and secondary switches and light load efficiency. Further, it has simple control to implement current regulation throughout the charging, and does not require transfer function calculation and dedicated controller. Another notable benefit of the proposed charger is the operation at resonant frequency that helps in minimizing the magnetic size, thereby, further improving the power density of the charger.

3.6 Conclusion

This chapter presented a novel current-driven fractional power processing based resonant DAB converter. The dc/dc converter of the proposed charger handles only a fraction of the total power delivered to the battery. Therefore, the converter power rating required to achieve ultra-fast charging is reduced significantly, making the charger suitable for ultra-fast charging application.

Table 3.4 Comparison of Existing Literature on FPP Applied to EV Charging

Reference	[79]	[80]	[81]	[82]	[83]	[86]	**Proposed**
Architecture	Step-Down	Step-Down	Step-Down	Step-Down	Step-Down	Step-Up	Step-Up
DC/DC Converter	Interleaved H-bridge	Flyback	Phase-Shifted Full-Bridge	DAB Series Resonant	Full Bridge Boost	Phase-Shifted Full-Bridge	Current-Driven Resonant DAB
System Properties							
Soft-switching	No	–	No	Only secondary ZVS	Only Secondary: Near-ZVS	–	Prim. & Sec. both ZVS
Bi-directionality	No	Yes	No	Yes	Yes	No	Yes
Ligh-load Efficiency	–	Decays	Poor	–	Decays	–	Higher
Control Implementation	Cascaded PI	–	Cascaded PI	–	PI	PI	Direct Phase shift control
Experimental Validation							
Range of K	0.36	0.23 - 0.4	0.1332	0.18 – 0.4	0.4 – 0.9	0.27	0.28 – 0.98
Power rating	×	5.5 kW	7 kW	×	4 kW	3.2 kW	1.3 kW
Frequency	20 kHz	50 kHz	100 kHz	10 kHz	100 kHz	50 kHz	100 kHz
Converter Efficiency	95.10 % *	–	96.3% (avg.) 97.3% (peak)	×	97%	96.3% (0.5 Ipu) 97.87 % (1 Ipu)	95.86 %
System Efficiency	98.30 % *	99.11%	99.11%	×	98 %	97.5% (0.5 Ipu) 98.48 % (1 Ipu)	98.33 %

× = Not validated experimentally; – = Data not available; * = Simulation results

The proposed charger achieves ZVS for entire range of battery voltage and fractionality ratio, ensuring high efficiency battery charging through-out the range. It also enables significant reduction in the size of input inductor compared to full power processing approach because of the differential current $(I_{dc} - I_{bat})$ at input. Further, due to its current driven nature and resonance operation, the proposed charger offers simple yet robust battery current regulation, while eliminating the need of any complex controller.

The operation of the proposed charger is discussed in detail and its performance for ultra-fast charging application is analyzed in this chapter.

The behavior of the charger and its control performance is experimentally verified through a 1.32 kW laboratory developed charger prototype. The results validated that the proposed charger has reduced current and voltage stress and achieve soft-switching for the entire range. This provides an opportunity to select low-rated, less costly and more efficient components. Further, dynamic performance verifies that the proposed charger can efficiently charge in CC mode for wide range as desired in UFC application by varying a single control variable, thus, minimizing the control requirement. Additionally, the proposed charger retains the benefits of reduced components cost, heat sink requirement, and ease of component selection, as in other FPP solutions. Further, by utilizing the already available isolation in grid-side power electronics interface, the proposed ultra-fast charger achieves isolation comprehensively between the MVAC grid and the EV under charging, as recommended in IEEE 1547 standard for UFC charger. The proposed FPP charger achieves a significant improvement in the overall charging efficiency therefore, it is suitably be applied to UFC application.

Though the proposed charger addresses the problems in establishing off-board ultra-fast charging solutions, the fear of being stranded with a discharged EV can be a significant cause of deter in consumer interest in EV adoption. The evolving EV ecosystem further demands a comprehensive solution that can interface diverse charging facilities such as slow AC charging, or fast DC charging. Overall, there is a need for reducing the size and cost of on-board charger to serve as a fast charger, and also enabling V2aux and V2V charging. To address this gap a novel interoperable multi-utility fractional power processor is proposed in the next chapter.