Chapter 3

A Quadratic Boost Converter with Ripple-Free Input Current for PV Application

3.1 Introduction

The Kyoto protocol is being implemented across the globe by states and companies to reduce greenhouse gas emissions [6]. The unpredicted and rapid change in the price of fossil fuels has shifted the attention toward renewable energy sources. The recent decade has seen significant investment in the implementation and research of solar, wind, and fuel cell energy sources. The solar and off-shore wind power generations are the cheapest energy sources known today [14]. The problems associated with photovoltaic (PV) generation are as follows:

- The PV generation systems have low output voltage.
- Increasing the output voltage by using long strings leads to potential induced degradation (PID) and predominant shading effect losses.
- Ripple in current from the solar panels oscillates the operating point around the maximum power point (MPP), leading to reduced efficiency and heating of panels [102].

The adverse effects of integrating renewable energy sources into the AC grid are a

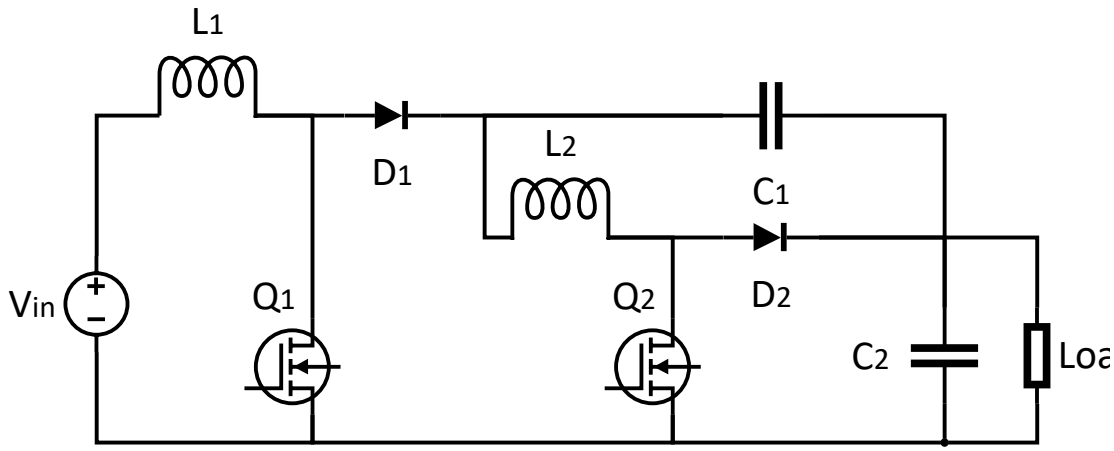


Figure 3.1: Topology of the proposed converter

topic of great concern among researchers [28, 46, 60]. Recent research has put forth many mitigation techniques [28]. The end-to-end efficiency of DC microgrid systems is higher than AC microgrids for renewable energy generations [104]. Thus, a highly distributed low voltage solar power generation system integrated with a DC microgrid is a viable solution to the grid integration problem.

This chapter presents a new high gain DC-DC boost converter for solar power integration in a DC microgrid. The single-phase topology of the proposed converter topology is shown in Figure 3.1. The major highlights of the proposed converter are:

- The number of components per phase is low due to common capacitors for all phases.
- The voltage stress on input-side switches is low.
- The input current ripple is eliminated.

The manuscript is organized as follows. The circuit description and converter's operation are explained in section II. The design and analysis of the proposed converter are dealt with in section III. Section IV presents the simulated and hardware results obtained with discussions. The presented work is concluded in Section V.

3.2 Circuit Description and Converter Operation

The converter topology of the modified interleaved boost converter is presented in Figure 3.2. The proposed converter has quadratic voltage gain, with both switches Q_1 and Q_2

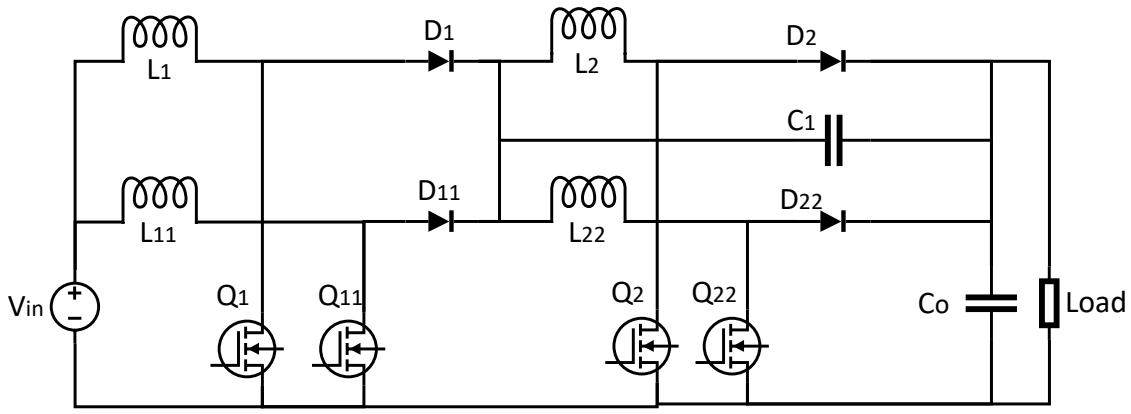


Figure 3.2: Interleaved topology of the proposed converter

operated at same duty. To eliminate the input current ripple, the duty of switches Q_1 and Q_{11} is fixed at 0.5. The proposed two-phase interleaved converter consists of switches- (Q_1, Q_{11},Q_2, & Q_{22}) , inductors - (L_1, L_{11},L_2, & L_{22}), Diodes - (D_1, D_{11}, D_2 & D_{22}). A common coupling capacitor C_1 and an output filter capacitor C_o. The working of the converter in continuous inductor current mode (CICM) is described in the following four modes of operation.

3.2.1 Mode-1

In this mode of operation, the switches Q_1 and Q_2 are in 'ON' state. While switches Q_{11} and Q_{22} are in 'OFF' state. Thus, input inductor L_1 is charging through Q_1 and inductor L_2 is charging through switch Q_2. The inductor L_{11} is discharging through diode D_{11} across capacitors C_1 and output capacitor C_o. Inductor L_{22} is discharging through diode D_{22} across capacitor C_o. The capacitor C_o is discharging in the load. The converter operation in mode-1 is depicted in Figure 3.3a.

3.2.2 Mode-2

The converter operation in mode-2 is depicted in Figure 3.3b. In this mode of operation, switches Q_1 and Q_2 are in 'OFF' state. While switches Q_{11} and Q_{22} are turned 'ON'. The inductor L_1 is discharging through diode D_1 across capacitors C_1 and C_o. The inductor L_2 is discharging through diode D_2 in capacitor C_o. Inductor L_{11} is charging through

switch Q_{11} and inductor L_{22} is charging through switch Q_{22}. The output capacitor C_o keeps discharging in the load.

3.2.3 Mode-3

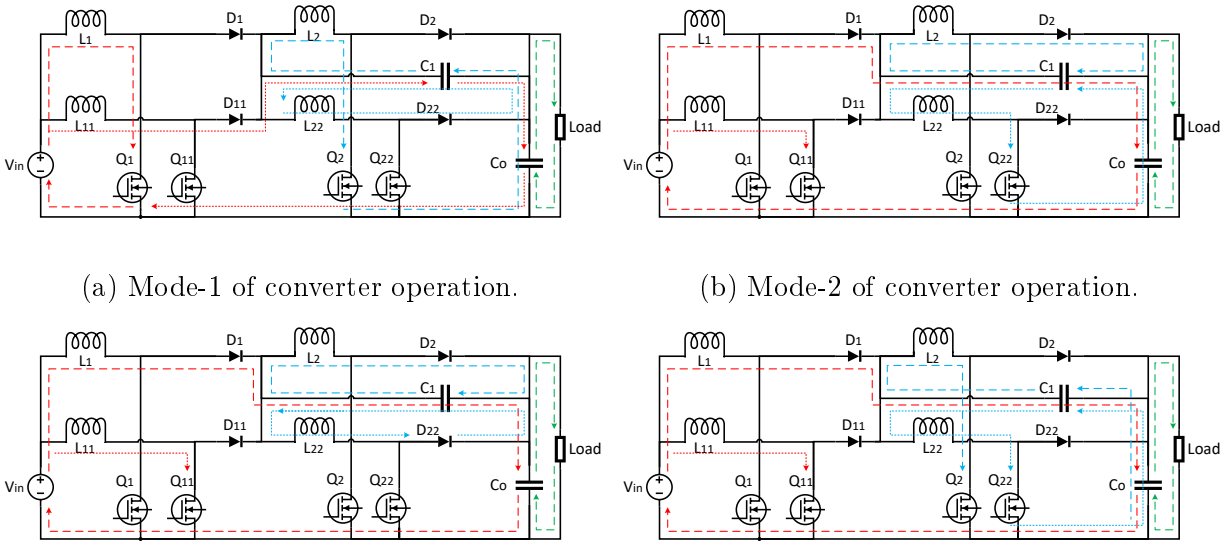
The mode-4 of converter operation is depicted in Figure 3.3c. In this mode the switches Q_1 & Q_{11} are operating in accordance to either mode-1 or mode-2 of conveter operation. The switches Q_2 & Q_{22} are in 'OFF' state, allowing the inductor L_2 & L_{22} to discharge in capacitor C_o through diodes D_2 and D_{22}.

3.2.4 Mode-4

The operation of the converter in mode-3 is shown in Figure 3.3d. The converter operates in this mode only when the duty of (Q_2 & Q_{22})<0.5. Switch Q_1 & Q_{11} are operating as in mode-1 or mode-2 at fixed duty of 0.5. Both the switches Q_2 and Q_{22} are in 'ON' state. The inductors L_2 & L_{22} are charging as C_1 and C_o are discharging through them. The diodes D_2 and D_{22} are in reverse blocking state.

The working of the proposed interleaved quadratic boost converter is explained in the four modes of operations. The key waveforms of the converter current and voltages during mode 1, 2,& 3 of converter operation is presented in Figure 3.4 as the converter can operate either in mode-3 or mode-4 depending on the value of working duty of the switches Q_2 & Q_{22}.

The selected values of capacitors are assumed to be large enough so that V_c and V_o are constant in a switching cycle. The working duty of Q_2 is D. The inductors are working in continuous current mode. Switches and diodes used are ideal switches. The converter operation can be explained using a single-phase topology of the converter. In the presented work, the duty of the input side switch is fixed at 0.5. Moreover, it is assumed that the duty of Q_2 is less than Q_1.



(a) Mode-1 of converter operation.

(b) Mode-2 of converter operation.

(c) Mode-3 of converter operation.

(d) Mode-4 of converter operation.

Figure 3.3: Different modes of converter operation.

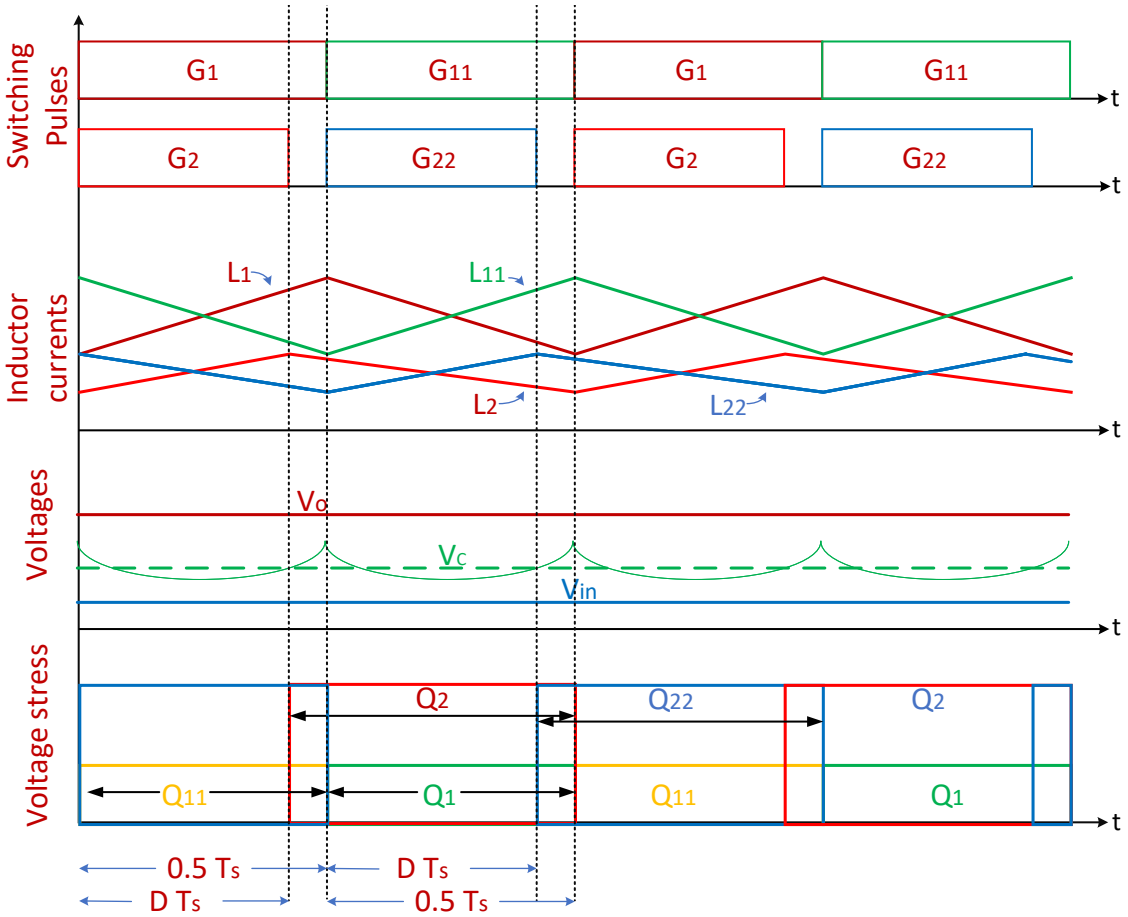


Figure 3.4: Key waveforms of proposed converter.

For t= 0 to DT_s(Both Q_1 and Q_2 are 'ON')

$$L_1\dot{i}_1 = V_{in} \tag{3.1}$$

$$L_2\dot{i}_2 = V_o - V_c \tag{3.2}$$

$$C_1\dot{v}_c = I_2 \tag{3.3}$$

$$C_o\dot{v}_o = -I_o - I_2 \tag{3.4}$$

For t= DT_s to $0.5T_s$(Q_1 is 'ON' and Q_2 is 'OFF')

$$L_1\dot{i}_1 = V_{in} \tag{3.5}$$

$$L_2\dot{i}_2 = -V_c \tag{3.6}$$

$$C_1\dot{v}_c = I_2 \tag{3.7}$$

$$C_o\dot{v}_o = -I_o \tag{3.8}$$

For t= $0.5T_s$ to T_s(Both Q_1 and Q_2 are 'OFF')

$$L_1\dot{i}_1 = V_{in} + V_c - V_o \tag{3.9}$$

$$L_2\dot{i}_2 = -V_c \tag{3.10}$$

$$C_1\dot{v}_c = I_2 - I_1 \tag{3.11}$$

$$C_o\dot{v}_o = I_1 - I_o \tag{3.12}$$

Applying volt-second balance on (3.1), (3.5), & (3.9).

$$DV_{in} + (0.5 - D)V_{in} + 0.5(V_{in} + V_c - V_o) = 0 \tag{3.13}$$

Applying volt-second balance on (3.2) (3.6) & (3.10).

$$D(V_o - V_c) + (0.5 - D)(-V_c) + 0.5(-V_c) = 0 \tag{3.14}$$

The expression of output voltage is obtained by solving (3.13) and (3.14), which is presented as a function of the working duty (D), input voltage (V_{in}) and voltage of the capacitor (C_1) as:

$$V_o = 2V_{in} + V_c \tag{3.15}$$

$$\implies V_o = \frac{2V_{in}}{1 - D} \tag{3.16}$$

3.3 Converter Design and Small Signal Analysis

The converter has four passive components in a single phase topology, namely inductors L_1 & L_2 and capacitors C_1 & C_o. A design example is presented for the proposed converter with output connected to a DC microgrid. The specifications for the design example are:

1. Input voltage (V_{in}) = 70 V.
2. Output voltage (V_o) = 230 V.
3. Output Power (P)= 1000 W.
4. Switching Frequency (f) = 50 kHz

3.3.1 Selection of duty D

Putting the values of input voltage and output voltage in (3.16) the value of duty ratio is calculated as;

$$D = 1 - \frac{2V_{in}}{V_o} = 39.1\%.$$

3.3.2 Selection of inductors

The value of the inductor is calculated for a single-phase circuit topology, as the interleaving of multiple phases does not lead to a change in inductor values. Input inductor value is calculated at input current ripple of 20 %. Thus,

$$L_1 = \frac{0.5V_{in}}{f\Delta I_1} \tag{3.17}$$

As the input side switches have a fixed working duty of 0.5. The calculated value of the input inductor is 244.7 µH. The nearest available inductor value of 270 µH is used in this work.

Similarly, the value of inductor L_2 is calculated as:

$$L_2 = \frac{D(V_o - V_c)}{f\Delta I_2} \tag{3.18}$$

From 3.15 it is observed that the value of $(V_o - V_c)$ is equal to $2V_{in}$. Thus, for a current ripple of 40 %, the value of inductance is calculated to be 492.2 µH. The nearest available value of 560 µH is selected in this work.

Table 3.1: DESIGN PARAMETERS

Input voltage	70V
Output voltage	230 V
Power	1000 W
Switching frequency	50 kHz

Table 3.2: REACTIVE COMPONENTS

Input inductor (L_1)	270 µH
Output inductor(L_2)	560 µH
Intermediate capacitor (C_1)	15 µF
Output filter capacitor (C_o)	100 µF

3.3.3 selection of capacitors

The value of intermediate capacitor C_1 is calculated so that it maintains a constant voltage throughout each switching cycle. It is observed from (3.3) & (3.7) that the current through C_1 is i_2 for the period of t= 0 to $0.5T_s$. Thus, the value of C_1 is calculated as:

$$C_1 = \frac{0.5I_2}{2f\Delta V_c} \tag{3.19}$$

By keeping the voltage ripple under 5 % i.e 4 V.The value of the capacitor C_1 is calculated to be 8.87 µF, a higher available value of 15 µF is chosen for this work. As stated earlier, the intermediate capacitor is a common element for all phases of the interleaved converter. Thus, the frequency is doubled in the case of capacitor calculation as the frequency of the current ripple is twice with two phases.

In this work, the output is connected to a DC microgrid. Thus output capacitor value is not relevant. A capacitor value of 100 µF can be connected at the output to filter the output current.

The design specifications are tabulated in Table 3.1. In the developed laboratory prototype, the selected values of reactive components are given in Table 3.2.

3.3.4 Small signal analysis

In Figure 3.2 the two-phase interleaved topology of the converter is depicted. A simplified converter topology is analyzed in this work for better understanding. The symbols and polarity signs of converter states for small signal analysis are given in Figure 3.5. The conventional method of defining states is not applicable in this work, as the output of the converter is connected to a DC microgrid. Thus, a resistive DC microgrid impedance of 1.5 Ω is assumed for state-space analysis [105]. Accordingly, the equations defining the converter operation are as follow:

For t = 0 to DT_s

$$L_1\dot{i}_1 = V_{in} - I_1 r_1 \tag{3.20}$$

$$L_2\dot{i}_2 = V_o - V_c - I_2(r_c + r_2) \tag{3.21}$$

$$C_1\dot{v}_c = I_2 \tag{3.22}$$

$$C_o\dot{v}_o = (V_d - V_o)/R - I_2 \tag{3.23}$$

For t = DT_s to $0.5T_s$

$$L_1\dot{i}_1 = V_{in} - I_1 r_1 \tag{3.24}$$

$$L_2\dot{i}_2 = -V_c - I_2(r_c + r_2) \tag{3.25}$$

$$C_1\dot{v}_c = I_2 \tag{3.26}$$

$$C_o\dot{v}_o = 0 \tag{3.27}$$

For t = $0.5T_s$ to T_s

$$L_1\dot{i}_1 = V_{in} + V_c - V_o - I_1 r_1 - r_c(I_1 - I_2) \tag{3.28}$$

$$L_2\dot{i}_2 = -V_c - I_2(r_c + r_2) + I_1 r_c \tag{3.29}$$

$$C_1\dot{v}_c = I_2 - I_1 \tag{3.30}$$

$$C_o\dot{v}_o = I_1 + (V_d - V_o)/R \tag{3.31}$$

Where, r_1, r_2, & r_c are equivalant series resistance (ESR) of inductor L_1, L_2, and capacitor C_1 respectively. V_d is the DC microgrid stiff voltage and R is the grid resistance.

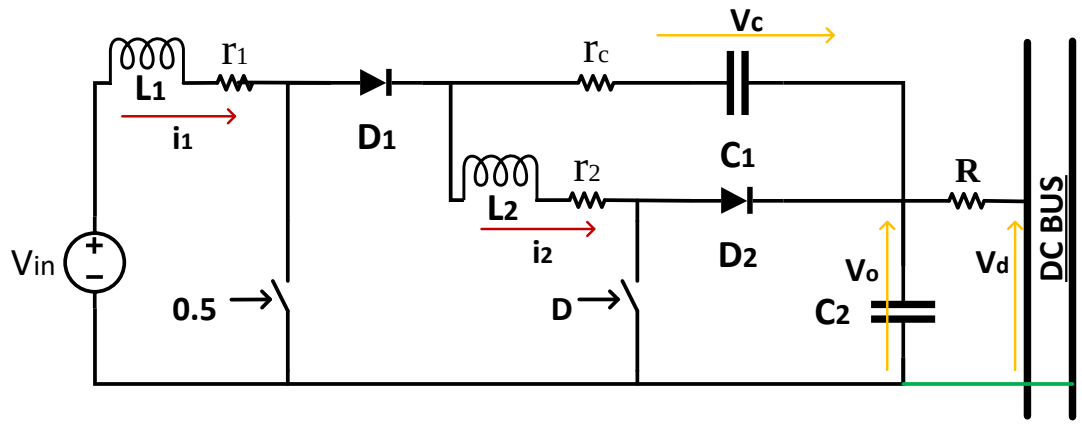


Figure 3.5: Converter parameters for small signal analysis.

Introducing perturbations as:

$$v_{in} = V_{in} + \hat{v}_{in} \qquad i_1 = I_1 + \hat{i}_1 \qquad i_2 = I_2 + \hat{i}_2$$
$$v_c = V_c + \hat{v}_c \qquad v_o = V_o + \hat{v}_o \qquad d = D + \hat{d}$$

with the assumption that $\hat{V}_d = 0$ and average value of $V_d = V_o$, the state-space matrix is found as:

$$A = \begin{bmatrix} -\frac{r_1 - 0.5r_c}{L_1} & r_c/2L_1 & 1/2L_1 & -1/2L_1 \\ r_c/2L_2 & -\frac{r_2+r_c}{L_2} & -\frac{1}{L_2} & \frac{D}{L_2} \\ -\frac{0.5}{C_1} & \frac{1}{C_1}1 & 0 & 0 \\ 0.5 & -D & 0 & -\frac{0.5+D}{C_o R} \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & \frac{V_o}{L_2} \\ 0 & 0 \\ 0 & \frac{-I_2}{C_o} \end{bmatrix}, \; X = \begin{bmatrix} \hat{i}_1 \\ \hat{i}_2 \\ \hat{V}_c \\ \hat{V}_o \end{bmatrix}, \; U = \begin{bmatrix} \hat{V}_{in} \\ \hat{d} \end{bmatrix}$$

Where, $\dot{X} = A[X] + B[U]$

The output to input transfer functions for $|\hat{i}_1/\hat{v}_{in}$, $|\hat{i}_1/\hat{d}$, $|\hat{i}_2/\hat{v}_{in}$, $|\hat{i}_2/\hat{d}$, $|\hat{v}_c/\hat{v}_{in}$, $|\hat{v}_c/\hat{d}$, $|\hat{v}_o/\hat{v}_{in}$, & $|\hat{v}_o/\hat{d}$ can be found using the matrices A, B, X & U. By putting in the design values of passive components and DC microgrid resistance of (R=1.5 Ω), transfer function for $|\hat{i}_1/\hat{d}$ is found to be:

$$\frac{\hat{i}_1}{\hat{d}} = \frac{2.835\times10^8 s^2 + 5.365\times10^{13} s + 1.022\times10^{18}}{s^4 + 23620 s^3 + 2.564\times10^8 s^2 + 3.943\times10^{12} s + 5.3\times10^{15}}$$

Table 3.3: DEVICE SPECIFICATIONS

component	Number	specification
MOSFETs	2	IPW60R160C6FKSA1
MOSFETs	2	STW52NK25Z
Diodes	4	IDP15E65D2XKSA1
Gate driver	4	FOD3184
Capacitor(C_1)	1	F611FY156M400ZLH0J
Capacitor(C_o)	1	MCKSK400M101K32S
Inductor	2	PCV-2-274-10
Inductor	2	PCV-2-564-08
PV emulator	1	ETS600X8D-PVF

3.4 Results and Discussion

The working of the proposed converter is validated by developing a Matlab/Simulink model using the calculated parameters given in Table 3.2. A laboratory prototype of the converter is developed as well, the specifications of the devices used in development of prototype and testing system is presented in Table 3.3. The results obtained from the simulations and the hardware prototype verifies the working principle and theory presented in Section 3.2.

The simulated results of the converter at an input voltage of 63 V is presented in Figure 3.6, showing the input switch stress and input inductor currents. The converter is performing MPP tracking using the incremental conductance(INC) technique. As the output voltage is fixed at 230 V and the capacitor (C_1) voltage is at 104 V, the relation between the output voltage, input voltage, and capacitor voltage given in (3.15) is verified.

The voltage stresses on the input diodes are shown in Figure 3.7, unlike conventional boost converter, the voltage stress is reduced to ($V_o - V_c$). Thus switches and diodes with lower voltage ratings having lower on-resistance can be used in this converter, which increases the conversion efficiency.

Figure 3.8 presents the relation between the inductor currents, input voltage, and output voltage. The simulated waveform of currents in inductors L_1 and L_2 are depicted

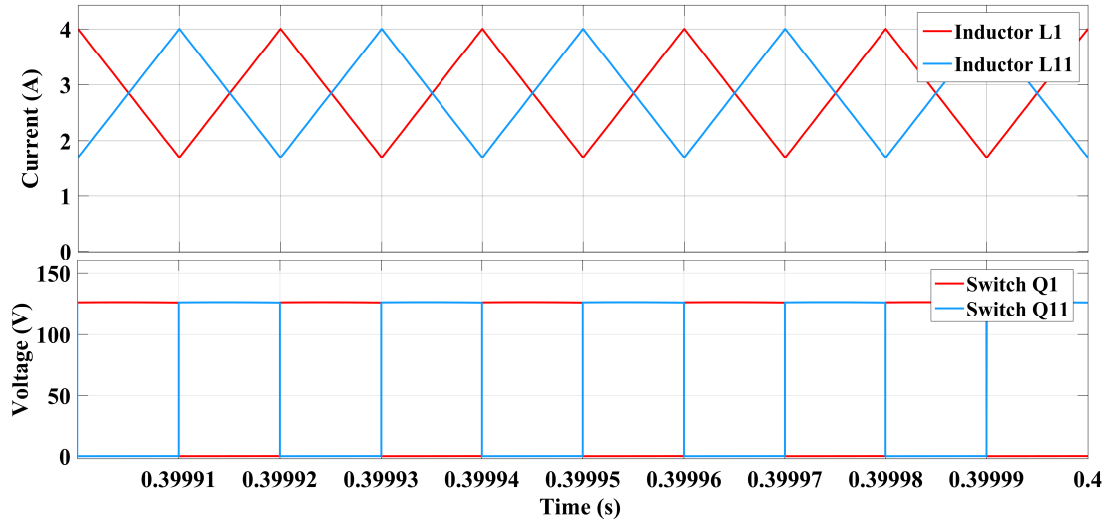


Figure 3.6: Simulated results showing the input inductor currents with voltage stresses on the switches Q_1 & Q_{11}.

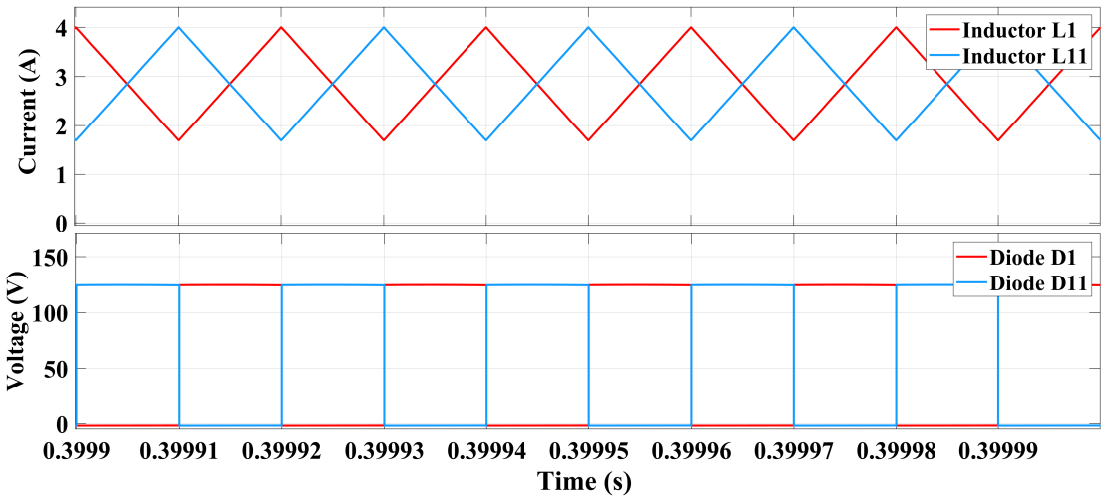


Figure 3.7: Simulated voltage stress on diodes D_1 & D_{11} with inductor currents of L_1 & L_{11}.

here. The mean value of input inductor current is 3.2 A and output inductor is 1.6 A. This satisfies the relation i_1=2×i_2 obtained by solving (3.3),(3.7) & (3.11) for steady state.

The voltage stress on switches Q_1 & Q_2 with voltage of intermediate capacitor and output voltage is shown in Figure 3.9 in steady state. It is evident from this result that the voltage stress on the input switch Q_1 is significantly lower than the output switch Q_2.

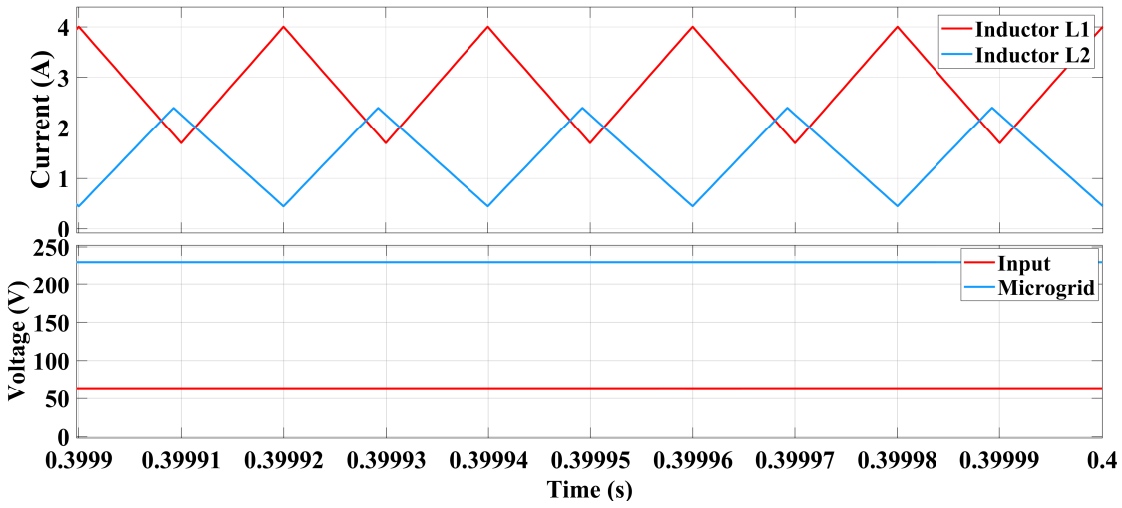


Figure 3.8: Simulated inductor currents of L_1 & L_2 with input and output voltages.

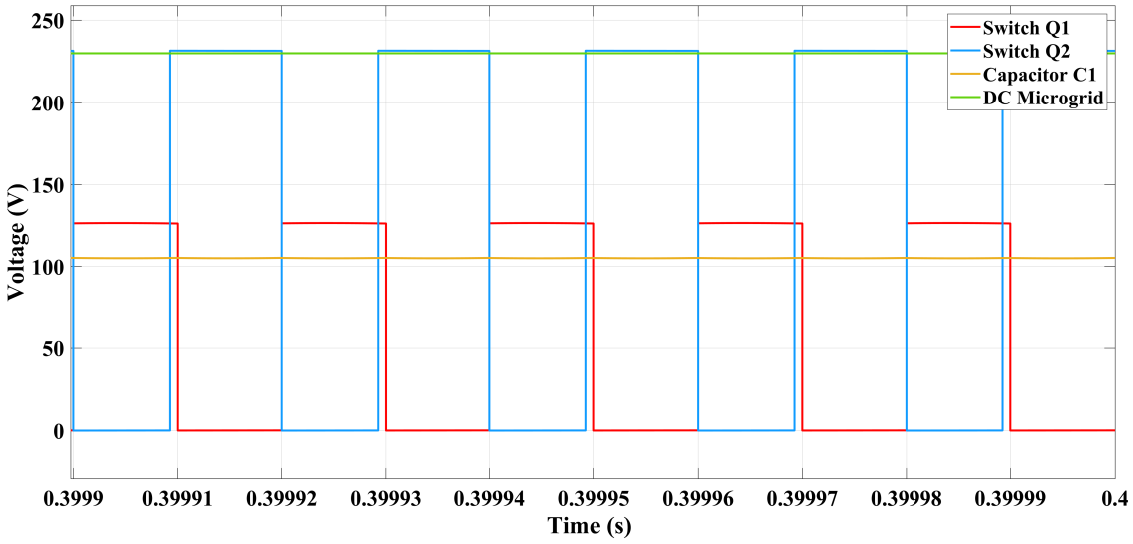


Figure 3.9: Simulation result showing voltage stresses on switches and relation between output DC microgrid voltage and voltage of capacitor C_1.

A brief comparison of the proposed converter with conventional converters is presented in Table 3.4. The laboratory setup is shown in Figure 3.10. The states of all the passive components in the converter per phase obtained from the hardware prototype are presented in Figure 3.11. The fixed output voltage from the DC microgrid is captured on channel-4 of the digital storage oscilloscope (DSO). Channel-1, channel-2 and channel-3 captured the current i_1, i_2 and voltage of intermediate capacitor C_1, respectively.

Voltage stresses on input side switches Q_1 & Q_{11} and inductor currents in L_1, & L_{11}

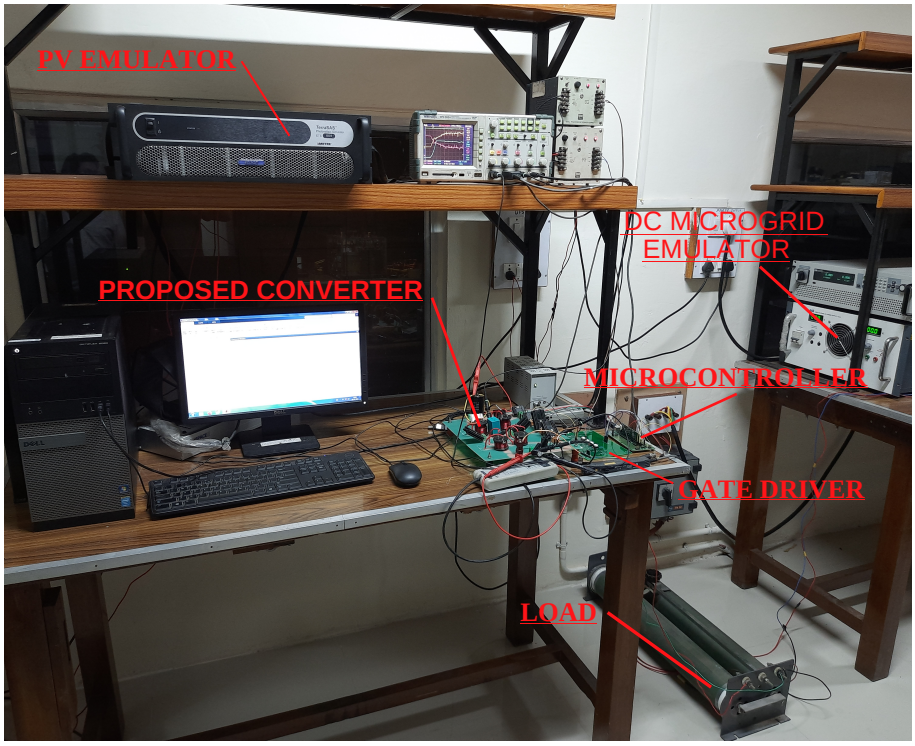


Figure 3.10: Experimental setup.

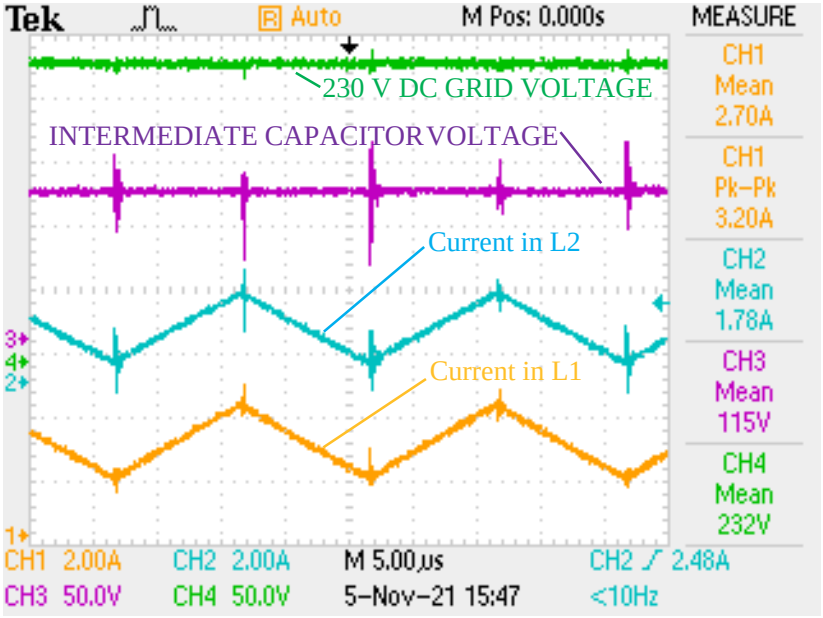


Figure 3.11: Inductor current of L_1, L_2, capacitor voltage, output voltage.

and are shown on channel 1,2,3 & 4 of Figure 3.12, respectively. The input inductor are operating in CICM at 0.5 duty as expected. This leads to a ripple free input current as depicted on channel-1 in Figure 3.13. The inductor currents in L_1 and L_2 are depicted on channel-2 & 3 with the output voltage on channel-4.

Table 3.4: COMPARISON WITH CONVENTIONAL CONVERTERS

Topology	Operation mode	Components per phase				Voltage gain	Current ripple
		S	D	L	C		
High gain with coupled inductor [52]	Boost	2	2	3	4	$\frac{NK}{(1-D)}$	non-zero.
High step-up resonant converter [59]	Boost	6	0	4	4	$4n\gamma$, where γ <1	zero
SEPIC ripple eliminating circuit [7]	Buck-Boost	1	2	4	4	$\frac{1+D}{1-D}$	non zero
Semiquadratic buck-boost converter [62]	Buck-Boost	2	3	4	5	$\frac{2D(2-D)}{(1-D)^2}$	non-zero
Non-inverting high gain converter [63]	Boost	1	6	2	5	$\frac{2(2-D)}{(1-D)^2}$	non-zero
Proposed converter	Boost	2	2	2	2	$\frac{2}{(1-D)}$	zero

*S=switches, D=diodes, L=inductors, C=capacitors

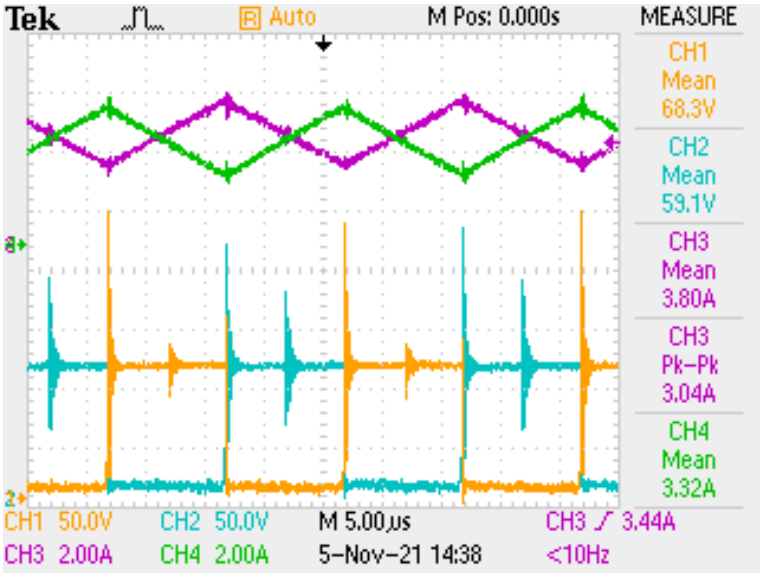


Figure 3.12: Voltage stress on Q_1, Q_{11}, inductor currents of L_1 and L_{11}.

The output side characteristics of the converter are presented in Figure 3.14. The voltage stress on switches Q_2 & Q_{22} with currents of inductors L_2 & L_{22} are shown on channels 1,2,3 & 4, respectively. It is observed from Figure 3.12 & Figure 3.14 that the mean values of currents in output side inductors are half of the mean values of currents

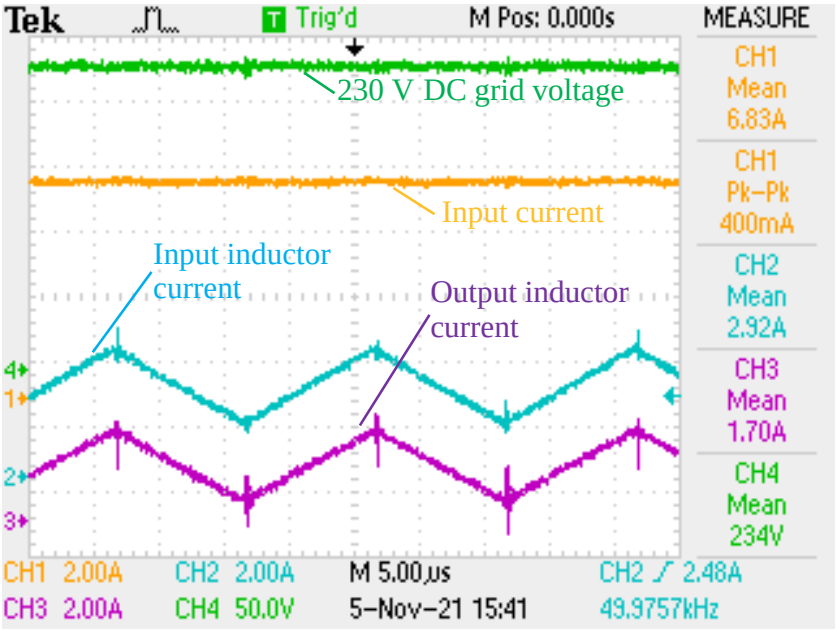


Figure 3.13: Input source current, current of inductor L_1, L_2, output voltage.

in input side inductors.

The voltage stress on the diodes D_1, D_2, input voltage, and output voltage are shown in Figure 3.15. It is evident from the result that the voltage stress on the input side diode is very low, and thus diodes with low forward voltage can be used to minimize losses. The input voltage from the solar panel is at around 60 V, with no significant oscillations without any filter capacitor.

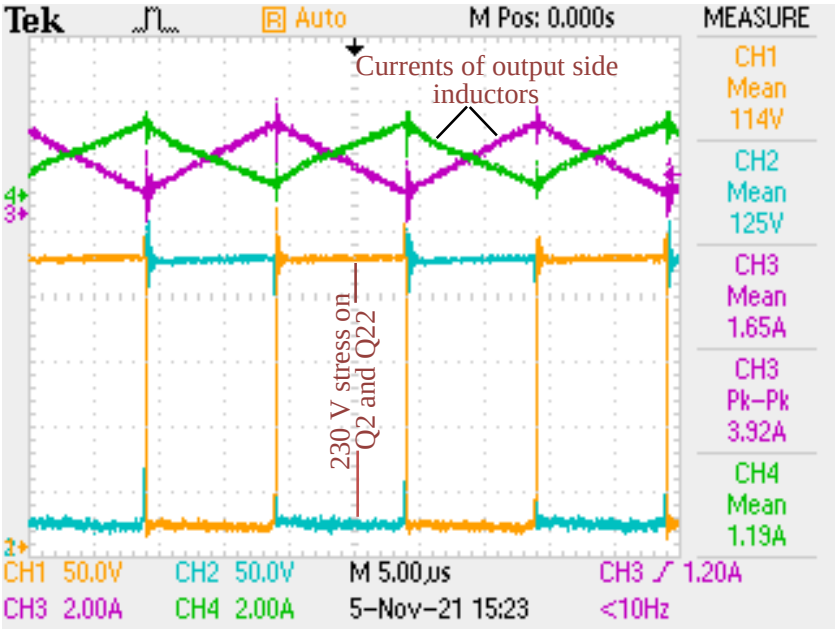


Figure 3.14: Voltage stress on switch Q_2, Q_{22}, current of inductor L_2, L_{22}.

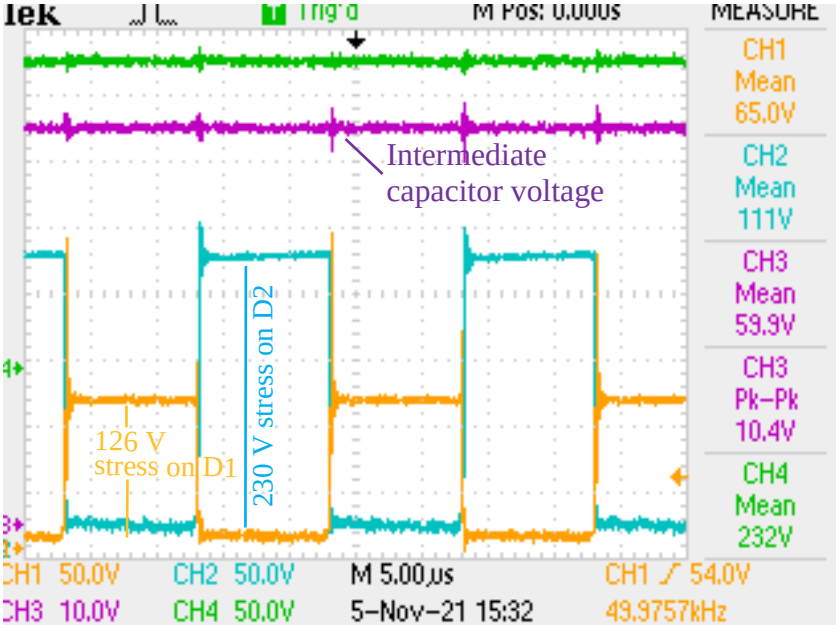


Figure 3.15: Voltage stress on diode D_1 on channel-1, voltage stress on diodes D_2 on channel-2, input voltage on channel-3, output voltage on channel-4.

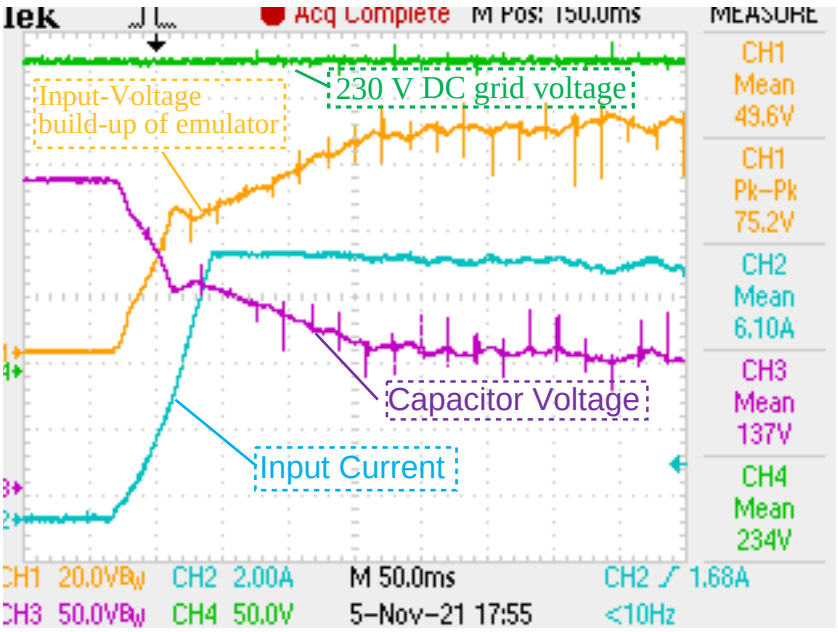


Figure 3.16: Transient response of the converter states; input voltage on channel-1, input current on channel-2, capacitor voltage on channel-3, output voltage on channel-4.

The transient response of the system with INC MPP technique is shown in Figure 3.16. The input voltage, input current, intermediate capacitor voltage and output voltage are shown in channel 1,2,3, & 4 respectively. The steady state MPPT response is presented in Figure 3.17, the system is found to be working at ≈ 99.5 % of the MPP.

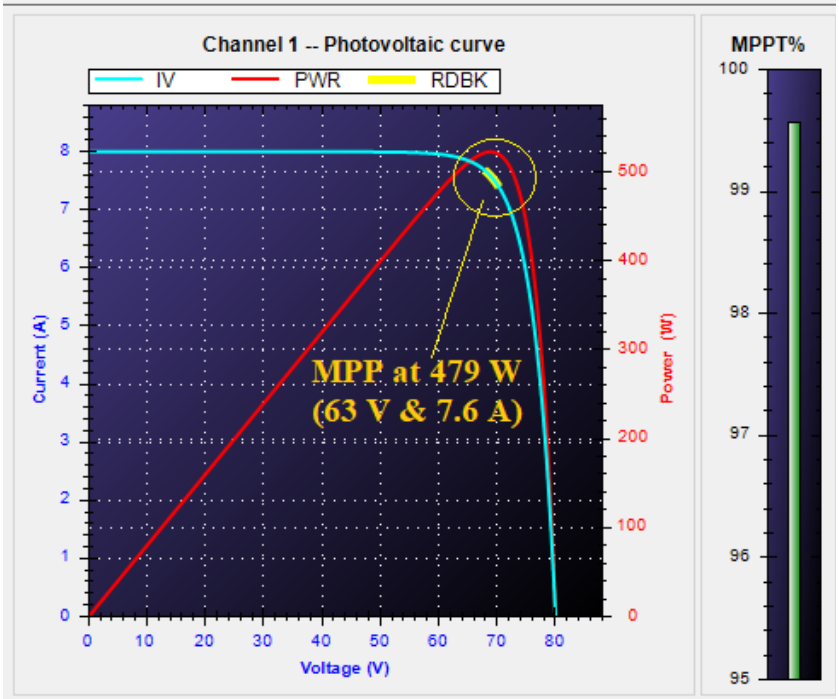


Figure 3.17: MPPT response.

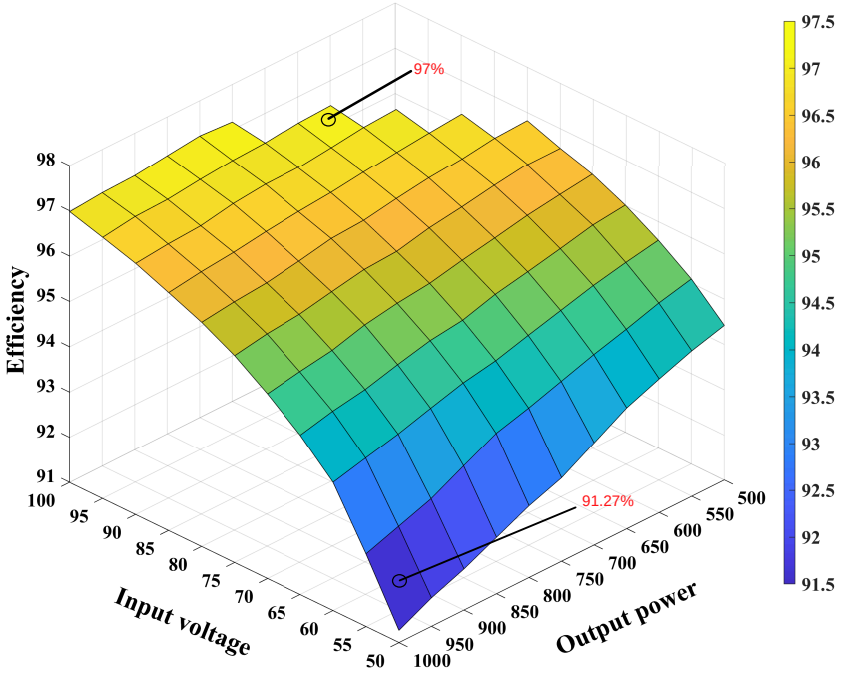


Figure 3.18: Efficiency curve with output power and input voltage.

The developed prototype is tested with varying input voltage from 50 V to 100 V and output power from 500W to 1000 W. The power is varied by controlling the output voltage across a 200 Ω resistor. The calculated efficiency of the converter is presented in Figure 3.18. With a decrement in output power, the capacitor voltage increases resulting in lower voltage stress across the switches. Thus, it is observed that an increment in input voltage and a decrement in the output power results in higher conversion efficiency.

3.5 Summary

This work has designed, developed, and analyzed a new topology of a two-phase interleaved quadratic boost converter. The designed converter is simulated in Matlab/Simulink, and the results are compared with the hardware results obtained from a laboratory-developed prototype of 1000 W. A high voltage gain of $2V_{in}/(1-D)$ is obtained with a ripple-free input current. By integrating a common intermediate capacitor, the objective of component reduction and voltage stress reduction is achieved, as demonstrated by the obtained results. Thus, validating the suitability of the converter for integrating PV generation into a DC microgrid. The converter is tested under a varying input voltage (50 V-100 V), and output power ($500\text{W} - 1\text{kW}$). The maximum efficiency of 97 % is obtained at (95 V & 650W) and the minimum efficiency of 91.27 percent is obtained at 50 V input and 1000 W power output. The converter's application in a PV generation system is verified by implementing the INC MPP technique on an emulated solar panel with V_{oc}=80 V and I_{sc}=8 A. The presented results show that the MPP is successfully tracked when connected to a 230 V DC microgrid.

After dealing with the challenges related to photovoltaic generation, the problems related with WECS is presented in the next chapter. The next chapter deals with development of a new converter topology, for single-stage three-phase AC to DC conversion.