Chapter-3

Impact of Interface Trap Charges (ITCs) on the Performance of SiO_2/HfO_2 Stacked Gate Oxide Ge/Si Heterojunction STFET

3.1 Introduction

The literature review carried out in chapter-1 shows that the Si/SiO_2 interface trap charge is highly responsible for the degradation of the performance of the CMOS devices [128]-[130]. This chapter presents an extensive survey on the impact of interface trap charges on studied TFETs. The trap charges at the Si-SiO_2 interface always creates reliability issues [128]-[130], [166]-[169]. These charges are developed at the interface during the fabrication process itself. Interface charges may be stress-induced [170], process-induced [171], or maybe radiation-induced [172]. The genesis of interface trap charges is basically because of Si dangling bonds. These bonds are present at the interface of silicon and silicon dioxide. Now as oxidation on the silicon surface is carried out oxygen reacts with silicon and satisfies a plethora of dangling bonds and the count of dangling bonds is minimized, but still, there is a possibility that post oxidation some dangling bonds are present which are the major cause of interface trap charges [170]-[173]. Interface charges are present all over the forbidden energy gap and depending upon the Fermi level they can be either empty or filled [173]. So as the gate voltage is applied, bands bend up or down depending upon the type of input applied at the gate and these interface states change their occupancy hence their electronic activity changes and correspondingly affects the device performance [128]-[130], [172]-[173].

In Chapter-2 it was discussed that use of heterojunction engineering (i.e., use of Ge at source side) along with gate oxide engineering (i.e., vertical stacking of HfO_2/ SiO_2/) not only increased the drive current but also increased the I_{ON}/I_{OFF} ratio. Furthermore, it was

also discussed that use of SELBOX increased the thermal insulation and decreased the leakage current. Dual material gate engineering (use of two different gate electrode materials connected in a cascade to form gate-electrode contact in such a way that the higher work function material is placed near the source side to form the control gate or tunnel gate while the lower work function material is placed on the drain side to act as the screening gate or auxiliary gate [174]) along with lateral HfO_2/SiO_2 gate stack engineering is known to increase trapped charges reliability. Therefore in this present chapter comparative performance between dual-material (DM) lateral-stacked (LGS)-HJ-STFET and dual-material (DM) verticle stacked (VGS)-HJ-STFET (proposed device in chapter-2 with exception of dual material gate instead of single material gate), respectively. The objective of this chapter is to analyze degradation in performance of our proposed devices due to the presence of interface trap charge present between the Si-SiO_2 interface [166]-[167]. The effect of interface trap charges on drain current, transconductance, higher-order transconductance, linearity, and distortion parameter (VIP2, VIP3, IIP3, IMD3, Zero crossover point, 1-dB compression point) has been studied [168]-[169]. High linearity and low distortion demand high value of VIP2, VIP3, IIP3, 1-dB compression point and low value of IMD3, Zero crossover point, and higher-order transconductance parameter. Through our simulations, we have found that the presence of interface trap charges leads to curtailment in reliability and lifetime of the device. The donor interface trap acts as a positive interface trap charge when it's empty and a neutral charge when it is filled with electrons. Acceptor interface charges act as negative interface traps when filled with an electron and neutral charges when it is empty.

The effects of oxide interface trap charges (ITCs) at the Si/SiO_2 interface on the DC/RF and linearity performances of the proposed LGS-HJ-STFET structure have been analyzed using a commercial TCAD tool [157]. Finally, a device-level performance comparison is

made by considering the LGS-HJ-STFET over vertically gate stacked (VGS)-HJ-STFET in the presence of interface trap charges

This chapter is organized as follows: The schematic architectures and fabrication feasibility of the studied TFETs are discussed in section 3.2. In section 3.3, the possible manufacturing steps for realizing the suggested structure are discussed. A device-level performance comparison was done in section 3.4. Finally, section 3.5 contains the current chapter's summary and conclusion.

3.2 Device Under Study

3.2.1 Schematic Structures

Figures 3.1 (a) and (b) show the 2D schematic structures of the studied LGS-HJ-STFET and VGS-HJ-STFET, respectively. The material with a work function of 4.2 eV is used near the source side for forming the tunneling gate while the work function of 3.8 eV is used for the auxiliary gate at the drain side of the TFET. The tunneling gate is responsible for the tunneling of electrons from source to channel region [175]. The high-k HfO_2 is placed under the tunneling gate and low-k SiO_2 is maintained under the auxiliary gate to form a laterally-connected HfO_2/SiO_2 oxide structure to improve the ON-state current of the device [176]-[177]. Low band gap material (Ge) is used in the source region to form a Ge/Si heterojunction with the channel for increasing the ON-state current [164], [174]. The device parameters used for TCAD simulation are listed in Table 3.1.

3.2.2 Fabrication Feasibility

The fabrication process flows for the LGS-HJ-STFET are depicted in Figure 3.2, and the fabrication steps for the VGS-HJ-STFET have already been covered in Chapter 2. The fabrication process of the proposed STFET device is demonstrated in Figure 3.2 following the method proposed in ref. [109]. We may start with a p-type substrate, in which, the SiO_2 layer can be grown by the thermal oxidation method. The SELBOX

structure is created by etching away an undesired portion of the SiO_2 layer near source region. Then Ge based source and Si-based channel (drain) regions can be grown on the SELBOX based substrate using molecular beam epitaxy (MBE). The SiO_2/HfO_2 staked gate-oxide structure can be created by thermal oxidation of HfO_2 over SiO_2. Finally, metal electrodes for source, gate, and grain can be fabricated by depositing metals in the respective regions by the vacuum evaporation method.

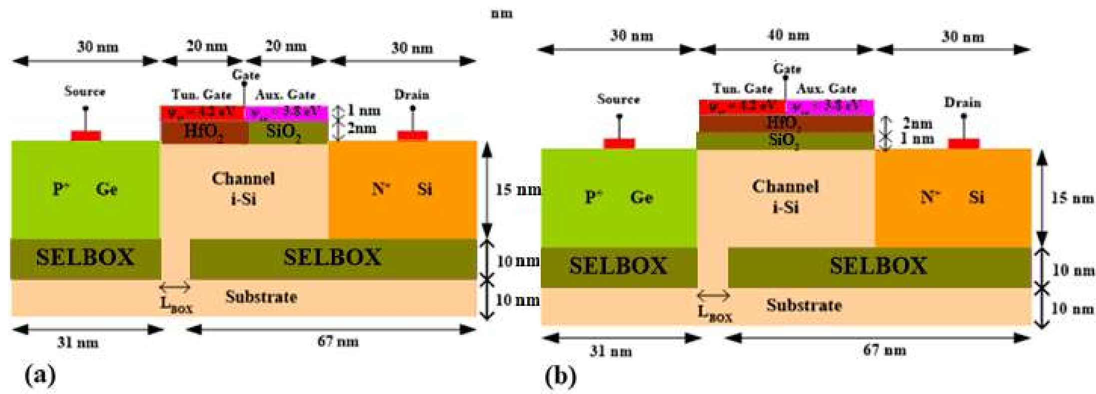


Figure 3.1 Schematic structures of (a) LGS-HJ-STFET, and (b) VGS-HJ-STFET.

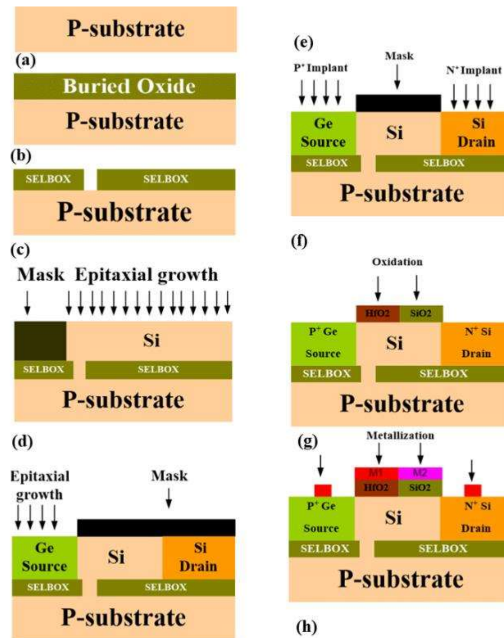


Figure 3.2 Possible fabrication process steps of the proposed VGS-HJ-STFET [109].

Table 3.1: Device Specifications.

Parameters	VGS-HJ-STFET	LGS-HJ-STFET
Source doping concentration (N_S)	1×10^{19} cm^{-3}	$1\times10^{19}$$cm^{-3}$
Channel doping concentration (Nch)	1×10^{15} cm^{-3}	1×10^{15} cm^{-3}
Drain doping concentration (N_D)	5×10^{18} cm^{-3}	5×10^{18} cm^{-3}
The thickness of the channel (t_{Si})	15 nm	15 nm
The thickness of SiO_2 gate oxide (t_{ox})	1 nm	2 nm
The thickness of High-k gate oxide (t_{ox})	2 nm	2 nm
Effective Oxide Thickness (EOT)	1.312 nm	-----
SiO_2 gate dielectric permittivity (ε)	3.8	3.8
HfO_2 gate dielectric permittivity (ε)	25	25
Gate length (L_G)	40 nm	40 nm
Source length (L_S)	30 nm	30 nm
Drain length (L_D)	30 nm	30 nm
Thickness of buried oxide (BOX) (t_{BOX})	10 nm	10 nm
Length of SELBOX gap (L_{BOX})	2 nm	2 nm
Hole tunnel mass in silicon (m_{htSi})	$0.24m_o$	$0.24m_o$
Hole tunnel mass in germanium (m_{htGe})	$0.044m_o$	$0.044m_o$
Electron tunnel mass in silicon (m_{etSi})	$0.20m_o$	$0.20m_o$
Electron tunnel mass in germanium (m_{etGe})	0.082mo	0.044mo
Lattice constant of Ge	5.656 ^{0}A	5.656 ^{0}A
Lattice constant of Si	5.429 ^{0}A	5.429 ^{0}A
Bandgap energy Ge	0.70 eV	0.70 eV
Bandgap energy Si	1.12 eV	1.12 eV
Electron affinity Ge	4.01 eV	4.01 eV
Electron affinity Si	4.05 eV	4.05eV
Tunneling gate work function Ψ_T, (M_1)	4.2 eV	4.2 eV
Tunneling gate work function Ψ_{Aux}, (M_2)	3.8 eV	3.8 eV

3.2.3 Calibration of the Models

We have first calibrated the models used for simulation using SILVACO ATLAS^{TM} TCAD tool for our proposed TFET structures of Figure 3.1 [157]. The TCAD simulation results of the Ge/Si heterojunction based TFET have been compared with the measured data reported by A. Biswas *et al*. [158]. The device design parameters of the Ge/Si heterojunction based TFET was kept same as the experemetal data based on fabrication report by A. Biswas et al. [159] at V_{DS} of 0.1 V and of 0.5 V. Better fitting with the experimental data can be obtained by adjusting the effective masses (ME.TUNNEL and MH.TUNNEL) of the carriers in the material statement. However, we used the values of the effective masses of the carriers from the ATLAS manual which are listed in the Table-3.1. Fine rectangular meshing is used to define various regions of interest (e.g., tunneling junction, at contact terminals etc.) of the proposed device. We observed a reasonably good matching between the two results which ensures the validity of the chosen models. A slight difference between the simulation and experimental results in Figure 3.3 can be attributed to the non-ideal measured characteristics of the practical SOITFET.

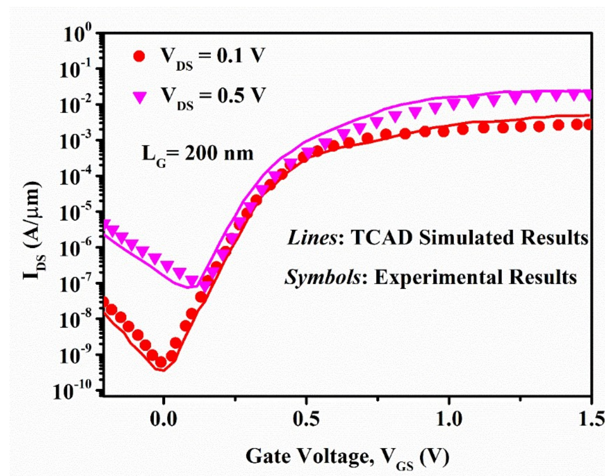


Figure 3.3 Calibration of simulated result with the experimental result [158].

3.3 Results and Discussion

In this section, we will first present a device-level performance analysis of LGS-HJ-STFET and VGS-HJ-STFET, respectively.

3.3.1 DC Performance Analysis

Figure 3.4 (a) shows the plots of the energy band diagram in presence of interface charges of LGS-HJ-STFET in OFF-state and ON-state, respectively, whereas, Figure 3.4 (b) shows the plots of the energy band diagram of VGS-HJ-STFET in OFF-state and ON-state, respectively. In OFF-state, carrier tunneling from the valence band of the source to the conduction band of the channel is not possible because of misalignment between the valence band of the source and the conduction band of the channel as depicted in Figure 3.4 (a) [41]-[45]. In ON-state, due to the application of gate bias, the conduction band of the channel gets proper alignment with the valence band of the source which allows the carriers to tunnel through the source-channel interface [41]-[45]. Tunneling width is defined as the minimum distance between the valence band of the source and the conduction band of the channel which should be as low as possible for better tunneling phenomena [44]-[47]. It can be observed from Figure 3.4 that in ON-state the tunneling width of LGS-HJ-STFET is lower than VGS-HJ-STFET. Due to the lower tunneling width in the proposed LGS-HJ-STFET, the BTBT generation rate is very high which in turn enhances the ON-state current. In addition, as we have considered different interface trap charges (positive, negative, and neutral) at the oxide-semiconductor interface, the influence of these trap charges is also analyzed in the energy band diagram. The presence of positive interface charges helps in the reduction of tunneling width whereas the presence of negative interface charges increases the tunneling width. This can be seen in Figure 3.4 for both the TFETs under study.

Figure 3.5 shows the graphs of the electric field vs. the device length for LGS-HJ-STFET and VGS-HJ-STFET including the effects of interface charges. LGS-HJ-STFET has a maximum value of electric field (4.8 MV/cm) as compared to VGS-HJ-STFET (3.2 MV/cm). The reason for the higher electric field can be attributed to the presence of high-k dielectric nearer to the source region of the LGS-HJ-STFET. The higher electric field at the source channel junction for LGS-HJ-STFET gives rise to a higher band to band tunneling rate which in turn enhances the ON-state current [179].

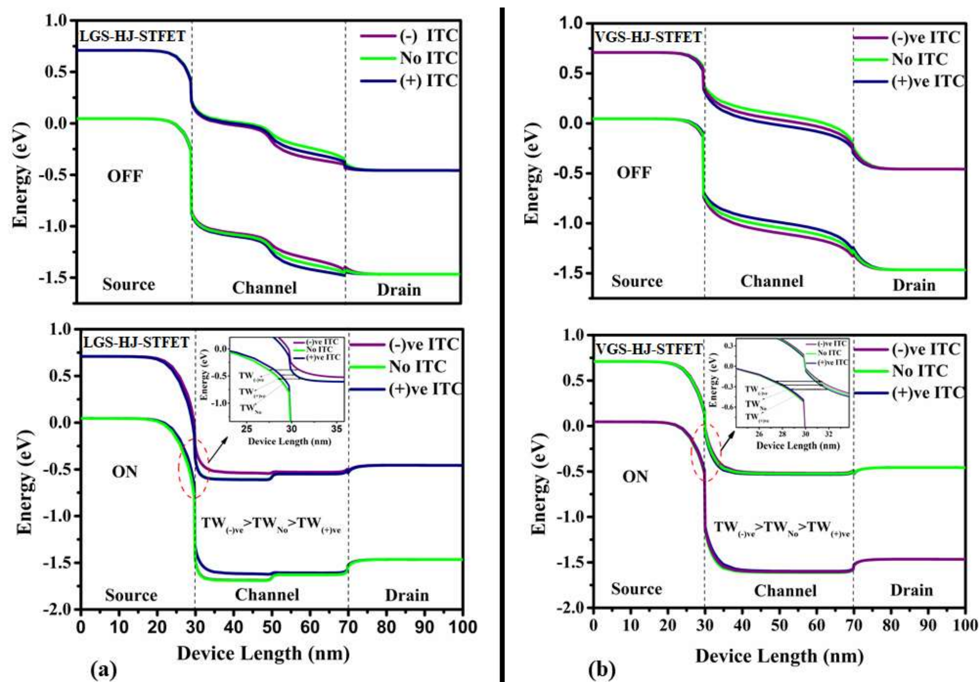


Figure 3.4 Plots of energy band diagram in (a) OFF and ON-state of LGS-HJ-STFET and (b) OFF and ON-state of VGS-HJ-STFET.

Figure 3.6 (a) shows the graphs of drain current in a logarithmic scale vs. gate voltage for the devices i.e., LGS-HJ-STFET and VGS-HJ-STFET at V_{DS} = 0.5 V. The subthreshold swing (SS) of LGS-HJ-STFET are lower (20 mV/dec) as compared to VGS-HJ-STFET (39.5 mV/dec). This makes the LGS-HJ-STFET more suitable for low power applications than VGS-HJ-STFET. I_{ON} (1.77×10^{-5}) of LGS-HJ-STFET is higher than VGS-HJ-STFET (1.001×10^{-5}), which indicates that the proposed device has higher conduction efficiency

than VGS-HJ-STFET. I_{ON}/I_{OFF} ratio of LGS-HJ-STFET exhibited higher (7.092x10^{10}) compared to VGS-HJ-STFET (6.935x10^{10}) without the presence of interface charges. A detailed comparison of all the DC parameters including the effects of interface trap charges is listed in Table 3.2.

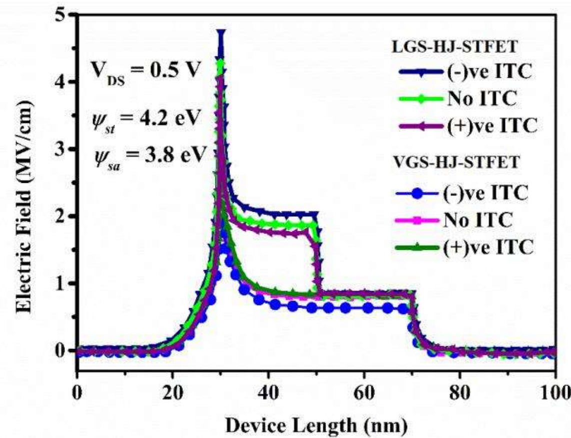


Figure 3.5. Plots of the electric field vs. device length of LGS-HJ-STFET and VGS-HJ-STFET at V_{DS} = 0.5 V.

Figure 3.6 (b) shows the plots of the transconductance of both the aforementioned TFETs. The proposed TFET (LGS-HJ-STFET) has a higher value of transconductance (50 μS) than the VGS-HJ-STFET structure (24.9 μS). Output conductance is defined as $g_d = \frac{\partial I_D}{\partial V_D}$ [179], where V_{DS} is drain voltage and I_{DS} is the drain current. Figure 3.6 (c) shows the output conductance of both the TFETs presented for a study where it can be concluded that the g_d of LGS-HJ-STFET is higher than VGS-HJ-STFET. The reason for the same is attributed to the higher transportation rate of tunneling from source to channel for LGS-HJ-STFET for which a higher value of gd got attained compared to VGS-HJ-STFET. LGS-HJ-STFET is also found to have less variation in output conductance in presence of interface trap charges compared to VGS-HJ-STFET which is shown in the same figure. Transconductance generation factor (TGF) is one of the decisive parameters for analog applications. Figure 3.6 (d) shows the plots of TGF vs. V_{GS} which represents

available gain per unit of power dissipation [180]. TGF is maximum in the weak inversion region and decreases monotonically as the drain current increases. In the weak inversion the value of $\frac{g_m}{I_d}$ is exhibited by the proposed device (LGS-HJ-STFET) is 3.3 (KV^{-1}), which is higher than that of VGS-HJ-STFET. Figure 3.7 shows the variation of sub-threshold swing and threshold voltage in presence of interface trap charges. It is found that the sub-threshold swing (SS) increases with an increase in negative interface trap charges whereas the sub-threshold swing is getting decreased with an increase in positive interface trap charges. At the same time, it can be also observed from the same figure that the variation in SS is found to be minimum for the proposed LGS-HJ-STFET compared to VGS-HJ-STFET. The same trend is also observed for the threshold voltage (V_{th}) which decreases in the presence of negative traps and increases are obtained for positive traps as shown in Figure 3.7.

Table. 3.2 Comparative table of dc parameters between LGS-HJ-STFET and VGS-HJ-STFET for negative, positive, and neutral interface trap charges (ITCs) with $\pm 1x10^{12}/cm^2$ concentration.

Parameters	**LGS-HJ-STFET**			**VGS-HJ-STFET**		
	(-)ve ITC	**No ITC**	**(+)ve ITC**	**(-)ve ITC**	**No ITC**	**(+)ve ITC**
I_{on} (A/μm)	$1.76x10^{-5}$	$1.78x10^{-5}$	$1.79x10^{-5}$	$8.05x10^{-6}$	$9.01x10^{-6}$	$1.12x10^{-5}$
I_{off} (A/μm)	$2.52x10^{-16}$	$2.51x10^{-16}$	$7.41x10^{-15}$	$1.71x10^{-16}$	$1.30x10^{-16}$	$4.41x10^{-16}$
SS (mV/dec)	22	20	18	43	39.9	38.1
I_{on}/I_{off}	$6.98x10^{10}$	$7.09x10^{10}$	$2.42x10^{9}$	$4.70x10^{10}$	$6.93x10^{10}$	$2.54x10^{10}$
V_{th} (V)	0.3	0.28	0.26	0.56	0.49.5	0.40
$[g_m (\mu S)]_{max}$	48	49	50	23.4	24.9	27.3
$[g_m/I_d (KV^{-1})]_{max}$	2.53	3.25	3.25	1.031	0.8	1.25

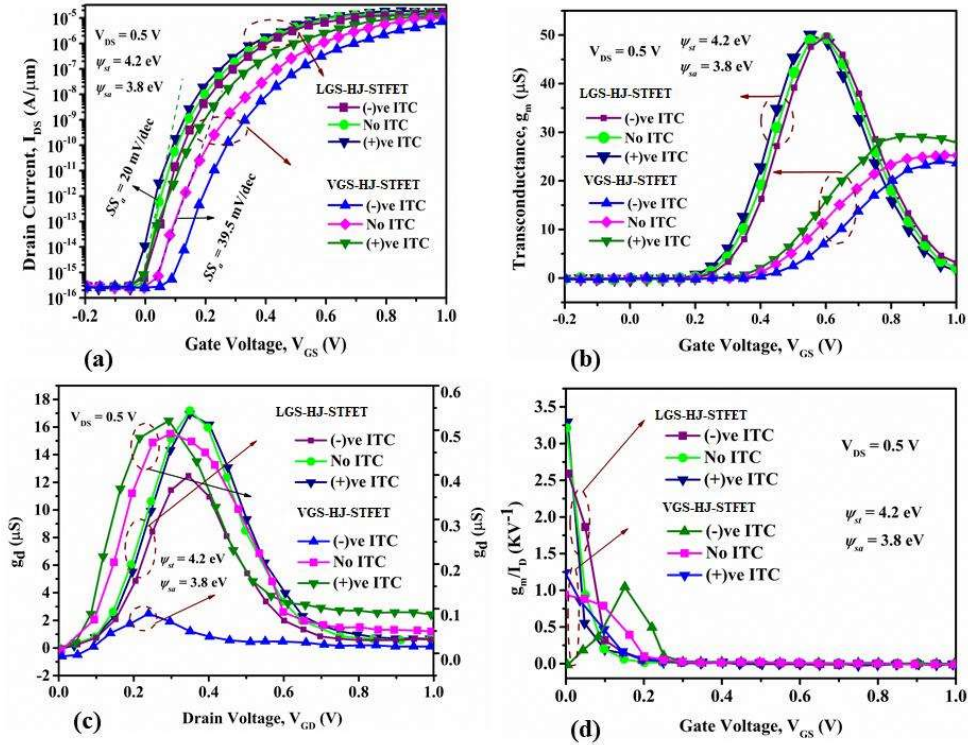


Figure 3.6 Plots of **(a)** drain current, **(b)** transconductance, **(c)** output conductance, and **(d)** transconductance generation factor (TGF) with respect to V_{GS} of LGS-HJ-STFET and VGS-HJ-STFET at V_{DS} = 0.5 V.

3.3.2 Analog/RF Performance Analysis

RF analysis plays an important role in analyzing device performance at the circuit level. Some parameters such as gate-drain capacitances (C_{gd}) are used to predict the charge conduction mechanism and the cut-off frequency of AC-current gain (f_T) which is defined as the frequency at which current gain is unity is considered the key parameters to investigate RF/analog performances [181]. In Figure 3.8 (a) we have observed that the LGS-HJ-STFET is showing a higher value of Cgd than that of VGS-HJ-STFET in all cases, such as negative, positive, and neutral interface trap charges present in the gate oxide. Fig 3.8 (b) shows the plots of cut-off frequency ($f_T = \frac{g_m}{2\pi C_{gg}}$). The proposed device is showing a higher peak value of f_T (13 GHz) as compared to VGS-HJ-STFET. Further, we have analyzed the effects of oxide interface trap charges (ITC) on cut-off frequency

[182].

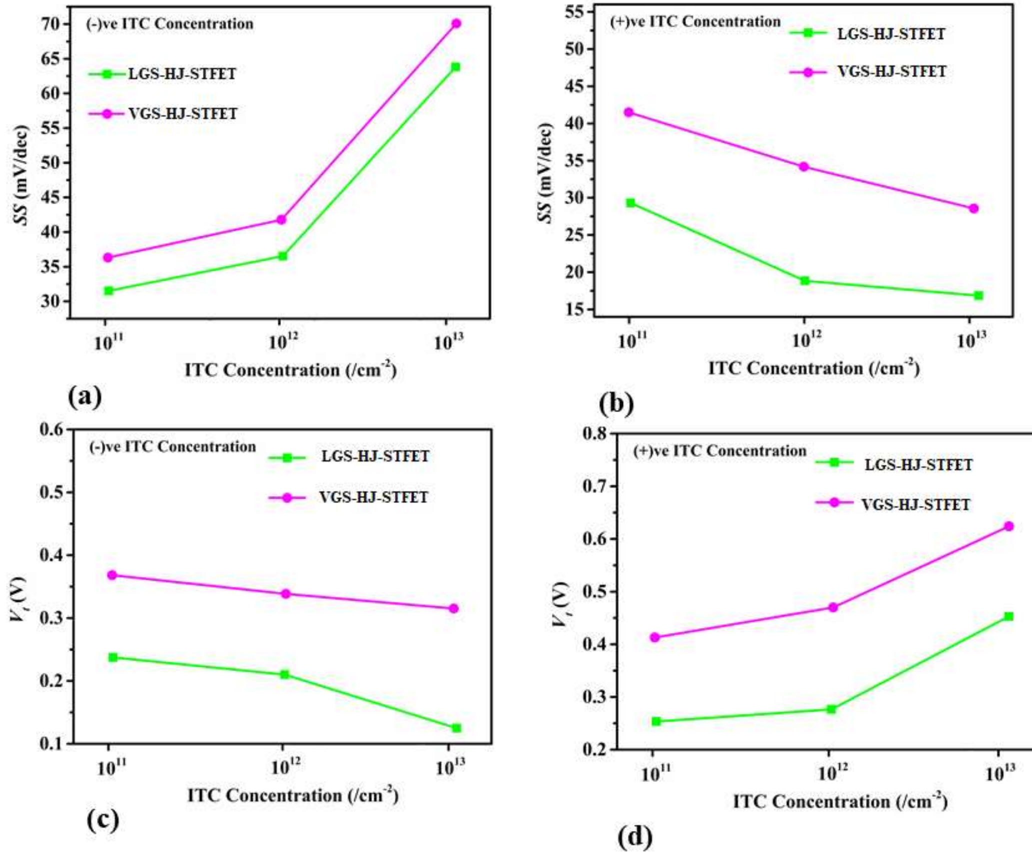


Figure 3.7 Variation of (a) *SS* for (-) ve ITC concentration, (b) *SS* for (-) ve ITC concentration, (c) V_{th} for (-) ve ITC concentration and (d) V_{th} for (+) ve ITC concentration of LGS-HJ-STFET and VGS-HJ-STFET, respectively.

The f_T of studied LGS-HJ-STFET is showing less variation in presence of interface trap charges due to the presence of high-k dielectric towards the source side as compared to VS-STFET structure. The transit time of the carriers is defined as; $t = \frac{1}{2\pi f_T}$. For the subthreshold reason, the transit time is maximum for both TFETs presented for the study whereas transit time starts decreasing with an increase in V_{GS} [181]. The presence of positive interface trap charges (ITCs) shows lower transit time over the full range of V_{GS} for both TFETs as shown in Figure 3. 8 (c). Gain bandwidth product (GBP) is also an important analog parameter which is expressed as, $GBP = \frac{g_m}{20\pi C_{gd}}$ [181] where g_m is

transconductance and C_{gd} is the gate to drain capacitance. Figure 3.8 (d) shows the plots of GBP of the aforementioned devices. It clearly shows that due to the donor (positive) trap charges, the GBP increases because of an increase in BTBT whereas acceptor (negative) trap charges reduce BTBT for which GBP decreases for both the devices presented for the study [182]. LGS-HJ-STFET shows an insignificant variation of GBP with ITC as compared to VGS-HJ-STFET as shown in Figure 3.8 (d).

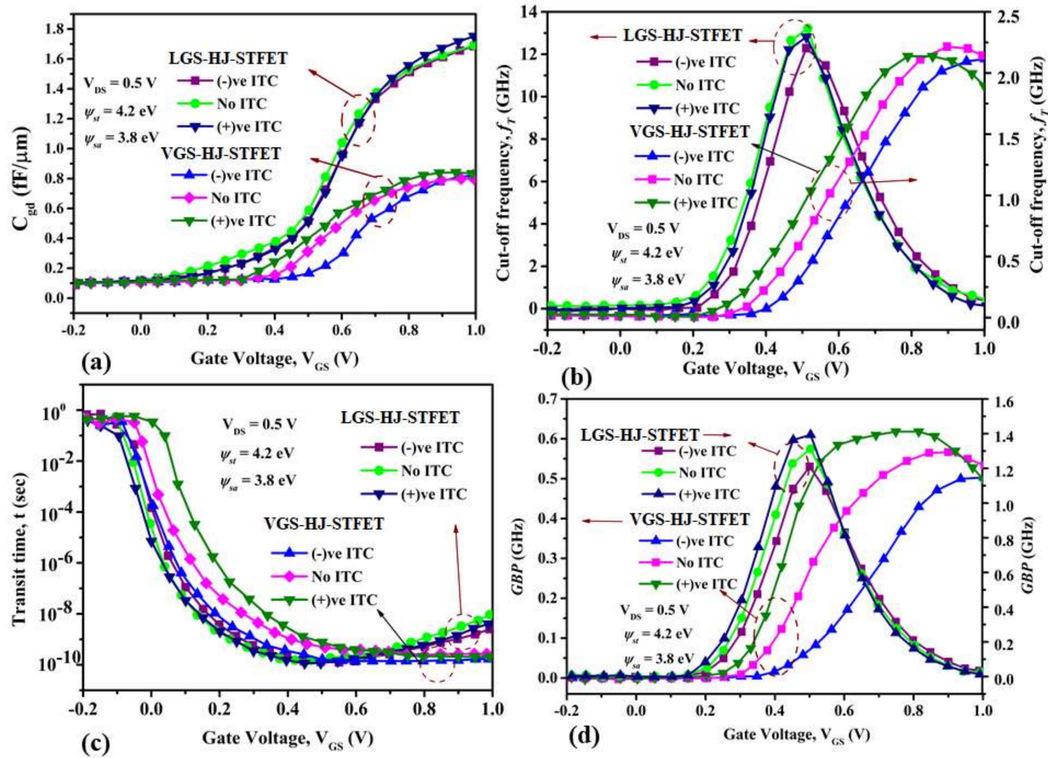


Figure 3.8 Variation of (a) C_{gd}, (b) cut-off frequency (f_T), (c) transit time (t), and (d) gain-bandwidth product (*GBP*) for various trap concentration of LGS-HJ-STFET and VGS-HJ-STFET respectively.

Table 3.3 contains the comparison of different RF parameters discussed earlier for LGS-HJ-STFET and VGS-HJ-STFET with the presence of positive, negative, and neutral interface trap charges having a concentration of $\pm 1\text{x}10^{12}/\text{cm}^2$. The proposed LGS-HJ-STFET in presence of positive trap charges (donor) is showing good analog/RF performances as compared to negative and neutral trap charges. Similarly, VGS-HJ-STFET is shown to have the same trend as LGS-HJ-STFET in the presence of different

trap charges but the overall performance of the proposed LGS-HJ-STFET is found to have better analog/RF performance compared to VGS-HJ-STFET.

Table 3.3 Comparative table of analog/RF parameters between LGS-HJ-STFET and VGS-HJ-STFET for negative, positive, and neutral interface trap charges (ITCs) with $\pm 1 \times 10^{12}/cm^2$ concentration value.

Parameters	**LGS-HJ-STFET**			**VGS-HJ-STFET**		
	(-)ve ITC	**No ITC**	**(+)ve ITC**	**(-)ve ITC**	**No ITC**	**(+)ve ITC**
$[C_{gd}$ (fF/μm)$]_{max}$	1.704	1.69	1.755	0.744	0.773	0.800
$[f_T$ (GHz)$]_{max}$	12.5	13	12.9	2.2	2.25	2.23
t_{min} (psec)	0.188	0.188	0.163	0.350	0.360	0.354
Peak GBP (GHz)	1.24	1.31	1.27	0.61	0.532	0.510

3.3.3 Linearity Performance Analysis

For distortionless performance, the linearity performance of the device should be as good as possible. The linearity performance can be investigated in terms of g_{m2}, g_{m3}, VIP2, VIP3, IIP3, IMD3, and 1-dB compression point [183]. The mathematical formulation of all these parameters is given below in (3.1)-(3.5),

$$VIP2 = 4 \times \left(\frac{g_m}{g_{m2}} \right) \tag{3.1}$$

$$VIP3 = \sqrt{24 \times \left(\frac{g_m}{g_{m3}} \right)} \tag{3.2}$$

$$IIP3 = \frac{2}{3} \times \left(\frac{g_m}{g_{m3} \times R_s} \right) \tag{3.3}$$

$$IMD3 = \left[\frac{9}{2} \times (VIP3)^3 \times g_{m3} \right]^2 \times R_S \tag{3.4}$$

$$1 - dBCompressionPoint = 0.22\sqrt{\frac{g_m}{g_{m3}}} \tag{3.5}$$

where $R_s = 50\ \Omega$ [183]

It is required to have a higher value of g_{m3} at lower V_{GS} to have better linearity performance. In Figure 3.9 (a), the peak of gm3 in the proposed structure (LGS-HJ-STFET) attains higher amplitude as compared to VGS-HJ-STFET and its peak occurs at lower V_{GS}. The zero-crossover point (ZCP) can be calculated from g_{m3} plots. The gate voltage at which g_{m3} attempts the first zero value is known as the zero crossover point, and it should be as low as possible to have better linearity because it indicates the biasing behavior of the device. Figure 3.9 (b) shows the bar plots of zero crossover point (ZCP) for both the TFETs presented for study in presence of different ITC (positive, negative, and neutral). The parameter VIP3 is otherwise called significant linearity figure-of-merits which gives data about the distortion qualities. The parameters VIP3 ought to be sufficiently high to accomplish higher linearity and distortion less behavior [183]. VIP3 is the generalized input voltage point where the 1st and 3rd harmonic voltages should be the same. Figure 3.10 (a) shows the effect of ITCs on VIP3 at V_{gs} = 1.0 V for LGS-HJ-STFET and VGS-HJ-STFET. From Figure 3.10 (a), the amplitude of VIP3 is higher for LGS-HJ-STFET in comparison with VGS-HJ-STFET, which means that dual-material having lateral stacking of gate gives high linearity and low distortion when contrasted with VGS-HJ-STFET. Additionally, the height of VIP3 shifts at lower gate voltage, and also peak value increases (decreases) with the presence of ITCs. Other important parameters which test the linearity are IIP3 and IMD3. IIP3 is a linearity parameter which means the third-order intercept input power ought to be as high as conceivable to have less distortion while IMD3 signifies the third-order intermodulation distortion which must be of low plentifulness to accomplish better linearity qualities. Figure 3.10 (b) and

figure 3.10 (c) denotes the variation of IIP3 and IMD3 at V_{gs} = 1.0 V considering the effect of ITCs. In the proposed LGS-HJ-STFET, better IIP3 and IMD3 are achieved than in VGS-HJ-STFET. The 1-dB compression point is another fundamental reason to quantify the higher limit of linearity activity. Figure 3.10 (d) shows the variation of the 1-dB compression point of both TFETs under study for negative, positive, and neutral interface trap charges (ITCs). It is mentioned as an information power level at which output power moves from linearity by 1-dB. All the linearity parameters for LGS-HJ-STFET are showing less variation with dielectric interface trap charges (ITC_s) as compared to VGS-HJ-STFET, so the proposed structure (LGS-HJ-STFET) is more reliable in presence of dielectric interface trap charges as compared to VGS-HJ-STFET.

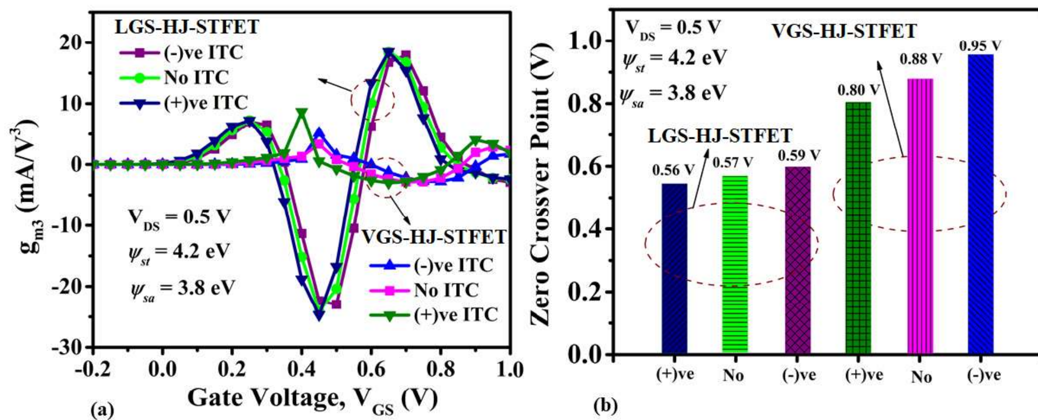
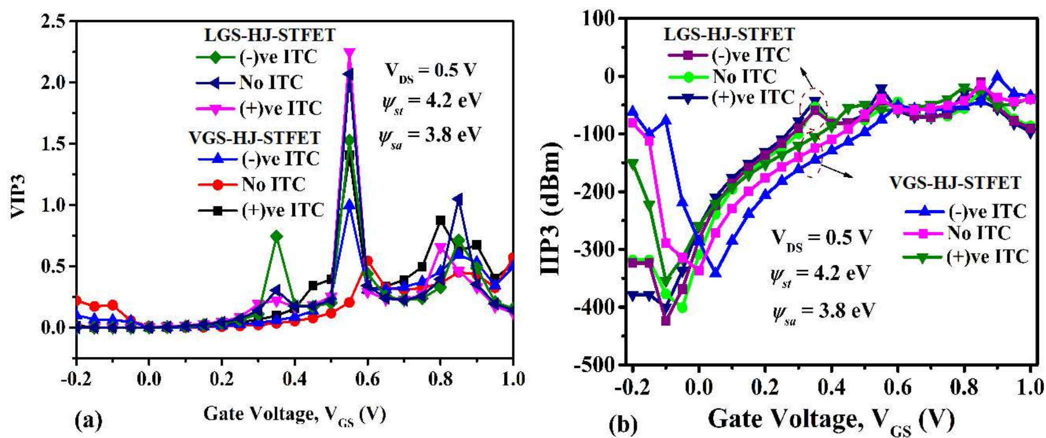


Figure 3.9 Plots of (a) g_{m3} and (b) zero crossover point (ZCP) of both TFETs at V_{DS} = 0.5V.



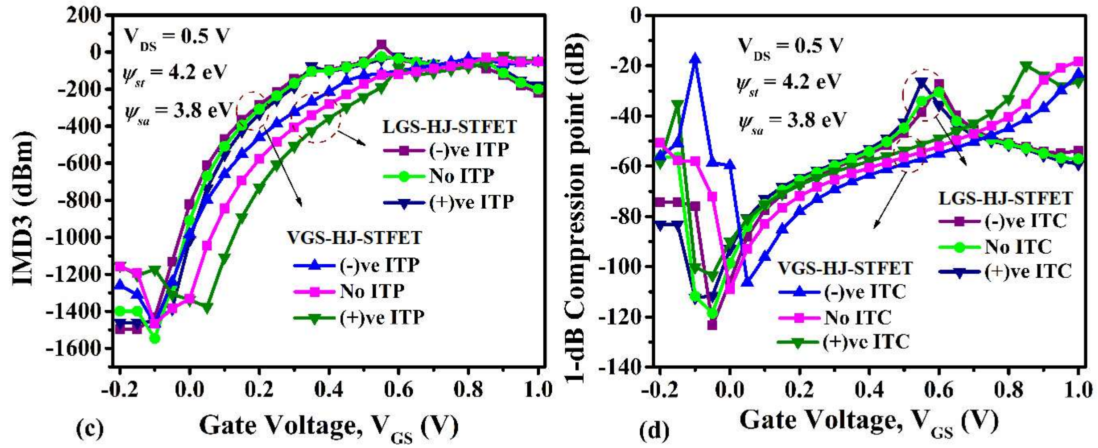


Figure 3.10 Comparative Plots of (a) *VIP3*, (b) *IIP3* (c) *IMD3*, and (d) 1-dB compression point vs. V_{GS} of both TFETs.

3.4 Conclusion

In this chapter, we have investigated the influence of both the donor and acceptor type interface trap charges (ITCs) on the reliability of LGS-HJ-STFET and VGS-HJ-STFET in terms of their DC, analog/RF, and linearity parameters. Better improvements in DC, analog/RF, and linearity characteristics are observed in the LGS-HJ-STFET structure than those of the VGS-HJ-STFET device, because only HfO_2 is used below the tunneling gate, which provides lower physical length of the gate oxide as compared to gate oxide physical length of VGS-HJ-STFET. The presence of ITCs causes more effects on the performance degradation of VGS-HJ-STFET than the LGS-HJ-STFET structure, but the fabrication steps of LGS-HJ-STFET is more complex than VGS-HJ-STFET. Another point to note is that we employed dual metal in this study, which improves performance but adds fabrication complexity, which is why we are not addressing dual metal gates in the next chapters. Therefore, the VGS-HJ-STFET device structure will be employed in the next chapters of this thesis.