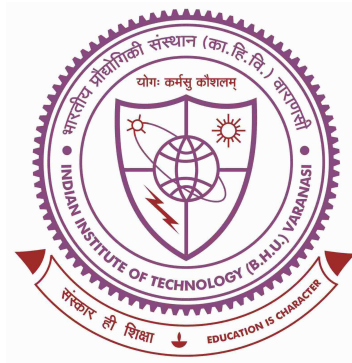


Switched LC based High Voltage Gain Power Electronic Interfaces for Low Voltage DC Sources



Thesis submitted in partial fulfillment
for the award of degree

Doctor of Philosophy

by

Aakash Singh

DEPARTMENT OF ELECTRICAL ENGINEERING
Indian Institute of Technology
(Banaras Hindu University)
Varanasi

Roll No: 18081004

2023

List of Tables

1.1	Salient features of impedance source topologies	14
1.2	Boosting techniques in DC–DC converters	16
2.1	Voltage stress across devices	26
2.2	Comparative analysis of Z-source converters	26
2.3	Device and components used in experiment	30
2.4	Specification and parameter of the proposed converter-1	30
3.1	Voltage stress across devices	40
3.2	Current stress of devices	40
3.3	Proposed converter-2 specification	44
3.4	Device and components used in experiment	45
3.5	Proposed qZS converter for hybrid operation	53
3.6	Comparison of proposed converter-2 with existing topologies	56
4.1	Comparison of proposed converter-4 with existing topologies.	69
4.2	Specification and Parameter of proposed Converter-4	75
4.3	Device and components used in experiment	75
4.4	Specification of interleaved converter	87
5.1	Current stress of capacitor and diodes	100
5.2	Voltage stress across diodes and switches CCM operation	100
5.3	Comparison of proposed converter-5 with existing topologies	103
5.4	Specification and parameter of converter	105
5.5	Device and components used in experimental setup	105

List of Figures

1.1	Typical struture for DC nanogrid and application of DC-DC converter.	2
1.2	Classification of voltage boosting techniques.	4
1.3	Self-lift cell structure.	4
1.4	Basic SL cell.	5
1.5	Voltage multiplier cell.	6
1.6	Voltage multiplier cell with inductor and capacitor.	6
1.7	Basic charge pump circuit.	7
1.8	SC based network.	7
1.9	Cascade network.	8
1.10	SC voltage multiplier.	9
1.11	Coupled inductor based network.	10
1.12	Boost converter with VSI.	11
1.13	General structure of Z-source converter [31].	12
1.14	Quasi-Z source converter.	12
1.15	Trans-quasi-Z source converter [33].	12
1.16	Active switched capacitor/ SL qZS converter [44].	14
1.17	Diode assisted Z-source converter.	15
1.18	Capacitor assisted Z-source converter.	15
1.19	Embedded Z-source converter	15
1.20	SL/Improved Quasi Z-source converter.	15
1.21	(a) Switched boost network (b) SC-Quasi switched boost converter. . .	15
1.22	Impedance source topologies and its classification.	15
2.1	Quasi Z-source converter with discontinuous input current [48].	20
2.2	Proposed version-1 Z-source DC-DC converter.	20

2.3	Proposed (version-2) Z-source high gain converter-1.	21
2.4	Steady state waveforms of proposed converter-1 during CCM.	21
2.5	Operating Mode 1.	22
2.6	Operating Mode 2.	22
2.7	Converter in reference [47].	27
2.8	Converter in reference [51].	27
2.9	Converter in reference [49].	27
2.10	Converter in reference [36].	27
2.11	Converter in reference [50].	27
2.12	Proposed converter-1.	27
2.13	Voltage gain comparison of existing Z-source converters.	27
2.14	Switch stress variation with respect to duty cycle.	28
2.15	Analytical voltage gain plot with different load condition.	28
2.16	Photograph of proposed Z-source converter.	31
2.17	Measured Input-output volatge and current.	31
2.18	Zoomed inductor current and switch stress.	31
2.19	Measured voltage stress across D_1 , D_2 and D_5	32
2.20	Measured voltage across C_2 , C_3 , C_4 and C_5	32
3.1	Typical structure of qZS DC-DC converter.	34
3.2	Diode assisted extented boost qZS DC-DC converter [48].	35
3.3	Active switched boost qZS DC-DC converter [56].	35
3.4	Active switched qZS high gain proposed converter-2.	35
3.5	ON mode equivalent circuit.	36
3.6	OFF mode equivalent circuit.	36
3.7	Bode plot without controller.	41
3.8	Bode Plot with PI controller.	43
3.9	Measured input-output voltage and load current of proposed converter.	45
3.10	Measured source current $i_{in} = i_{L1}$ and inductor L_2 current waveforms.	46
3.11	Measured voltage stress of both switch with gating pulse.	46
3.12	Measured voltage stress across diodes D_1 , D_2 and D_3	46
3.13	Measured voltage stress across diode D_4 and D_0	47
3.14	Measured mean value of voltage across capacitors.	47

3.15	Closed loop response to increase in I_0	48
3.16	Closed loop response to decrease in I_0	48
3.17	Closed loop response to increase in V_{in}	48
3.18	Closed loop response to decrease in V_{in}	48
3.19	Proposed converter-2 for hybrid load.	49
3.20	Shoot through state equivalent circuit.	49
3.21	Active state equivalent circuit.	50
3.22	DC output and DC link voltage during hybrid operation.	52
3.23	Three phase AC output voltage during hybrid operation.	52
3.24	Experimental setup for qZS converter for hybrid operation	54
3.25	Measured inductors current and DC link V_P voltage.	54
3.26	Measured DC voltage and AC voltage during hybrid operation.	54
3.27	Boost factor comparison.	57
3.28	Overall gain considering inverter extension.	57
4.1	ASL based derived converter version-1 [10].	60
4.2	ASL based derived converter version-2 [10].	60
4.3	ASL derived proposed converter-3.	61
4.4	ON state operation of ASL based Converter.	62
4.5	OFF state operation of ASL based converter.	62
4.6	ASL based proposed converter-4.	63
4.7	Operating CCM waveform.	63
4.8	ON time equivalent circuit diagram.	64
4.9	OFF time equivalent circuit diagram.	65
4.10	Operating waveform during DCM condition.	66
4.11	Boundary condition CCM/DCM.	67
4.12	Boost factor of existing non-isolated converters with wide duty operation.	70
4.13	Normalized switch stress.	70
4.14	Bode plot of converter with and without controller.	72
4.15	Experimental setup for proposed converter-4	76
4.16	Measured steady state input-output voltage and current $V_{in} = 22 V$	76
4.17	Measured steady state input-output voltage and current $V_{in} = 24 V$	76
4.18	Zoomed inductor current of when $V_0 = 180 V$	77

4.19	Zoomed inductor profile of ASL network for $V_0 = 200 V$	77
4.20	Voltage stress across diodes for $V_0 = 180 V$	77
4.21	Voltage stress across diodes for $V_0 = 200 V$	77
4.22	Switch and output diode stress for $V_0 = 180 V$	77
4.23	Switch and output diode stress for $V_0 = 200 V$	77
4.24	Measured mean value across capacitors when $V_0 = 180 V$	78
4.25	Mean value across capacitor $V_0 = 200 V$	78
4.26	Measured dynamic response with load current variation.	78
4.27	Measured dynamic response with source voltage variation.	78
4.28	Voltage tracking performance with given reference voltage V_{0ref} . point .	79
4.29	Distribution of power loss for the proposed converter at a 200 W load	80
4.30	Experimental efficiency vs output power.	81
4.31	Proposed converter-4 with parasitic capacitance to achieve ZVS.	82
4.32	At Boundary condition of CCM/DCM [69].	82
4.33	Operating in DCM to achieve ZVS [69].	82
4.34	Proposed ASL converter with discontinuous inductor current.	82
4.35	Proposed converter with parasitic capacitance to achieve ZVS.	83
4.36	Proposed interleaved high gain converter.	84
4.37	Switching pattern and waveform of two phase interleaved converter. . .	84
4.38	State-1 switches S_1, S_2 ON.	85
4.39	State-2 switches S_1 OFF, S_2 ON.	85
4.40	State-3 switches S_1 ON, S_2 OFF.	86
4.41	Measured input-output waveform of interleaved converter.	87
4.42	Measured value of inductor current with gate signal.	88
4.43	Measured value of switch stress and output voltage.	88
4.44	Turn ON ZVS for both switches.	89
4.45	Input current and inductor current waveform during ZVS.	89
4.46	Input-output voltage and switch voltage in ZVS operation.	90
4.47	Measured inductor and input current waveform during ZVS.	90
4.48	Loss distribution of plot without ZVS and with ZVS.	91
5.1	Flexible high gain proposed converter-5.	94
5.2	Operating waveform during CCM.	95

5.3	Mode 1 equivalent circuit.	95
5.4	Mode 2 equivalent circuit.	96
5.5	Mode 3 equivalent circuit.	96
5.6	Voltage gain of converter in CCM with variation of D_1 and D_2	97
5.7	Steady state waveform during DCM.	98
5.8	Proposed converter-5 boundary condition.	99
5.9	Comparison of voltage gain of various converter for $D_2 = 0.25$	102
5.10	Zoomed plot of voltage gain.	102
5.11	Normalized switch stress across S_3	102
5.12	Voltage and current stress of switch.	104
5.13	Photograph of the proposed converter-5.	106
5.14	Measured steady state input-output waveform.	106
5.15	Measured inductor current profile for proposed converter	106
5.16	Switch stress of main switch S_1 and S_2	107
5.17	Voltage stress across diodes D_1 , D_2 and D_3	107
5.18	Voltage stress across output diode D_4 and auxiliary switch S_3	107
5.19	Voltage stress across capacitors C_1 and C_2	108
5.20	Power loss distribution for proposed converter at 400 W.	110
5.21	Comparison of theoretical and measured efficiency.	111

To
The Supreme Radha Swami
and
My beloved family

DECLARATION

I, **Aakash Singh**, certify that the work embodied in this thesis is my own bonafide work and carried out by me under the supervision of **Dr. Santosh Kumar Singh** from July-2018 to November-2023, at the Department of Electrical Engineering, Indian Institute of Technology (BHU), Varanasi. The matter embodied in this thesis has not been submitted for the award of any other degree/diploma. I declare that I have faithfully acknowledged and given credits to the researchers wherever their works have been cited in this thesis. I further declare that I have not willfully copied any other's work, paragraphs, text, data, results, etc., reported in journals, books, magazines, reports, dissertations, theses, etc., or available at websites and have not included them in this thesis and have not cited as my own work.

Date: 5-Jun-2024

Place: Varanasi



(Aakash Singh)

CERTIFICATE BY THE SUPERVISOR

It is certified that the above statement made by the student is correct to the best of my/our knowledge.



Dr. Santosh Kumar Singh

IIT(BHU), Varanasi


5/6/24

Signature of Head of Department/Coordinator of School

आचार्य व विभागाध्यक्ष / PROFESSOR & HEAD
विद्युतीय अभियंता विभाग / Department of Electrical Engineering
भारतीय प्रौद्योगिकी संस्थान / Indian Institute of Technology
(काशी हिन्दू विश्वविद्यालय) / (Banarus Hindu University)
varanasi, U.P. (INDIA)

COPYRIGHT TRANSFER CERTIFICATE

Title of the Thesis: **Switched LC based High Voltage
Electronic Interfaces for Low Voltage DC Sources**

Name of Student: **Aakash Singh**

Copyright Transfer

The undersigned hereby assigns to the Indian Institute of Technology (Banaras Hindu University) Varanasi all rights under copyright that may exist for the above thesis submitted for the award of the Doctor of Philosophy.

Date: *5-Jun-2024*

Place: *Varanasi*

Aakash Singh
(Aakash Singh)

Note: However, the author may reproduce or authorize others to reproduce material extracted verbatim from the thesis or derivative of the thesis for author's personal use provided that the source and the Institute's copyright notice are indicated.

Acknowledgments

Though, only my name appears on the cover of this dissertation, so many great people have contributed to its production. I owe my gratitude to all those people who have made this thesis possible and because of whom my post graduate experience has been one that I will cherish forever.

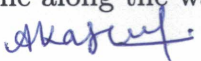
With sincere appreciation, I take this opportunity to express my profound gratitude and deep regards to my Supervisor Dr. Santosh Kumar Singh, Professor, Electrical Engineering Department IIT(BHU), Varanasi for his exemplary guidance, monitoring and constant encouragement throughout the course of this dissertation.

I am obliged to faculty members, in particular Dr. N. K. Swami Naidu, Dr. Shyam Kamal, and staff members, in particular Mr. Dharmendra, Mr. Patel, Mr. R.C. Sharma and Mr. B. L. Singh, of Electrical Engineering Department, IIT(BHU), Varanasi. In addition, I want to express my deepest gratitude to Dr. Avneet Kumar who supported me throughout my thesis work. I am grateful to Dr. M. Raghuram, Dr. Motiur Reza, Dr. Kumar Abhishek and Dr. Mukesh Kumar who provided me technical, moral and emotional support during my research program.

A very special gratitude goes out to my colleagues and friends with special mention to Mr. Vulavakayala Siva, Mr. Vikram Singh, Mr. Ashish Prajapati, Mr. Sunil Patel and Mr. Batta Sivaprasad.

Last but not the least, I thank specially to my parents, Mr. Akshyvur Singh and Mrs. Shyam Pyari, my wife Mrs. Ritu Singh, my sister Dr. Anuradha Singh, and my brothers, Mr. Amit Yadav, Mr. Prashant K Singh for their constant support and encouragement, without which this assignment would have not been completed at all. I am grateful to my other family members who have supported me along the way.

Date: 5-Jun-2024


Aakash Singh

Abstract

Power electronic converters have experienced a surge in popularity due to their ability to meet the expanding demands of industrial applications. Power electronics applications require either a DC supply or an AC supply for operation. Among the power electronics converters, DC-DC converters occupy a significant portion of the power handling scale. The current focus is on enhancing energy efficiency and integration of renewable energy sources with step-up converters. Broadly, DC-DC converters with high voltage gain act as front-end converters for driving various loads. High-intensity discharge lamps (HID) for automobiles, network servers, data centers, and fuel cell electric vehicles are a few of the applications of high-voltage gain converters.

This thesis proposes high-voltage gain converters to meet the requirements of DC loads. Two categories of power converters are demonstrated in this thesis based on the duty cycle operation. This thesis enhances the performance of high-gain DC-DC converters by integrating voltage-boosting techniques with unique structural arrangements at the input side. The first contribution of the thesis is achieving a high voltage conversion ratio through low-duty cycle operation while minimizing voltage stress on both the switches and diodes. Initially, the thesis demonstrates the high-gain DC-DC converters based on impedance source networks to power DC loads. Within this category, a quasi-impedance source-based converter is presented, which can also supply both DC and AC loads as a hybrid converter. These converters offer higher voltage gains compared to contemporary alternatives. The low-duty operation of these converters reduces the conduction losses caused by switches, diodes, and the internal resistance of passive components. Performance improvements include reduced voltage stress, reduced costs, and improved efficiency.

The second contribution of this thesis involves arranging converters in a manner that allows for achieving a high voltage conversion ratio with low current stress

through the inductors. Additionally, wide-duty operation-based converters are proposed. However, impedance source converters require larger-rated inductors to achieve the same output power, resulting in bulkier sizes. In this type of network, only active switches participate in charging the inductor without the need for an additional switch. The input current is equally divided into ASL networks, and inductors carry an equal amount of current for the entire duty cycle range ($0 < D < 1$). The key features of the ASL network are low switch current and low voltage across it (one-fourth of output voltage). Furthermore, an interleaved converter is proposed with a similar gain to achieve soft switched-based zero voltage switching (ZVS) without using additional components. The third contribution of this thesis introduces a modified ASL network with the shared ground to minimize low electromagnetic interference (EMI) and achieve flexible higher gain through a combination of two duty cycles.

Finally, a closed-loop PI controller controls the proposed converters for voltage regulation. Analyzing the operation of these converters involved detailed and comprehensive analytical derivations and simulation studies. Moreover, the performance of the proposed converters was evaluated against that of previously reported converters. Experimental validation of the converters' operation was conducted using laboratory prototypes. These proposed converters present a promising alternative to existing converter options in residential and industrial applications requiring higher DC voltages.