CHAPTER-3

SHJ solar cells on adequately thin (~30 μm) c-Si wafer with a unique dome-like front and a double layer of ITO nanoparticles as backlight trapping arrangements

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3.1. Introduction

Even though there are multiple thin and cost-effective solar cells developed worldwide [160-167] in the last few decades, crystalline silicon (c-Si) based solar cells are still leading the solar photovoltaics (SPV) market due to their high conversion efficiency, robustness, reliability, and natural abundance of raw materials [168]. Since the first invention of the silicon solar cells [169]; silicon technology has progressed a lot by the improvement of material quality of silicon [170,171], shallow junction formation [172,173], introduction of back surface field (BSF) [174-175], light trapping by surface texturization [176-177], anti-reflection coating [178-179], and surface passivation [180-184]. Now, the technology is very close to the efficiency limit of c-Si solar photovoltaic technology [185]. Recently, several research groups have reported different types of c-Si-based solar cells [186-193] with high efficiency, among them; heterojunction solar cells are known to have the highest performance capabilities compared to others due to their excellent passivation, low temperature (<200°C) processability with better temperature coefficient than conventional c-Si solar cells [194-195]. With this heterojunction technology, researchers are constantly approaching the theoretical photo-conversion limit of ~29% as predicted by Shockley and Queisser for c-Si based solar cell [185,195] and hopefully, it will be reached by the year 2030. Even after such advancements in solar PV technology, the cost of solar power is higher than that of conventional power sources like thermal and nuclear. Generally, about 30-40% of the total cost for the c-Si based solar modules is due to the cost of the bulk Si material [196]. So, it is necessary to enhance the conversion efficiency of the cell, as well as to reduce the fabrication cost to make SPV more popular. One of the most effective ways for reducing the cost of a c-Si based module is to cut down the material cost by lowering the thickness of the active c-

Si layer. It has been estimated that a ~50 µm thick wafer has the potential to minimize the module cost by 28% [197] without compromising cell efficiency. According to the recommendations made by the international technology roadmap for photovoltaics (ITRPV) in 2019, 'thinning' of silicon-based solar cells to 110 µm is crucial to achieve cost-effectiveness of the modules within the year 2029.

As far as the silicon heterojunction (SHJ) solar cells are concerned, *Sanyo* reported 22.8% efficiency on a 100 µm wafer [198] and 24.7% efficiency on a 98µm thick wafer [199]. Very recently *Sai* and *Matsui* [200] have achieved 22% efficiency on ~50 and ~46 µm thin wafer using SHJ structure. It was stated that the parasitic absorption at a longer wavelength is a function of wafer thickness and fill factor is also sensitive to surface recombination, which varies with the wafer thickness [201]. Later, *Balaji et.al*.demonstrated ~22.48% efficiency for a ~40 µm thick silicon wafer by optimizing the i-a-Si:H layer by varying the compositional ratio of silane to hydrogen gas [202]. These works were performed on wafers with notably high carrier lifetime ~2 ms. On the other hand, *Dikshit* et. al.have successfully fabricated 12.25% efficient single-junction solar cells on ~30 µm c-Si wafer with a lifetime of 100 µs [203]. However, cutting down the absorber layer thickness up to specificlevel results in less photocarrier generation and lowered short circuit current density (J_{SC}) as the thinner c-Si substrate is relativelytransparent to the incident light having longer wavelengths, mainly in the near-infrared (NIR) region [204]. For this reason, well-suited front scattering and back reflection arrangements are essential to fabricate a solar cell (either with SHJ structure or single junction) with notably suitable cell parameters.

This work includes the fabrication of SHJ solar cells on ~30 µm thick n-type c-Si wafers as a pilot scheme to go inline with ITRPV-2019 recommendations regarding using a thinner active layer. As this ~30 µm wafer is quite transparent to incident light with

wavelengths >700 nm, proper light trapping tricks like the use of dome-shaped front scatterer and properly positioned indium tin oxide (ITO) nanoparticle (NP) array as back reflector layers (BRLs) were introduced. The dome-shaped front textured surface also helps to improve the shunt resistance, open-circuit voltage (V_{oc}), and fill factor of the cell. To the best of our knowledge, there is no previous reference on the fabrication of such thin (~30 μm) SHJ cells with this kind of front and back-light trapping arrangement.

3.2. Experimental Details

The conventional baseline fabrication procedure for SHJ solar cells has been modified and optimized to make thin SHJ cells on ~30 μm wafers in this case. For the fabrication of SHJ solar cells, 3”×3”, 180 μm thick n-type monocrystalline <100> Si wafer (CZ) commercially available having carrier lifetime ~100 μs were taken and scaled down to ~30 μm following the procedure as mentioned elsewhere [203]. In brief, the wafers were mounted vertically in a borosilicate beaker containing 10% NaOH solution at a temperature of 85°C. After 55 minutes the wafers were removed and washed thoroughly with de-ionized cold water. This yielded wafers with ~30 μm thickness. These wafers were cut into 18 mm×18 mmpieces using Nd:YAG laser (λ = 1064 nm, Argus, China) to fabricate the cells. Before texturization, one side of such wafers was blocked using silicon nitride (SiN_X) coating with the help of a plasma-enhanced chemical vapor deposition (PECVD) cluster tool (Hind High Vacuum) under 1 torr pressure, 400°C process temperature, and30-watt RFpower for 10 minutes with a gas flow (sccm) ratio of 45:45:65 for NH_3:H_2:SiH_4.This restricts texturization of the wafer on the SiN_X coated side. Texturization was done by placing such a wafer vertically in a bath containing a mixture of 2% aqueous KOH solution and 5% isopropyl alcohol (IPA) preheated at 80°C. The wafer was removed from the solution after 40 minutes, washed thoroughly with normal isopropyl alcohol, and dried using compressed nitrogen flow. This yielded

pyramidal shapes on the SiN_X uncoated (front) surface and removal of the nitride coating followed by the generation of some undulations on the other (back) surface. These wafers were divided into two sets. Back side polishing of a set of such wafers was carried out using an indigenous single side etcher with the help of a 20% KOH solution so that the front side remains pyramidal. The second set was treated with HNA solution (HF: HNO_3:CH_3COOH) with a concentration ratio of 5:1:1 at ambient temperature for 4 minutes to create dome shapes out of the pyramidal structures. The HNA treatment in this case also performs backside polishing of the wafers. Cleaning of the wafers was accomplished with the help of the standard wet cleaning process of RCA-1 and RCA-2 followed by 1% HF dip and cleaning by running de-ionized water. The ITO layers and nanoparticles were deposited using RF magnetron sputtering (Hind High Vacuum) from a SnO_2 doped indium oxide (In_2O_3) target. The detailed ITO deposition procedure has been elaborated in the respective section for easy reading. The amorphous and microcrystalline silicon-based layers like p-a-SiO:H, i-a-Si:H, n-a-Si:H and n-μc-Si:H are required to fabricate the SHJ cells were deposited using a five-chamber PECVD cluster tool (Hind High Vacuum) following the recipe as mentioned in Table 3.1. The PECVD system used in this case cannot deposit amorphous layers simultaneously on both sides of the wafer without compromising the vacuum release. To deposit amorphous layers on the rear side, the wafer needs to be taken out from the PECVD system after top side coating, and has to be loaded again to carry out deposition on the other side. This may affect the surface passivation and might be the reason for not getting state-of-the-art V_{OC}. The carrier lifetime of the wafer also influences the electrical properties of the fabricated cells. It may be noted that the wafers used by *Sai et. al.* [196] and *Balaji et. al.* [197] have better carrier lifetime, however, about ten times costlier than the case reported here. The thickness of the individual layers was monitored using in-built dynamic thickness

monitor. An ITO layer with a thickness of 50 nm was placed between the silicon substrate and back contact using RF magnetron sputtering. A top ITO layer with the same thickness was also sputtered on the finished cell before taking the top Al contacts. Top and back metallic Al contacts were taken from the finished cells using thermal evaporation (Hind High Vacuum). The thickness of the back contact was 300 nm, whereas, it was 250 nm for the front contact that was taken through an E-mask. Morphological analyses of the textured surface and ITO NPs were carried out using a field emission scanning electron microscope (FESEM, Zeiss Sigma). Optical reflectance and external quantum efficiency (EQE) were investigated using a Bentham PVE-300 Series spectral response unit. The current density–voltage (J–V) characteristic was measured with the help of a Cell Tester CT-50AAA from PET, California, USA. Both reflectance and J–V characteristics were measured under AM 1.5G simulated radiation.

Table 3.1: Detailed recipe for the deposition of amorphous and microcrystalline layers

Type of layer	**SiH_4:H_2**	**B_2H_6 (sccm)**	**PH_3 (sccm)**	**CO_2 (sccm)**	**P_d (mW/cm^2)**	**P_r (torr)**	**Thickness (nm)**
p-a-SiO:H	1:25	3	NA	2.5	60	1	12
i-a-Si:H	1:6	NA	NA	NA	30	1	5
n-a-Si:H	1:5	*NA*	0.2	NA	40	1	25
n-µc-Si:H	1:50	NA	0.04	NA	35	1	20

3.3. Results and discussion

3.3.1. Fabrication of thin SHJ solar cells on 30 µm wafer

To start with, thin SHJ cells on ~30 µm wafers with two different front surface morphologies have been fabricated as per the scheme shown in Fig.3.1. The recipe as

elaborated in Section 3.2 was followed to make the cells. During the deposition of top i-a-Si:H, p-a-SiO:H, and ITO layers on the thin wafer with the pyramidal front surface, it has been observed that due to the presence of sharp spikes on the textured top, punching of these ultrathin layers occur that leads to the poor shunt of the cell. Hence, the fill factor (FF) and V_{OC} of the cell are sacrificed. Technically, conformal covering of the pyramids (with ~ 3µm height) by ultrathin amorphous layers are difficult. This could be resolved by partial etching of the pyramidal textured surface that leads to dome shaped topography. The cross-sectional FESEM image (Fig.3.2) of the textured thin c-Si wafer before and after HNA treatment are clearly showing the formation of dome shaped morphology after partial etching of the pyramidal textures. The height of such domes was found to be within 1–1.5µm. It can clearly be understood from Fig.3.2b, that rounding off of the surface will facilitate conformal deposition of the ultrathin amorphous layers on the top of the thin c-Si wafer which is essential to achieve good electrical property of the SHJ cell.

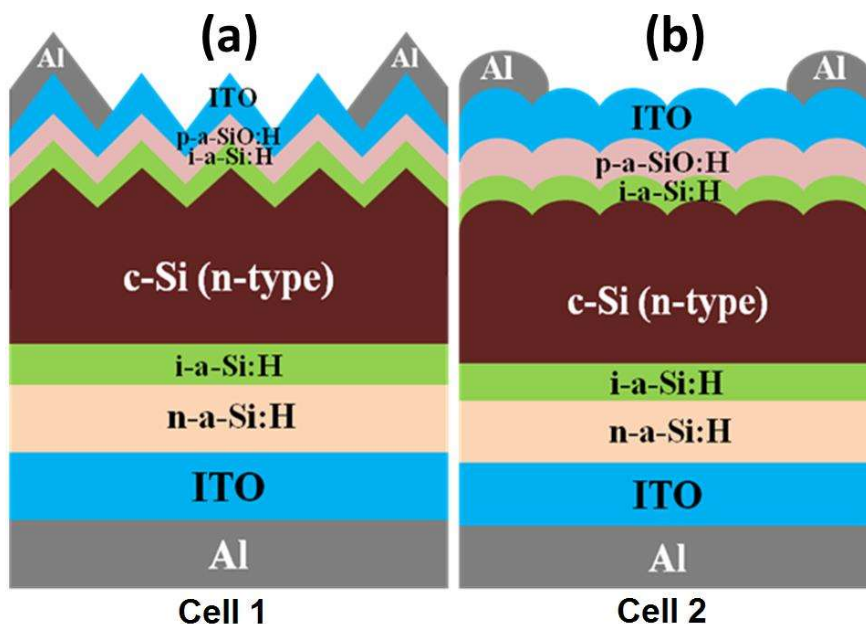

Fig.3.1: Schematic of thin (~30 µm) SHJ cells (a) with pyramidal front texture (Cell 1) and (b) with dome shaped front surface (Cell 2)

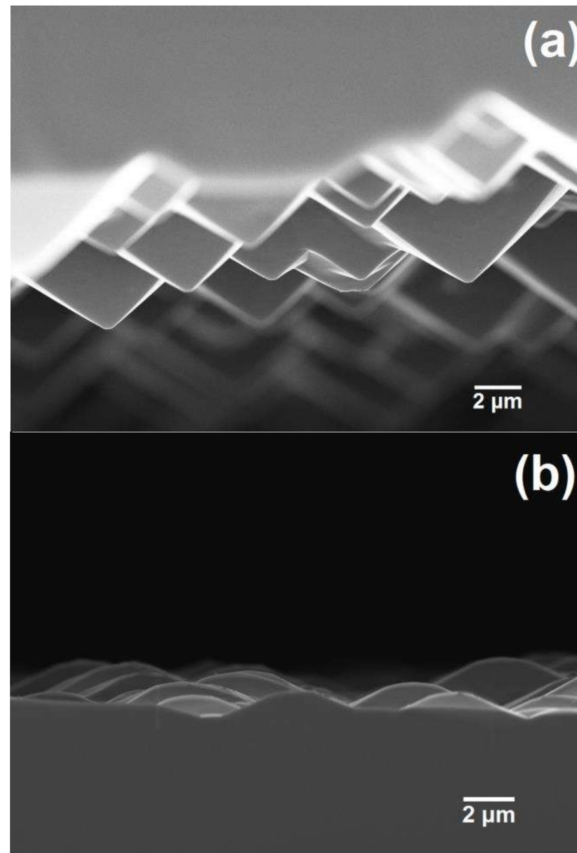

Fig.3.2: Cross-sectional view of the textured thin c-Si wafer (a) before HNA treatment and (b) after HNA treatment. Partial etching of the pyramidal structure leading to dome shaped topography is evident.

However, it is worth mentioning that the rounding off of the pyramidal surface to dome like morphology will put some detrimental effect on the optical property of the wafer. In order to study any such effect, reflectance from the thin c-Si wafer with pyramidal and dome shaped structures was measured within 300 –1100 nm wavelength region and is presented in Fig.3.3. A total loss of 2.7% in the integrated reflectance was observed after rounding off the pyramidal textures, which is not quite significant as the gain in electrical properties predominates in the latter case. This has been established by measuring the performance of the two SHJ cells as per the schemes presented in Fig.3.1. The advanced thin silicon solar cells of recent times involve the use of flat rear surface

rather than a textured surface. This is done to obtain better passivation as reported by Kim et al [205] and Kung et al [206]. The same concept has been adopted here.

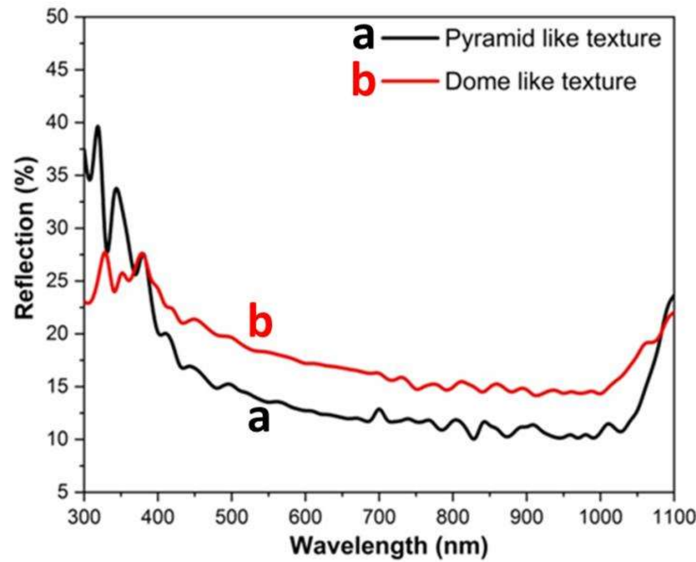

Fig.3.3: Reflection characteristics of the surface of c-Si wafer with (a) pyramidal and (b) dome shaped textures.

The J–V characteristics of Cell 1 and Cell 2 are presented in Fig.3.4 and the cell parameters are summarized in Table 3.2. It has been found that Cell 1 yielded V_{OC} and J_{SC} as 627 mV and 30.98 mA/cm^2, respectively; with a fill factor (FF) of 0.62. The conversion efficiency was 12.04%. Whereas, for Cell 2; the values for V_{OC}, J_{SC} and FF were 638 mV, 30.36 mA/cm^2 and 0.69, respectively. This leads to a conversion efficiency of 13.37% for this case. Here, the obtained V_{OC} is some what lesser than the previous reports. This might be attributed to the use of as-cut CZ wafers having carrier lifetime ~100 µs, which is notably lower than the value (~2 ms) of the referred cases. As well as, the fabrication limitations as mentioned earlier; in depositing the amorphous layers on both sides without breaking the vacuum of the PECVD chamber could be the other reason.The effect of 'doming' of front textured surface on the optical and electrical properties is quite evident from the cell parameters of Cell 2. About 2% loss in J_{SC} is attributed to the light loss due to enhanced reflection by the dome like front structure.

Whereas, the gain in V_{OC} and FF is due to better passivation and improved shunt attained after doming the front textures. This resulted in an overall 11.04% increase in the photoconversion efficiency.

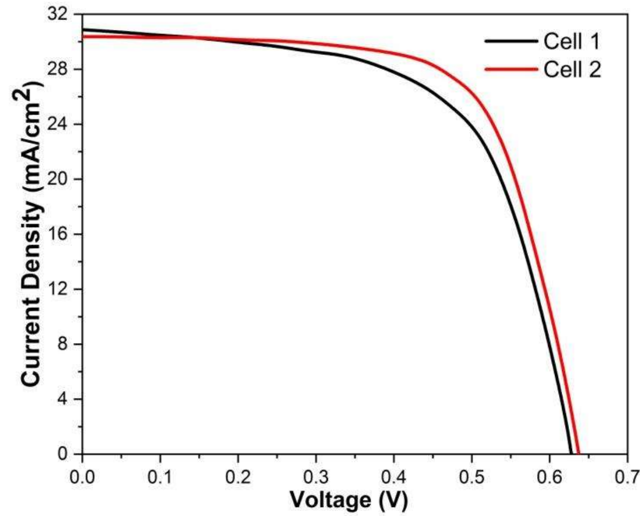

Fig.3.4: J – V characteristics of the thin SHJcell with pyramidal (Cell 1) and dome shaped (Cell 2) front textures.

Though the photoconversion efficiency (13.37%) for Cell 2 is quite promising for a thin SHJ cell fabricated on 30 μm wafer, however, this could be further improved by implementing proper back reflection architecture. Minimizing the transmission loss of the longer wavelengths through the thin active materials is one of the crucial steps that need to be taken care of in this regard.

3.3.2. ITO NPs as the back reflectors

It is well known that the semiconductor nanoparticles (like ITO NPs) have lower parasitic absorption than metal (Au, Ag) NPs. This means, light loss due to Joule heating will be less in case of ITO NPs than metal NPs. For this reason, the use of ITO NPs has been adopted in the back reflecting structure in this case. This will also help to compare between the flat and nanoparticle array of ITO layers in terms of their light reflection capabilities. It can be seen from Fig.3.1 that a flat ITO layer with 50 nm thickness was

introduced between the n-a-Si:H and back Al contact for both Cell 1 and Cell 2. This ITO layer actually plays two roles, viz. (i) helps in forming good ohmic contact between then-a-Si:H and metallic Al layer and (ii) increases the probability of light reflection from the back.

The flat ITO layers with 50 nm thickness were deposited using RF magnetron sputtering from an ITO (SnO_2:In = 90:10) target at a process pressure of 2×10^{-5} mbar and temperature 180°C with power density 1.2W/cm^2. Sputtered gas argon (Ar) has been used along with oxygen (O_2) with a flow (sccm) ratio of 99:1. Same sputtering chamber and sputtered gas Ar was utilized for the realization of ITO NPs keeping the target closed by astainless steel lid. However, to form the ITO NPs, the initial thickness of the layer was taken as 20 nm. Process pressure and power density were kept fixed at 0.5 torr and 100mW/cm^2, respectively. Ar plasma exposure time was varied from 5 min to 15 min for the realization ITO NPs with various diameters. Fig.3.5 represents the morphology of the flat ITO layer and Ar plasma treated ITO NPs. It can be seen from Fig.5b to 5d that the particles become discrete with increasing size as the duration of Ar plasma treatment increases. In this case, the ITO nanoparticle array (with particle diameter within 80 – 100 nm) obtained after 15 minutes of Ar plasma treatment (Fig.3.5d) has been chosen as back reflecting structure along with the flat one (Fig.3.5a) to carry out a comparative investigation.

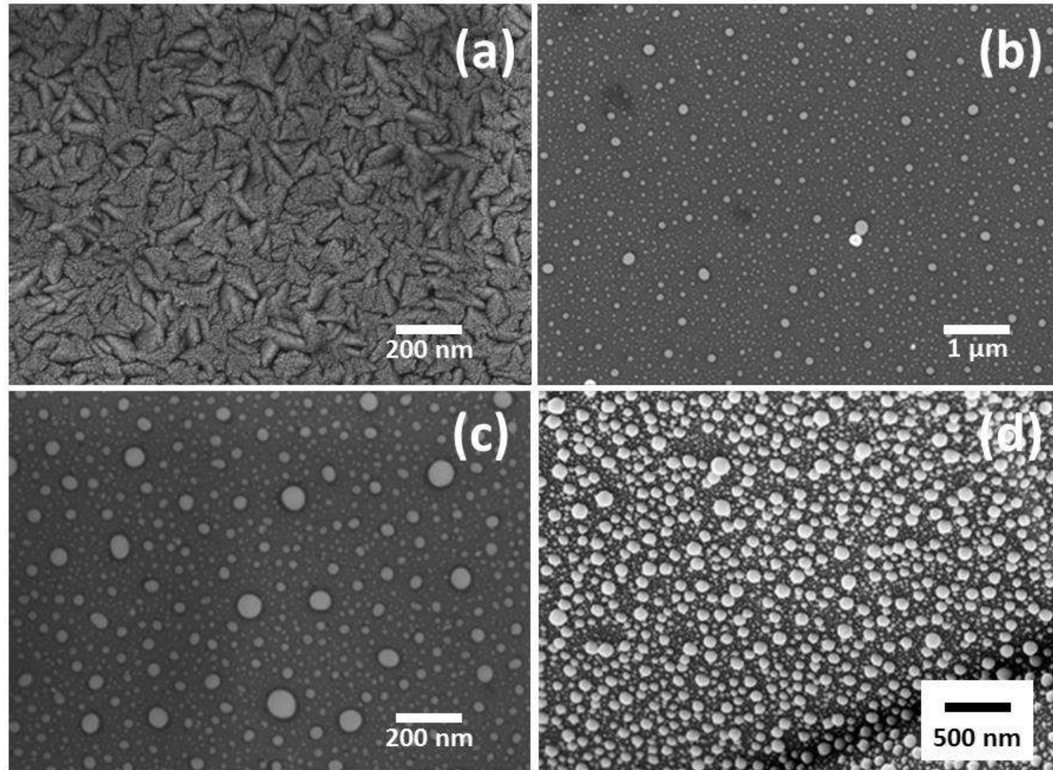

Fig.3.5: Morphology of the ITO layers (a) 50 nm thick flat sampleand 20 nm thick Ar plasma treated samples for (b) 5 min (c) 10 min and (d) 15 min.

3.3.2.1. Transmission and reflection properties of the BRLs:

Transmission of light with longer wavelengths through a thin (c.a. 30 µm) silicon substrate is a typical problem. To explore the exact scenario in this case, five different back layer configurations with thin (30 µm) c-Si wafer and ITO layer/NPs have been prepared as described in Fig.3.6. In this case, the thickness of the ITO layers was 50 nm in all cases, whereas, the ITO NPs bear the properties as mentioned in the earlier section. Being significantly small in thickness, the other amorphous silicon based layers on the top were not considered.

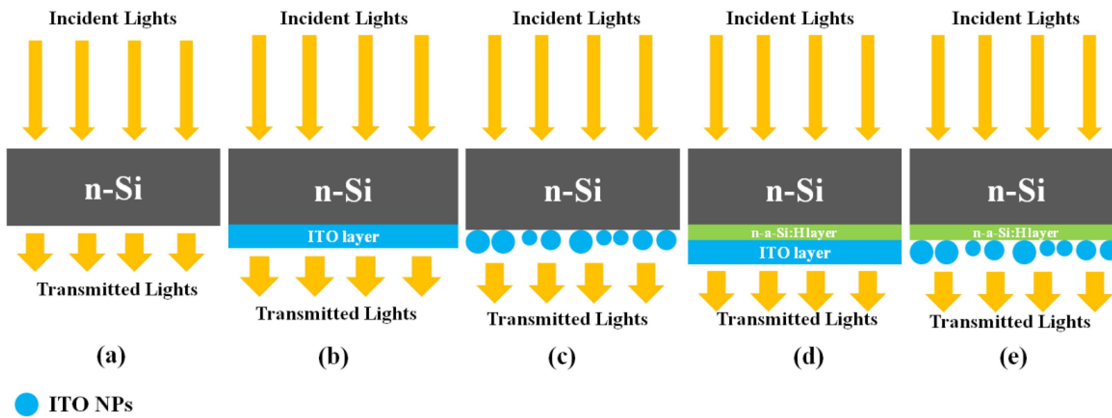

Fig.3.6: Transmission analysis configurations with 30 µm c-Si and ITO layer/NPs.

The light transmission properties of the back layer configurations as presented in Fig.3.6 were experimentally measured within the wavelength range 500 – 1100 nm are the results are shown in Fig.3.7. A sharp rise in transmittance of light through the 30 µm substrate has been observed after 750 nm for all the five configurations. The thin and bare c-Si showed maximum transmittance, whereas, the thin wafer decorated with n-a-Si:H layer and ITO NPs (Fig.3.6e) showed minimum transmittance of light within 750–1100 nm. The integrated transmittance was found to be 17.38, 16.99, 13.20, 14.14 and 11.16 for thin n-c-Si wafers with conditions (a) bare (b) coated with 50 nm ITO layer (c) decorated with ITO NPs (d) coated with both n-a-Si:H (25 nm) and ITO layer (50 nm) and (e) coated with 25 nm n-a-Si:H layer and decorated with ITO NPs, respectively. It is clearly evident from the curves presented in Fig.3.7 and the integrated transmittance values that ITO, specifically in the form of almost spherical NPs, plays a significant role in lowering the light transmission loss within 750–1100 nm through the ~30 µm thin n-c-Si active layer. This might be attributed to the good light reflection behaviour of ITO NPs that reflect back a part of the incident light coming through the n-c-Si thin wafer.

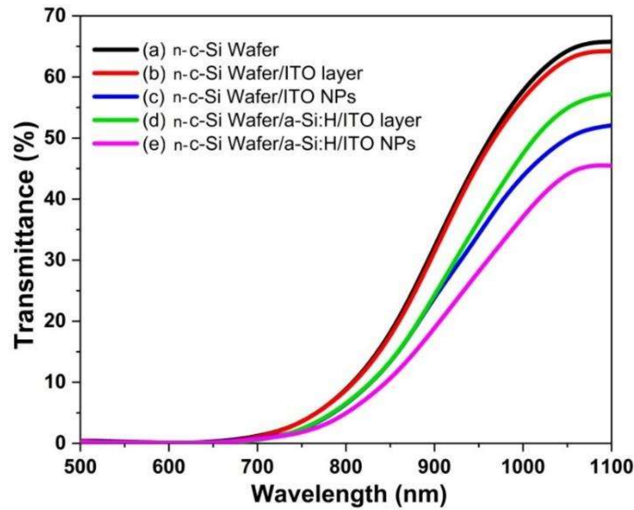

Fig.3.7: Transmittance curves for 30 µm c-Si wafer decorated with ITO layer/NPs.

This could be further validated by measuring reflectance from the proposed back layer configurations as mentioned in Fig.3.6a-e. To do so, initially it has been tried to measure the reflections from the top of n-c-Si substrate after depositing the layers on it, however, no prominent signal was received and this might be due to the absorbance of small intensity back reflected lights within the active layer. In order to address this problem, inverted back reflection configurations were mimicked on properly cleaned glass substrates as elaborated in Fig.3.8. As it has been seen from the transmittance measurements that the 30 µm thin c-Si wafer allows the light to pass through mainly after 700 nm in wavelength, light reflection from the top of these configurations has been measured within 700 – 1100 nm and the curves are presented in Fig.3.9.

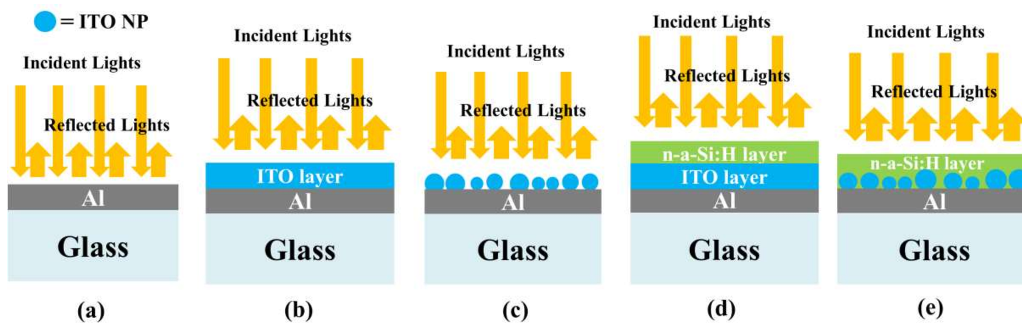

Fig.3.8: Back reflection measurement configurations with five different structures.

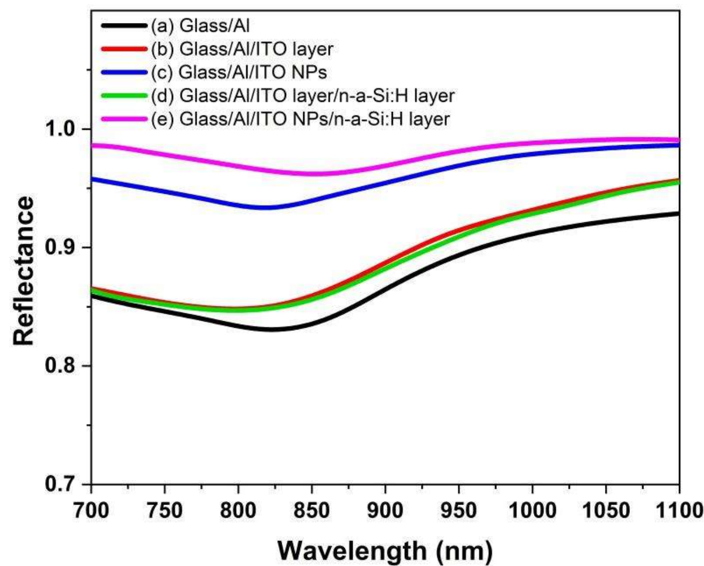

Fig.3.9: Reflectance curves as obtained from the back layer configurations prepared on glass.

It is evident from Fig.3.9 that incorporation of ITO, either as flat layer or in the form of NPs, enhances reflection in comparison to the blank Al layer coated on glass within the longer wavelength region. Again, ITO, in the form of NPs, showed better reflectance than the flat ITO layers within the same environment. This might be attributed to better light scattering phenomenon exerted by the almost sphere-like ITO NPs than the flat morphology. The presence of discrete spherical clusters in the ITO matrix with diameters less than the wavelengths of incident light promotes the probability of localized surface plasmon resonance than the flat ITO structure, hence, scattering increases in the former case [207]. It has also been observed that the ITO NPs deposited on glass/Al substrate and embedded within n-a-Si:H layer (as shown in Fig 8e) has better reflectance property than the bare ITO NPs deposited on glass/Al. The n-a-Si:H coating makes the ITO NPs more confined and hence, the scope of localized surface plasmon resonance increases in this case. The integrated reflectance was found to be 87.63, 89.34, 96.09, 89.16 and 97.94 for the curves as presented by the lines (a), (b), (c), (d) and (e),

respectively, in Fig.3.9. This means, about 11.76% and 9.62% enhancement in back reflection can be achieved by incorporating ITO NPs in n-a-Si:H layer rather than choosing the conventional bank Al or Al/ ITO(flat) back reflection configurations, respectively.Thus, the ITO NPs behave like nano-mirrors and reflect back a notable amount of light from the rear side of the cell, mainly with the longer wavelengths. Hence, it would be worth implementing such ITO NPs as the back reflectors for the performance enhancement of SHJcells fabricated on 30 μm thin c-Si wafer.

3.3. Fabrication of thin SHJ solar cells with ITO NP embedded back reflector architecture:

It is quite obvious that,to get maximum effect of back reflection of the unabsorbed light of first pass from the ITO NPs, proper positioning of them in the rear side of the cell along with the other layers is very crucial. This is essential so that maximum light can be obtained without hampering the other attributes of the device. In this case, three different SHJcells were fabricated on 30μm n-c-Si wafer by placing ITO NPs at different positions(Fig.3.10) in the rear side stacks of the cells in the following ways: (i) between

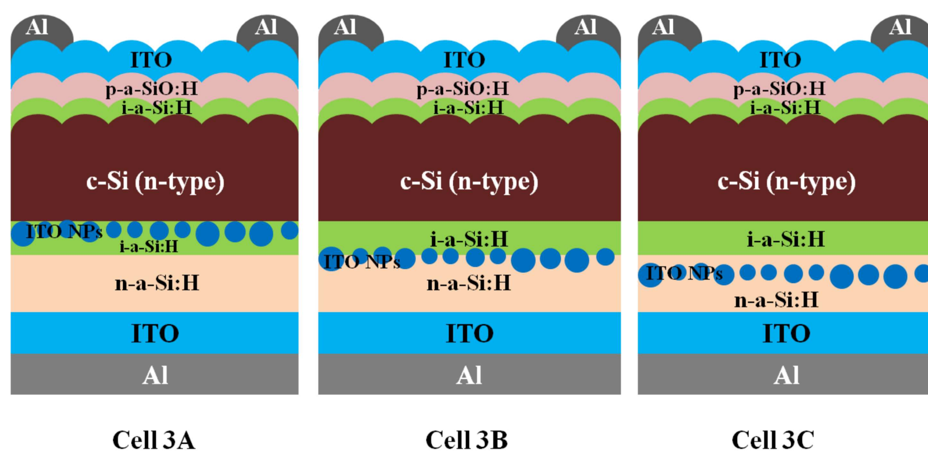

Fig.3.10: Schematic showing the relative positions of ITO NPs at the rear side of the SHJ cells fabricated on thin n-c-Si wafer.

n-c-Si and back i-a-Si:Hlayers (Cell 3A) (ii) betweenbacki-a-Si:H and n-a-Si:H layers (Cell 3B) and (iii) Embedded within n-a-Si:H layer (Cell 3C). In all cases, the ITO NPs were synthesized using the recipe as mentioned in Section 3.3.2.A systematic investigation on the performance of these three cells (Cell 3A, Cell 3B and Cell 3C) has been carried out and the values have been compared with Cell 2, i.e., the thin SHJ cell with no ITO NPs at the back but with all other structures as same. The J–V curves of these four cells are presented in Fig.3.11.

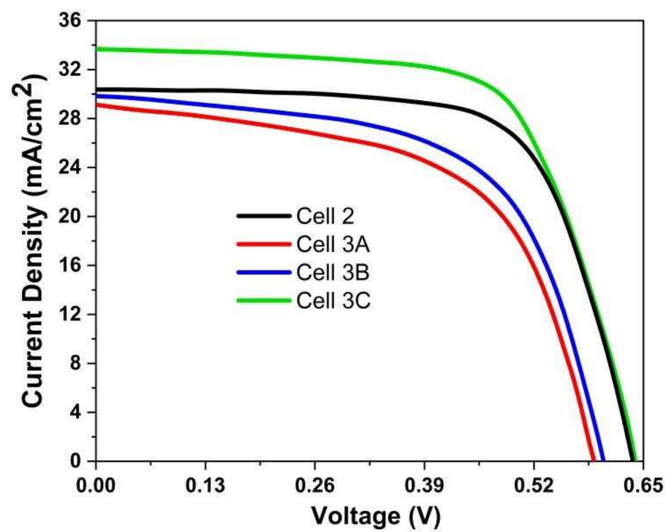

Fig.3.11: J – V curves for Cell 2, Cell 3A, Cell 3B and Cell 3C.

Case-I (Cell 3A): According to the back layer architecture adopted here, the light of the first pass from n-c-Si wafer will first interact with this array of ITO NPs. As well as, these ITO NPs are at the farther most position from the back Al/ITO layer. Hence, maximum reflection of the unabsorbed first pass lights will be obtained from these NPs. But, placing the ITO NPs at the interface of n-c-Si and back i-a-Si:H layers will affect the surface passivation of the wafer immensely which has adverse effect on the cell parameters as shown in Fig.3.11. For this cell the open circuit voltage (V_{OC}) and fill factor (FF) were found to be 591 mV and 0.58, respectively. It can clearly be seen (Table 3.2) that the V_{OC} and FF were affected majorly due to inferior back surface

passivationoccurred by the incorporation of ITO NPs at this interface, than the cell without ITO NPs, i.e. Cell 2. There is drop in V_{OC} from 638 mV (Cell 2) to 591 mV (Cell 3A). Even, the short circuit current density (J_{SC}) was found to be reduced (29.11 mA/cm^2) adequately than Cell 2 (30.36 mA/cm^2) owing to the high carrier recombination caused by poor passivation at the immediate back surface of the thin n-c-Si wafer. Cell 3A yielded high series resistance (R_S) with lower shunt resistance (R_{SH}) of 6.12 **Ω** and 102.76 **Ω**, respectively. The photoconversion efficiency was 9.98% in this case.

Case II (Cell 3B): Due to the adverse effect of positioning the ITO NPs at the interface of n-c-Si and back i-a-Si:H layers as observed in the case of Cell 3A, now in Cell 3B, the ITO layer was placed after depositing theback i-a-Si:H layer (at the interface of back i-a-Si:H and n-a-Si:H layers) aiming to the minimization of surface passivation of the crystalline wafer by detaching it from the ITO NPs. Eventually, it did not help much in improving the PV parameters as can be seen from Table 3.2. This might be attributed to two factors as follows: (i) deposition of ITO layer through sputtering ruptures the very thin (5nm) i-a-Si:H layer due to high energy bombardent which in turn, again, results in poor surface passivation. The extent of surface passivation is somewhat better in this case that has been reflected by nominal increase in V_{OC} and J_{SC}, and (ii) Ar plasma treatment to make ITO NPs from ITO layer might cause partial crystallization of the i-a-Si:H layer which could have been the reason behind poor fill. The series and shunt resistance (5.84 **Ω** and 132.54 **Ω**, respectively) also got some improvements than Cell 3A. Some what better performance of Cell 3B in comparison to Cell 3A indicates that seperating out the ITO layer from the n-c-Si layer has some positive influence in enhancing the cell parameters by improving surface passivation. The photoconversion efficiency achieved for this cell architecture was 10.78%.

Case III (Cell 3C): In this case, the ITO NPs were embedded within the n-a-Si:H layer as shown in Fig.3.10. To do so, first a 10 nm thick n-a-Si:H layer was deposited on the i-a-Si:H layer followed by the deposition of ITO NPs using the recipe as mentioned in Section 3.2. Then another 15 nm layer of n-a-Si:H was deposited on it followed by the complete cell fabrication. It has been found that, there was a notable increase in cell parameters (Table 3.2) that yielded a significantly high conversion efficiency of 14.73%. The result clearly shows that a balance between the optical and electrical properties of the BRL configuration has been achieved by placing the ITO NPs within the n-a-Si:H layer. According to the reflectance measurements (Fig.3.9), the BRL architecture adopted in Cell 3C has maximum back reflectance attribute than the other adopted configurations. On the other hand, well speration of the ITO NPs from the thin n-c-Si wafer exerts positive impact on surface passivation and the electrical properties of the active layer. Hence, a balance between the optical and electrical properties has been established in this cell structure.The external quantum efficiency (EQE) curves (Fig.3.12) clraely predicts that there is a notable increase in EQE mainly within 700–1100 nm in Cell 3C in comparison to Cell 2 which does not have any ITO NPs at the back. This might be attributed to good amount of reflection back of transmitted light with longer wavelengths in Cell 3C, and the result is well corroborated with the reflectance studies. It is worth mentioning here that the light reflected or scattered back by the ITO NPs will face multiple bounces within the active layer of the cell, and hence, the prospect of photocarrier generation will be increased [208].

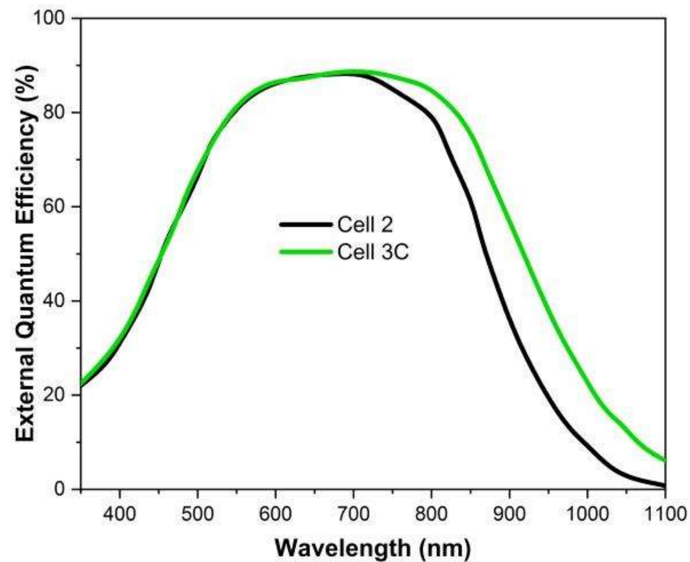

Fig.3.12: EQE curves for Cell 2 and Cell 3C.

Case IV (Cell 3D): The results obtained so far indicate that ITO NPs are excellent candidates in back reflection of transmitted lights without compromising the electrical properies of the SHJ cells fabricated on 30 μm thin c-Si wafer, if placed properly in the back reflector structure. With this improvization, another SHJ cell, designated as Cell 3D, was fabricated on thin n-c-Si substrate with double array of ITO NPs as depicted in the inset of Fig.3.13a. In this case, two layers of ITO NPs seperated by n-a-Si:H layer were embedded at the rear surface. The first layer of ITO NPs was embedded within the n-a-Si:H layer in a similar process as desribed in Case III. To embed the seceond layer of ITO NPs, a 20 nm ITO layer was deposited followed by Ar plasma treatment in the same chamber and finally those ITO NPs were covered by a 15 nm thick n-μc-Si:H layer. The other structural attributes of the cell remained unchanged.

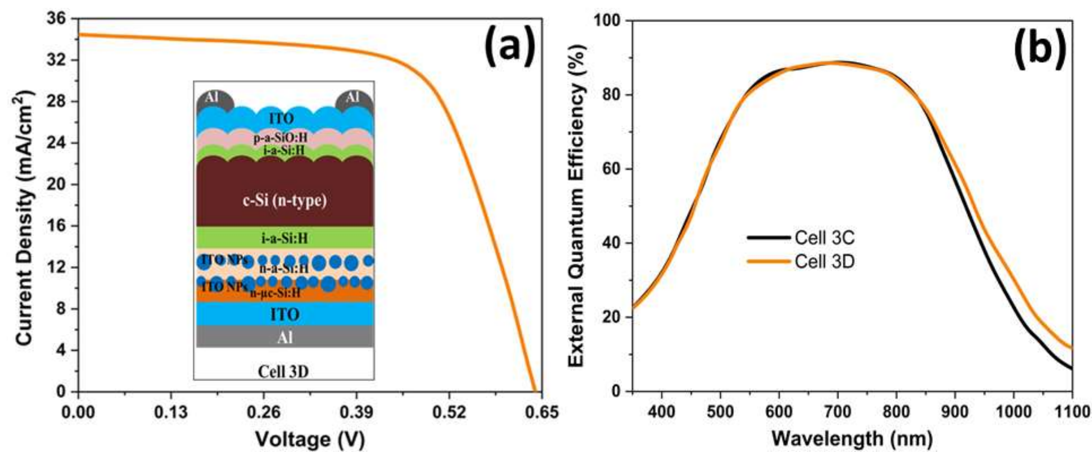

Fig.3.13: (a) J – V characteristics (inset: schematic of Cell 3D) and (b) EQE curve for Cell 3D.

The performance of Cell 3D was the best among the lot. It can be seen from the J–V curve (Fig.3.13a) and Table 2 that inserting two layer of ITO NPs at the back did not hamper the V_{OC} and FF of the cell. The shunt resistance was compromised to slightly, which was countered by lowered series resistance in comparison to Cell 3C. Most importantly, there was an increament in J_{SC} from 33.80 to 34.46 mA/cm^2 (than Cell 3C) that might be attributed to better light back reflection by the double layer of ITO NPs in Cell 3D. The NPs in each layer in this case work as nanomirrors and improvise multiple scattering/bounces of light within the cell. This increament in J_{SC} was further supported by the marginalenhancement in EQE in the NIR region in comparison to Cell 3C as depicted in Fig.3.13b. Eventually, Cell 3D yielded 13.50% enhancement in J_{SC} and 12.34% increament in photoconversion efficiency than those of Cell 2, which has the same dome like front surface but does not have ITO NPs as the back reflecting structure.

From the above discussions, it is clear that SHJ solar cells on adequately thin (~30 μm) c-Si wafer can be prepared with notable photoconversion efficiency by adopting suitable front and back light trapping architectures. Proper placing of ITO NPs at the back

of the cell plays an important role in balancing between the optical and electrical properties of the fabricated cells.

Table 3.2: Cell parameters of the fabricated SHJ cells on 30 µm wafer with various light management schemes

Sl No.	J_{SC} (mA/cm2)	V_{OC} (mV)	FF	E_{ff} (%)	Series resistance (Ω)	Shunt resistance (Ω)
Cell 1	30.98	627	0.62	12.04	5.13	149.80
Cell 2	30.36	638	0.69	13.37	5.17	344.33
Cell 3A	29.11	591	0.58	9.98	6.12	102.76
Cell 3B	29.84	602	0.60	10.78	5.84	132.54
Cell 3C	33.80	641	0.68	14.73	5.20	323.15
Cell 3D	**34.46**	**641**	**0.68**	**15.02**	**5.11**	**315.83**

3.4. Chapter Conclusions

SHJ solar cells on an adequately thin (~30 µm) n-c-Si wafer were fabricated as a pilot scheme to comply with the 'thinning' benchmark set by ITRPV-2019. To address the light trapping related issues in thin c-Si substrates without compromising with the devices's electrical properties, proper measures like 'doming' of the pyramidal front textures and the use of ITO NPs as the back reflector materialwas adopted. It has been found that proper positioning of the ITO NPs in the back reflector architecture is crucial achieving a balance between the optical and electrical properties of the device. ITO NPs with 80–100 nm diameters were found to exhibit better light reflection properties from the back than the commonly used flat configuration, which has been proved using reflectance and external quantum efficiency measurements. Compared to only Al or Al/ITO back reflector structure, the ITO NPs showed better back reflection of transmitted light in the longer wavelengths, specifically after 700 nm. This might be attributed to the localized surface plasmon effect exhibited by the ITO NPs due to their degenerate

electronic configuration and discrete distribution in the BRL. However, these NPs should be sufficiently away from the n-c-Si surface so that the surface passivation does not get hindered. The best cell showed 15.02% photo-conversion efficiency with (~1/6th) of active layer thickness for conventional SHJ cells. The wafers used in this case were as-cut CZ wafers with carrier lifetime ~100 μs and about ten times cheaper than the wafers commonly used in fabricating state-of-the-art-cells in the laboratory. Further, it has been realized that, by using better fabrication facility like PECVD system with both side coating facilities in one go without breaking the vacuum and by using c-Si wafer having a higher lifetime in milliseconds, V_{OC} greater than 700 mV,and efficiency >20% could be achieved.