Chapter 5

Switched Boost USMC

5.1 Introduction

Integration of the impedance network with USMC facilitated the development of expanded topologies. This impedance network can be placed at the input side or DC-link side. Integrating the Z source/quasi Z source impedance network at the input side, voltage gain can be improved, but this approach requires more number switches, passive components, and high rated elements for USMC. So, based on the above considerations, various impedance networks are integrated between the rectifier and inverter of USMC. By integrating the Z source (ZS-USMC) impedance network at the DC-link, voltage gain is improved but the main drawbacks of ZS-USMC are (i) High inrush current at startup, due to this ZS-USMC cannot achieve soft starting capability [108], (ii) The discontinuous nature of the input current leads to large input filter [48], (iii) Four passive elements to develop ZS-USMC. The quasi Z-source USMC (QZ-USMC) structure requires four passive elements and one diode at the DC-link of the USMC. Due to more passive elements at its DC-link side, the size of the converter becomes large, especially for high power applications. Series Z source USMC (SZ-USMC) is introduced by integrating a series Z source impedance network with a limited load power factor range (≥ 0.866). Switched inductor Z source USMC (SWZ-USMC) [49] gives a high boosting function but needs high rating capacitors and inductors. This structure also suffers from high inrush current at startup. SWZ-USMC also requires six additional passive elements and six diodes for implementation. By reducing some components in SWZ-USMC, a hybrid switched inductor USMC (HSWZ-USMC) is developed [50].

The limitation of HSWZ-USMC is that it produces low voltage gain with more components in the impedance network. Switched capacitor USMC (SC-USMC) [51, 52] is developed by inserting a switched capacitor impedance network. A significant limitation of SC-USMC is that it needs more shoot-through period to achieve high voltage and also requires three passive components in the impedance network. High voltage gain is achieved by inserting a modified quasi Z source impedance network (MQZS-USMC) [109]. MQZS-USMC has problems like the accidental shorting of the DC-link with different capacitor ratings which leads to the development of huge currents. This converter draws more current at a lower shoot-through period. All the above converters required more passive elements to enhance the voltage gain. So, achieving better voltage gain with the requirement of fewer passive components is the motive of this chapter. In this chapter, the switched boost (SB) impedance network is integrated with USMC to achieve higher voltage gain with only two passive components. The conventional SVM technique is applied to the SB-USMC to understand the SB-USMC working principle.

5.2 Switching strategy for SB-USMC

The proposed SB-USMC is developed by integrating the SB network between the rectifier and inverter stages, as depicted in Figure 5.1. It consists of a CSR, which employs one switch and four diodes in each leg and output is connected to the SB network. SB network consists of a capacitor (C), inductor (L), diodes (D_1, D_2), and switch (S). The output of the impedance network is input to the VSI. The inverter structure is similar to the two level VSI. Switches of both CSR and VSI are controlled by applying the SVM technique. In CSR, there are six active vectors $[I_{ab}, I_{bc}, I_{ca}, I_{ba}, I_{cb}, I_{ac},]$ form six equal sectors (I to VI) as shown in Figure 5.2(a). The reference current vector I_{ref} is synthesized by two active vectors out of six active vectors. In the same way, VSI reference vector V_{ref} can be synthesized by two active vectors out of six active vectors $[V_1, V_2, V_3, V_4, V_5, V_6]$ and two zero vectors $[V_0, V_7]$ as depicted in Figure 5.2(b). Active vectors duty ratio in Sector I for CSR and VSI are given in equation (5.1).

$$\begin{aligned} dI_{ab} &= m_i sin(\frac{\pi}{3} - \alpha), \quad dI_{ac} = m_i sin(\alpha) \\ dV_1 &= m_v sin(\frac{\pi}{3} - \beta), \quad dV_2 = m_v sin(\beta) \end{aligned} \tag{5.1}$$

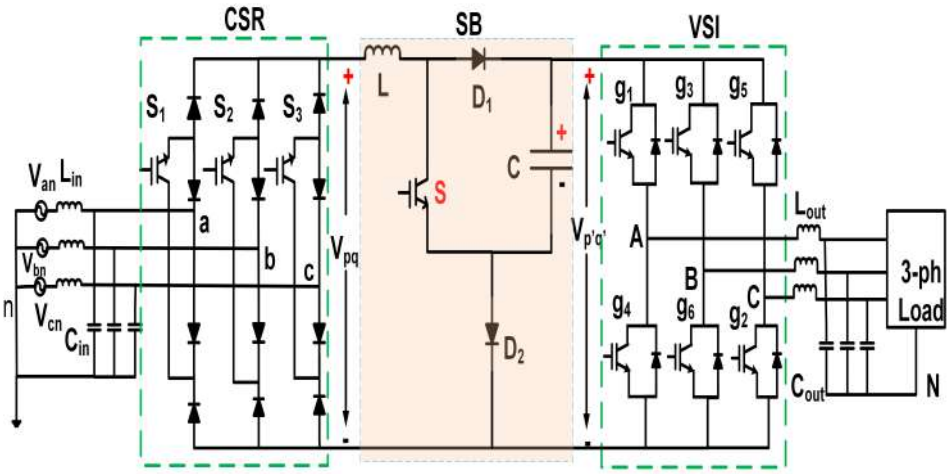


Figure 5.1: Switched boost ultra sparse matrix converter (SB-USMC)

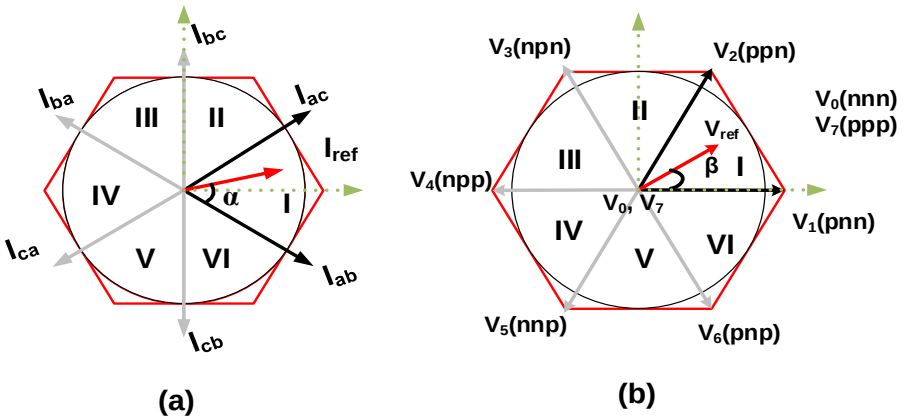


Figure 5.2: Space vectors diagram for a) CSR b) VSI

Here, α and β are the CSR and VSI reference vector angles and m_i, m_v are the CSR, VSI modulation indexes. To obtaining maximum DC-link voltage, keep $m_i = 1$. Multiplication of CSR and VSI active vectors duty ratios gives SB-USMC active vectors duty ratios and zero vectors duty ratio (d_0) can be obtained from equation (5.2). Here, d_{st} is the shoot-through duty ratio and m is the SB-USMC modulation index. SB-USMC should operate for some time at the shoot-through (d_{st}) stage to get the boosting function. SB-USMC operates in two modes: 1) shoot-through (ST) mode and 2) non shoot-through (NST) mode. Figure 5.3 shows the sector I switching sequence for the switching frequency f_S ($= \frac{1}{T_S}$).

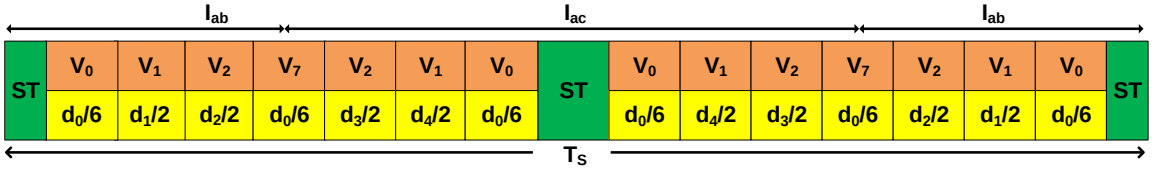


Figure 5.3: Switching strategy for the SB-USMC converter

$$\begin{aligned} d_1 &= dI_{ab}dV_1, \quad d_2 = dI_{ab}dV_2 \\ d_3 &= dI_{ac}dV_2, \quad d_4 = dI_{ac}dV_1 \\ d_0 &= 1 - d_1 - d_2 - d_3 - d_4 \\ m + d_{st} &\leq 1 \quad (m = m_i \times m_v) \end{aligned} \tag{5.2}$$

CSR uses active vectors in both modes, but in the VSI section, during the NST mode, active and zero vectors are applied to deliver the power and during ST mode, any one leg of the VSI is shorted to store the energy, as shown in Figure 5.4. For equal distribution of ST mode between two CSR active vectors, placed at both corners and middle of the sequence. The sequence starts with the active vector I_{ab} in the CSR stage while the VSI stage cycles through the sequence (ST) - (V_0) - (V_1) - (V_2) - (V_7). After that, I_{ab} is replaced by I_{ac} and the VSI sequence repeats in reverse order. VSI side sequence is repeated after $\frac{T_S}{2}$ to improve the quality of the output. For better understanding, Figure 5.5 shows the NST mode connection diagram in sector I when CSR active vector I_{ab} and VSI active vector V_1 are applied. In this mode, switches S_1 and S_2 at the CSR side, g_1, g_2, and g_6 in the VSI and diodes of the SB network D_1, D_2 are in conduction, highlighted in red colour. Figure 5.4 represents the connection diagram for ST mode in the same sector. In this mode S_1, S_2, g_1, g_4, and SB switch S are in conduction.

5.2.1 Mathematical modelling

For input $v_{an} = \hat{V}_m cos(wt)$, $v_{bn} = \hat{V}_m cos(wt - 120^o)$, $v_{cn} = \hat{V}_m cos(wt - 240^o)$, CSR rectified average output voltage (V_{pq}) is

$$V_{pq} = dI_{ab}v_{ab} + dI_{ac}v_{ac} = 1.5\hat{V}_m \tag{5.3}$$

The average of the rectified voltage acts as a source to the SB network. From Figure 5.5, during NST, impedance network switch S is OFF, diodes D_1 and D_2 are ON and

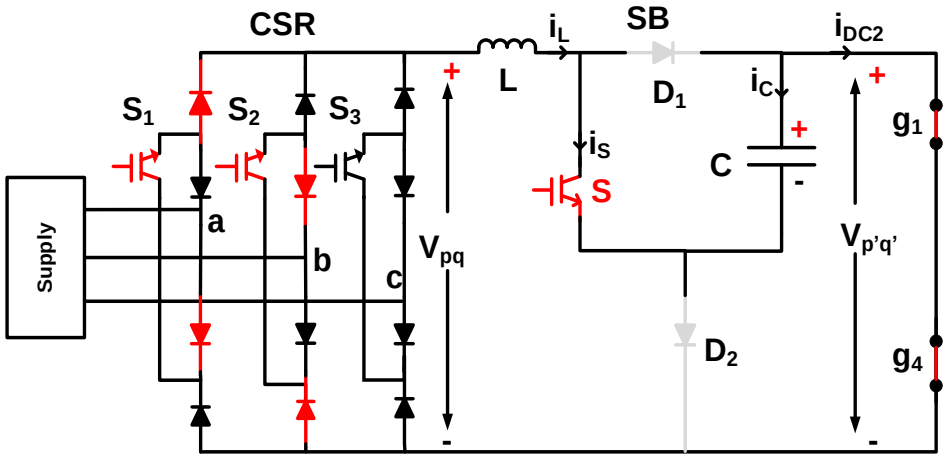


Figure 5.4: Shoot-through state

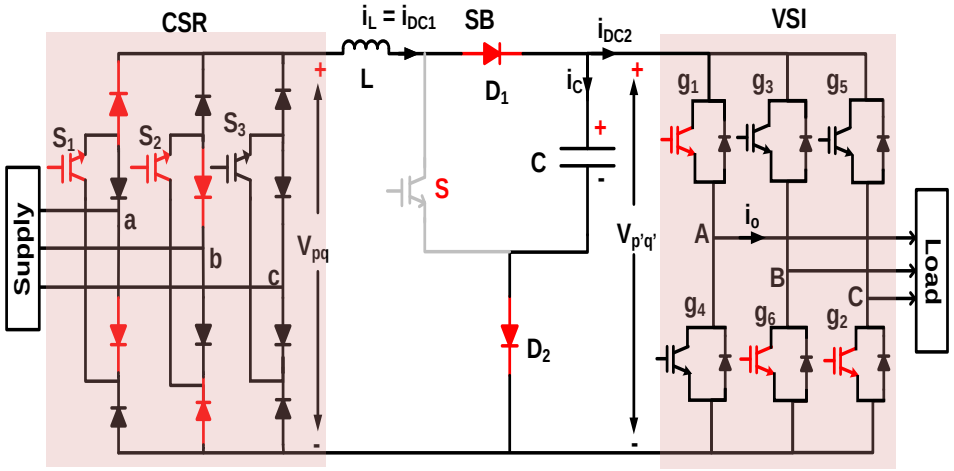


Figure 5.5: Non shoot-through state

the inductor current is discharged through the capacitor and load. The voltage across the inductor and current through the capacitor during this mode is given in equation (5.4).

$$v_L = V_{pq} - V_C, \quad i_C = i_L - i_{DC2} \tag{5.4}$$

Here i_L is current through the inductor, V_C is the voltage across capacitor C, and i_{DC2} is the VSI input current. During ST mode S is ON, diodes D_1 and D_2 are OFF and shorting the VSI leg, as shown in Figure 5.4. The inductor gets charged through rectified voltage and capacitor. The voltage across the inductor and current through the capacitor is calculated as.

$$v_L = V_{pq} + V_C, \quad i_C = -i_L \tag{5.5}$$

By applying the volt-second balance Law across the inductor in one complete cycle (T_s), the voltage across capacitor V_C and the boosted voltage $V_{p'q'}$ are calculated in equation (5.6).

$$V_{p'q'} = V_C = \frac{1}{1-2d_{st}} V_{pq} \tag{5.6}$$

From equation (5.6), the impedance network boosted the voltage level from V_{pq} to $\frac{1}{1-2d_{st}} V_{pq}$ and for SVM switching strategy the peak output voltage is

$$\hat{V}_o = \frac{m}{\sqrt{3}} V_{p'q'} \tag{5.7}$$

Taking into account the input power factor ($cos(\phi_{in})$), from equations (5.3) to (5.7), the overall voltage gain of the proposed SB-USMC converter is given as

$$\frac{\hat{V}_o}{\hat{V}_m} = \frac{\sqrt{3}m}{2} \frac{1}{1-2d_{st}} cos(\phi_{in}) \tag{5.8}$$

For getting maximum voltage gain, $(cos(\phi_{in})) = 1$ and corresponding boosting factor (B)

$$B = \frac{\sqrt{3}m}{2} \frac{1}{1-2d_{st}}, \quad d_{st} = \frac{2B - \sqrt{3}m}{2B}, \quad \hat{V}_o = B\hat{V}_m \tag{5.9}$$

5.3 Selection of impedance network elements

The selection of inductor is chosen based on the ripple ($\Delta = 25\%$) in the inductor current (I_L) with the switching frequency $f_S = 5\, kHz$. During ST mode, from equation (5.5) and Figure 5.3, $L\frac{dI_L}{dt} = V_{pq} + V_C$ and dt is $\frac{T_s \times d_{st}}{3}$. So from equation (5.6), the ripple in the inductor current is

$$\Delta I_L = \frac{V_{pq} T_s 2 d_{st}(1-d_{st})}{3L(1-2d_{st})}, \quad P_{dc} = V_{pq} \times I_L \tag{5.10}$$

The inductance value for the required amount of power is

$$L = \frac{3}{2} \frac{\hat{V}_m^2 d_{st}(1-d_{st}) cos^2(\phi_{in})}{\Delta f_S P_{dc}(1-2d_{st})} \tag{5.11}$$

Similarly For the percentage ripple in the capacitor voltage ($\Delta_C = 1\%$), the required capacitance is calculated in equation (5.12).

$$C\frac{dV_C}{dt} = I_L, \quad C = \frac{4P_{dc} d_{st}(1-2d_{st})}{27 f_S \Delta_C \hat{V}_a^2 cos^2(\phi_{in})} \tag{5.12}$$

During NST mode, switch S is OFF and parallel to the capacitor. So, voltage stress

Table 5.1: SB network current and voltage stresses

Mode	V_S	I_S	V_{D1}	I_{D1}	V_{D2}	I_{D2}
ST	0	$(1+\frac{\Delta}{2})\frac{\sqrt{3}m(1-d_{st})}{2(1-2d_{st})}I_o$	$\frac{1}{1-2d_{st}}V_{pq}$	0	$\frac{1}{1-2d_{st}}V_{pq}$	0
NST	$\frac{1}{1-2d_{st}}V_{pq}$	0	0	$(1+\frac{\Delta}{2})\frac{\sqrt{3}m(1-d_{st})}{2(1-2d_{st})}I_o$	0	$\frac{\sqrt{3}m(1+\frac{\Delta}{2}(1-d_{st}))}{2(1-2d_{st})}I_o$

across the switch is $V_C = \frac{1}{1-2d_{st}}V_{pq}$. The detailed voltage and current stresses of the SB network switch and diodes are given in Table. 5.1. Here, I_o is the load current amplitude.

5.4 Analysis of the proposed converter

In this section, a thorough analysis is provided to understand the effects of various factors including load power factor, voltage gain, and output frequency.

5.4.1 Operating range of the load power factor ($cos(\phi_o)$)

One of the main limitations of the USMC is the limited output power factor angle ($-\frac{\pi}{6}$ to $\frac{\pi}{6}$) with a minimum power factor of 0.866 to avoid the negative DC-link current [32]. However, this restriction varies to the proposed converter. To obtain the power factor range of the proposed converter, consider that the converter is in NST mode as shown in Figure 5.5. In this mode, CSR output current i_{DC1} is equal to the sum of the VSI input current i_{DC2} and capacitor current i_C. For SB-USMC, DC-link current i_{DC1} should be positive. So,

$$i_{DC1} = i_{DC2} + i_C \geq 0 \tag{5.13}$$

From the power balance condition at VSI input and output sides,

$$i_{DC2} = \frac{\sqrt{3}}{2} m \hat{I}_{om} cos(\phi_o) \tag{5.14}$$

During NST mode, the capacitor current is positive magnitude. So, from the above equations, the power factor angle that can be applied to the proposed converter is 90^o. However, this value depends on the impedance network rating as well. For ripple in the inductor current (Δ), the minimum value of DC-link current and maximum current of

i_{DC2} are given in equation (5.15).

$$i_{DC1} = (1-\Delta)\frac{1}{1-2d_{st}} i_{DC2}, \quad i_{DC2max} = \hat{I}_{om} \tag{5.15}$$

For positive capacitor current,

$$i_{DC1} - i_{DC2} = (1-\Delta)\frac{1}{1-2d_{st}} i_{DC2} - \hat{I}_{om} \geq 0 \tag{5.16}$$

The minimum load power factor that can be applied is

$$cos(\phi_o) = \frac{(1-2d_{st})}{\sqrt{3}(1-d_{st})(1-\Delta)} \tag{5.17}$$

For $L = 3\ mH$, $C = 120\ \mu F$, the minimum power factor angle that can be applied to the proposed converter is 60^o. Beyond this value, the converter goes into a nonzero discontinuous current mode (NZ-DCM) [110], as shown in Figure 5.6. During this mode, the voltage across inductor $V_L = 0$. Since $V_C > V_{pq}$, D_2 is in reverse bias. Hence, capacitor C is un-clamped, eventually boosting output voltage and higher capacitor stress. Equation (5.18) gives the voltage across the capacitor in NZ-DCM. Here d_1 is the duty ratio of the NZ-DCM.

$$V_C = \frac{1-d_1}{1-2d_{st}-d_1} V_{pq} \tag{5.18}$$

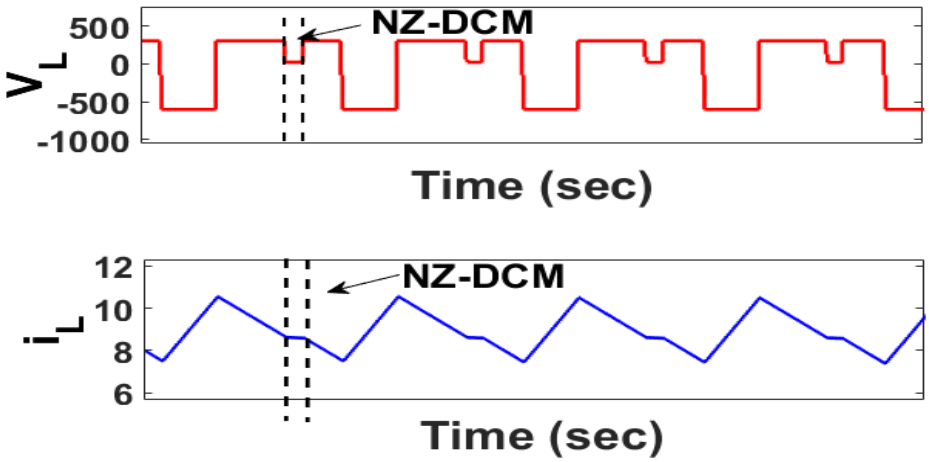
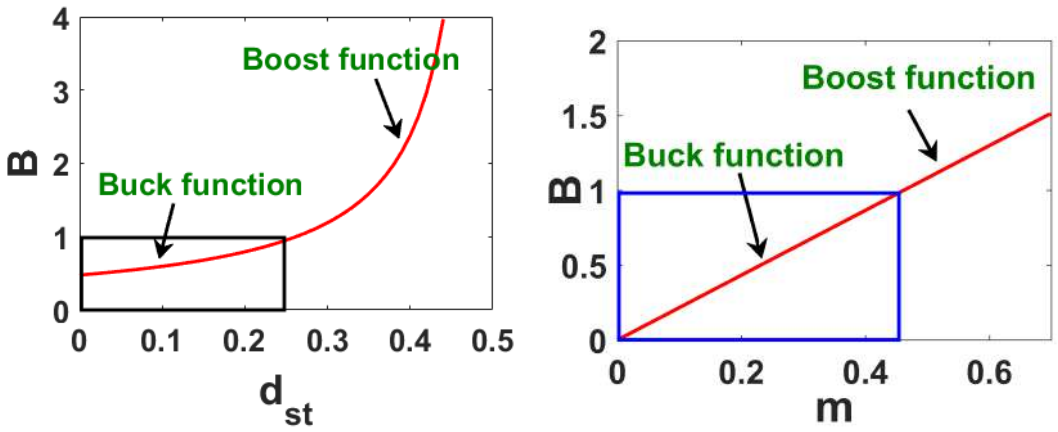


Figure 5.6: Voltage and current profile of inductor in NZ-DCM



(a) (b)

Figure 5.7: Variation of boosting factor a) with d_{st} at $m = 0.55$, b) with m at $d_{st} = 0.3$

5.4.2 Relation between m and d_{st}

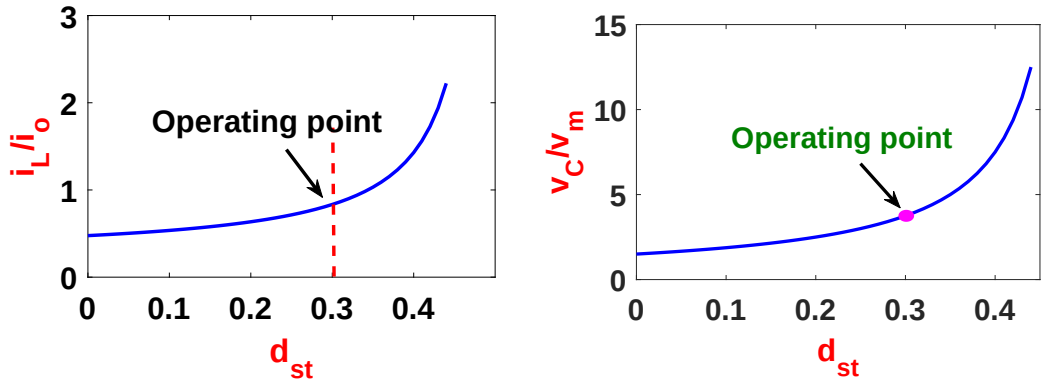
For the linear operation between the shoot-through duty ratio (d_{st}) and modulation index (m), d_{st} doesn't overlap with the active interval of the SB-USMC. So d_{st} should be placed within the zero vector interval of the SB-USMC. So, the total width of the d_{st} does not exceed the zero vector interval d_0. Hence, the maximum shoot-through duty ratio is

$$d_{stmax} = d_0 \tag{5.19}$$

The sum of the active and zero vector intervals is unity ($d_0 + m = 1$). So, from the above equations, $d_{st} + m \leq 1$.

5.4.3 Overall voltage gain of the proposed converter

From equation (5.9), the overall boosting factor ($B = \frac{\sqrt{3}m}{2}\frac{1}{1-2d_{st}}$) of the proposed converter depends on both d_{st} and m. The maximum d_{st} that can be applied to the proposed converter is 0.5. Figure 5.7(a) shows the variation of B by changing d_{st} from 0 to 0.45 at $m = 0.55$. To get a boosting factor more than unity, $d_{st} > 0.25$ is observed. Figure 5.7(b) shows that voltage gain greater than unity m should be greater than 0.45. Considering the above conditions, d_{st} and m are chosen as 0.3 and 0.7, respectively. For these values, the overall voltage gain is 1.514.



(a) (b)

Figure 5.8: Variation of a) current stress through inductor, b) voltage stress across capacitor with d_{st}

5.4.4 Voltage and current stresses of the passive components

The main advantage of the proposed converter is having only one inductor and one capacitor in the impedance network. The current and voltage stresses of the proposed converter are shown in Figure 5.8(a) and Figure 5.8(b), respectively. The capacitor voltage is only a function of the shoot-through duty ratio, increasing steadily up to $d_{st} = 0.3$. For $d_{st} = 0.3$, the voltage across the capacitor is 3.75 times the supply phase voltage. The inductor current depends on both the modulation index and shoot-through duty ratio. Similarly, the inductor current stress profile also increases steadily up to $d_{st} = 0.3$, after which higher values are obtained for a slight variation in d_{st}.

5.5 Simulation and Experimental Results

5.5.1 Simulation Results

The proposed converter has been validated through MATLAB software with 100 V, 50 Hz input to deliver 150 V, 100 Hz load at 2 kW power. Other important parameters are given in Table 5.2. By supplying 100 V to the CSR, the rectified voltage is pulsed between the two largest line voltages which is shown in Figure 5.9. The maximum peak to peak voltage is observed as 88 V, which is varied from 173.2 V to 85 V with a mean average of 149.6 V with a frequency six times the supply frequency. It acts as a supply to the switched boost network. During ST mode, boosted voltage attains zero voltage

Table 5.2: Parameters for the simulation

S. no	*Parameter*	*Value*
1	Input voltage	100 V
2	Input frequency	50 Hz
3	d_{st}, m	0.3, 0.7
4	SB Inductor (L)	3 mH
5	SB capacitor (C)	120 uF
6	Output frequency	100 Hz
7	Power Rating	2 kW
8	Switching frequency	5 kHz

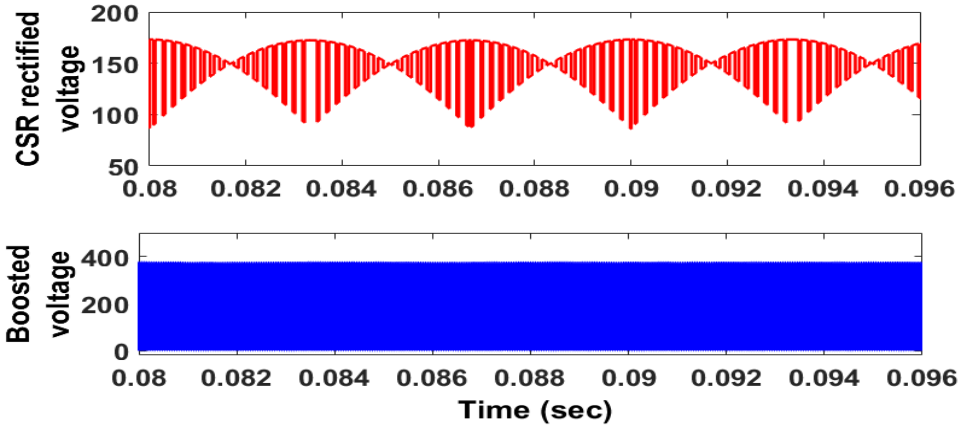


Figure 5.9: Rectifier and SB network output voltages

due to the shorting of the VSI leg. During the NST state, it attains capacitor voltage. For the shoot-through duty ratio of 0.3, the measured boosted voltage is 372 V in NST mode and 0 V in ST mode, as shown in Figure 5.9. Figure 5.10 shows the voltage stress across diodes D_1, D_2 and inductor current. During ST mode, both diodes are in OFF and blocking the voltage of 372 V. The inductor current increases and reaches the maximum value (15.42 A). During NST mode, the inductor delivers energy and its current reaches to a minimum value (12.8 A). Diodes are in forwarding conduction mode. The capacitor voltage, voltage stress across switch S, and impedance network output voltage ($V_{p'q'}$) are shown in Figure 5.11. Capacitor voltage maintains a constant

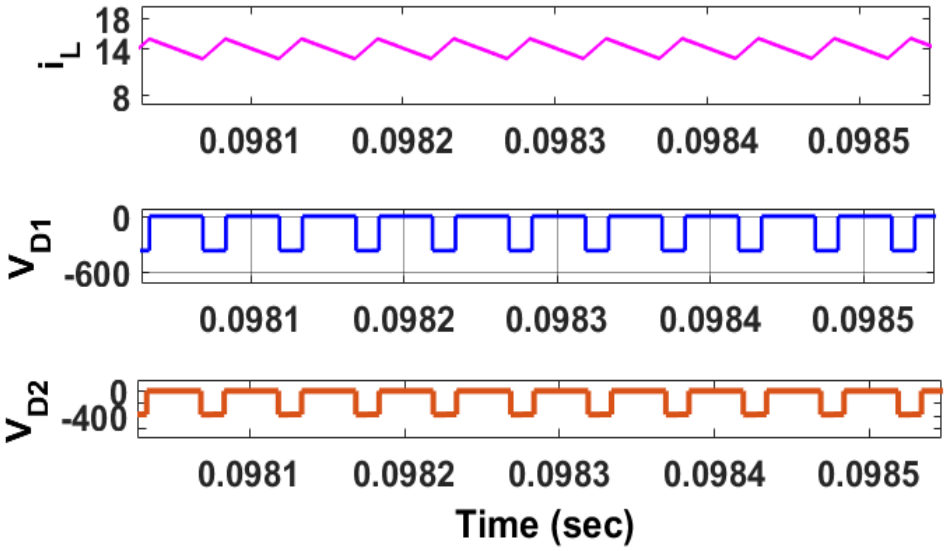


Figure 5.10: Behaviour of the inductor current, diode voltages

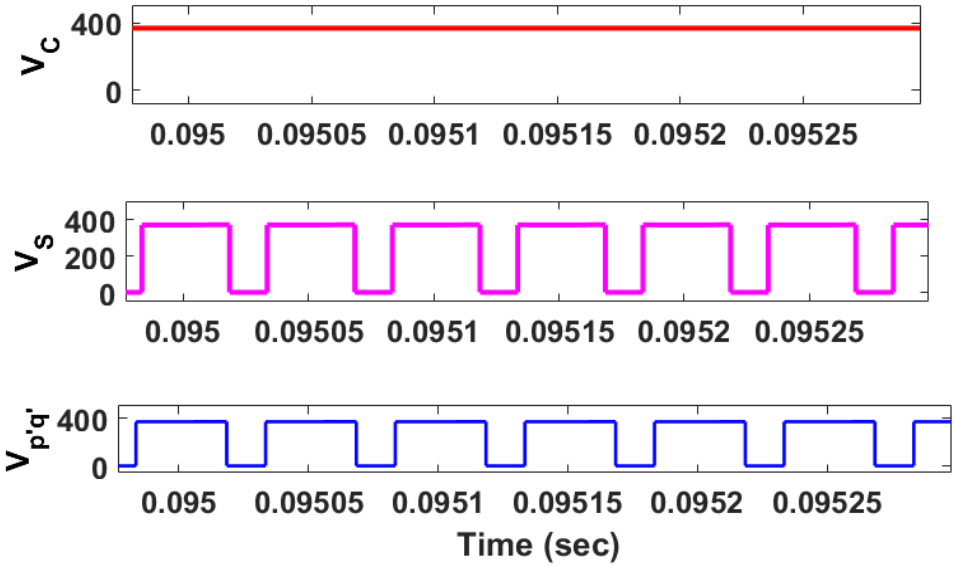


Figure 5.11: Voltage across capacitor, switch and SB output

value at 372 V. During ST mode, switch S is ON and the boosted voltage ($V_{p'q'}$) attains zero voltage due to a short circuit. During NST ($V_{p'q'}$) is getting 372 V due to the parallel connection with a capacitor. By choosing ($m = 0.7$) the maximum phase output voltage is 150 V, which is shown in Figure 5.12. By varying the modulation index, voltage gain can vary with a limitation of $m + d_{st} \leq 1$.

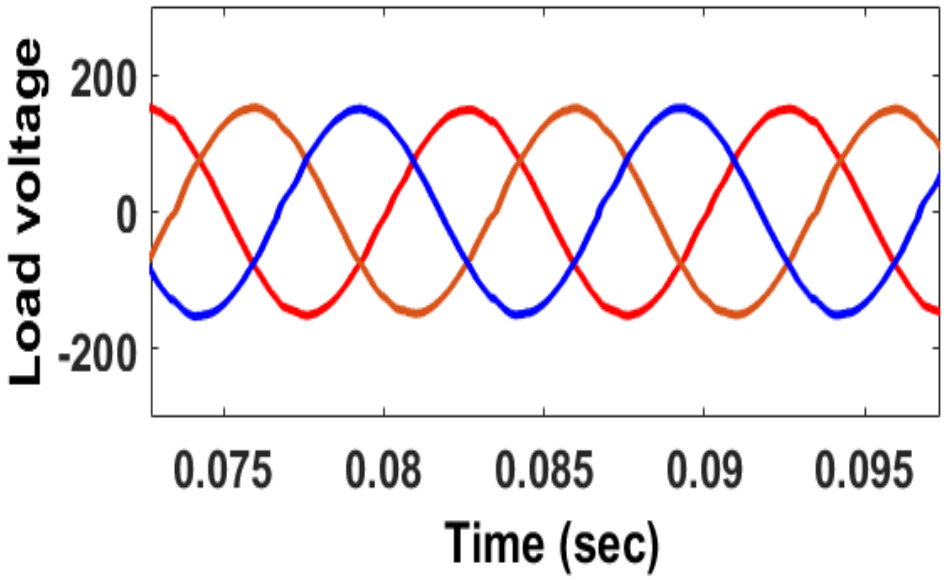


Figure 5.12: Three phase output voltages of the proposed converter

5.5.2 Experimental Results

The experiment has been carried out to support the proposed converter. Figure 5.13 shows the proposed converter experimental prototype. High-frequency SVM technique

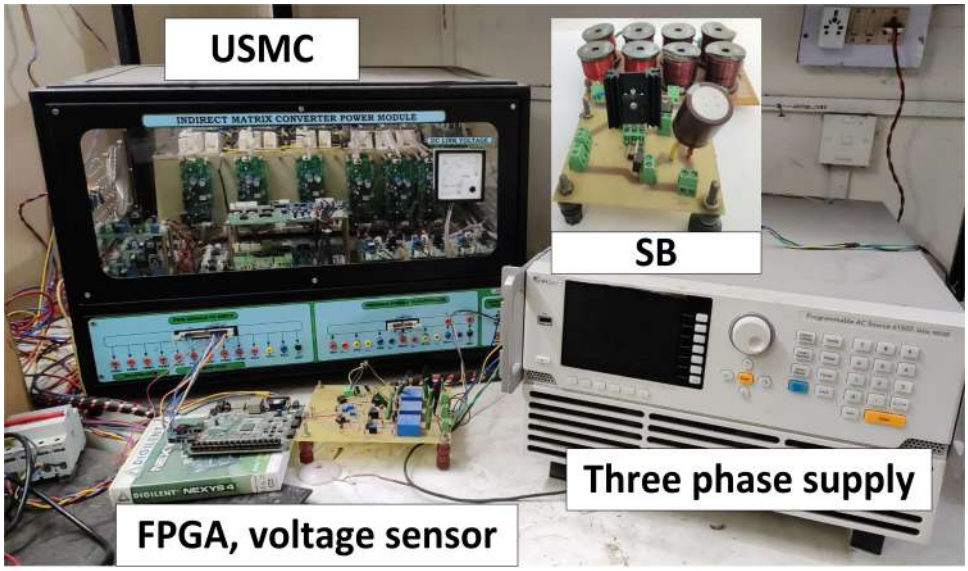


Figure 5.13: Experimental setup for the proposed method

pulses are generated by using the Atrix7100CGS324-1 FPGA board. This experiment has been conducted with the input phase supply $\hat{V}_{an} =$ 46 V, 50 Hz at 250 W load power. The remaining parameters are the same as the simulation parameters. By supplying this input to the CSR, a rectified output voltage with an average value of 69

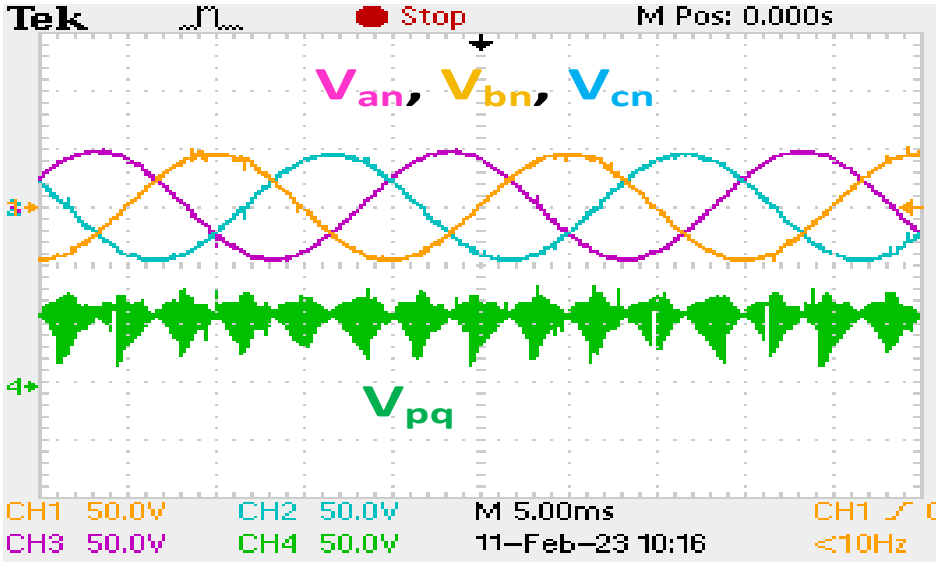


Figure 5.14: Input supply and CSR output voltage

V is obtained. The obtained voltage is pulsating in nature with a frequency six times the supply frequency (50 Hz). The nature of the rectified output voltage is shown in Figure 5.14. Considering shoot-through duty ratio and modulation index are 0.3 and 0.7, respectively. Voltage stress across the impedance network switch and diode D_2 is depicted in Figure 5.15. From Figure 5.15, during ST mode inductor current is rising

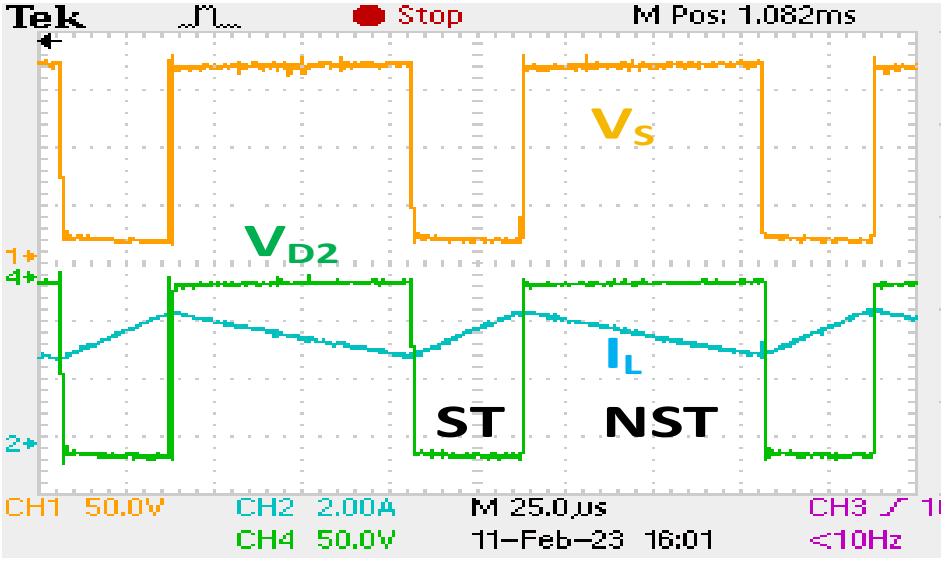


Figure 5.15: Voltage across the switch, diode $D2$ and current through inductor

and reached 4.2 A, during NST mode inductor current falls to 2.8 A. These maximum and minimum values of the inductor current changes (within one complete cycle) with respect to CSR rectified voltage is clearly observed in Figure 5.16. Figure 5.17 shows

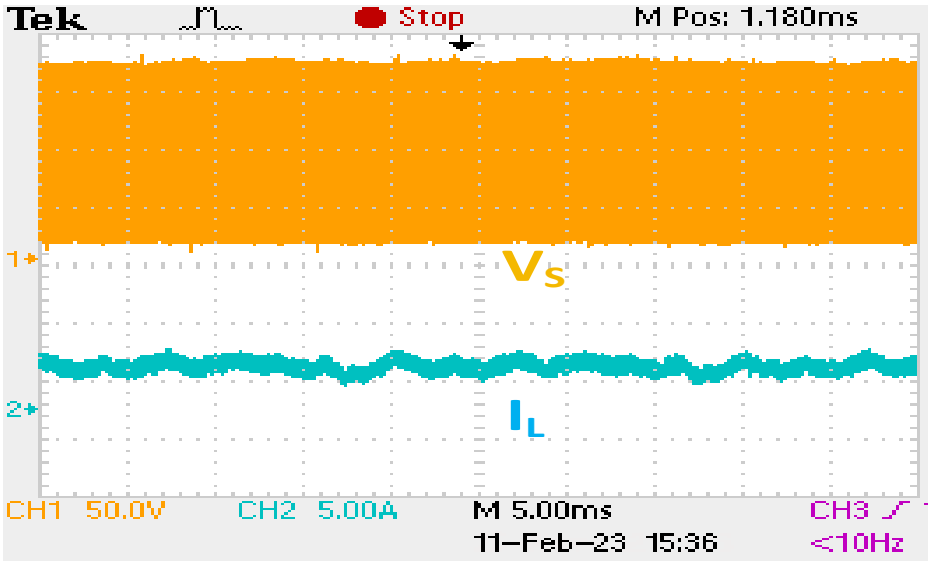


Figure 5.16: Voltage across the switch and inductor current

the impedance network boosted voltage and voltage stress across the diode D_1. During the ST mode, boosted terminals are shorted so the voltage is zero and the diode attain 168 V blocking voltage. In the same manner, during the NST mode boosted voltage

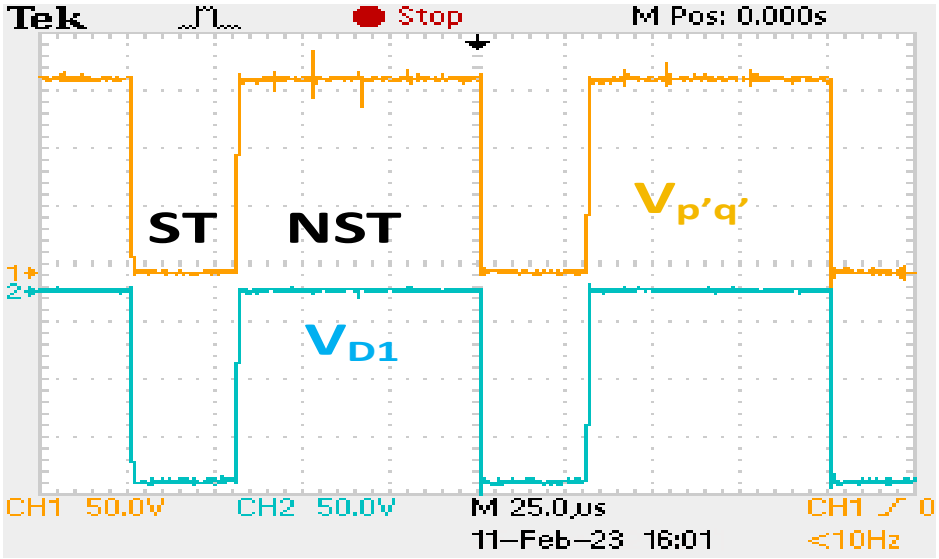


Figure 5.17: Impedance network boosted voltage and voltage across diode D_1

is 168 V which acts as a source for VSI. Voltage stress across diode D_1 is measured as 168 V. During both (ST & NST) modes, the capacitor maintains the same voltage level which is equal to 168 V, as shown in Figure 5.18. From the same Figure 5.18 the measured output current is 2.4 A. The output phase voltage of the proposed converter is measured as 70 V, which is shown in Figure 5.19. The behaviour of load voltage

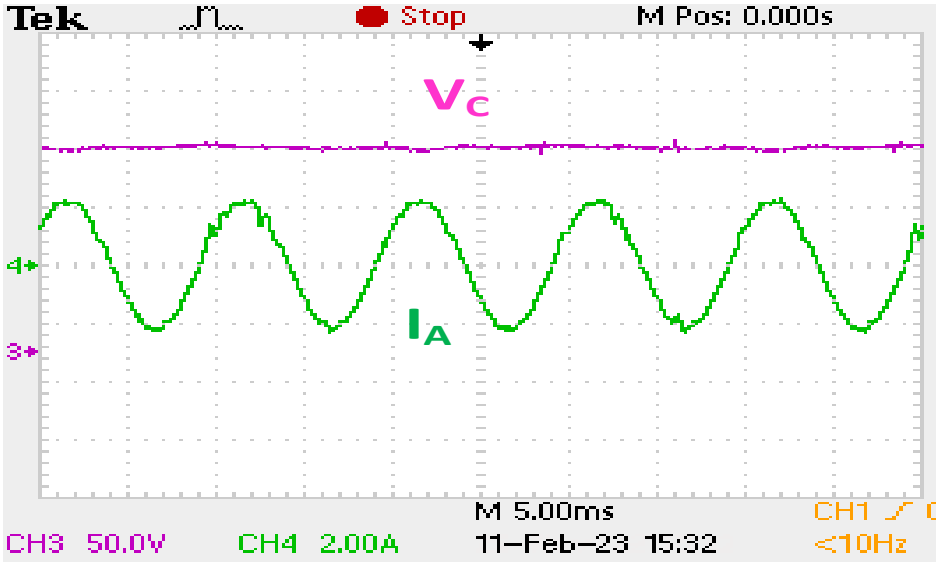


Figure 5.18: SB-USMC output current and voltage across capacitor

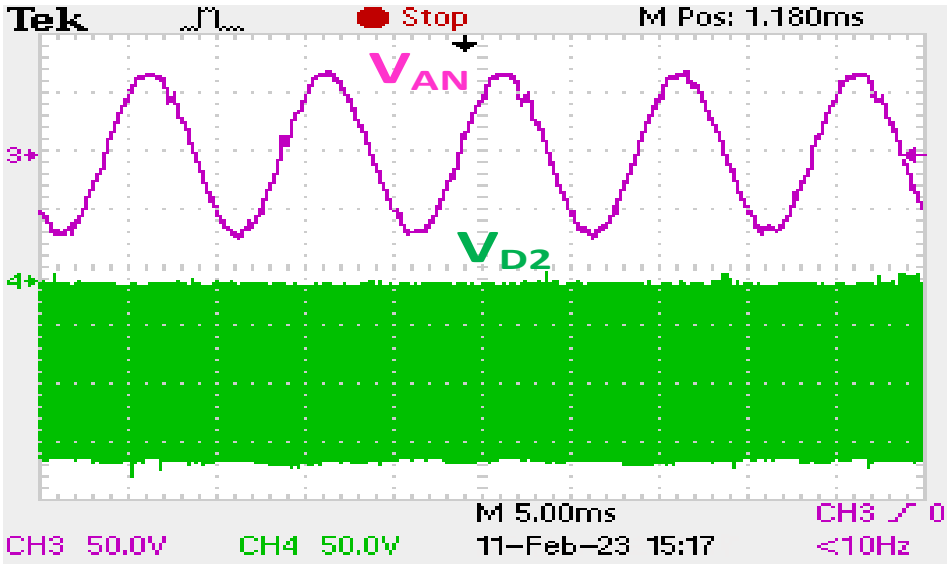
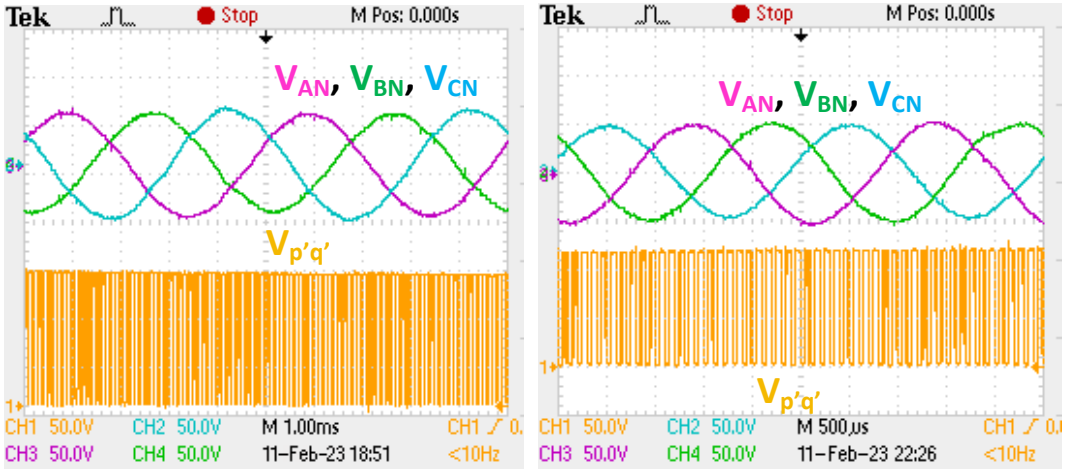


Figure 5.19: SB-USMC output voltage and voltage stress across doide D_2

under load frequency of 200 Hz and 400 Hz are shown in Figure 5.20(a), Figure 5.20(b), respectively.

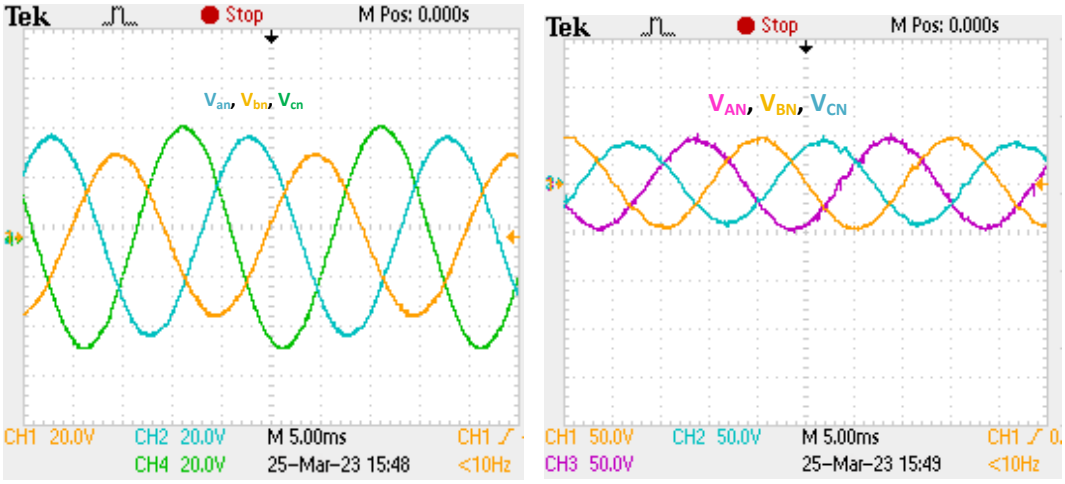
5.5.3 Unbalanced input voltage conditions

To observe the behaviour of the proposed converter under unbalanced conditions, the voltage magnitude is decreased by 10% in one phase and 20% in another phase, as shown in Figure 5.21(a). Even with an unbalanced supply, the proposed converter delivers balanced output voltage as depicted in Figure 5.21(b). This is mainly due to



(a) (b)

Figure 5.20: Experimental waveforms for the three phase load voltages with a) 200 Hz frequency, b) 400 Hz frequency



(a) (b)

Figure 5.21: Output voltages during unbalanced input voltage conditions

the presence of an impedance network between input supply and output. During ST mode, the inductor stores energy. During NST mode, the capacitor delivers stored energy to the output. Thereby the unbalanced nature of input is suppressed and provides balanced output voltages.

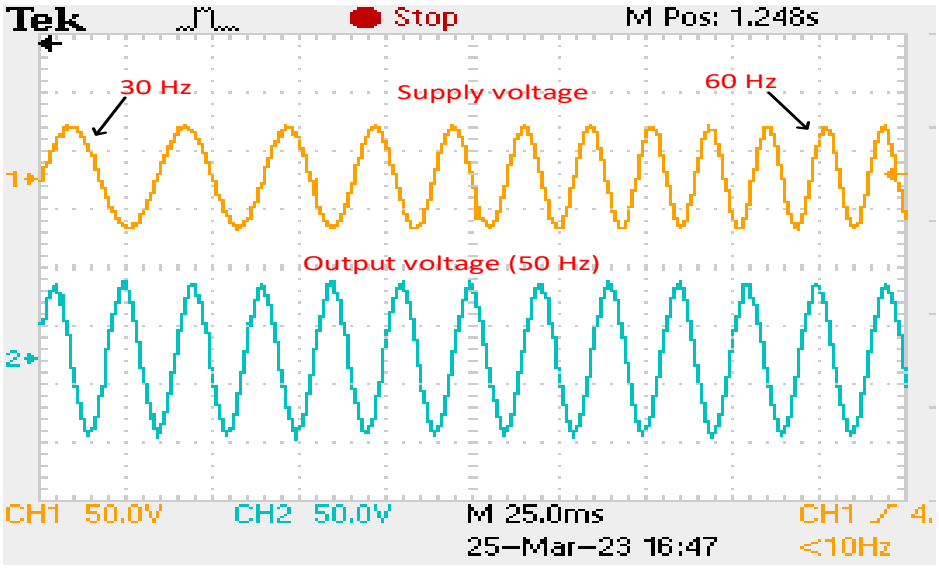


Figure 5.22: SB-USMC output voltage under input frequency variation

5.5.4 Variable input frequency analysis

To observe the suitability of SB-USMC for wind applications, it is necessary to do a variable input frequency analysis. Wind speed is not constant and changes throughout the day, which is reflected in the input frequency of the converter. So, observing the proposed converter behaviour under various input frequencies is essential. The proposed converter is tested for an abrupt shift in input frequency from 30 Hz to 60 Hz to analyze the impact of input frequency fluctuations on output frequency. Figure 5.22 shows the converter's input frequency variation from 30 Hz to 60 Hz by keeping a constant magnitude. The observed output voltage provides a constant output frequency at 50 Hz, and the output voltage at 75 V.

5.6 Comparative analysis

Converters are developed by integrating the Z source/ quasi Z source impedance network at the input side. The major concern of these converters is that they require more passive elements and switches. In addition, higher rating switches are needed in the USMC section. To overcome the above limitations, research is focussed on integrating impedance networks at the DC-link side. By integrating various impedance networks at the DC-link, different converters are proposed like cascaded Z source USMC (ZS-USMC), series Z source USMC (SZ-USMC), switched inductor Z source (SWZ-

Table 5.3: Various Z source AC-AC converters comparison table.

Converter	**Inductor current**	**Capacitor voltage**	**passive elements**	**diodes**	**switches**	**Minimum operating** $cos(\phi_o)$	**maximum** m
ZS-USMC	$I_L = \frac{\sqrt{3}m(1-d_{st})I_o}{2(1-2d_{st})}$	$V_{c1} = \frac{(1-d_{st})}{(1-2d_{st})}V_{pq}$ $V_{c2} = \frac{(1-d_{st})}{(1-2d_{st})}V_{pq}$	4	18	9	$\frac{(1-2d_{st})}{\sqrt{3}(1-d_{st})(1-\Delta)}$	$1-d_{st}$
QZ-USMC	$I_L = \frac{\sqrt{3}m(1-d_{st})I_o}{2(1-2d_{st})}$	$V_{c1} = \frac{(1-d_{st})}{(1-2d_{st})}V_{pq}$ $V_{c2} = \frac{(d_{st})}{(1-2d_{st})}V_{pq}$	4	19	9	$\frac{(1-2d_{st})}{\sqrt{3}(1-d_{st})(1-\Delta)}$	$1-d_{st}$
SZ-USMC	$I_L = \frac{\sqrt{3}m(1-d_{st})I_o}{2(1-2d_{st})}$	$V_{c1} = \frac{(d_{st})}{(1-2d_{st})}V_{pq}$ $V_{c2} = \frac{(d_{st})}{(1-2d_{st})}V_{pq}$	4	19	9	0.866	$1-d_{st}$
SWZ-USMC	$I_L = \frac{\sqrt{3}m(1-d_{st})I_o}{(1-3d_{st})}$	$V_{c1} = V_{c2} = \frac{(1-d_{st})}{(1-3d_{st})}V_{pq}$	6	24	9	$\frac{(1-4d_{st})}{\sqrt{3}(1-d_{st})(1-\Delta)}$	$1-d_{st}$
HSWZ-USMC	$I_L = \frac{\sqrt{3}mI_o}{2(1-d_{st})}$	$V_c = \frac{(1+d_{st})}{(1-d_{st})}V_{pq}$	3	22	10	$\frac{(1-4d_{st})}{\sqrt{3}(1-d_{st})(1-\Delta)}$	$1-d_{st}$
SC-USMC	$I_L = \frac{\sqrt{3}mI_o}{2(1-d_{st})}$	$V_c = \frac{1}{(1-d_{st})}V_{pq}$	3	20	10	$\frac{(1-2d_{st})}{\sqrt{3}(1-d_{st})(1-\Delta)}$	d_{st}
MQZS-USMC	$I_L = \frac{\sqrt{3}mI_o}{2(1-d_{st})}$	$V_{c1} = \frac{1-d_{st}}{(1-d_{st})}V_{pq}$ $V_{c2} = \frac{(d_{st})}{(1-2d_{st})}V_{pq}$ $V_{c3} = \frac{1}{(1-2d_{st})}V_{pq}$	5	20	10	$\frac{(1-2d_{st})}{\sqrt{3}(1-d_{st})(1-\Delta)}$	$1-d_{st}$
Proposed	$I_L = \frac{\sqrt{3}m(1-d_{st})I_o}{2(1-2d_{st})}$	$V_c = \frac{1}{(1-2d_{st})}V_{pq}$	2	20	10	$\frac{(1-2d_{st})}{\sqrt{3}(1-d_{st})(1-\Delta)}$	$1-d_{st}$

USMC), hybrid switched inductor (HSWZ-USMC), switched capacitor (SC-USMC) and modified quasi Z source (MQZS-USMC). The voltage gain of ZS-USMC, SZ-USMC, QZS-USMC and SB-USMC converter is $\frac{\sqrt{3}m}{2(1-2d_{st})}$, whereas for SC-USMC, SWZ-USMC, HSWZ-USMC and MQZS-USMC it is $\frac{\sqrt{3}m}{(1-d_{st})}$, $\frac{\sqrt{3}m(1+d_{st})}{2(1-3d_{st})}$, $\frac{\sqrt{3}m(1+d_{st})}{2(1-d_{st})}$, $\frac{\sqrt{3}m}{2}(1+\frac{1}{(1-2d_{st})})$, respectively. The maximum modulation index that can be applied to all converters except HSWZ-USMC, SC-USMC is $1-d_{st}$, and for SC-USMC is d_{st}, HSWZ-USMC is 1. For voltage gain 3, the proposed converter requires $d_{st} = 0.415$, SC-USMC requires $d_{st} = 0.63$, SWZ-USMC requires $d_{st} = 0.24$, HSWZ-USMC requires $d_{st} = 0.552$ and MQZS-USMC requires $d_{st} = 0.39$ as shown in Figure 5.23. From Table 5.3, for this operating condition, the MQZS-USMC converter shows a high inductor current stress of 2.92, SWZ-USMC attains 1.79, SC-USMC shows 1.47 and for the proposed converter, it is 1.74. The current stress of the SZ, ZS, and QZS converter is the same as that of the proposed converter. It is noted that the proposed converter requires only two passive components, and this count is higher in the remaining converters. However, the proposed SB-USMC requires one extra switch compared to ZS-USMC. The voltage and current rating of the additional switch S are the same as the capacitor voltage and inductor current ratings. The proposed converter gives a better load power factor range than the SZ-USMC. Figure 5.24 shows the efficiency plot for the proposed SB-USMC and other impedance network USMCs under similar loading conditions and the same input supply. SC-USMC shows a better efficiency profile up to the boosting

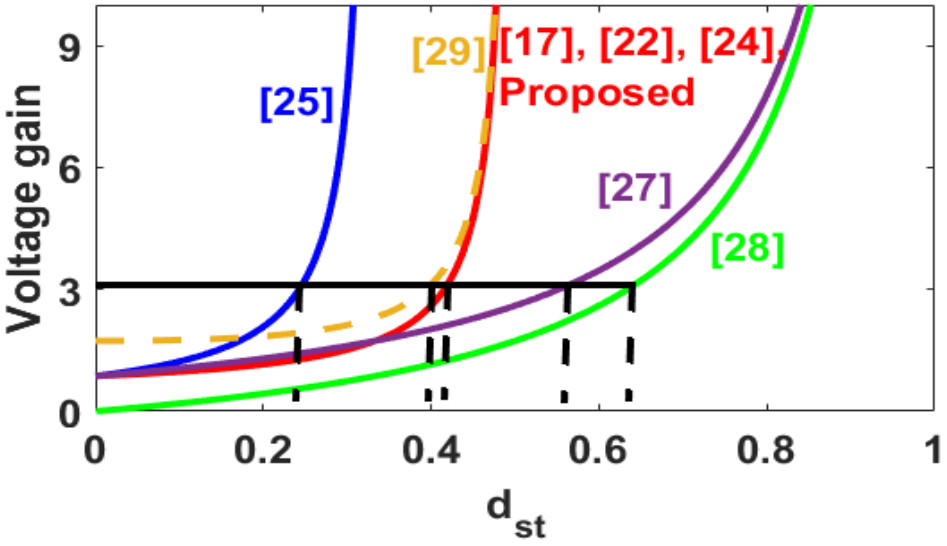


Figure 5.23: Voltage across the switch and inductor current

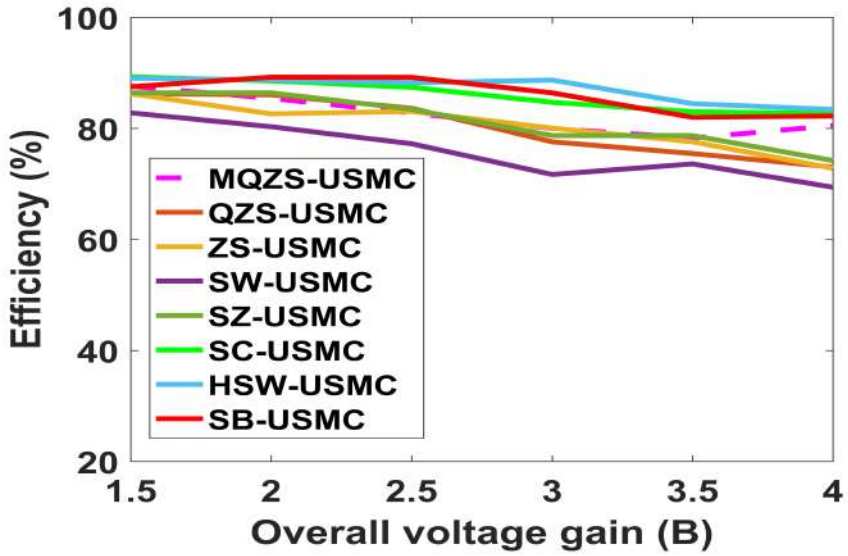


Figure 5.24: Voltage across the switch and inductor current

factor $1.4 < B < 1.7$. For the boosting factor $1.7 < B < 2.7$, proposed converter shows higher efficiency than other converters with maximum efficiency of 89 % at 2.5 boosting factor. For boosting factor $2.7 < B < 4$, HSW-USMC offers better performance.

5.7 Summary

In this chapter, a new SB-USMC is proposed to enhance the voltage gain with fewer passive components. The conventional SVM method is used to explain the working

principle and steady state operations of the SB-USMC. The proposed converter successfully operated with a 1.5 boosting factor to produce a load frequency of up to 400 Hz. Compared to the SC-USMC and SWZ-USMC, the proposed converter shows better inductor current stress. In addition, the proposed converter offers better voltage stress across the capacitor than the SWZ-USMC. The proposed SB-USMC converter reduces the required number of passive elements (only 2) in the impedance network and improves the load power factor range.

This chapter utilizes the conventional SVM technique to validate the new SB-USMC operational procedure and compare it with other existing converters. CMV analysis of the SB-USMC is not discussed in this chapter. The following chapter will address the calculation of CMV in the SB-USMC and introduce the modified Three Vector Space Vector Modulation (TVSVM) technique to alleviate peak CMV.