Chapter 3

Improved Benchmark Performance with Triangular Modulation and Quasi Single-Stage AC-DC DAB

3.1 Introduction

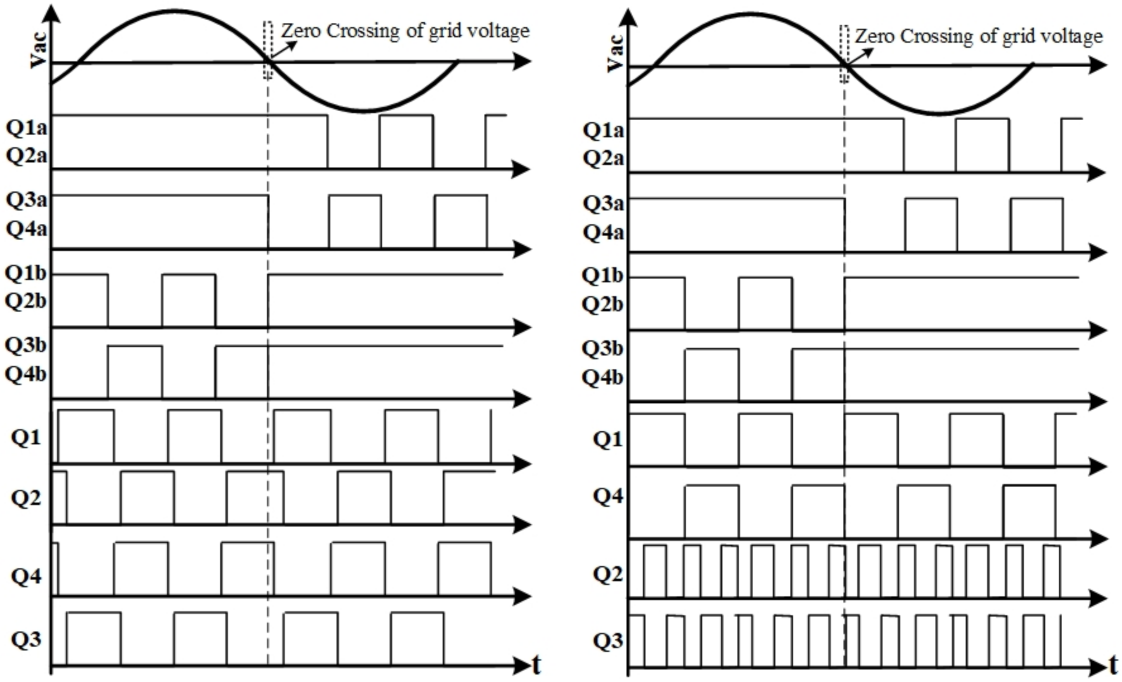
In Chapter 2, novel modulation techniques were introduced, each achievable through two distinct methods, with their realizations using a single carrier discussed in detail. While these techniques demonstrated improved soft-switching performance and ensured true soft-switching compared to conventional methods, the benchmark performance analysis was not addressed in the previous work.

This chapter explores the application of the proposed TRM technique to a different converter topology, aiming to maintain performance while further reducing computational complexity. It discusses how the number of distinct PWM signals can be minimized by implementing an asymmetrical switching sequence-based TRM in Q1S bidirectional AC-DC DAB converter with an intermediate capacitor. The investigation highlights that selecting appropriate modulation techniques, aligned with the chosen topology, can enhance control realization performance and achieve improved benchmarks using Texas

Instruments-based TMS320F28335.

In the C2000 real-time microcontroller, PWM signals are generated using the Enhanced Pulse Width Modulation (EPWM). The EPWM modules in the TMS320F28335 microcontroller are designed for precise signal generation in real-time control applications, offering adjustable duty cycles, frequency, and phase. Each of the six modules (EPWM1 to EPWM6, each generates two PWM signals) includes a time base unit with features like up/down counting, dead-time insertion, and module synchronization [152]. These modules are ideal for motor control, power converters, and digital signal processing, providing flexible control with minimal CPU intervention. However, utilizing more EPWM modules in a modulation technique increases the computational burden due to the added complexity of signal generation, synchronization, and potential phase shifts, requiring more processing resources for efficient operation. In the previous chapter, a single carrier was utilized to reduce the computational burden. In this chapter, the proposed modulation technique is introduced, demonstrating how its application to the Q1S bidirectional AC-DC DAB converter can further reduce the number of EPWM modules required.

Fig. 3.1 shows the number of PWM signals needed to generate the switching sequence for both conventional and proposed TRM using the Matrix-type AC-DC DAB Converter shown in Fig. 2.1). The figure also illustrates the nature of high-frequency signals near the grid voltage zero-crossing points. Although both TRMs require 12 distinct PWM signals (utilizing EPWM 1 to 6 with the TMS320F28335), the proposed TRM using Method 1 only needs a single carrier. The same performance can be achieved by applying the proposed TRM using Method 1 to a Q1S bidirectional AC-DC DAB converter, leading to a reduced computational burden. This can be understood from Fig. 3.2, which shows the number of PWM signals required to generate the switching sequence for both conventional and proposed TRM using the Q1S AC-DC DAB Converter shown in Fig. 3.3. The figure illustrates the nature of high-frequency signals near the grid

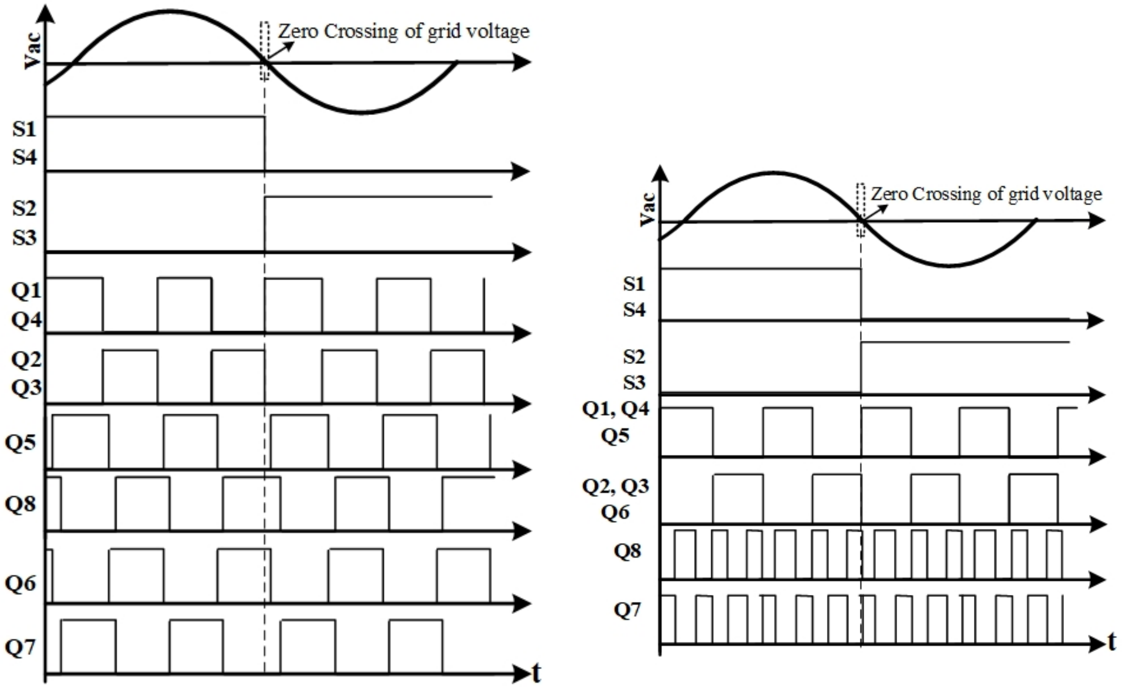


(a) (b)

Figure 3.1: Switching sequence of the Matrix-type AC-DC DAB Converter showing zoomed in view near the grid voltage zero crossing: (a) Conventional [120] (b) Proposed TRM.

voltage zero-crossing points. In both TRMs, devices S1 to S4 operate at line frequency, while Q1 to Q8 operate at high frequency. As a result, the conventional TRM requires 6 distinct PWM signals, whereas the proposed TRM requires only 4. Therefore, the conventional TRM using the Q1S AC-DC DAB Converter needs 3 EPWM modules, while the proposed method requires only 2 EPWM modules. Based on the above discussion, various modulation techniques and DAB converters are compared and summarized in a Table 3.1, highlighting the distinct EPWM required for their realization.

The existing literature predominantly imposes a higher computational burden due to the increased requirement for carriers, as discussed in the previous chapter, and EPWM modules, as discussed above. To address these challenges, this work proposes an asymmetrical switching sequence-based TRM, integrated with the mixed-device Q1S DAB topology. Research combining asymmetrical switching sequences with mixed-



(a) (b)

Figure 3.2: Switching sequence of the Q1S AC-DC DAB Converter showing zoomed in view near the grid voltage zero crossing (a) Conventional (b) Proposed TRM.

Table 3.1: Summary and Comparison with Various Converter Typologies and Modulation Techniques

Converter Topology	No of Devices	Device Operating at Line Frequency	No. of EPWM	Power Rating	Soft Switching				Control Complexity	Peak Efficiency	Remark
					Leg 1	Leg 2	Leg 3	Leg 4			
[65]	12	2	10	1.2 kW	ZVS ON ZVS OFF	ZVS ON ZVS OFF	ZVS ON HSF	ZVS ON HSF	Moderate	96.25%	Unipolar PWM with separate switching scheme for bidirectional power flow.
[70]	8	NIL	8	1.2 kW	ZVS ON HSF	ZVS ON HSF	ZVS ON HSF	ZVS ON HSF	Moderate	91.23%	TRM with one control variable and requires four carriers.
[114]	12	4	8	500 W	ZVS ON HSF	ZVS ON HSF	HSO ZCS OFF	ZVS ON HSF	Simple	92%	Three control variables with a linear power relationship.
[120]	12	^{1}4	12	1.44 kW	ZCS ON ZCS OFF	ZCS ON ZCS OFF	ZVS ON HSF	ZVS ON HSF	Simple	89.96%	TRM with single control variable and require three carriers.
[153]	8	2	6	500 W	ZVS ON HSF	NA	ZVS ON HSF	ZVS ON HSF	Complex	94.6%	Three control variables are utilized, with one of them being variable frequency.
Proposed	12	4	4	500 W	ZCS ON ZCS OFF	ZCS ON ZCS OFF	ZVS ON ZCS OFF	ZVS/ZCS ON ^{2}HSF	Simple	92.2%	TRM employing an asymmetric switching sequence with a single control variable and carrier.

HSF= Hard Switch OFF, HSO= Hard Switch ON, 1 AC side device stays ON for Half cycle of line frequency, 2 Devices undergo partial ZCS ON, NA=Not Applicable.

device topologies remains limited. Furthermore, the potential advantages of minimizing carrier count and control variables call for further investigation. The proposed approach integrates one leg of the DC side bridge with metal-oxide-semiconductor field-effect transistors (MOSFETs) and the other with insulated-gate bipolar transistors (IGBTs), highlighting its potential to enhance efficiency and reduce costs [154, 155, 156].

This chapter introduces a single-carrier asymmetric switching sequence-based TRM for the Q1S AC-DC DAB converter, which requires only four EPWM channels and is implemented using the TMS320F28335 microcontroller. In contrast to other TRMs, one leg of the DC side bridge is modulated using sinusoidally modified variable time-period PWM, while the phase shift between the PWM signal midpoints on the DC side bridge controls the power flow. Similar to method 1, the proposed TRM offers several advantages, including ZVS and ZCS during turn-on for one leg of the DC bridge operating at a variable time period, ZVS during turn-on and ZCS during turn-off for the other leg operating at a fixed frequency, and ZCS during both turn-on and turn-off for the pulsating DC bridge. Additionally, the proposed TRM supports open-loop PFC and UPF operation. A benchmark comparison between the proposed TRM and conventional TRM is also provided, highlighting the proposed method's efficiency and performance improvements. It has also been observed that the proposed TRM maintains linear efficiency across all loading conditions.

The rest of this chapter is organized as follows. The analysis, operating principle, and various modes of operation of Q1S AC-DC DAB are presented in Section 3.2. In Section 3.3, the realization and comparison of switching sequences between the conventional and proposed TRM are discussed using Q1S DAB, followed by a benchmark evaluation. The experimental results of the 500 W scale-down prototype are discussed in Section 3.4. In Section 3.5, the comparative analysis with existing literature is presented. Finally, this chapter is concluded in Section 3.6.

3.2 Analysis and Operating Principle of Q1S AC-DC DAB

The Q1S AC-DC DAB converter shown in Fig. 3.3 consists of a grid side active bridge, which is operated as an SR and a cascaded DC-DC DAB. Q1S AC-DC DAB is considered a single-stage converter because C_g is a high-frequency capacitor in the range of a few

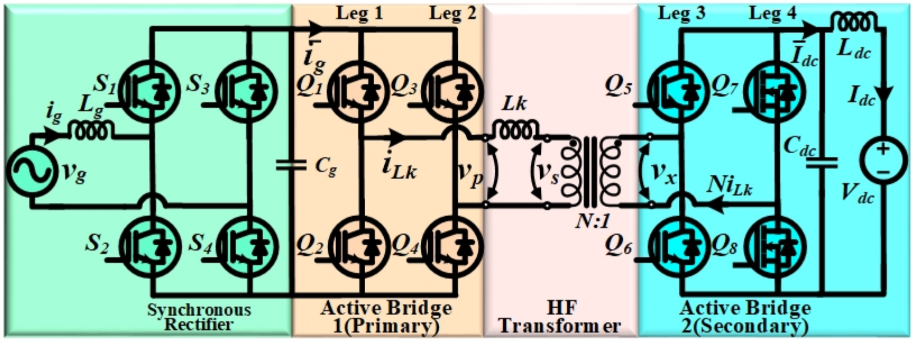


Figure 3.3: Schematic diagram of Q1S AC-DC bidirectional DAB converter.

microfarads, used as a filter between SR and DC-DC DAB, and it does not involve a bulky electrolytic capacitor. DC-DC DAB consists of two active bridges, namely the primary bridge and the secondary bridge shown in Fig. 3.3. The DC side secondary bridge has two legs, one leg operates at a fixed duty and time period (leg 3), whereas the other leg operates at a sinusoidally modified variable time period PWM (leg 4). Leg 4 consists of MOSFETs, and the remaining devices consist of IGBTs. The MOSFET is selected instead of the IGBT for Leg 4 because it operates at a frequency at least three times higher than the other switches, as shown in Fig. 3.4. L_k is the leakage inductance referred to the primary side of the transformer, which has a turn ratio of $N:1$. C_{dc} and L_{dc} are the DC side filter.

Fig. 3.4 shows the principle operating waveform of the proposed asymmetric switching sequence TRM. Duty ratio *k(t)* governs PFC/UPF operation of the Q1S AC-DC DAB and is given by (3.1).

$$k(t) = \left|\frac{v_g}{NV_{dc}}\right| = \frac{V_g}{NV_{dc}}\left|\sin\left(2\pi f_g t\right)\right| \tag{3.1}$$

Where v_g is the instantaneous grid voltage, which equals $V_\mathrm{g}\sin(2\pi f_\mathrm{g}t)$, V_dc is the output DC voltage, and $k(t)$ is the duty ratio responsible for generating the PWM for Leg 4 of the DC-side full bridge. The maximum value of $\hat{k}$ is given by $\frac{V_\mathrm{g}}{NV_\mathrm{dc}}$. By choosing the appropriate turn ratio, it is possible to operate the converter in either buck or boost

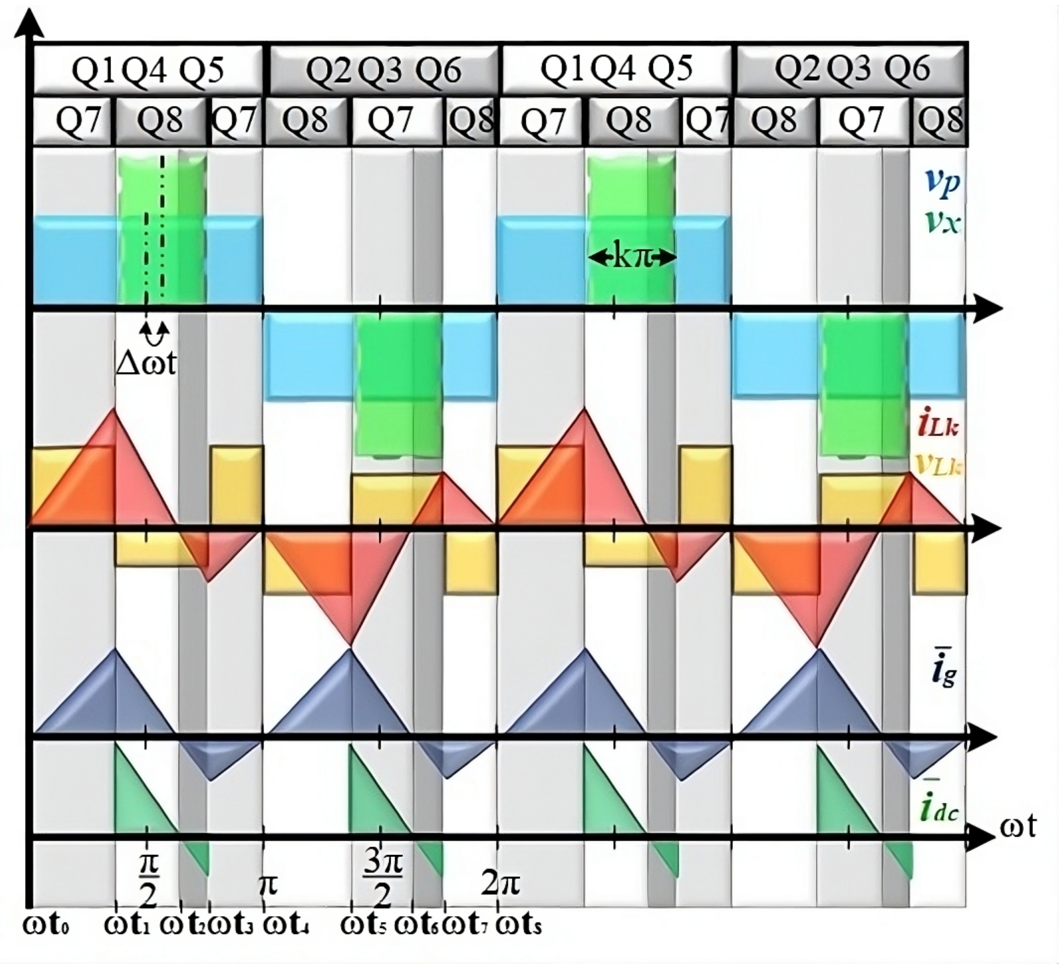


Figure 3.4: Key operating waveform of proposed TRM.

mode. A phase shift ratio γ is responsible for the direction and the amount of power flow, which is given by (3.2).

$$\gamma = \frac{2\Delta\omega t}{\pi} \tag{3.2}$$

The $\Delta\omega$t is the phase shift measured from the midpoint of primary transformer voltage (v_p) and secondary transformer voltage (v_x) as shown in Fig. 3.4. The term $\omega = 2\pi F_s$, where F_s is the switching frequency. The range of γ is from -(1-$\hat{k}$) to (1-$\hat{k}$), which is responsible for the amount of power transfer from one side to another side and considered positive when power is delivered from AC to DC side. The secondary voltage v_x is reflected to the primary side, represented as v_s. It must be considered that

$v_p/v_s < 1$. Various transformer voltages appear across various switching instances as shown in Fig. 3.4, and are given by (3.3) and (3.4).

$$v_p = \begin{cases} v_g & 0 < t \leqslant \pi/\omega \\ -v_g & \pi/\omega < t \leqslant 2\pi/\omega \end{cases} \tag{3.3}$$

$$v_x = \begin{cases} 0, 0 < t \leqslant \frac{\pi}{2\omega}\left(1+\gamma-k\right) \\ V_{dc}, \frac{\pi}{2\omega}\left(1+\gamma-k\right) < t \leqslant \frac{\pi}{2\omega}\left(1+\gamma+k\right) \\ 0, \frac{\pi}{2\omega}\left(1+\gamma+k\right) < t \leqslant \frac{\pi}{2\omega}\left(3+\gamma-k\right) \\ -V_{dc}, \frac{\pi}{2\omega}\left(3+\gamma-k\right) < t \leqslant \frac{\pi}{2\omega}\left(3+\gamma+k\right) \\ 0, \frac{\pi}{2\omega}\left(3+\gamma+k\right) < t \leqslant \frac{2\pi}{\omega} \end{cases} \tag{3.4}$$

Utilizing equations (3.3),(3.4), $v_s{=}Nv_x$, and applying the inductor volt-second balance across L_k, the current through the leakage inductance i_{Lk} at various instances is given by

$$i_{Lk}(t_0) = i_{Lk}(t_4) = i_{Lk}(t_8) = 0 \tag{3.5}$$

$$i_{Lk}(t_1) = -i_{Lk}(t_5) = \frac{v_g(1-k+\gamma)\pi}{2\omega L_k} \tag{3.6}$$

$$i_{Lk}(t_3) = -i_{Lk}(t_7) = -\frac{v_g(1-k-\gamma)\pi}{2\omega L_k} \tag{3.7}$$

Using (3.5),(3.6),(3.7), the average input current $\bar{i}_{\mathrm{g}}$ over half switching cycle is given by

$$\bar{i}_g(t) = \frac{1}{\pi}\int_0^{\pi} i_{Lk}(\theta)d\theta = \frac{\pi\gamma N V_{dc} k(t)}{2\omega L_k} \tag{3.8}$$

The $\bar{i}_{\mathrm{g}}$ is the function of $k(t)$, so $\bar{i}_{\mathrm{g}}$ is sinusoidal and has the same phase as the voltage, resulting in PFC/UPF operation. Similarly, using power balance the average output current ($\bar{i}_{\mathrm{dc}}$) and average output power ($\bar{P}_{\mathrm{dc}}$) over half switching cycle is given by

$$\bar{i}_{dc}(t) = \frac{\pi\gamma N v_g k(t)}{2\omega L_k} = \frac{\pi\gamma V_g^2 \sin^2(\omega_g t)}{2\omega L_k V_{dc}} \tag{3.9}$$

$$\bar{P}_{dc}(t) = \frac{\pi\gamma N v_g V_{dc} k(t)}{2\omega L_k} = \frac{\pi\gamma V_g^2 \sin^2(\omega_g t)}{2\omega L_k} \tag{3.10}$$

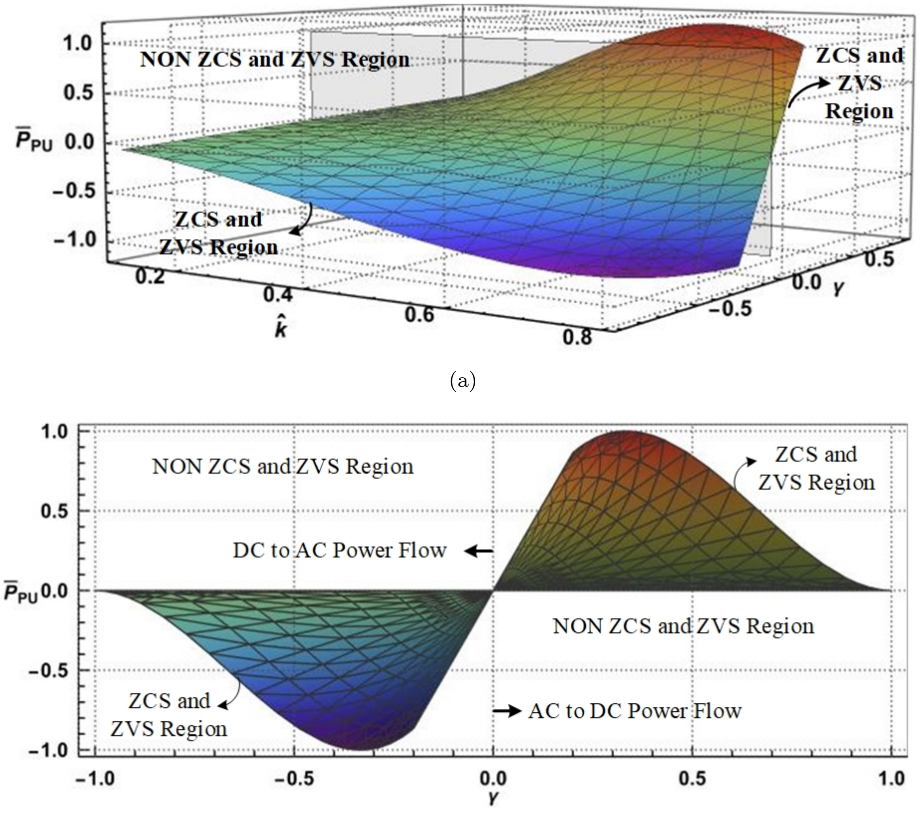
From the equation (3.9) and (3.10) it can be observed that the $\bar{i}_{\mathrm{dc}}(t)$ and $\bar{P}_{dc}(t)$ are pulsating in nature. The average power over one cycle of line frequency is expressed as (3.11).

$$\bar{P}_{dc,avg}(t) = \frac{\pi\gamma N v_g V_{dc} k(t)}{2\omega L_k} = \frac{\pi\gamma V_g^2}{4\omega L_k} \tag{3.11}$$

It can be concluded from (3.11) that the average power in either direction is a linear function of the γ. The average power in per unit ($\bar{P}_{PU}$) over the full cycle of grid frequency as a function of $k(t)$ and γ is plotted and shown in Fig. 3.5(a). A plane divided $\bar{P}_{PU}\sim\gamma$ plot showing the direction of power. Moreover, Fig. 3.5(b) displays the front view of Fig. 3.5(a), illustrating $\bar{P}_{PU}$ as a function of γ. $\bar{P}_{PU}$ is selected in such a way that the maximum power of 1 PU appears at γ=1/3 and $\hat{k}$=2/3. Additionally, the plot shows the region where soft switching occurs, which is defined by the condition -(1-$\hat{k}$)$\leqslant\gamma\leqslant$(1-$\hat{k}$), and the empty space where soft switching is lost when this condition is not met. Also, both γ and $\hat{k}$ are inversely related.

3.2.1 Operation of Q1S DAB Using Proposed Technique

The Q1S DAB is operated using the proposed modulation technique, and for $v_g>0$ and $i_g>0$, modes of operation are shown in Fig. 3.6. The switching frequency is much greater than the grid frequency $(F_s>>f_g)$ and the power is delivered from AC to the DC side. The modes of operation are shown and discussed for half switching cycle ($0<\omega t\leq\pi$), and the modes of operation are the same for the other half of the cycle. Since $v_g>0$ so, $S1$ and $S4$ remains ON for all the modes. It is noteworthy to mention that the body



(a)

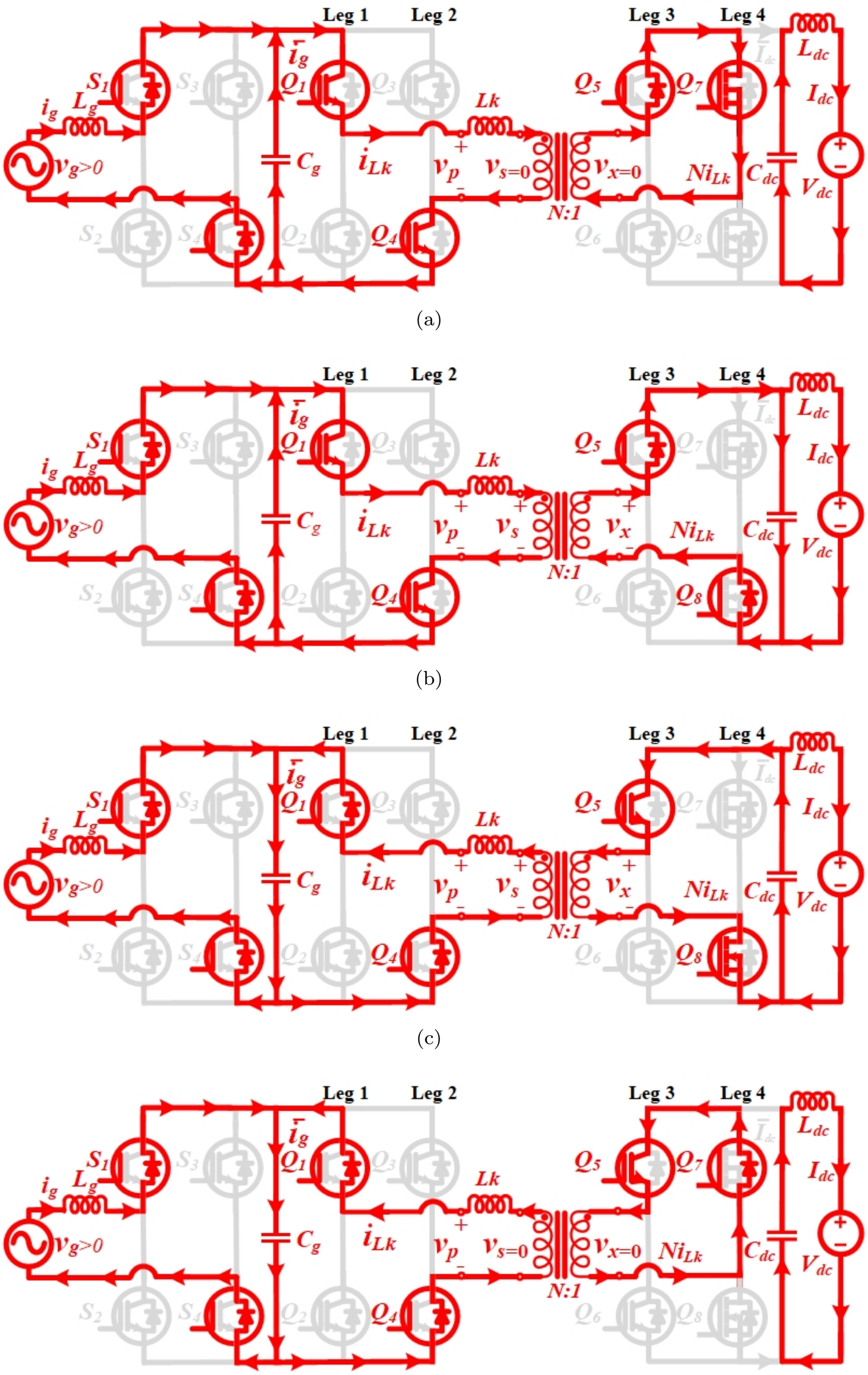
(b)

Figure 3.5: Plot showing soft switching region (a). Avenge power in per unit ($\bar{P}_{PU}$) as a function of $\hat{k}$ and γ (b). Front view showing $\bar{P}_{PU}\sim\gamma$.

diode of the device Qx is referred to as Dx (x=1, 2...8), and the direction of all the currents is considered positive as referred in Fig. 3.3.

Mode 1 [t_0 −t_1]: In this mode, the gate pulses of the devices $Q1$, $Q4$ of the primary side bridge and $Q5$, $Q7$ of secondary side bridge is applied. On the primary side, v_g appear as v_p and current i_{Lk} flows through $Q1$, L_k, primary of the transformer and $Q4$. On the secondary side, v_x=0 and the current Ni_{Lk} flows through the secondary of the transformer, $D5$, and $Q7$ as shown in Fig. 3.6(a). Since, $i_{Lk}(t_0)$ is zero hence $Q1$, $Q4$, and $Q7$ turn ON at zero current and slope of i_{Lk} is positive.

Mode 2 [t_1 −t_2]: In this mode, the gate pulse to device $Q7$ is removed and $Q8$ are applied. On the primary side i_{Lk} flows in the same way as in the previous mode. On the secondary side, now v_{dc} appears as v_x, and the current Ni_{Lk} flows through the



(a)

(b)

(c)

(d)

Figure 3.6: Equivalent circuits of the Q1S DAB using proposed modulation technique (a). Mode 1 $[t_0 - t_1]$. (b). Mode 2 $[t_1 - t_2]$. (c). Mode 3 $[t_2 - t_3]$. (d). Mode 4 $[t_3 - t_4]$.

secondary of the transformer, $D5$ and $D7$ as shown in Fig. 3.6(b). The slope of i_{Lk} now becomes negative.

Mode 3 [t_2 −t_3]: The mode 3 is shown in Fig. 3.6(c), the current i_{Lk} becomes negative at time t_2. The secondary device $Q5$ and $Q8$ is now turned ON at zero voltage. On the primary side, the current i_{Lk} flows through the primary of the transformer, L_k, $D1$, C_g, and $Q4$ as in the previous mode. On the secondary side, the current Ni_{Lk} flows through secondary of transformer, $Q8$, C_{dc} and $Q5$. The slope of the i_{Lk} remains negative till t_3.

Mode 4 [t_3 −t_4]: In this mode, the gate pulse to device $Q8$ is removed and $Q7$ is applied. On the primary side, the current flows in the same direction as in the previous mode however, on the secondary side v_x=0 and the current Ni_{Lk} flows through the secondary of the transformer, $D7$ and $Q5$ as shown in Fig. 3.6(d). The slope of i_{Lk} will change to positive till i_{Lk} reaches zero at time t_4.

3.3 Realization and Comparison of Switching Sequence for Q1S DAB

3.3.1 Realization of Conventional TRM

The conventional TRM is based on the inner mode of duty cycle modulation of a single H-bridge [120], and the typical block diagram of the switching sequence is shown in Fig. 3.7. To realize the conventional switching sequence for Q1S DAB, three EPWM modules (each module has two channels, i.e., A, B, C, and their complements shown in Fig. 3.7) are required. The EPWM modules typically offer high-resolution PWM, allowing for precise control of the duty cycle of the output signal at high frequency, while general-purpose input-output (GPIO) is preferred at a lower frequency. Each EPWM module is responsible for generating two gate signals that complement each other. All the switches are operated at 50% duty, and reference (Ref) input for the EPWM block

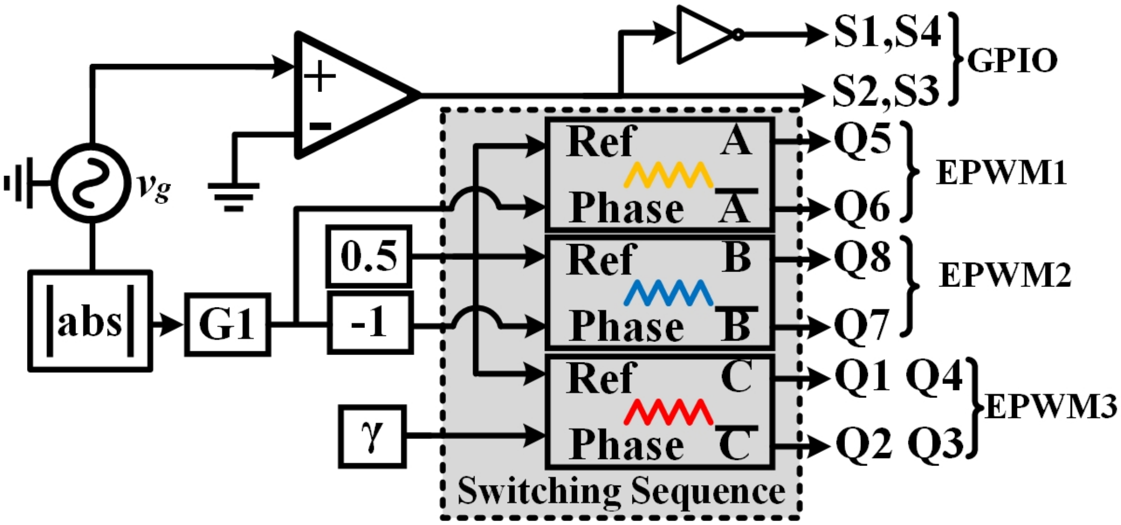


Figure 3.7: Block diagram representation of switching sequence for the conventional TRM

is provided with a duty of 0.5 as shown in Fig. 3.7. To generate the desired PWM for the secondary bridge, v_g is sensed, and the absolute value of v_g is multiplied by gain G1, which is responsible for the maximum width of secondary voltage at V_g. γ is responsible for power transfer and provides a phase shift between the primary and secondary transformer voltage.

To realize the switching sequence using the conventional modulation technique, three carriers are required as shown in Fig. 3.8 (red, yellow, and blue). It must be considered that the peak value of the up-down carrier/counter is half of the time period of the carrier generated by the DSP. In Fig. 3.8, the red carrier is shifted by γ degrees from the reference (red y-axis shown as reference). This phase shift is responsible for the direction of power flow in Q1S DAB. $k(t)$, which governs the operation of the converter responsible for advancing yellow and blue carriers away from reference and opposite to each other when perceived at any switching instance over a time period of line voltage and vice versa. Red and yellow carriers move away from each other by $\pi/4$ times $k(t)$ when the slope of $k(t)$ is positive and vice versa when the slope is negative. In the conventional technique, $k(t)$ appears as a phase reference for two carriers and is

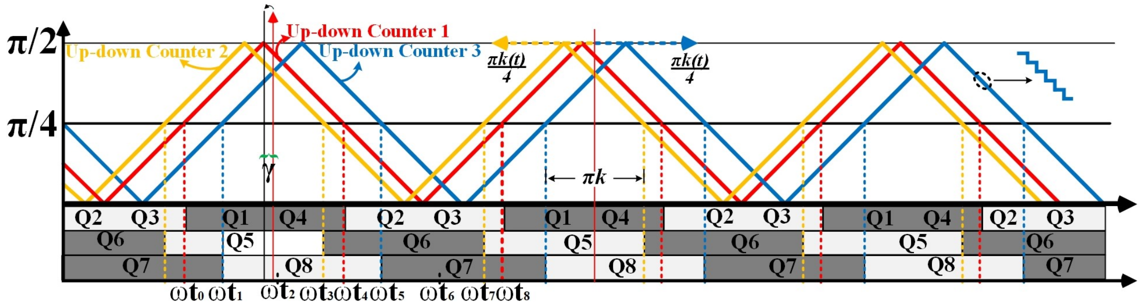
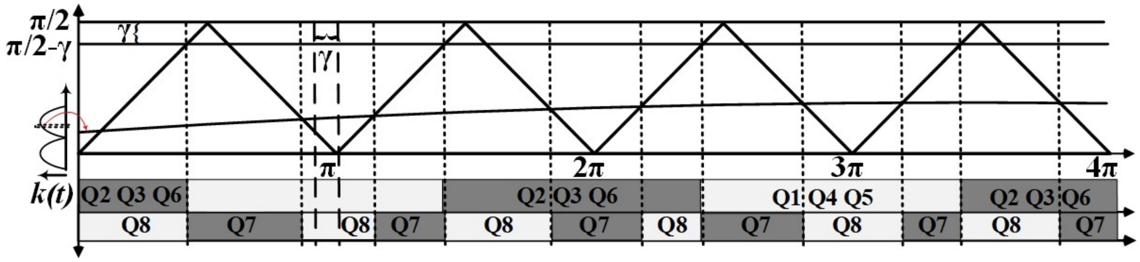


Figure 3.8: Switching sequence of the conventional TRM.

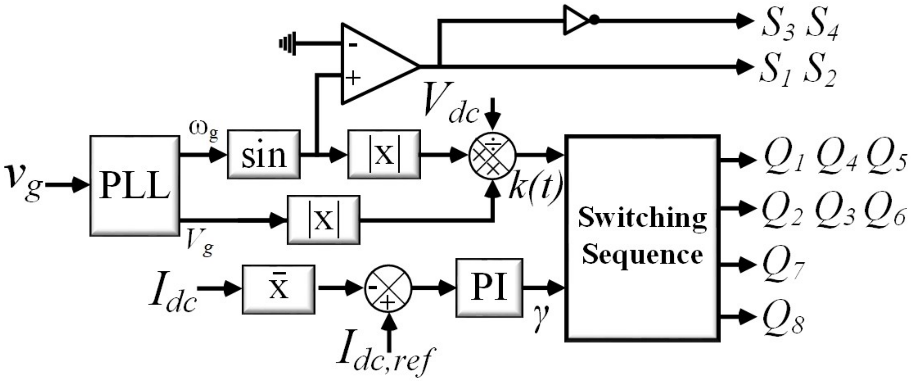
responsible for sinusoidally modulating the DC side bridge at a fixed duty and time period.

3.3.2 Realization of Proposed TRM

In the proposed TRM, instead of modulation single H-bridge, one leg of the H-bridge is modulated using sinusoidally modified variable time period PWM. In the proposed modulation technique, a single up-down carrier and two reference signals are required as shown in Fig. 3.9(a). The frequency of the up-down carrier is twice the converter switching frequency. Switching signals for the primary bridge and one leg (leg 3 in Fig. 3.3) of the secondary bridge can be obtained by toggling each time when the reference 1 $\left(\frac{\pi}{2} - \gamma\right)$ hits up-slope of the up-down counter. In contrast with the conventional technique, $k(t)$ appears as one of the references in the proposed TRM, and switching signals for another leg (leg 4 in Fig. 3.3) of the secondary bridge can be obtained by toggling each time when reference 1 hit up-slope and $m(t)$ hit up/down-slope of the up-down counter. It should be noted that in Fig. 3.9(a), $m(t) = \pi k(t)/2$ and appears constant w.r.t the high-frequency carrier. The primary bridge and one leg of the secondary bridge are operated at the same PWM at 50% duty, and another leg with a variable time period; hence, only two EPWM modules are required to generate four distinct PWM as compared to three EPWM modules in conventional TRM. Based on the proposed switching scheme shown in Fig. 3.9(a), the overall control block diagram



(a)



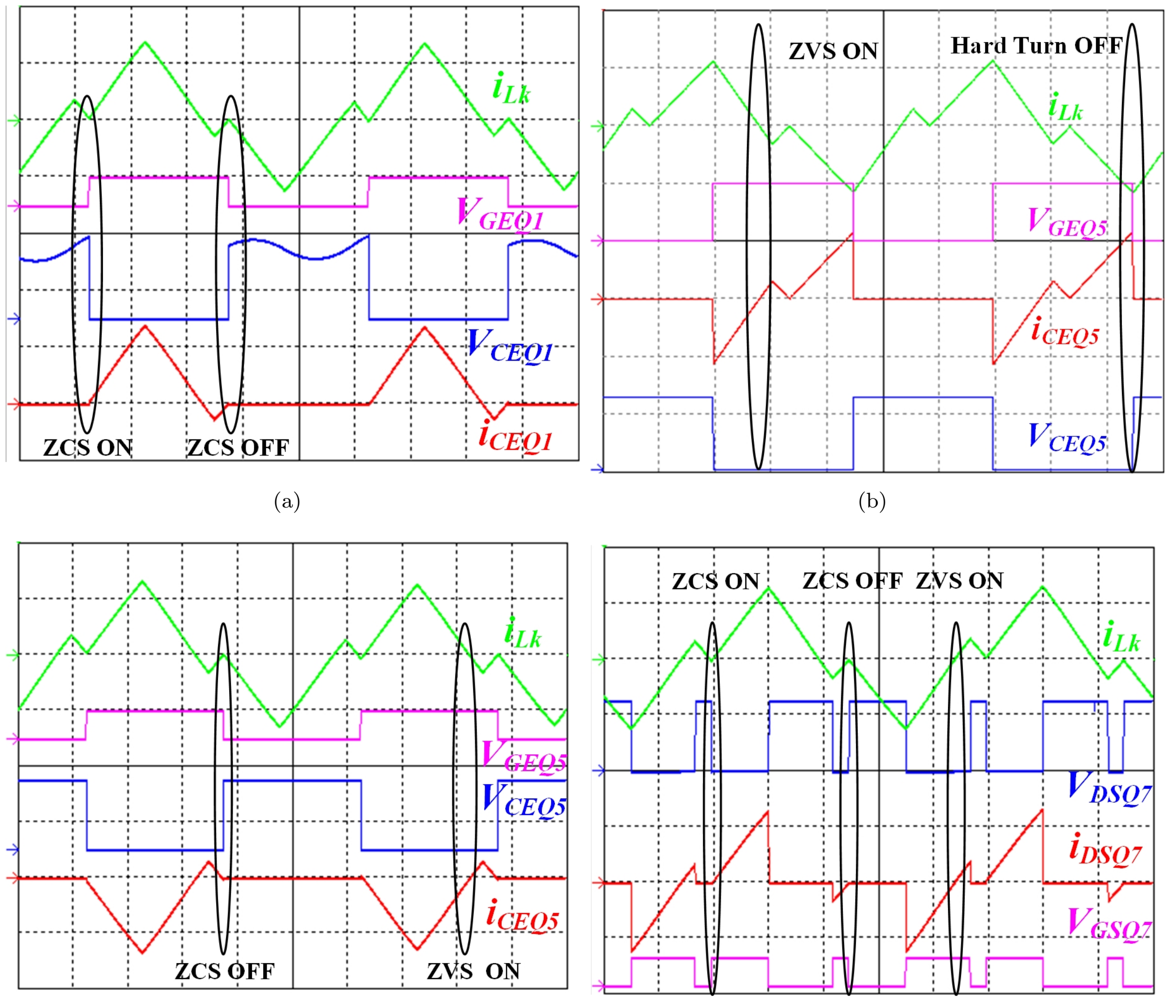
(b)

Figure 3.9: (a) Proposed switching sequence using a single carrier. (b) Overall control block diagram.

has been developed and is depicted in Fig. 3.9(b).

3.3.3 Comparison Between Conventional and Proposed TRM

The device status for both the conventional TRM and the proposed TRM is illustrated in Fig. 3.10 with device voltage, current, gate pulses, and i_{Lk}. In Fig. 3.10(a), the operational state of the primary device $Q1$ is shown, and it is the same for both the TRM. When v_{GEQ1} is applied, the device current i_{CEQ1} and i_{Lk} at that switching instance is zero. The switch $Q1$ turns ON at zero current. During turn OFF, the i_{CEQ1} and i_{Lk} which was previously flowing through the diode reaches zero, v_{GEQ1} is removed and v_g appear as v_{CEQ1} resulting in ZCS turn OFF. The status of the remaining devices on the primary side full bridge is identical to that of $Q1$. In Fig. 3.10(b), the operational state of the secondary side device $Q5$ is shown, and the device status is different from that of



(a) (b)

(c) (d)

Figure 3.10: Status of devices. (a) Primary side device $Q1$ status using both TRM. (b) Secondary side device $Q5$ status using a conventional TRM. (c) Secondary side device $Q5$ status at a fixed time period using the proposed TRM. (d) Secondary side device $Q7$ status at a variable time period using the proposed TRM.

the proposed TRM. When the gate pulse v_{GEQ5} is applied at that instance, the body diode is conducting, and the device voltage v_{CEQ5} is zero. Upon the device's current i_{CEQ5} attaining a positive value, the device initiates conduction, leading to ZVS ON. The $Q5$ undergoes a hard turn OFF using the conventional TRM, as demonstrated in Fig. 3.10(b), and the status of the remaining devices on the secondary side full bridge is identical to that of $Q5$.

The device status using the proposed TRM for devices Q_x (x=1,2..4) is the same as that of the primary side full bridge devices using conventional TRM. However, on the secondary side, the status of devices operating at the fixed and variable time periods is different. The device $Q5$ is operating at a fixed duty of 50%, and when a gate pulse is applied at that instance, the diode conducts as shown in Fig. 3.10(c). At time instance t_2, the current i_{CEQ5}, Ni_{Lk} starts to commutate from the body diode to the device, resulting in ZVS turn ON of $Q5$. Similarly, once the i_{CEQ5} reaches zero at time instance t_4, the gate pulse is withdrawn, resulting in ZCS turn OFF of device $Q5$. Similarly, variable time period devices $Q7$ and $Q8$ undergo ZCS and ZVS turn ON over the full switching period as shown in Fig. 3.10(d). Additionally, there is a time interval between t$\in$ $[t_4$ to $t_5]$ when v_{GSQ7} was present, but during this period, the diode was conducting. The brief comparison between conventional and proposed TRM is shown in Table 3.2. It should be worth mentioning that the devices $Q7$ undergo ZCS turn OFF $t = t_4$ as shown in Fig. 3.10(d). However, in the comparison Table 3.2, hard switching (HS) is mentioned with an asterisk mark.

Table 3.2: Comparison between the status of devices

Modulation Technique		**Q1**	**Q2**	**Q3**	**Q4**	**Q5**	**Q6**	**Q7**	**Q8**
Conventional TRM [120]	Turn ON	ZCS	ZCS	ZCS	ZCS	ZVS	ZVS	ZVS	ZVS
	Turn OFF	ZCS	ZCS	ZCS	ZCS	HS	HS	HS	HS
Proposed TRM	Turn ON	ZCS	ZCS	ZCS	ZCS	ZVS	ZVS	ZVS/ZCS	ZVS/ZCS
	Turn OFF	ZCS	ZCS	ZCS	ZCS	ZCS	ZCS	HS*	HS*
*Switches partially undergo ZCS turn OFF									

3.3.4 Benchmark Evaluation of Both TRM

The performance analysis of real-time code execution profiles on TI C2000 Targets in XCP external mode [157], utilizing the TMS320F28335, has been conducted for both conventional and proposed modulation techniques. The mean execution time for the conventional TRM [120] is 20.3 μs, whereas, for the proposed modulation technique, it is 17.4 μs. The code execution time demonstrates a 14% improvement with the proposed modulation, indicating its efficiency in requiring less computational time compared to conventional modulation. This improvement is due to the reduced number of carriers and EPWM modules.

3.4 Experimental Validation

A scaled-down prototype of 500 W shown in Fig. 3.11 is developed to verify the proposed modulation technique using TMDSDOCK28335. Various parameters and specifications selected for the developed prototype are shown in Table 3.3. It's worth noting that, inherently, for $N = 1$, AC to DC power flow has a boosting nature. Nevertheless, the proposed topology is designed to operate in buck mode with $N = 4$. A Metek AST1501 AC/DC power supply is used as an AC or DC source to provide the respective voltage, whereas resistance is used as a load during bidirectional power flow. Tektronix MDO3054 with MDO3PWR power analysis application module, TCP0030A current probes, and THDP0200 voltage probes are used to measure various experimental results.

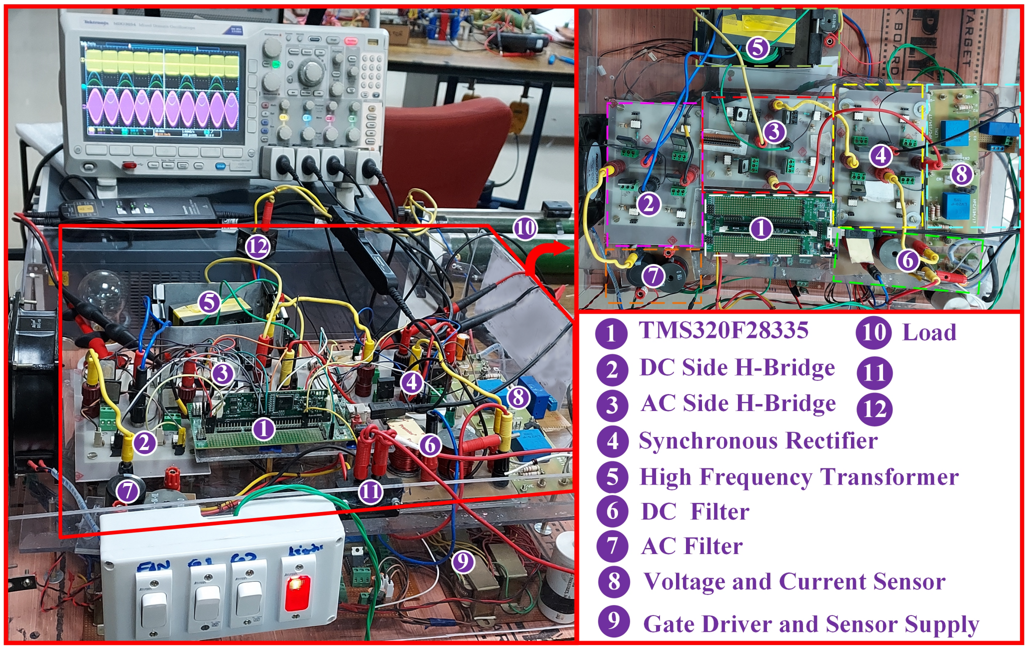


Figure 3.11: Experimental prototype of bidirectional Q1S DAB with asymmetrical full bridge.

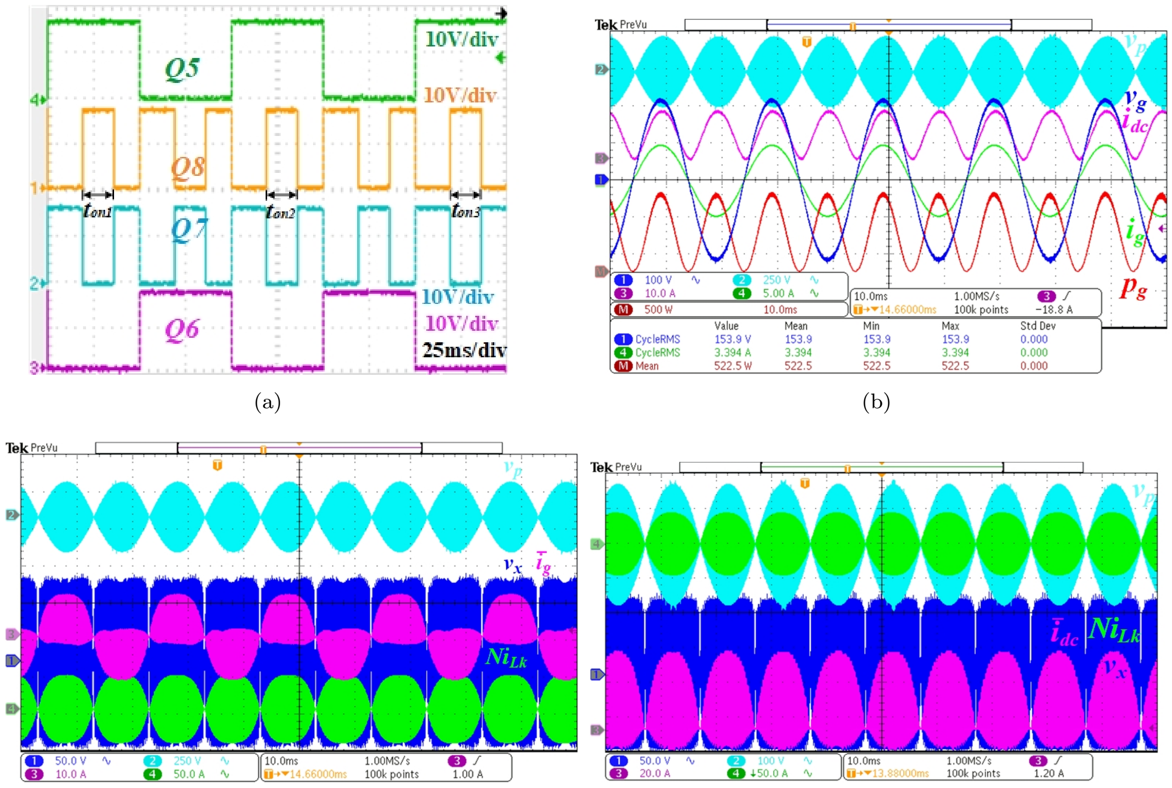
Table 3.3: Specifications of Various Components

Parameter	Value	Components	Part Name
Power Rating (P_o)	500 W	Gate Driver	FOD3184
Grid Voltage (v_g)	140-155 V	IGBT	IKW75N65EL5
DC Voltage (V_{dc})	100-120 V	MOSFET ($S1, S2$)	IXFH120N30X3
Line Frequency (f_g)	50 Hz	Transformer Core	EE8040 (CF139)
Switching Frequency (F_s)	10 kHz	Microcontroller	TMS320F28335
Leakage Inductance (L_k)	384 µH	Voltage Sensor	LV 25-P
Turns Ratio ($N : 1$)	4:1	Current Sensor	LA 55-P
DC Capacitance (C_{dc})	180 µF	DC Capacitor	ELG187M400
DC Inductance (L_{dc})	184 µH	DC Inductor	PCV-2-184-10L
AC Capacitance (C_g)	2×10 µF	AC Capacitor	Arcos
AC Inductance (L_g)	2×560 µH	AC Inductor	PCV-2-564-08L

3.4.1 Validation of AC→DC Power Flow

Fig. 3.12(a) shows the switching sequence for the various devices for the DC side full bridge at $\gamma = 5^\circ$ and captured near the peak value of v_g. It should be worth noting that the $Q1$, $Q4$, $Q5 = \overline{Q2}$, $\overline{Q3}$, $\overline{Q6}$ and $Q7 = \overline{Q8}$, this requires the utilization of a total of four EPWM channels instead of six EPWM channels compare to conventional modulation [120]. Fig. 3.12(b) shows the v_g, v_p, I_{dc}, i_g, and p_g. The converter draws 531 W of power from the grid at a rated converter voltage of 154.6 V, with an RMS current of 3.44 A. The i_g is in phase with the v_g, and near unity power factor operation can be seen during AC→DC power flow. The average DC output current is 5 A. Fig. 3.12(c) and Fig. 3.12(d) shows the transformer voltage v_p, v_x, secondary current Ni_{Lk}, high-frequency AC $\bar{i}_{ac}$ and DC current $\bar{i}_{dc}$. The different waveforms illustrate the characteristics of various high-frequency voltages and currents when observed in relation to the line frequency. Moreover, the folded nature of $\bar{i}_{ac}$ and unfolded nature of $\bar{i}_{dc}$ can be depicted in Fig. 3.12(c) and Fig. 3.12(d).

The switching status of the devices can be determined by the transformer voltage, currents, and input-output bridge current. The magnified view of the various voltages

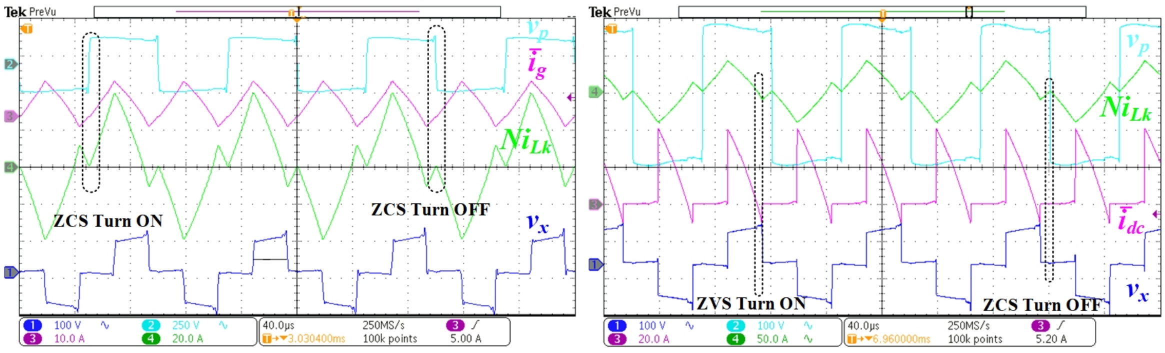


(a) (b)

(c) (d)

Figure 3.12: (a) Gate pulses for the various devices. (b) v_g, v_p, I_{dc}, i_g, and p_g. (c) v_x, v_p, $\bar{i}_{ac}$, and Ni_{Lk}. (d) v_x, v_p, $\bar{i}_{dc}$, and Ni_{Lk}.

and currents near the peak value of the v_g at switching frequency is shown in Fig. 3.13. The switching status of $Q1$ of the pulsating DC side full bridge can be determined from the Fig. 3.13(a) showing the v_x, v_p, $\bar{i}_{ac}$, and Ni_{Lk}. When gate pulses are supplied to devices of Leg 1 and 2, the pulsating DC voltage at that switching instance appears across the transformer's primary. This causes i_{Lk} to commence from zero, and the devices begin conducting, leading to ZCS turning ON. Likewise, gate pulses are withdrawn once i_{Lk} reaches zero, leading to ZCS turn OFF. The same goes for the devices Q2 and Q3 during the negative half of v_p. The switching status of Leg 3 of the DC side full bridge can be determined from Fig. 3.13(b) showing the v_x, v_p, $\bar{i}_{dc}$, and Ni_{Lk} near peak of v_g. When gate pulses are supplied to devices of Leg 3, the voltage across the devices of Leg 3 is zero, and Ni_{Lk} flows through the diode. As soon as the current Ni_{Lk} turns



(a) (b)

Figure 3.13: (a) Magnified view of v_x, v_p, $\bar{i}_{ac}$, and Ni_{Lk} near peak of v_g. (b) Magnified view of v_x, v_p, $\bar{i}_{dc}$, and Ni_{Lk} near peak of v_g.

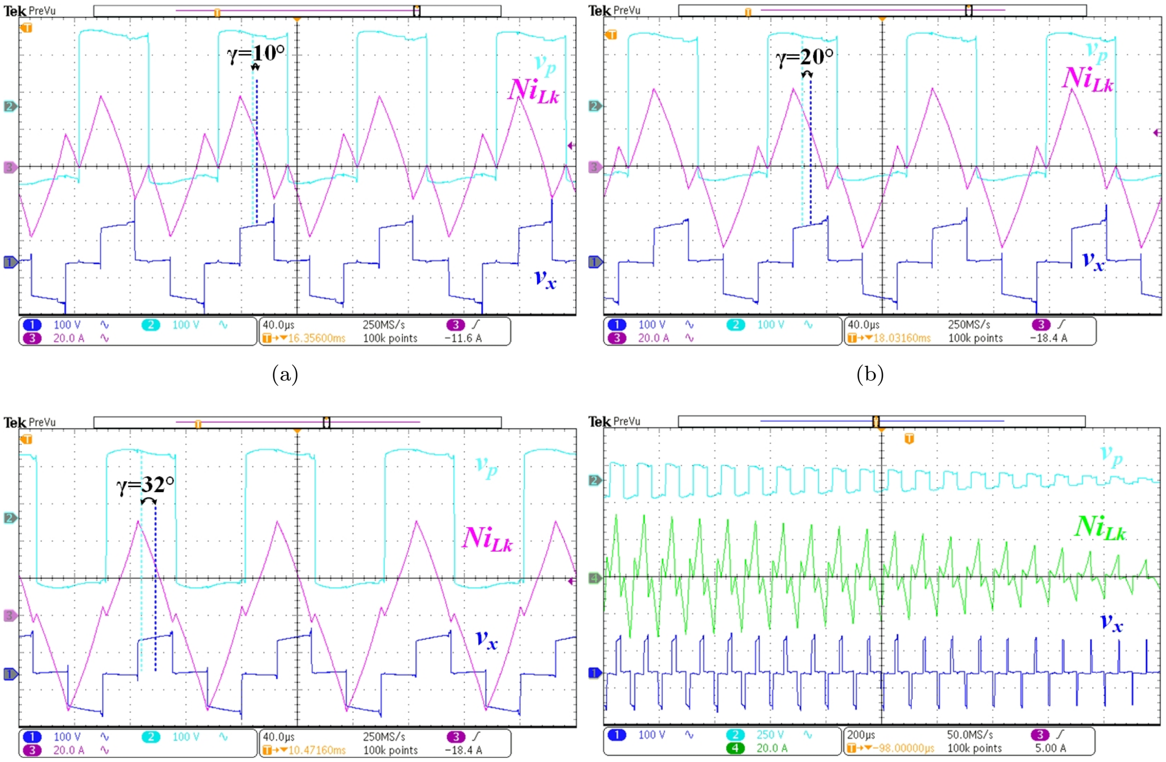
negative, the switches begin to conduct, resulting in the ZVS turning ON. The ZCS turn-off of Leg 3 initiates in the same manner as it does for Leg 1.

3.4.2 Status of Various Devices at Different Values of γ

The v_p, v_x, and Ni_{Lk} at different values of γ is shown in Fig. 3.14 (a)-(c). Compared to [149], the proposed modulation enables soft switching events at lower phase shift ratios. In comparison with the conventional TRM [120], the proposed modulation technique maintains soft switching near the zero crossing of v_g, as illustrated in Fig. 3.14(d). According to Fig. 3.14, soft switching remains intact across the entire envelope of line frequency and at different phase shift ratios.

3.4.3 Validation of DC→AC Power Flow

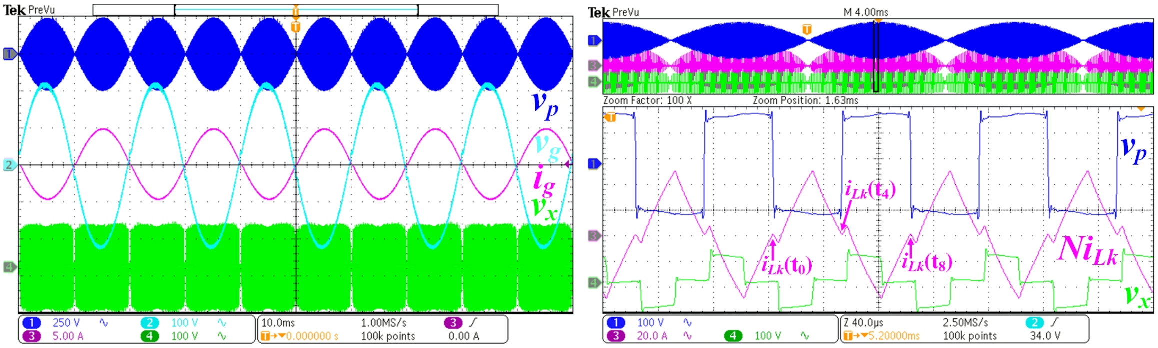
The DC→AC power flow for the Q1S DAB is tested by connecting the DC supply across V_{dc} and the resistive load across v_g. Ametek AST1501 is used as a DC source to maintain v_{dc} at 100 V. The γ is now negative to ensure power flows from the DC to the AC side. The experimental waveform for DC to AC power flow is shown in the Fig. 3.15(a), displaying v_g, i_g, v_p, and v_x. The i_g is now out of phase with reference to the v_g. The magnified view of the v_x, v_p, and Ni_{Lk} is shown in Fig. 3.15(b). In contrast to



(a) (b)

(c) (d)

Figure 3.14: Transformer voltages and current at different γ (a) v_p, v_x, and Ni_{Lk} at γ = 10°. (b) v_p, v_x, and Ni_{Lk} at γ = 20°. (c) v_p, v_x, and Ni_{Lk} at γ = 32°. d). v_x, v_p and Ni_{Lk} near zero crossing.



(a) (b)

Figure 3.15: (a) v_g, i_g, v_p, and v_x. (b) Magnified view of v_x, v_p, and Ni_{Lk}.

the AC→DC power flow, the secondary transformer voltage v_x now leads the primary transformer voltage v_p (when referred from the midpoint of any half). Additionally, the current through the secondary of transformer Ni_{Lk} is also zero at switching times

t_0, t_4, and t_8, enabling soft switching of various devices during turn-ON and turn-OFF transitions.

3.4.4 Dynamic Characteristics of the Proposed System

The dynamic response of proposed modulation during DC→AC power flow is illustrated in Fig. 3.16 for approximately 50% step change in load. Before the load change, the converter was operating at 487 W and drawing i_g of 3.2 A. After dynamics, the converter is now drawing i_g of 1.76 A at 270 W. The transition is observed to be seamless from 487 W to 270 W. The corresponding behaviour of v_p and v_x is shown in Fig. 3.16 as well. It can be observed that the output voltage stabilizes at the desired reference value within three cycles of the line frequency.

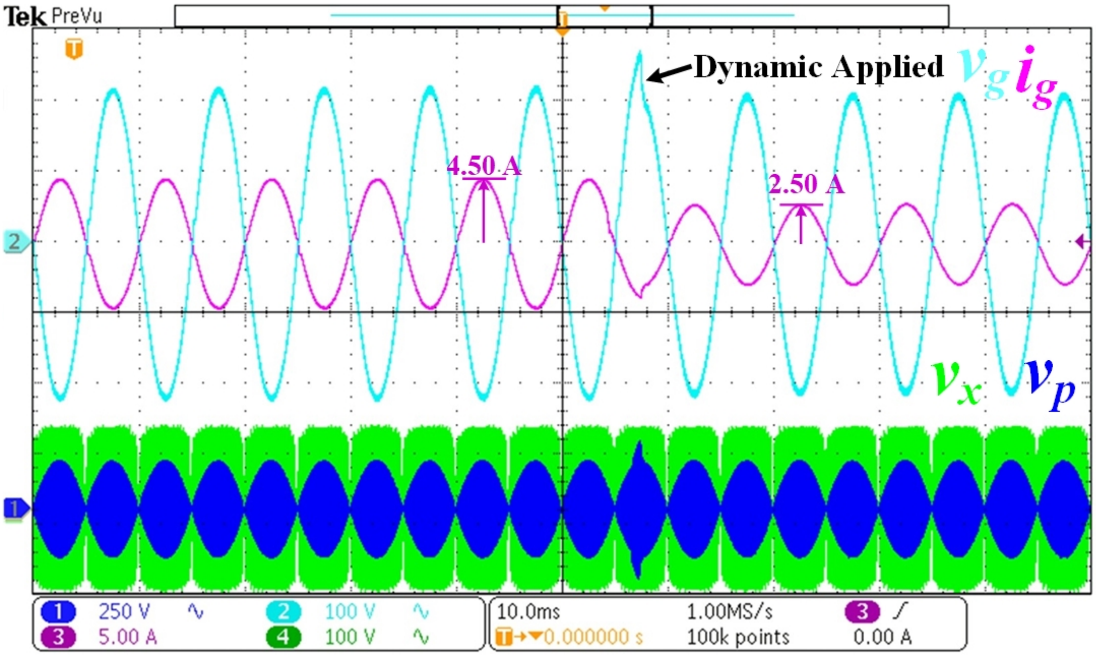
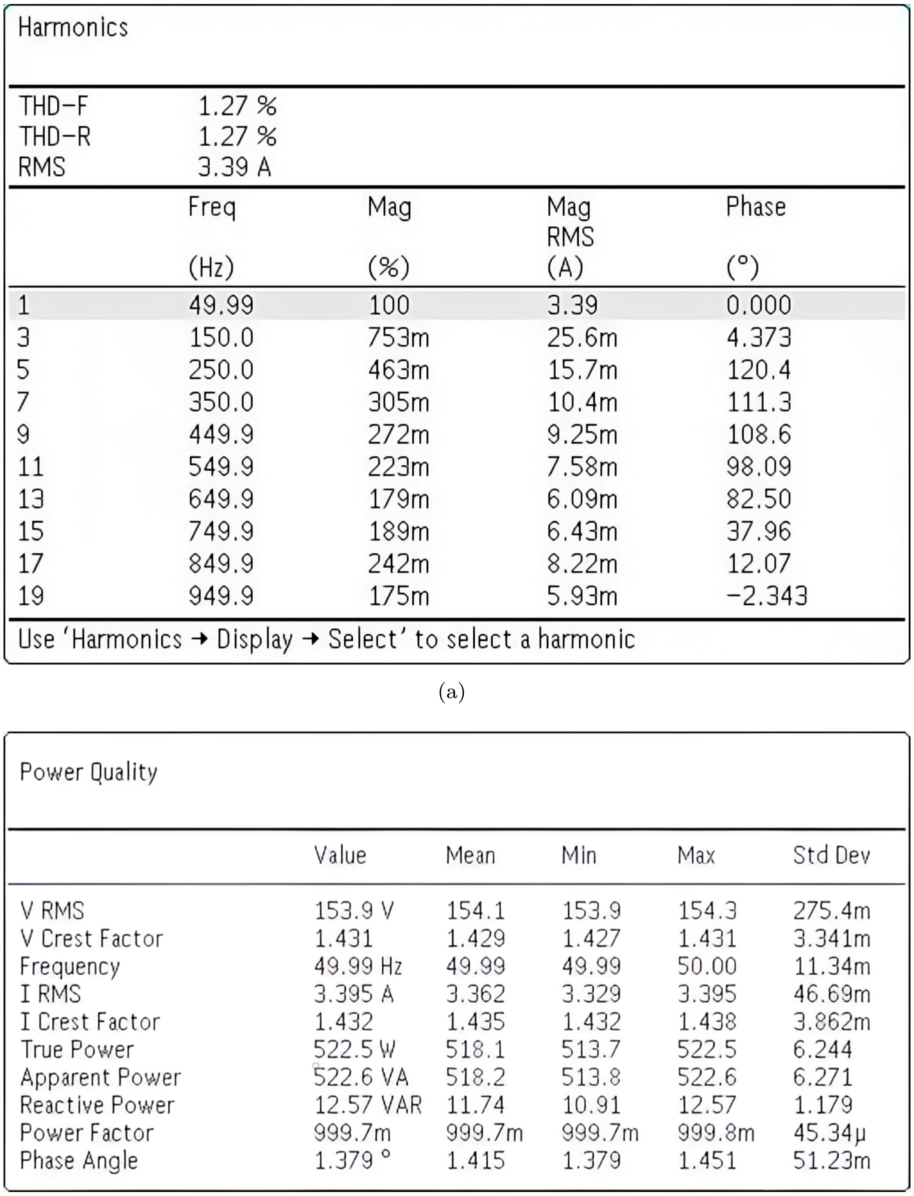


Figure 3.16: Dynamic response for a step change in load from 487 W to 270 W.

3.4.5 Analysis of THD and Other Power Quality

The MDO3PWR power application for the MDO3054 is capable of measuring 100^{th}, used to measure THD and the various power quality parameters shown in Fig. 3.17.



Harmonics

THD−F	1.27 %
THD−R	1.27 %
RMS	3.39 A

	Freq (Hz)	Mag (%)	Mag RMS (A)	Phase (°)
1	49.99	100	3.39	0.000
3	150.0	753m	25.6m	4.373
5	250.0	463m	15.7m	120.4
7	350.0	305m	10.4m	111.3
9	449.9	272m	9.25m	108.6
11	549.9	223m	7.58m	98.09
13	649.9	179m	6.09m	82.50
15	749.9	189m	6.43m	37.96
17	849.9	242m	8.22m	12.07
19	949.9	175m	5.93m	−2.343

Use ‘Harmonics → Display → Select’ to select a harmonic

(a)

Power Quality

	Value	Mean	Min	Max	Std Dev
V RMS	153.9 V	154.1	153.9	154.3	275.4m
V Crest Factor	1.431	1.429	1.427	1.431	3.341m
Frequency	49.99 Hz	49.99	49.99	50.00	11.34m
I RMS	3.395 A	3.362	3.329	3.395	46.69m
I Crest Factor	1.432	1.435	1.432	1.438	3.862m
True Power	522.5 W	518.1	513.7	522.5	6.244
Apparent Power	522.6 VA	518.2	513.8	522.6	6.271
Reactive Power	12.57 VAR	11.74	10.91	12.57	1.179
Power Factor	999.7m	999.7m	999.7m	999.8m	45.34µ
Phase Angle	1.379 °	1.415	1.379	1.451	51.23m

(b)

Figure 3.17: (a) Experimental THD of i_g up to 100^{th} harmonics. (b) Various power quality parameters.

The THD during AC-DC power flow at rated power is found to be 1.27%, which is well below the prescribed standards of IEEE-519-2022 as shown in Fig. 3.17(a). The power factor was found to be 99.97% when the converter drew a current of 3.4 A. Additionally, the various power quality parameters are listed in Fig. 3.17(b). From the various parameters, it can be concluded that the proposed asymmetric switching sequence-based

Table 3.4: Comparison of Efficiency and Other Key Parameters

Literature	**Power Rating**	**Grid Voltage (RMS)**	**Switching Frequency**	**Turns Ratio**	**Output Voltage**	**Peak Efficiency**
[58]	250 W	110 V	20 kHz	7:4	77 V	88% at 40% of the rated power
[120]	1441 W	70 V	10 kHz	1:1	400 V	89.96% at 93.62% of rated power
[153]	500 W	110 V	30-100 kHz	1:1	160 V	94.6% at 60.28% of the rated power
Proposed	500 W	140-155 V	10 kHz	4:1	100-120 V	92.2% at rated power

TRM shows good performance.

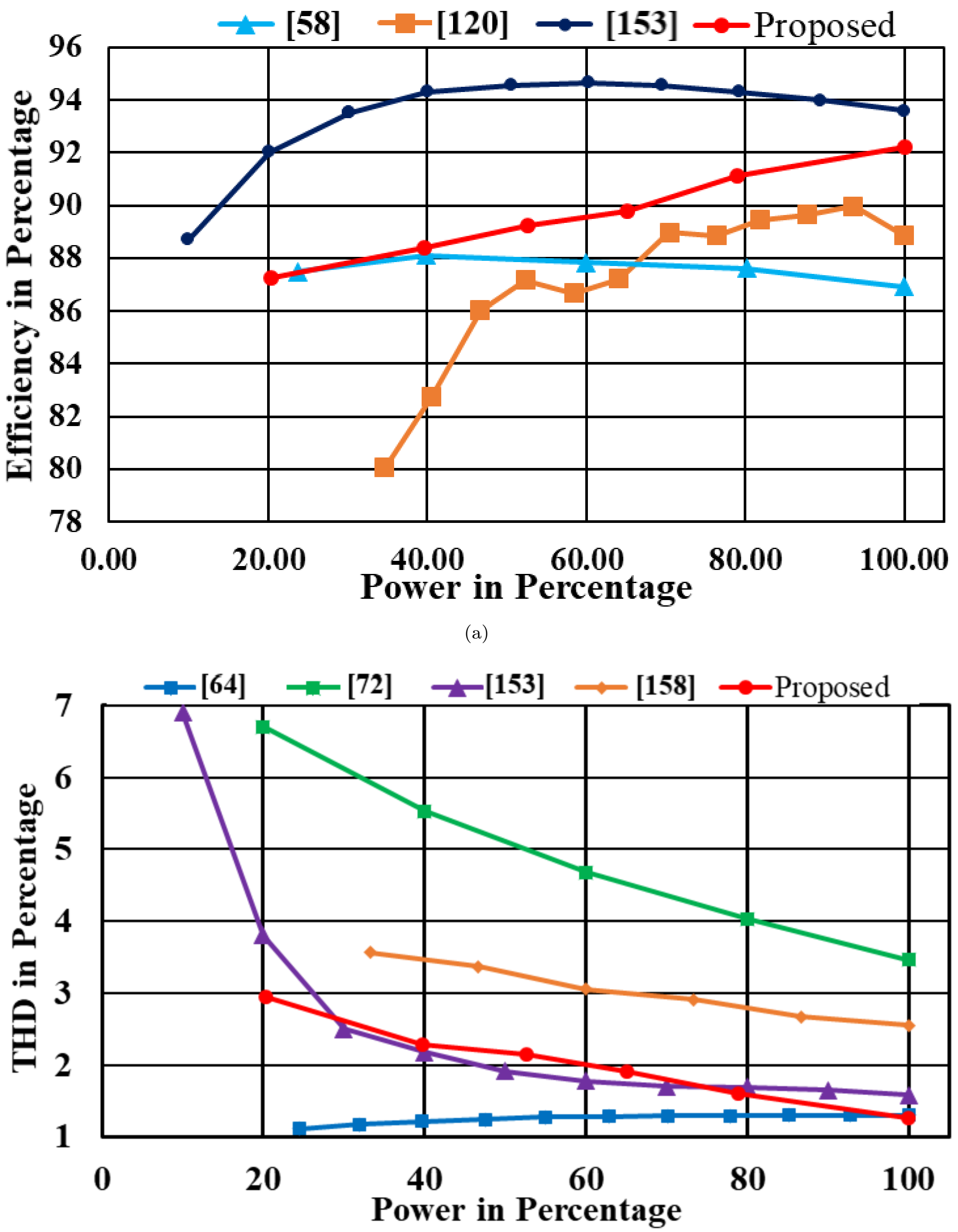
3.5 Comparison With Other Literature

3.5.1 Efficiency Comparison

Fig. 3.18(a) shows the efficiency comparison with other existing literature. The various literature selected features a common triangular nature of transformer current at least in one mode. The conventional TRM implemented in the matrix type DAB [120], the peak efficiency is found to be 89.96% at 93.61% of the rated power of 1.44 kW. In [153], a bridgeless single-stage AC-DC converter with quasi-fixed frequency control is presented, achieving a peak efficiency of 94.6% at 60.28% of the rated power of 500 W. Another solution presenting an improved hybrid current modulation based on TRM and TZM implemented in discontinuous Q1S DAB offering an efficiency of $\approx$ 88% at 40% of the rated power of 250 W [58]. The proposed TRM achieves a peak efficiency of 92.2% at the rated power of 500 W. Additionally, efficiency and other key parameters comparison is shown in Table 3.4.

3.5.2 Total Harmonics Distortion Comparison

Fig. 3.18(b) shows the THD comparison with other existing literature. An exceptionally low THD of 1.3% was observed at a rated power of 3 kW, dropping to 1.1% at 24% of rated power. Further improvements can be achieved by optimizing the input LCL filter and current-loop design, with the converter operating at 54 kHz and a grid-side



(a)

(b)

Figure 3.18: Comparison plot showing (a) Efficiency versus power plot ▬[58], ▬[120], ▬[153], ▬proposed. (b) THD versus power plot ▬[64], ▬[72], ▬ [153], ▬[158], ▬proposed.

Table 3.5: Comparison of THD and Other Key Parameters

Literature	Power Rating	Grid Voltage (RMS)	Switching Frequency	Grid Side Inductance	THD @ Rated Power
[64]	3 kW	240 V	54 kHz	1.27 mH	1.3%*
[72]	500 W	105 V	50 kHz	2 mH	3.46%
[153]	500 W	110 V	30-100 kHz	150 μH	1.58%**
[158]	1.5 kW	120 V	100 kHz	170 μH	2.55%
Proposed	500 W	140-155 V	10 kHz	1.12 mH	1.27%

*Lowest THD of 1.1% found at approx. 24.43% of rated power.

**The converter was operating at 30 kHz at rated power.

inductance of 1.27 mH, as presented in [64]. The THD at various wattages is measured using the proposed TRM, and the lowest THD is found to be 1.27% at rated power. This value is lower than the experimental THD of 1.58% measured at a rated power of 500 W operating at 30 kHz and a grid-side inductance of 150 uH [153], 2.55% measured at a rated power of 1.5 kW operating at 100 kHz and a grid-side inductance of 170 uH [158], and 3.46% measured at a rated power of 500 W operating at 50 kHz and a grid-side inductance of 2 mH [72]. Further, THD and other key parameters comparison is shown in Table 3.5.

3.6 Conclusion

This chapter introduces an asymmetrical switching sequence-based triangular modulation (TRM) for a quasi-single stage (Q1S) bidirectional AC-DC dual active bridge converter, utilizing a single carrier. In the proposed TRM, a mixed device bridge configuration is used where one leg of the DC side full bridge, consisting of MOSFETs, utilizes sinusoidally modified variable time period PWM, and the other leg consists of IGBTs operated at fixed duty and time period. This method relies on a single carrier and necessitates only four EPWM channels or two EPWM modules, in contrast to the six EPWM channels required in conventional TRM, thereby reducing the need for additional resources.

The advantages of the proposed technique include zero voltage switch (ZVS)/zero current switches (ZCS) turn ON for one leg of the DC bridge operating at a variable time period, ZVS turn ON and ZCS turn OFF for another leg operating at a fixed frequency, and ZCS turns ON/OFF for the pulsating DC side bridge. Thus, the proposed TRM eliminates the turn-on loss for all eight high-frequency devices and the turn-off loss for six devices. Further, the soft switching status of devices remains intact near zero crossing of line voltage and at a low phase shift ratio. The proposed TRM also offers open-loop power factor correction (PFC) and unity power factor (UPF) operations. The benchmark evaluation of the proposed TRM shows ≈14% improvement in real-time code execution profiles in comparison with conventional TRM. The proposed 500 W system exhibits values of 1.27% for THD, 0.99 for power factor, and 92.2% for efficiency. The experimental THD is well below the prescribed standard IEEE-519-2022.

In the next chapter, the issue of high RMS current in the proposed TRM is addressed, as it increases conduction losses, particularly under light loads. While the TRM enables soft-switching throughout the loading conditions, it suffers from high conduction losses. In battery charging applications, light load conditions persist for over 50% of the total charging time in CV mode, affecting both the proposed and existing TRM techniques. Despite achieving soft-switching, efficiency losses remain a concern. To mitigate this, an improved Method 1 is introduced, incorporating semi-variable frequency modulation to reduce harmonic distortion and current stress, thereby enhancing light-load performance. The next chapter also presents a comparison of the loss analysis under light load conditions, as well as current stress and THD throughout the loading conditions, between semi-variable frequency modulation and fixed-frequency modulation to validate the effectiveness of the improved Method 1.