Chapter 3

Switched Capacitor Ultra Sparse Matrix Converter

3.1 Introduction

Ultra sparse matrix converter (USMC) doesn't have any energy storage element at the intermediate DC link section. However, it requires a protection circuit consisting of braking capacitor and dissipating resistor [44]. In addition, USMC have load power factor within $\phi_o = (0, \frac{\pi}{3})$. Moreover it has voltage transfer ratio of 0.866. With these restrictions, USMC have not yet gained a popularity in industry applications. A converter is proposed in this chapter which overcomes the above restrictions of USMC by integrating switched capacitor network at intermediate DC link stage. Therefore, the proposed converter is termed as switched capacitor ultra sparse matrix converter (SC-USMC), which is shown in Figure.3.1.

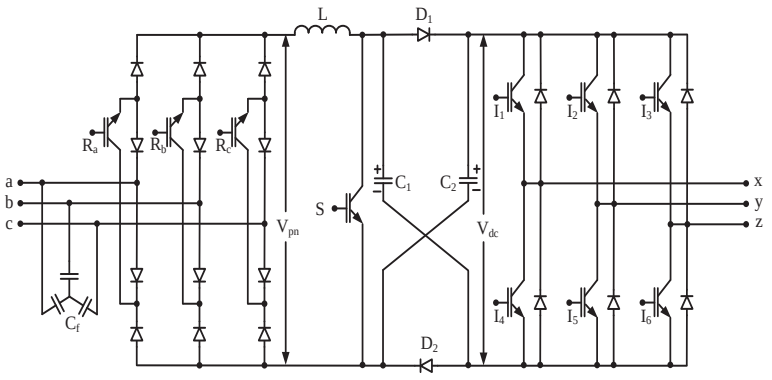


Figure 3.1: Switched capacitor ultra sparse matrix converter (SC-USMC)

3.2 Operating modes

To operate SC-USMC, the behaviour of switched capacitor network need to be understood. Figure.3.2 shows a switched capacitor network which consists of inductor, switch S followed by a lattice combination of diode and capacitors. The switched capacitor network is well known in DC-DC topologies [45]. The switched capacitor boosting network has two operating modes namely (i) ON mode and (ii) OFF mode.

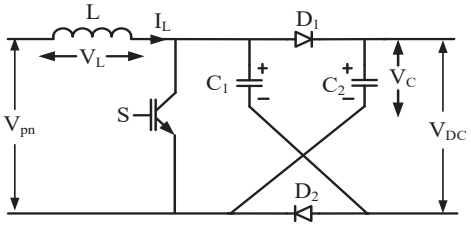


Figure 3.2: Switched capacitor(SC) network

ON mode : This mode is achieved by holding switch S in 'ON' position which makes the inductor energised with $V_L = L\frac{\Delta I_L}{T_{on}}$, as shown in Figure.3.3. Simultaneously, diodes D_1, D_2 are reverse biased connecting the capacitors in series via switch S. The voltage across capacitors (C_1, C_2) combine to enhance the DC link voltage to $2V_C$.

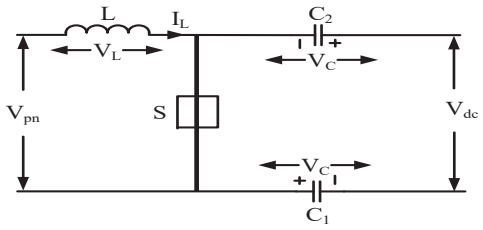


Figure 3.3: SC during ON state

OFF mode : During this mode, the diodes D_1, D_2 are forward biased, configuring inductor voltage in series with rectifier voltage V_{pn}, as shown in Figure.3.4. The inductor current acquires the path through capacitors (C_1, C_2) and inverter.

3.3 Steady State Analysis

The design and performance of the converter in terms of voltage gain is obtained using steady state analysis. Considering three phase input voltages, as given in eq.(3.1),

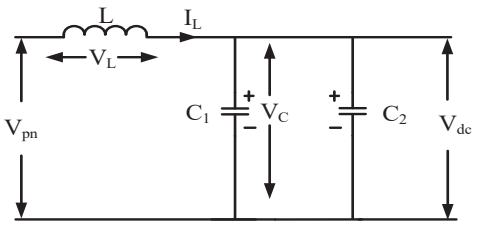


Figure 3.4: SC during OFF state

supply the converter

$$\begin{aligned} V_a &= \hat{V}_i \cos(2\pi f_i t) \\ V_b &= \hat{V}_i \cos(2\pi f_i t - 120°) \\ V_c &= \hat{V}_i \cos(2\pi f_i t - 240°) \end{aligned} \tag{3.1}$$

where $\hat{V}_i$ is the peak input voltage and f_i is the input frequency.

For negligible power loss in the converter, using power balance approach.

$\Rightarrow$ Input power supplied = Power after rectifier stage

$$\frac{3\hat{V}_i\hat{I}_i cos\phi_i}{2} = V_{pn}I_L \tag{3.2}$$

$$V_{pn} = \frac{3\hat{V}_i\hat{I}_i cos\phi_i}{2I_L} \tag{3.3}$$

$$V_{pn} = \frac{3\hat{V}_i m_c cos\phi_i}{2} \tag{3.4}$$

where $m_c = \frac{I_i}{I_L}$ = current modulation index, ϕ_i is the phase angle between $\hat{V}_i$ and $\hat{I}_i$ which are peak input voltage and current, respectively.

V_{pn} acts as source to the boosting network. By considering capacitors (C_1&C_2) equal, steady state expressions are obtained as follows:

During ON state (Figure.3.3) :

$$V_{pn} = L\frac{\Delta I_L}{T_{on}} \tag{3.5}$$

During OFF state (Figure.3.4):

$$V_c - V_{pn} = L\frac{\Delta I_L}{T_{off}} \tag{3.6}$$

By applying energy balance theory across the inductor, the voltage across capacitor can be derived as follows

$$V_c = V_{pn}\frac{(T_{on}+T_{off})}{T_{off}} = \frac{V_{pn}}{1-d} = \frac{3\hat{V}_i m_c cos\phi_i}{2(1-d)} \tag{3.7}$$

where $d = \frac{T_{on}}{T_{off}}$.
Gain of switched capacitor network is

$$B_{sc} = \frac{V_{dc}}{V_{pn}} \tag{3.8}$$

Output voltage of the inverter section is

$$\hat{V}_o = \frac{m_v V_{dc}}{\sqrt{3}} \tag{3.9}$$

where m_v is the voltage modulation index for the inverter stage.

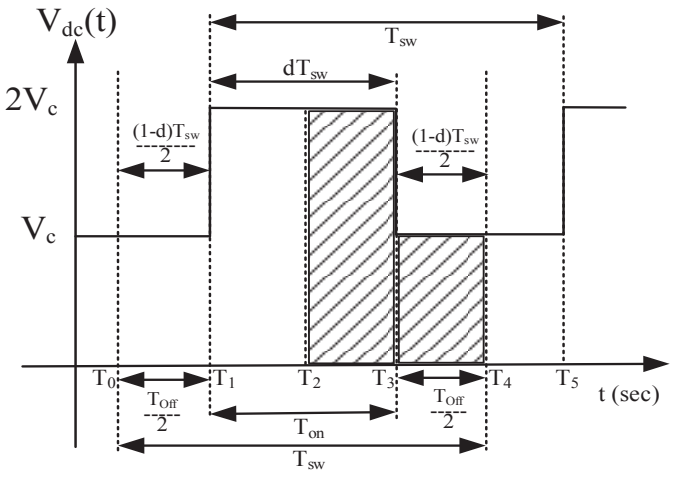


Figure 3.5: Timing waveform of V_{dc}

At the V_{dc} terminals, two voltage levels are possible i.e $2V_c$ and V_c corresponding to ON and OFF mode of the switch S, as shown in Figure.3.5. By placing inverter switching states for one cycle within T_{on} period of switch S gives eq.(3.10)

$$V_{dc} = \frac{2V_c\,(d)\,T_{sw}}{T_{on}} = 2V_c \tag{3.10}$$

If the inverter switching states for one cycle are placed during complete switching period $T_{sw} = T_{on} + T_{off}$, eq.(3.11) is obtained

$$V_{dc} = \frac{2V_c\,(d)\,T_{sw} + V_c\,(1-d)\,T_{sw}}{T_{sw}} = V_c\,(1+d) \tag{3.11}$$

In case of eq.(3.10) modulation index of inverter is with respect to $T_{on} = dT_{sw}$ period since one cycle of inverter switching states are placed in T_{on}. Where as in eq.(3.11) modulation index of inverter is with respect to T_{sw}. Substituting eq.(3.10) and eq.(3.11) in eq.(3.9), the possible output voltage is

$$\hat{V_o} = \frac{m_v V_{dc}}{\sqrt{3}} = \frac{m_v 2V_c}{\sqrt{3}} \text{ for } 0 \leq m_v \leq d \tag{3.12}$$

or

$$\hat{V_o} = \frac{m_v V_c(1+d)}{\sqrt{3}} \text{ for } d \leq m_v \leq 1 \tag{3.13}$$

However eq.(3.13) has lower $\hat{V_o}$ as compared to eq.(3.12), since $V_c(1+d) \leq 2V_c$. Hence to attain higher voltage gain at the output, eq.(3.12) is adopted for further discussion.

$$\hat{V_o} = \frac{m_v 2V_c}{\sqrt{3}} \text{ for } m_v \leq d \tag{3.14}$$

By substituting eq.(3.26) in eq.(3.14)

$$\Rightarrow \hat{V_o} = \frac{\sqrt{3} m_c m_v \hat{V_i} cos\phi_i}{(1-d)} \text{ for } m_v \leq d \tag{3.15}$$

Voltage gain (G) of Switched capacitor ultra sparse matrix converter is

$$G = \frac{\hat{V_o}}{V_i} = \frac{\sqrt{3} m_c m_v cos\phi_i}{(1-d)} \text{ for } m_v \leq d \tag{3.16}$$

The voltage transfer ratio variation with respect to m_v and d by keeping $m_c = 1$ & $cos(\phi_i) = 1$ for the converter is shown in Figure. 3.6. The gain (G) of the converter acquires higher values as a function of duty ratio. Design of components is based on

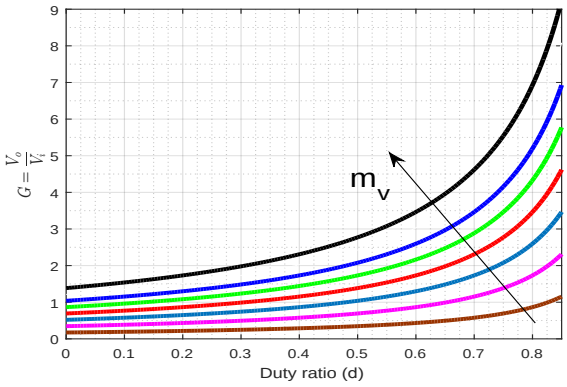


Figure 3.6: Gain variation

choice of current and voltage ripple corresponding to output power P. From eq.(3.5) and eq.(3.6), the inductor current and capacitor voltage ripples are calculated as follows

$$L\left(\frac{\Delta I_L}{T_{on}}\right) = V_{pn} \tag{3.17}$$

$$\Delta I_L = \frac{V_{pn} d}{f_{sw} L} \tag{3.18}$$

$$I_L = (2C)\,\frac{\Delta V_C}{T_{off}} \tag{3.19}$$

$$\Delta V_C = \frac{T_{off} I_L}{2C} = \frac{(1-d)\,I_L}{2 f_{sw} C} = \frac{(1-d)\,P}{2 f_{sw} C V_{pn}} \tag{3.20}$$

3.4 Switching strategy

From controller point of view, this converter consists of three sections namely rectification, boosting and inversion. To operate the converter, a well known space vector modulation (SVM) technique is adopted in this chapter. Two types of SVM for SC-USMC is proposed here.

3.4.1 Independent modulation technique for SC-USMC

An independent SVM algorithm consisting of rectifier section is operated using current space vectors to control the sinusoidal current waveforms at the input. The inverter section along with the boosting unit is operated by voltage space vectors to control the sinusoidal voltage waveforms at the output. To get balanced AC output voltages at the output of the inverter, the gating pulse for the boosting network is placed in coordination with the inverter switching signals.

For producing rectifier gating signals, three phase currents are sensed at input and is converted from three phase (i_a, i_b, i_c) to polar form $I^* \angle \theta_i$, where I^* represents magnitude of input current phasor, θ_i represents angle of reference which gives the exact position of phasor in space diagram. The current space vector diagram basically consists of six sectors with each sector having a 60° degree variant and line currents I_{ab}, I_{ac} of length $\frac{2}{\sqrt{3}} * I$, as shown in Figure.3.7. By projecting reference current phasor I^* on adjacent two switching states(or line currents), dwell timings d_μ, d_ν and d_z as given by eq.(3.21) is derived.

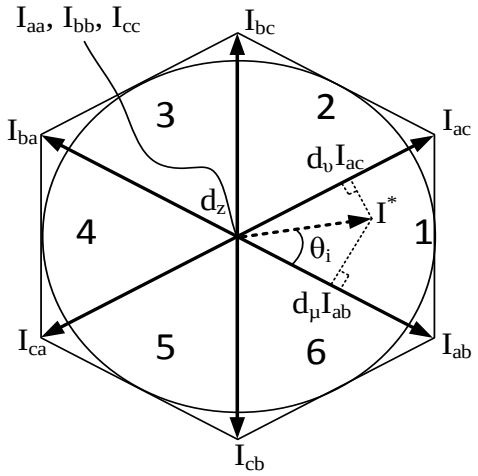


Figure 3.7: Current space vector (CSV) diagram

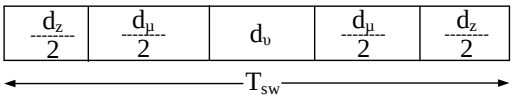


Figure 3.8: Rectifier switching states placement

$$\begin{aligned} d_\mu &= m_c.\sin\left(\sec tor\left(\tfrac{\pi}{3}\right) - \theta_i\right) \\ d_\nu &= m_c.\sin\left(\theta_i - \tfrac{\pi}{3}\left(\sec tor - 1\right)\right) \\ d_z &= 1 - (d_\mu + d_\nu) \end{aligned} \tag{3.21}$$

where $m_c = \frac{I^*}{I_L}$ is the modulation index of the current space vector and θ_i is the angle of the current space vector.

Space vector modulation have an advantage over shuffling the position of switching states, for placement of zero vector, thereby minimum switching states are achieved. The rectifier switching states are defined as shown in Figure.3.8.

The switching for boosting and inverter section are created using voltage space vector (VSV) diagram, as shown in Figure.3.9. From inverter point of view, output voltage space vector have two different voltage levels i.e., $\{V_c, 2V_c\}$. The V_c is achieved by OFF mode of switched capacitor network with corresponding active switching states $V_1 - V_6$. The $2V_c$ is achieved by ON mode of switched capacitor network with active switching sates $V_1^1 - V_6^1$. Dwell timings d_α, d_β and d_0 are calculated by projecting reference output voltage space vector (V^*) on adjacent two switching states V_1 & V_2, as defined in eq.(3.22).

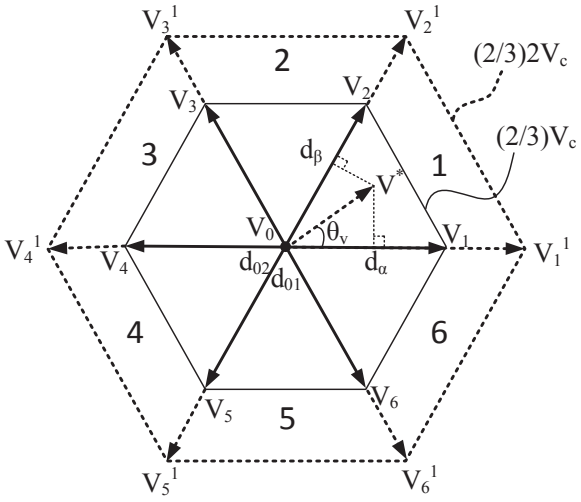


Figure 3.9: Voltage space vector (VSV) diagram

$$\begin{aligned} d_\alpha &= m_v.\sin\left(\sec tor\left(\tfrac{\pi}{3}\right)-\theta_v\right) \\ d_\beta &= m_v.\sin\left(\theta_v-\tfrac{\pi}{3}\left(\sec tor-1\right)\right) \\ d_0 &= d_{01}+d_{02}=1-(d_\alpha+d_\beta) \end{aligned} \tag{3.22}$$

Similarly considering dwell timings d^1_α, d^1_β and d^1_0 for dotted triangle as shown in Figure.3.9 are calculated and given in eq.(3.23)

$$\begin{aligned} d^1_\alpha &= m^1_v.\sin\left(\sec tor\left(\tfrac{\pi}{3}\right)-\theta_v\right) \\ d^1_\beta &= m^1_v.\sin\left(\theta_v-\tfrac{\pi}{3}\left(\sec tor-1\right)\right) \\ d^1_0 &= 1-d^1_\alpha-d^1_\beta \end{aligned} \tag{3.23}$$

where $m_v=\frac{\sqrt{3}V^*}{V_c}$, $m^1_v=\frac{\sqrt{3}V^*}{2V_c}$ is the modulation index of voltage space vector, θ_v is the angle of voltage space vector, d_{01} and d_{02} are zero states of the inverter section. The d_{01} corresponds to switch S-ON mode and d_{02} corresponds to switch S-OFF mode. Various

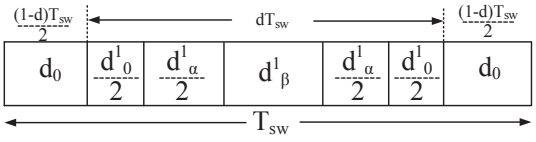


Figure 3.10: SC cascaded inverter switching states placement

patterns are possible for positioning active vectors and zero vector in a switching period. Discussion is presented in [46], for choosing an optimum pattern. Figure.3.10 suggests that over a period of one switching cycle, turn ON time of switch S is kept in middle position (occupied by d^1_α, d^1_β and d^1_0), while half of turn OFF time (d_0) of switch S is placed at the start and another half at the end of the total switching period (T_{sw}). By

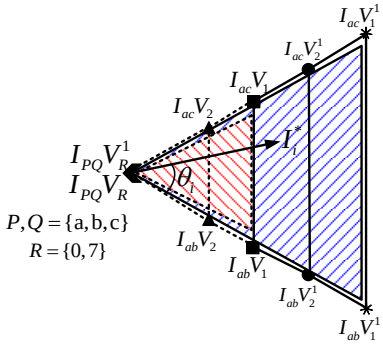


Figure 3.11: Integrated modulation technique

placing switching states in this manner, symmetrical switching is attained over half of the cycle. In addition to it higher voltage gain can be achieved.

3.4.2 Integrated modulation technique for SC-USMC

Since SC-USMC is to act as a single stage AC-AC converter, the rectifier, boost and inverter sections have to coordinate with each other for every switching cycle. It is possible either to superimpose VSV onto CSV or vice versa. By superimposing VSV onto CSV, proposed integrated modulation technique (IMT) for sector 1 is shown in Figure.3.11. In sector 1, VSV consists of 4 active vectors(V_1, V_2, V_1^1 and V_2^1) and zero vector (V_0), while CSV consists of 2 active vectors(I_{ab}, I_{ac}) and zero vector (I_{aa}). By superimposing VSVM on to CSV, active vectors of VSV occupies its position onto active vectors of CSV. For the available current with magnitude of I_{ab}, VSV vector decides the magnitude of current to be drawn from the source. In Figure.3.11, the region shaded with red indicates inverter switching operation during S-OFF region, whereas blue indicates inverter switching operation during S-ON region. For boosting network, it is inevitable either to eliminate S-ON or S-OFF mode. By having both S-ON and S-OFF mode, three cases are possible for integrated modulation technique.

Case IMT 1

If one cycle of inverter active states are placed in S-OFF region which is $T_3 - T_5$ period of Figure.3.5, it results a voltage boost of $V_{dc} = V_c = \frac{1}{1-d} * V_{pn}$, with remaining time period of $T_1 - T_3$, inverter is operated with zero states. This results in a condition such that modulation index of inverter and duty ratio of boosting network is related

as $m_v \leq (1-d)$. Projections of reference current vector onto adjacent switching states is defined by duty ratio which are calculated using eq.(3.24)

$$\begin{aligned} d_{\mu\alpha} &= d_\mu . d_\alpha \\ d_{\mu\beta} &= d_\mu . d_\beta \\ d_{\delta\alpha} &= d_\delta . d_\alpha \\ d_{\delta\beta} &= d_\delta . d_\beta \end{aligned} \tag{3.24}$$

Zero vector d^1_{z1} consists of combination of rectifier zero states with inverter active vectors (like $d^1_{z1} = I_{pp}V_1, I_{pp}V_2, ..$ where $p \in \{a,b,c\}$), inverter zero states with rectifier active states (like $d^1_{z2} = I_{pq}V_0, I_{pq}V_7, ..$ where $p,q \in \{a,b,c\}, \& \; p \neq q$) and rectifier zero states with inverter zero states (like $I_{pp}V_0, I_{pp}V_7, ..$ where $p,q \in \{a,b,c\}$)given in eq.(3.6) .

$$\begin{aligned} d^1_z &= d^1_{z1} + d^1_{z2} + d^1_{z3} \\ d^1_{z1} &= d_p . d_\alpha + d_p . d_\beta + d_p . d^1_0 + d_p . d_0 \\ d^1_{z2} &= d_\mu . d^1_0 + d_\mu . d_0 \\ d^1_{z3} &= d_\delta . d^1_0 + d_\delta . d_0 \end{aligned} \tag{3.25}$$

Based on eq.(3.24) and eq.(3.25), Figure.3.12 is drawn

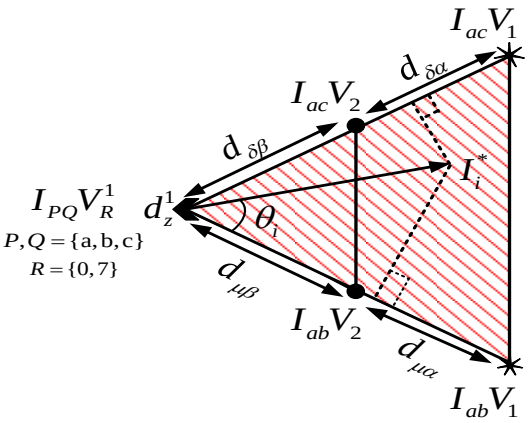


Figure 3.12: IMT 1 with duty ratio's

For one switching cycle, placement of switching states is shown in Figure.3.13.

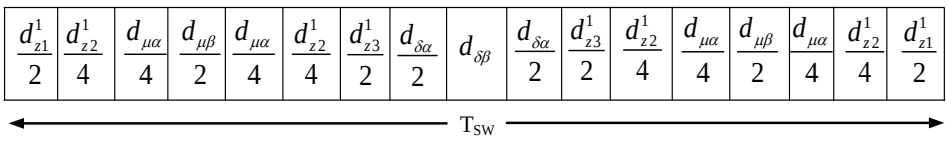


Figure 3.13: IMT 1 switching states positioning

Case IMT 2

Similarly if one cycle of inverter active switching states are placed in S-ON region during time T_1-T_3 (of Figure.3.5) and with remaining time period T_3-T_5 of inverter is operated with zero state, a voltage boost of $V_{dc} = 2V_c = \frac{2}{1-d} * V_{pn}$ is achieved. This results in a condition such that modulation index of inverter should be less than or equal to the duty ratio of boosting network i.e., $m_v \leq d$. Projections of reference current vector onto adjacent switching states is defined by duty ratios which are calculated by eq. (3.26) &*eq.* (3.27).

$$\begin{aligned} d^1_{\mu\alpha} &= d_\mu . d^1_\alpha \\ d^1_{\mu\beta} &= d_\mu . d^1_\beta \\ d^1_{\delta\alpha} &= d_\delta . d^1_\alpha \\ d^1_{\delta\beta} &= d_\delta . d^1_\beta \end{aligned} \tag{3.26}$$

$$\begin{aligned} d_z &= d_{z1} + d_{z2} + d_{z3} \\ d_{z1} &= d_p . d^1_\alpha + d_p . d^1_\beta + d_p . d_0 + d_p . d^1_0 \\ d_{z2} &= d_\mu . d_0 + d_\mu . d^1_0 \\ d_{z3} &= d_\delta . d_0 + d_\delta . d^1_0 \end{aligned} \tag{3.27}$$

For one switching cycle, placement of switching states as given by the above equations is shown in Figure.3.14 & Figure.3.15.

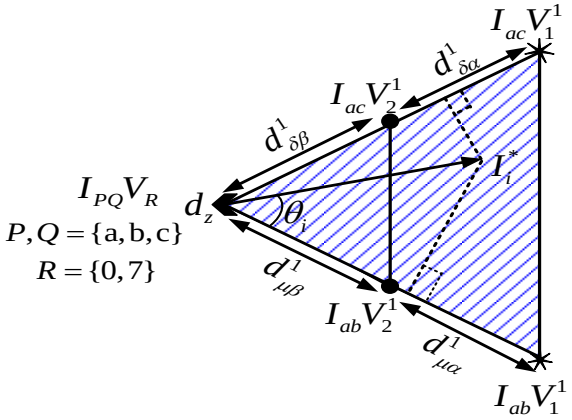


Figure 3.14: IMT 2 with duty ratio's

Case IMT 3

In this case inverter active switching states are placed in part of both S-ON and S-OFF modes during time T_2-T_4 (of Figure.3.5). Remaining period of S-ON and S-OFF

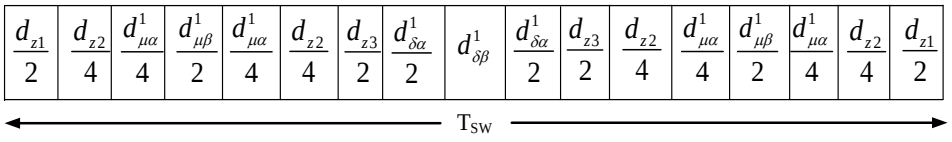


Figure 3.15: IMT 2 switching states positioning

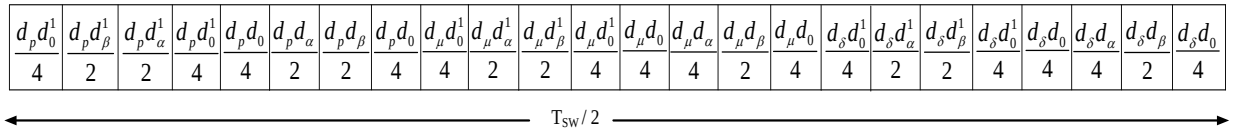


Figure 3.16: IMT 3 switching states positioning

states are occupied with inverter zero states. Projections of reference current vector onto adjacent switching states is defined based on time period placement active vectors percentage on S-ON state. By presuming 50% active vector placement on S-ON state results a voltage boost of $V_{dc} = \frac{2V_c+V_c}{2} = \frac{1+d}{1-d} * V_{pn}$. The switching states positioning are defined as shown in Figure.3.16. Moreover this case results in unbalanced output voltage condition since inverter input is accommodated by two voltage levels $2V_c$ & V_c.

Therefore, out of these three IMT schemes the voltage boosting in IMT 1, IMT 2 and IMT 3 are $V_{dc} = \frac{1}{1-d} * V_{pn}$, $V_{dc} = \frac{2}{1-d} * V_{pn}$ and $V_{dc} = \frac{1+d}{1-d} * V_{pn}$ respectively. For maximum output voltage, converter has been operated in case IMT 2.

Both independent and integrated modulation methods discussed above is applicable to proposed converter SC-USMC, the main difference is integrated modulation technique requires higher switching devices than independent modulation technique due to its switching pattern.

3.5 Validation

In order to validate the proposed concept, switched capacitor ultra sparse matrix converter is simulated in Matlab/simulink environment and same is implemented using experimental test rig with the specifications as listed in Table.3.1. At first, the independent modulation technique is implemented.

Table 3.1: Parameters

Power	$460W$
Input Voltage, $\hat{V_i}$	$70\ V$
Fundamental line frequency, f_i	$50\ Hz$
Fundamental output frequency, f_o	$100\ Hz$
Switching frequency, f_{sw}	$5\ kHz$
Boost inductance, L	$3\ mH$
Boost Capacitance, C_1, C_2	$290\ \mu$F

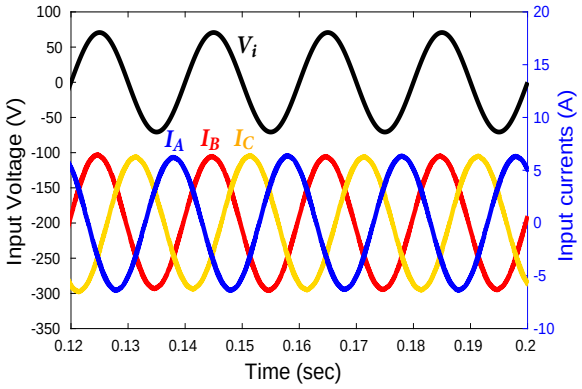


Figure 3.17: Simulation results of input voltage and currents

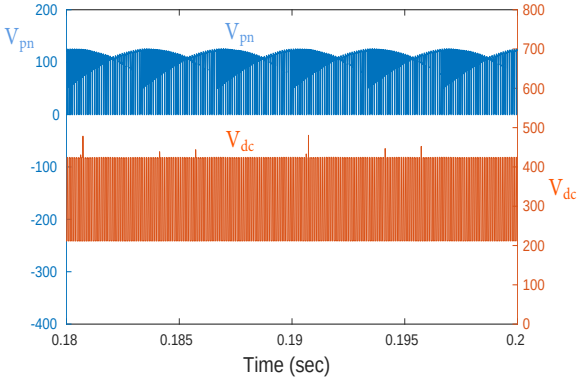


Figure 3.18: Simulation results of voltage at V_{pn} and V_{dc}

3.5.1 Simulation results

The SC-USMC is supplied with peak input voltage of $70V$, $50Hz$ as shown in Figure.3.17. It draws a peak current of amplitude $5.8A$ when rectifier section is operated with $m_c = 1$ and $cos\phi_i = 1$. As current modulation index given in eq.(3.4) sets to unity, the average current flowing in inductor is same as that of the peak input current

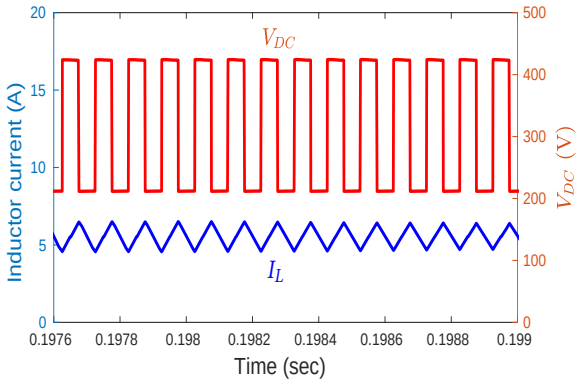


Figure 3.19: Simulation result of voltage at V_{dc} and inductor current

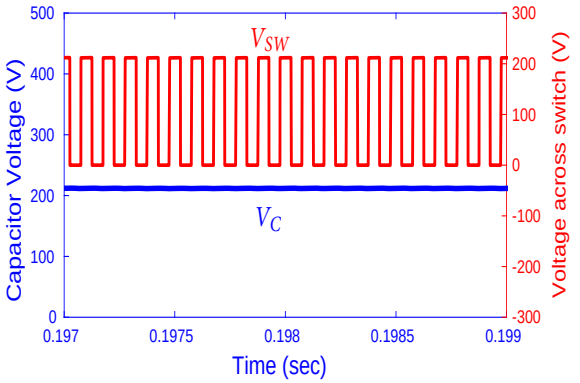


Figure 3.20: Simulation results of capacitor voltages and switch voltage

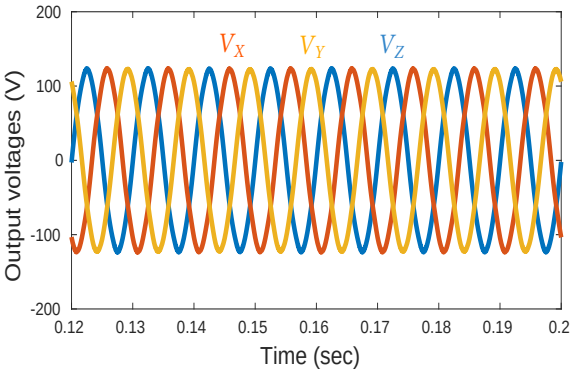


Figure 3.21: Simulation results of output voltages

drawn from the supply. The voltage produced at V_{pn} follows pattern of line voltages with switching among them. Figure.3.18 shows the voltage V_{pn} after the rectifier stage. Intermediate link voltage V_{pn} is boosted by the switched capacitor network with defined duty ratio $d = 0.5$. As shown in Figure.3.19, boosting is 4 times during switch S-ON mode and 2 times during switch S-OFF mode at the V_{dc}. Maximum value of V_{dc} would be $420V$ as per eq.(3.9) and minimum value is $210V$ which is confirmed by

Figure.3.18. During higher value of V_{dc}, inductor stores energy there by current flowing through inductor rises. Conversely, during lower value of V_{dc} inductor discharges its stored energy to capacitors. The inductor current profile is shown in Figure.3.19. By, eq.(3.26) voltage across capacitor would be $210V$ and voltage profile across switch S jumps between 0 to $210V$, with a frequency of $5kHz$ as shown in Figure.3.20. With inverter modulation index operated at $m_v = 0.48$ the peak output voltage according to eq.(3.15) would be $116V$, which is shown in Figure.3.21. Simulation setup of converter could be operated to higher power rating, but to easily match and compare the simulated results with the laboratory prototype results, specification of simulated converter is kept same as hardware.

3.5.2 Experimental results

To assess the practical feasibility of the proposed converter, a test setup was implemented as shown in Figure.3.22. Parameters having specifications for simulation was used for experimental setup. Switches and diodes used in the setup were realised with ST Microelectronics devices ($STW33N60DM2$ and $STPS60170CT$).

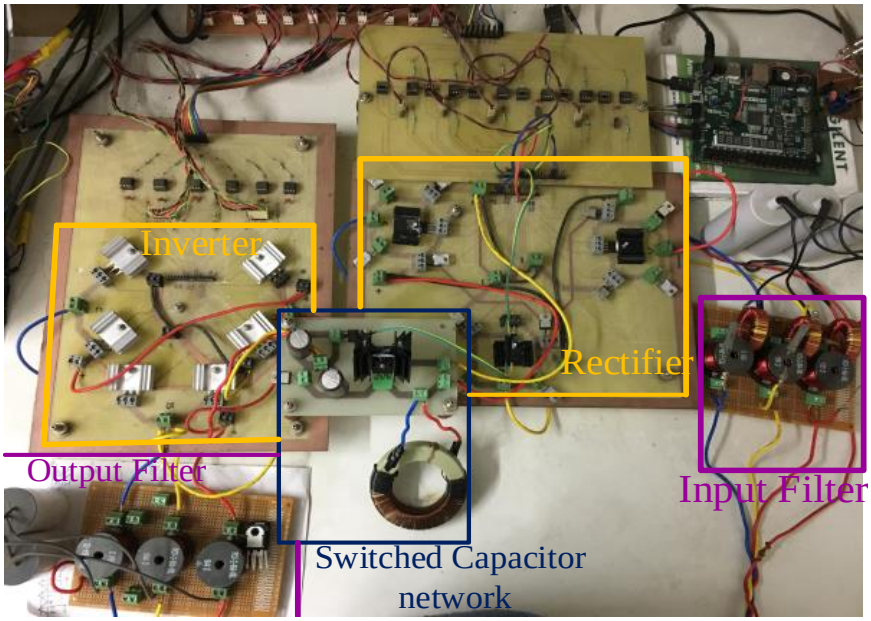


Figure 3.22: Test setup

A peak input voltage of $70V$ is given to the converter. It draws a current of $5.68A$ with total harmonic distortion (THD) of 5.41% which is close to IEEE standards, as shown in Figure.3.23 and Figure.3.24. Due to current space vector switching, resultant

intermediate DC voltage at V_{pn} terminals is shown in Figure.3.25. The dip in mean voltage V_{pn} is around $4V$ due to inherent property of forward voltage drop in switching devices. After rectification, intermediate link voltage is boosted by switched capacitor network with predefined duty ratio $d = 0.5$. As per eq.(3.26) capacitor voltage should have a value of $V_c = 210V$ however in experimental results it shows around $205V$, as shown in Figure.3.26. This difference in voltage is because of drop in rectified voltage, which is carry forwarded through switched capacitor network. Figure.3.26 shows voltage at V_{dc} and inductor current I_L. The V_{dc} voltage is switching in between $410V$ and $205V$. In addition, it shows spikes due to switching of inverter states. The voltage across switch S is shown in Figure.3.27. Figure.3.28 shows the inverter output voltages with switching states defined by SVM for $m_v = 0.48$. Based on output voltage equation eq.(3.15) experimental results in Figure.3.28 shows $110V$ at $100Hz$ output frequency.

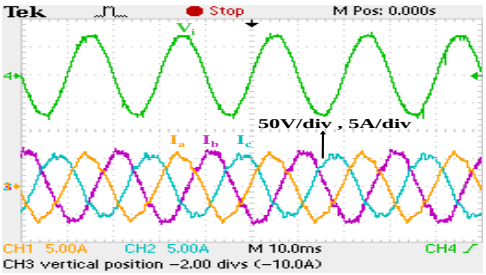


Figure 3.23: Experiment results of input voltage and currents

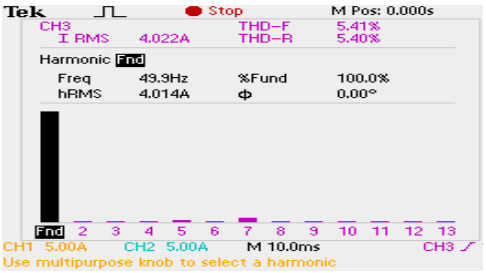


Figure 3.24: Input current THD

Operation with integrated modulation technique case IMT 2 results are shown in Figure.3.29, Figure.3.30 and Figure.3.31. Both independent and integrated modulation techniques proposed for SC-USMC are validated experimentally. It has been noticed that integrated modulation technique requires higher switching frequency compared to independent modulation. Moreover, independent modulation has additional benefit of

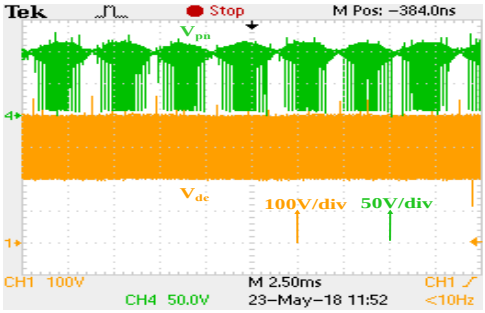


Figure 3.25: Experiment results of voltage at V_{pn} and V_{dc}

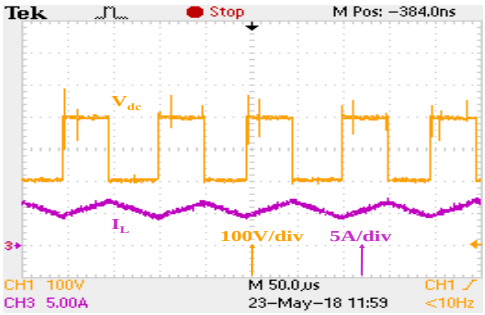


Figure 3.26: Experimental results of voltage at V_{dc} and I_L

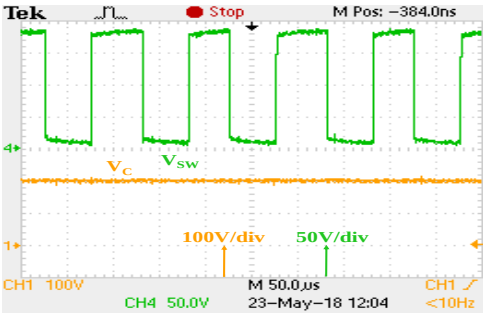


Figure 3.27: Experimental results of switch voltage and capacitor voltages

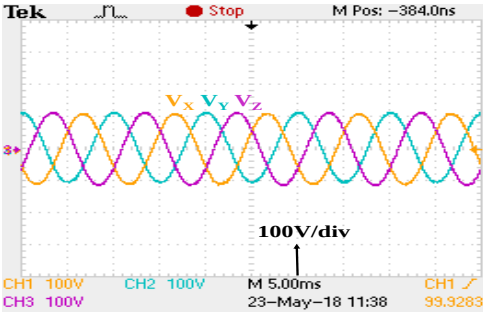


Figure 3.28: Experimental results of output voltages

producing balanced output voltage with unbalanced input voltage. In view of these benefits independent modulation scheme is considered as a better option. Based on this modulation scheme performance analysis of SC-USMC is presented in the remaining

part of this chapter.

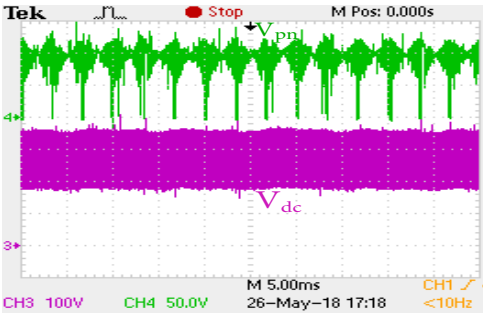


Figure 3.29: Experiment result of voltage at V_{pn} (50V/div) and V_{dc} (100V/div) using IMT

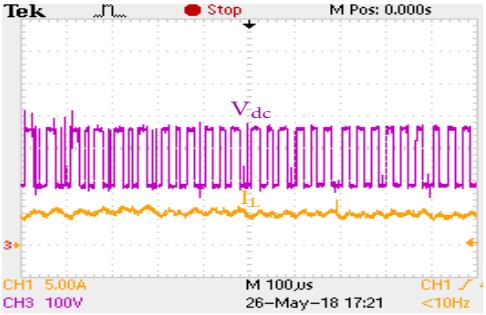


Figure 3.30: Experiment results of I_L (5A/div) and voltage at V_{dc} (100V/div) using IMT

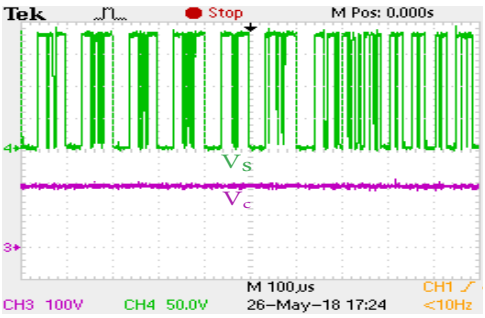


Figure 3.31: Voltage across switch S (50V/div) and capacitor voltage V_c (100V/div) using IMT

Step change in load variation

For assessing the proper operation of proposed converter subject to variation in load, experiment is done. Step change in load of 50% produces a change in peak input current from $4.8A$ to $6.2A$, as shown in Figure. 3.32, keeping input power factor at unity. However the voltage at V_{pn} terminals shows less impact towards change in load variation. The inductor current increases to deliver power with respect to change in load as shown in Figure. 3.33. Moreover the capacitor voltage decreases by $7V$ due to

over step change in load. Any load variation through inverter switches is absorbed by the two capacitors as shown in Figure. 3.34. In addition, output voltage level shows variation of $8V$, as shown in Figure. 3.35

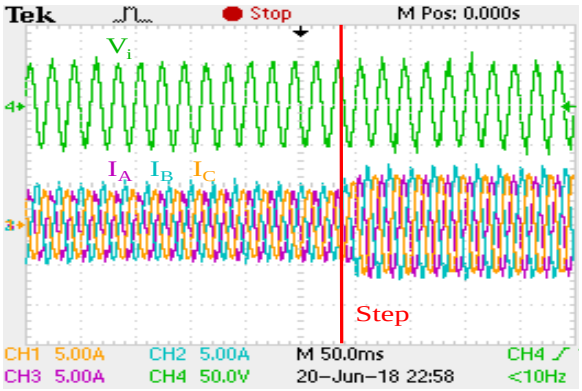


Figure 3.32: Input currents (5A/div) during step change

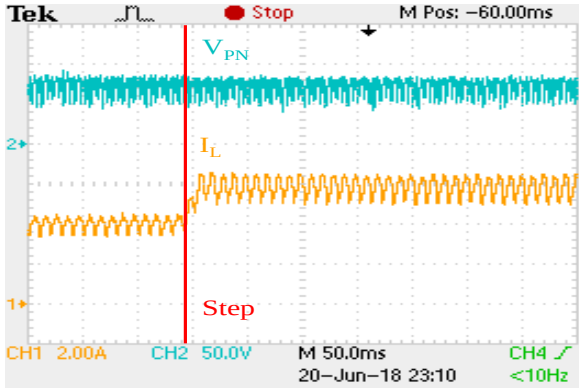


Figure 3.33: Inductor current I_L (2A/div) and V_{pn} (50V/div) during step change

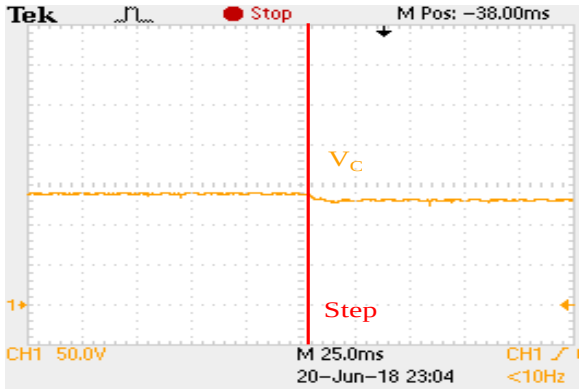


Figure 3.34: Voltage across capacitor (50V/div) during step change

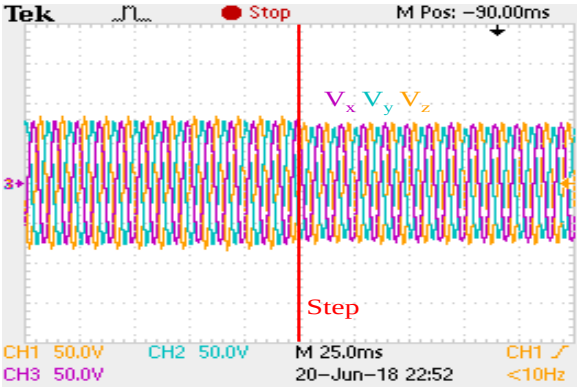


Figure 3.35: Output voltages (50V/div) during step change

Unbalanced input voltages

In power system, unbalanced input voltages occurs when external fault condition arises due to worn out of insulation material and common single phase ground fault. To observe the behaviour of proposed converter under voltage unbalance the input voltage is decreased by 15% in one phase and 30% in another phase, as shown in Figure.3.36. Under balanced condition, loci of input voltage is a circle whereas for unbalanced condition it is ellipse in shape. Figure.3.38 shows the loci of input voltages and output voltages with balanced (blue color) and unbalanced input (red color). Even with unbalance input supply, proposed converter delivers balanced output voltage. With decrease in magnitude of input voltage, the output voltage remains balanced but with decreased magnitude, as shown in Figure.3.36 & 3.39. This is achieved by maintaining the control parameters (m_c, $cos\phi_i$, m_v & d) constant. By observing the operating modes of SC-USMC, it can be noticed that inductor stores energy in the form of magnetic field during 'S' ON period, concurrently capacitors are delivering stored energy to the load. During 'S' OFF period, conversion of energy is taking place in the form of magnetic field to electric field. Thereby any voltage disturbance in input is suppressed during this conversion process, which leads to the production of balanced output voltages. This confirms robustness of the proposed converter

Load power factor variation

USMC is a unidirectional power flow converter. Corresponding to unity power factor at input, it restricts minimum load power factor angle to 30°. Without the protection circuit, converter goes beyond operating range during transients and regenerative load

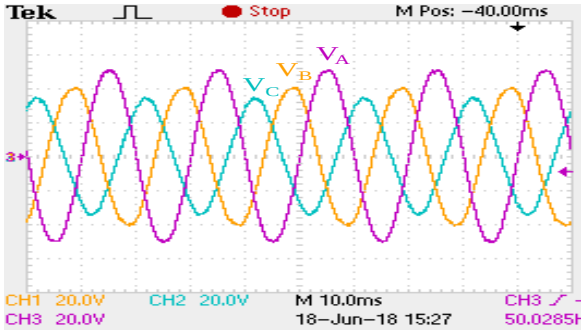


Figure 3.36: Unbalanced input supply voltages (20V/div)

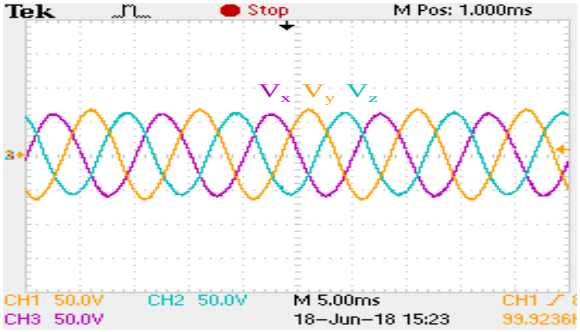


Figure 3.37: Output voltages (50V/div) during unbalanced input supply

conditions. Loading for USMC could be permanent magnet synchronous motor which posses the power factor value around unity or specially designed induction motors having power factor angle upto 30° at rated slip. However in general, power factor for induction motors used in industries lies in the range of $0.6 - 0.855$ when operated at rated slip as reported in Figure. (2) of [47]. Due to this, USMC is not a viable solution for induction motor loading. With the presence of capacitors connected across the input of the inverter in SC-USMC, the reverse currents generated during regenerative operation could be absorbed. Operating range of load power factor for SC-USMC

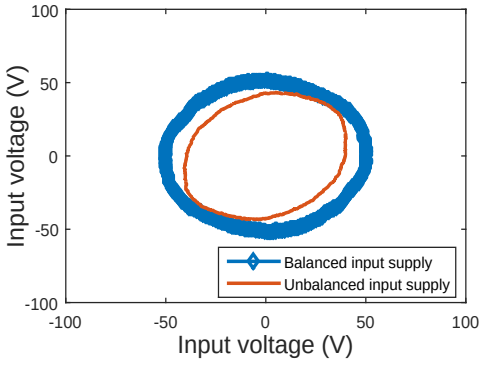


Figure 3.38: Loci of input voltage

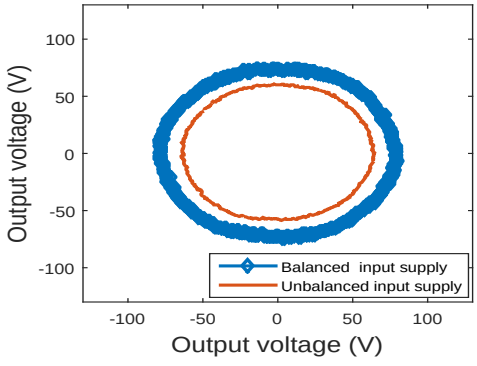
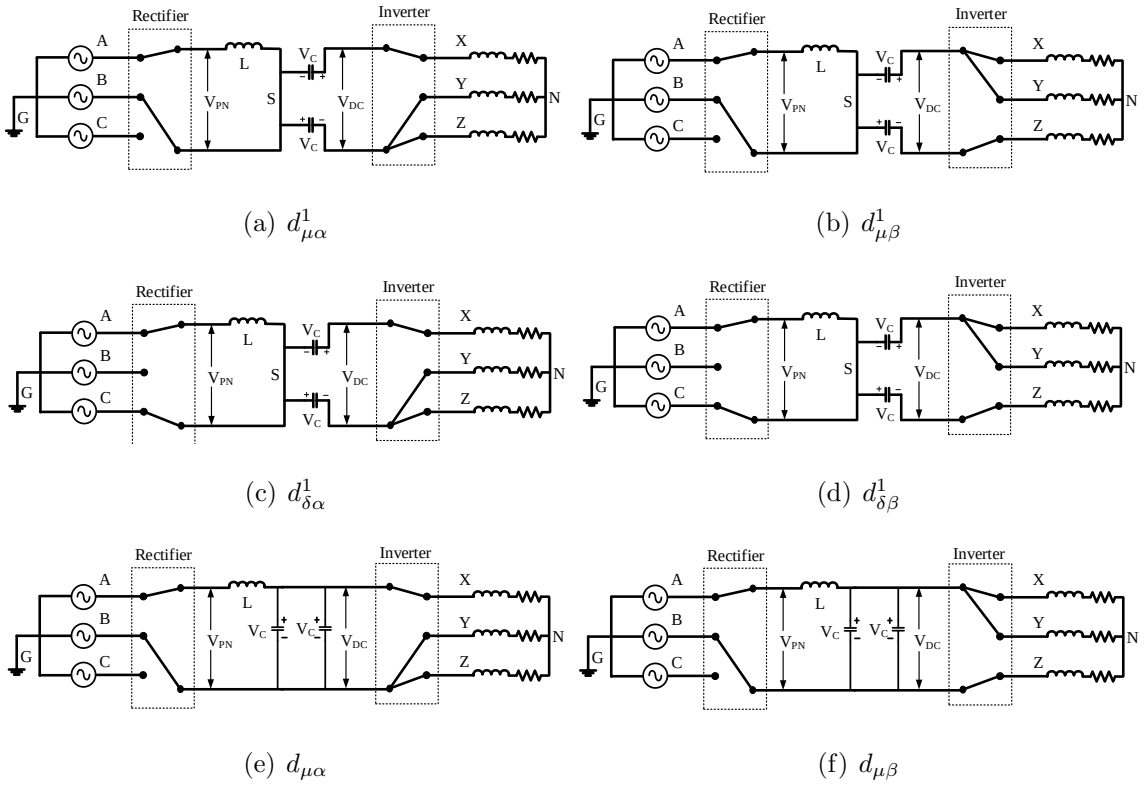


Figure 3.39: Loci of output voltage



(a) $d^1_{\mu\alpha}$ (b) $d^1_{\mu\beta}$

(c) $d^1_{\delta\alpha}$ (d) $d^1_{\delta\beta}$

(e) $d_{\mu\alpha}$ (f) $d_{\mu\beta}$

Figure 3.40: Switching states of SC-USMC

depends upon the rating of the capacitor used. For designed value of $C = 290\mu F$ used in this chapter the load power factor angle range is extended up to 80°, thereafter presence of imbalance in load currents is observed.

3.6 Common mode voltage analysis for SC-USMC

Common mode voltage analysis is an important consideration especially in case of driving motor loads. Insulation breakdown and bearing failure are main effects of excessive common mode voltage. In this section common mode voltage analysis for SC-USMC is done assuming converter is driving the RL load. Following discussion is restricted to sector 1 which constitutes of active states ($d^1_{\mu\alpha}, d^1_{\delta\alpha}, d^1_{\beta\alpha}, d^1_{\beta\alpha}, d_{\mu\alpha}, d_{\delta\alpha}, d_{\beta\alpha}, d_{\beta\alpha}$) and zero states ($d_z, d^1_z$). At an instant when converter is applied with state $d^1_{\mu\alpha}$ as shown in Figure.4.8(a), the voltage at node X can be written as $V_X = V_B + V_c$ with respect to ground G. Similarly at nodes Y and Z calculated as $V_Y = V_B - V_c$ & $V_Z = V_B - V_c$ respectively. The voltage across phases of RL can be written as

$$
\begin{aligned}
V_X &= R_X i_X + L_X \tfrac{di_X}{dt} + V_{NG} \\
V_Y &= R_Y i_Y + L_Y \tfrac{di_Y}{dt} + V_{NG} \\
V_Z &= R_Z i_Z + L_Z \tfrac{di_Z}{dt} + V_{NG}
\end{aligned} \tag{3.28}
$$

where R_X & L_X are referred as load resistance and inductance.

Solving above equation by considering balanced three phase load, the common mode voltage (V_{NG}) can be written as

$$
V_{NG} = \frac{V_X + V_Y + V_Z}{3} \tag{3.29}
$$

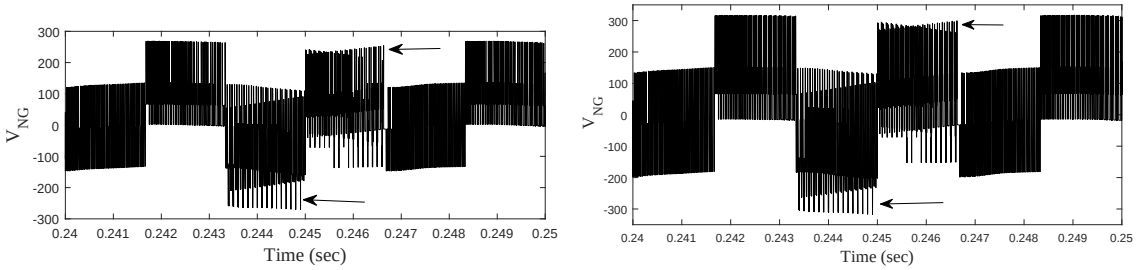
On substituting $V_X = V_B + V_c$, $V_Y = V_B - V_c$ & $V_Z = V_B - V_c$ in above equation gives

$$
V_{NG} = \frac{3V_B - V_c}{3} \tag{3.30}
$$

Similar analysis done on different switching states (Figure.3.40) which are calculated and given as

$$
\begin{aligned}
d^1_{\mu\beta} &\Rightarrow V_{NG} = \tfrac{3V_B+V_c}{3} \\
d^1_{\delta\alpha} &\Rightarrow V_{NG} = \tfrac{3V_C-V_c}{3} \\
d^1_{\delta\beta} &\Rightarrow V_{NG} = \tfrac{3V_C+V_c}{3} \\
d_{\mu\alpha} &\Rightarrow V_{NG} = \tfrac{3V_B-V_c}{3} \\
d_{\mu\beta} &\Rightarrow V_{NG} = \tfrac{3V_B+V_c}{3} \\
d^1_{p\alpha} &\Rightarrow V_{NG} = \tfrac{3V_A-V_c}{3} \\
d^1_{p\beta} &\Rightarrow V_{NG} = \tfrac{3V_A+V_c}{3} \\
d_{p\alpha} &\Rightarrow V_{NG} = \tfrac{3V_A+V_c}{3} \\
d_{p\beta} &\Rightarrow V_{NG} = \tfrac{3V_A+2V_c}{3}
\end{aligned} \tag{3.31}
$$

It can seen from above eq.(3.30)-(3.31) that the common mode voltage of proposed converter is depends upon the magnitude of input phase voltage (V_A, V_B, V_C), capacitor voltage (V_c) value and switching pattern. Figure.3.41 shows an example of common mode voltage variation corresponding to change in duty ratio by keeping other parameters constant. The peak value of V_{NG} increases as duty ratio increases. By careful selection of sequence of switching states in a switching period, the $\frac{dV_{NG}}{dt}$ is controlled, which is the main cause for insulation breakdown of the load. With a predefined modulation technique(pattern), common mode voltage of a SC-USMC is controlled by controlling capacitor voltage $V_c = \frac{3\hat{V}_i m_c \cos\phi_i}{2(1-d)}$.



(a) $d = 0.5$ (b) $d = 0.6$

Figure 3.41: V_{NG} voltage variation

This section presents basic idea about common mode voltage calculations as a base for future research work on common mode voltage reduction in the proposed converter.

3.7 Comparative analysis

The impedance source (Z source) matrix converters gained lot of attention by overcoming the inherent limitation of voltage gain and power fluctuations. In this section, proposed converter is compared with impedance source ultra sparse matrix converters. The impedance source network consists of L and C elements connected in the form of lattice network which acts as boosting circuit. By placement of different impedance networks at input stage or at intermediate stage in indirect matrix converter various topologies are produced. Locating impedance source network at input supply side of an indirect matrix converter resulted in ZSIMC [27], qZSIMC with discontinuous input current, qZSIMC with continuous input current [48], LC filter integrated qZSIMC [49] topologies. Topologies that are having impedance source network incorporated at input side results in limitations such as more number of passive elements and input filter elements, additional bidirectional switch for each phase and requirement of higher rated devices (including both rectifier and inverter switches). To overcome the aforementioned limitations, researchers focussed on locating impedance networks at intermediate stage. This resulted in cascaded Z source ultra sparse matrix converter (CZ-USMC) [30]- [50], series Z source ultra sparse matrix converter (SZ-USMC) [34], Quasi Z source ultra sparse matrix converter (QZ-USMC) [51] and switched inductor Z source ultra sparse matrix converter (SWZ-USMC) [31]. So, impedance source network placement at inter-

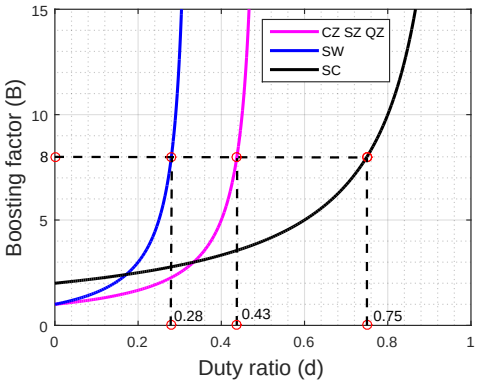


Figure 3.42: Boosting vs duty ratio

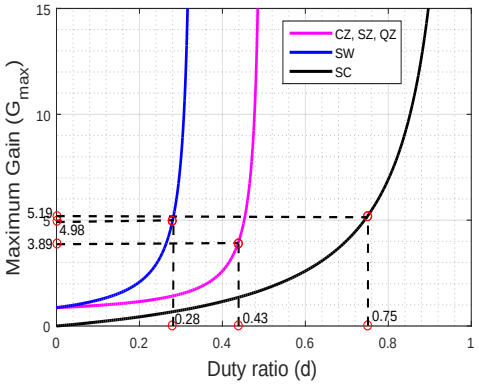


Figure 3.43: Maximum gain vs duty ratio

Table 3.2: Gain variation

Boost	Maximum modulation index ($m_v \leq (1-D)$)			Maximum Gain (G_{max})		
B	CZ,SZ,QZ-USMC	SWZ-USMC	SC-USMC	CZ,SZ,QZ-USMC	SWZ-USMC	SC-USMC
12	0.541	0.702	0.833	5.622	7.29	8.656
10	0.550	0.709	0.800	4.763	6.13	6.928
8	0.562	0.720	0.750	3.893	4.98	5.196
6	0.583	0.736	0.666	3.029	3.82	3.460
5	0.600	0.750	0.600	2.598	3.24	2.598
4	0.625	0.769	0.500	2.165	2.66	1.732

mediate DC link section of ultra sparse matrix converter are chosen as common ground for comparative analysis. Except SWZ network, remaining Z networks are having a common boosting factor $B_{CZ} = B_{SZ} = B_{QZ} = \frac{1}{1-2d}$, while the boosting achieved by SWZ network is $B_{SWZ} = \frac{1+d}{1-3d}$ and Boosting factor for SC (switched capacitor) network is $B_{SC} = \frac{2}{1-d}$. Their characteristics for boosting factor are shown in Figure.3.42. For same boosting factor (B) of CZ, SWZ source or Switched capacitor network as shown in Figure.3.43, the overall maximum gain (G_{max}) at the output terminals are different as mentioned in Table 3.2. It is shown that the maximum modulation index achieved by inverter in CZ-USMC, SZ-USMC, QZ-USMC and SWZ-USMC is $m_v \leq (1-d)$, where as in SC-USMC $m_v \leq d$. By considering $B = 8$, the maximum modulation index for CZ-USMC is 0.562, SWZ-USMC is 0.720 and for SC-USMC is 0.750, therefore the overall gain for CZ-USMC, SWZ-USMC and SC-USMC are 3.893, 4.98 and 5.196, respectively. As desired gain increases beyond 6, the SC-USMC delivers higher voltage than CZ-USMC, SZ-USMC, QZ-USMC and SWZ-USMC. Moreover, the boosting curve for Switched capacitor network has more linear region than other impedance source networks, which is beneficial under wide range of load variations.

A comprehensive comparison of the proposed converter and contemporary con-

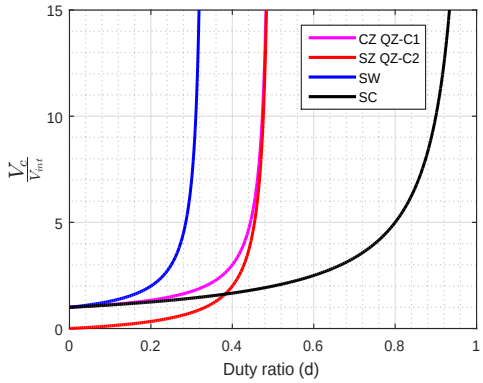


Figure 3.44: $\frac{V_c}{V_{pn}}$ vs duty ratio

verters are listed in Table 3.3. The voltage stress across capacitors are shown in Figure.3.44. Except SZ-USMC, for CZ-USMC, QZ-USMC and SWZ-USMC the capacitor voltage requirements are higher than SC-USMC as the duty ratio increases. To deliver maximum gain at output voltage CZ, SZ and QZ source networks need to operate around $d = 0.4$ (Figure.3.44), while SWZ source network need to operate around $d = 0.3$. Due to increased slope variation around this operating point, precise control of duty ratio is required by having higher sampling rate processor. On the other hand in SC network having a more linear region, cost effective lower sampling rate processor may be used. Moreover, SC network utilises higher modulation index when higher gain is desired compared to other impedance source networks. In CZ source network, there is inrush current problem at starting, this was later reduced in SZ and QZ source networks. Inrush happens with switched capacitor network but is lower in magnitude, since both inductor and switch comes in action at starting. In addition the number of passive elements required for implementation of switched capacitor is one less than other impedance source networks at the expense of one extra switch, as listed in Table 3.3. For deciding the inverter switch ratings, CZ-USMC, SZ-USMC, QZ-USMC

Table 3.3: Comparison table

Converter	Gain	Capacitor voltage	No.of passive elements	No. of diodes	No. of switches
CZ-USMC	$G = \frac{\sqrt{3}m_c m_v cos\varphi}{2(1-2D)}$	$V_{C1} = V_{C2} = \frac{(1-D)}{(1-2D)}V_{Int}$	4	18	9
SZ-USMC	$G = \frac{\sqrt{3}m_c m_v cos\varphi}{2(1-2D)}$	$V_{C1} = V_{C2} = \frac{(D)}{(1-2D)}V_{Int}$	4	19	9
QZ-USMC	$G = \frac{\sqrt{3}m_c m_v cos\varphi}{2(1-2D)}$	$V_{C1} = \frac{(1-D)}{(1-2D)}V_{Int}, V_{C2} = \frac{(D)}{(1-2D)}V_{Int}$	4	19	9
SWZ-USMC	$G = \frac{\sqrt{3}(1+D)m_c m_v cos\varphi}{2(1-3D)}$	$V_{C1} = V_{C2} = \frac{(1-D)}{(1-3D)}V_{Int}$	6	24	9
SC-USMC	$G = \frac{\sqrt{3}m_c m_v cos\varphi}{(1-D)}$	$V_{C1} = V_{C2} = \frac{1}{(1-D)}V_{Int}$	3	20	10

and SWZ-USMC have to consider both higher current rating (due to shoot through

current rating of a switch) and voltage ratings, where as for SC-USMC the switch rating is mainly based on voltage rating (because of $2V_c$ at inverter input terminals) with nominal load current rating. Efficiency plot for SC-USMC and other converters are simulated with output power rating of $500W$, diode forward voltage rating is chosen as $0.1V$ and switches $R_{DS(on)}$ value is chosen as 0.01Ω under similar loading condition for a constant input voltage, as shown in Figure.3.45. Over a range of voltage gains, SZ-USMC shows better efficiency at lower gains upto 2 where as SC-USMC shows improved performance at higher voltage gains. The maximum efficiency achieved by SC-USMC is 87% at voltage gain of 2 times the input.

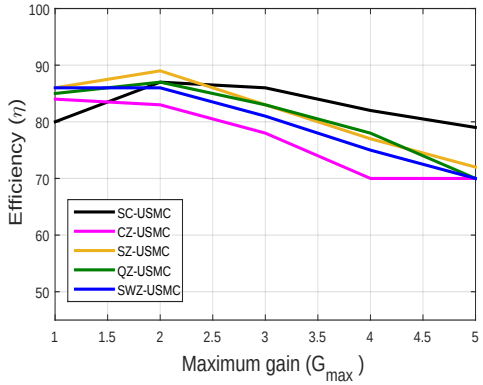


Figure 3.45: Efficiency Vs maximum gain (G_{max})

3.8 Conclusion

This chapter proposes enhanced voltage gain for ultra sparse matrix converter. By utilizing the idea of switched capacitor network, a modification is made to integrate it within USMC. This modification overcomes the inherent limitations of USMC without compromising on input and output THD performances. While analysing the boosting operation, experimental results are found to be in agreement with simulation and analytical calculation. The proposed topology has potential in terms of overall gain, linear operating region, design parameters and efficiency as compared to the contemporary converters.

Though SC-USMC utilises only three passive elements, one extra switch and two extra diode are required. For minimising the number of passive elements, enhanced EMI immune capability and to maintain voltage gain higher than unity switched boost

network based USMC is proposed in the next chapter.