Chapter 5

Triple-mode Flexible High gain Converter

5.1 Introduction

Low voltage and current stress in switch can reduce the losses in the converters. Furthermore, low electromagnetic interference (EMI) and shared ground are the good choice for DC microgrid applications. In this chapter, the ASL network is utilized, and the range of the duty cycle varies by incorporating an additional switch into the converter circuitry. ASL with SC topology is reported in [62], [63]. While operating at high duty ratios, these topologies strive for high gain, which leads to more conduction losses in the switches of the ASL network. This limitation is addressed by an enhanced version featuring an auxiliary switch configuration as proposed in [70]. However, this enhancement comes with drawbacks, such as lower gain and the absence of a common ground. The main features of an enhanced version of the ASL network are as follows: The main features of enhanced version of ASL network are as follows:

1. The converter uses low device count, to achieve flexible high voltage gain.

2. The flexible voltage is accomplished by different combination of duty cycles of the switches.

3. Voltage stress across switches and diodes are reduced compared to the output voltage.

5.2 Proposed converter-5

The proposed converter-5 is derived from the ASL network. The modified converter is composed of two Switches S_1, S_2 that act as a main switch (bidirectional for current) and two inductors L_1, L_2 at low voltage side, as shown in Figure 5.1. In addition to this, one auxiliary Switch S_3 is connected in series with Diode D_1 to achieve unidirectional current. SC cell (D_2 C_1), (D_3 C_2), and (D_4 C_0) are utilized in the converter to enhance the voltage gain of the converter. The duty cycle of the main and auxiliary switch is defined by D_1 and D_2, respectively.

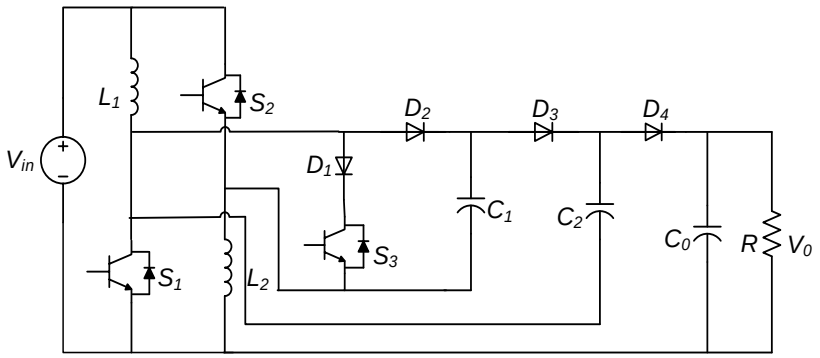

Figure 5.1: Flexible high gain proposed converter-5.

5.2.1 Operating principle and its modes

The proposed converter has three modes in continuous current mode (CCM), which can be summarized as follows. The steady state waveform during CCM mode is shown in Figure 5.2.

Mode 1

For this Mode, main switches S_1, S_2 are turned ON and auxiliary Switch S_3 is turned OFF. Both inductors L_1 and L_2 are magnetizes by input voltage V_{in}. Capacitor C_1 discharges its energy to charge C_2 through Diode D_3. The voltage across inductors and capacitors is expressed as follows using equivalent circuitry:

$$v_{L1} = v_{L2} = V_{in} \tag{5.1}$$

$$v_{C2} - v_{C1} = V_{in} \tag{5.2}$$

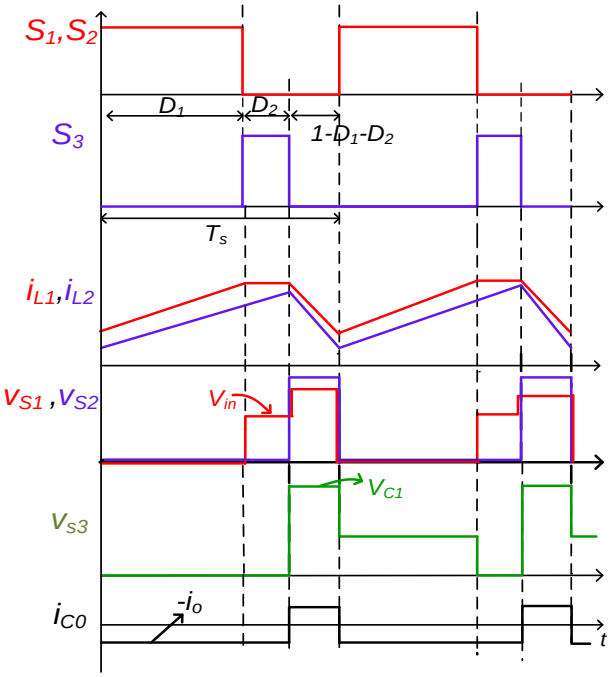

Figure 5.2: Operating waveform during CCM.

$$i_{c1} = -i_{c2} \tag{5.3}$$

$$i_{c0} = -i_0 \tag{5.4}$$

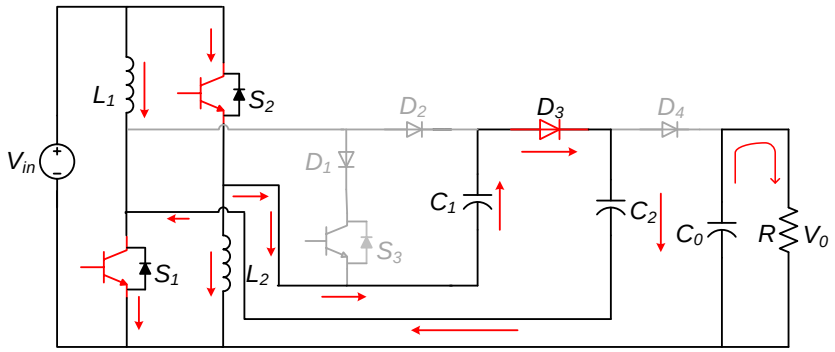

Figure 5.3: Mode 1 equivalent circuit.

Mode 2

Both switches S_1 and S_2 are turned OFF but auxiliary Switch S_3 is turned ON. The voltage across inductor L_1 is almost zero due to the reverse conducting diode of Switch

S_2. However, inductor L_2 is still magnetized with V_{in}.

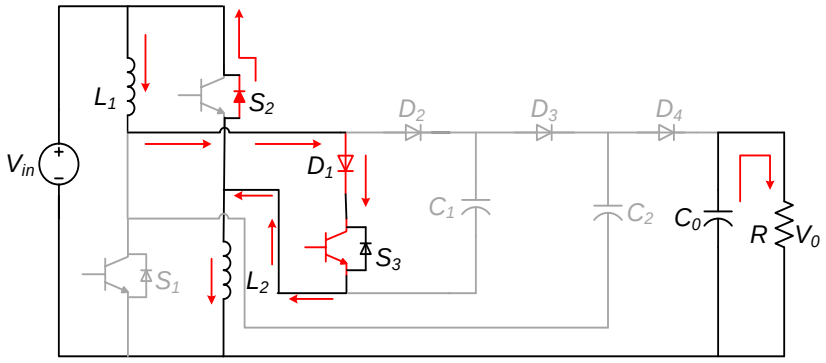

Figure 5.4: Mode 2 equivalent circuit.

$$v_{L1} = 0 \tag{5.5}$$

$$v_{L2} = V_{in} \tag{5.6}$$

$$i_{c1} = i_{c2} = 0, \quad i_{c0} = -i_0 \tag{5.7}$$

Mode 3

In this mode, all three switches are turned OFF. Inductor L_1 releases its stored energy to charge capacitor C_0, C_1 via Diodes D_4 and D_2. Similarly, L_2 releases its energy to charge capacitor C_1 through Diode D_2. The following equation holds for Mode-3:

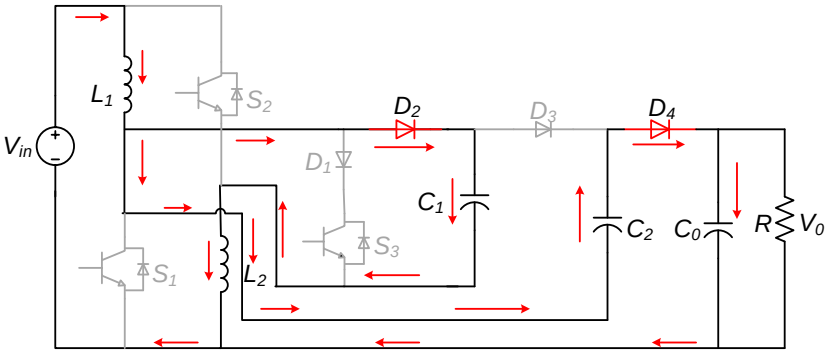

Figure 5.5: Mode 3 equivalent circuit.

$$v_{L1} = V_{in} + v_{C2} - v_0 \tag{5.8}$$

$$v_{L2} = V_{in} - v_{L1} - v_{C1} \tag{5.9}$$

$$v_{L2} = v_0 - v_{C1} - v_{C2} \tag{5.10}$$

$$i_{c1} = i_{L2} \tag{5.11}$$

$$i_{c2} = -i_{C0} - i_0 \tag{5.12}$$

The relation between output to input voltage transfer function depends on duty cycle of used switches, D_1 and D_2, respectively. The voltage gain relation can be deduced by the volt-second law across both inductor L_X (X=1,2)

$$\int_0^{D_1T_s} V_{L_X}dt + \int_0^{D_2T_s} V_{L_X}dt + \int_0^{(1-D_1-D_2)T_s} V_{L_X}dt = 0 \tag{5.13}$$

Substituting the value of V_{L1} and V_{L2}, results following expressions;

$$\left.\begin{aligned} V_{C1} &= \frac{(1+D_1)}{(1-D_1-D_2)}V_{in} \\ V_{C2} &= \frac{(2-D_2)}{(1-D_1-D_2)}V_{in} \end{aligned}\right\} \tag{5.14}$$

Therefore, output voltage of converter is

$$V_0 = \frac{(3-2D_2)}{(1-D_1-D_2)}V_{in} \tag{5.15}$$

Voltage gain M_{CCM} of proposed converter can be given by,

$$M = \frac{V_0}{V_{in}} = \frac{(3-2D_2)}{(1-D_1-D_2)} \tag{5.16}$$

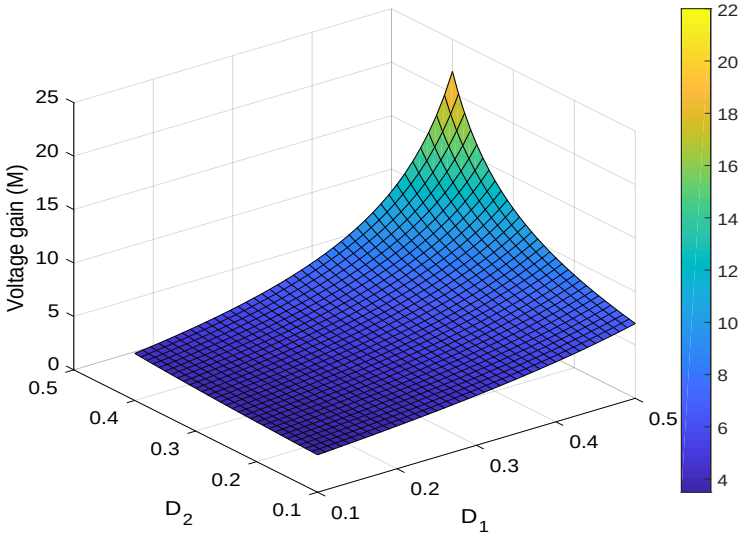

Figure 5.6: Voltage gain of converter in CCM with variation of D_1 and D_2.

The voltage gain variation of proposed converter-5 with respect to both duty cycle is illustrated in Figure 5.6.

5.2.2 DCM operation and boundary condition

DCM operation is divided into four operating modes shown in Figure 5.7. The first and second modes are the same as the CCM operation. The inductor current reaches zero in the third operating Mode (D_3), and in the final fourth Mode, all devices are turned OFF, and the inductor current becomes zero. Therefore, in DCM operation, the following relation can be derived.

$$\left.\begin{aligned} V_{in}D_1 + V_{in}D_2 + (V_0 - V_{C1} - V_{C2})D_3 + 0 = 0 \\ D_3 = \frac{(D_1 + D_2)}{(V_{C1} + V_{C2} - V_0)} V_{in} \end{aligned}\right\} \tag{5.17}$$

Capacitor discharge its stored energy to load. The average current through output capacitor for each switching state is given by;

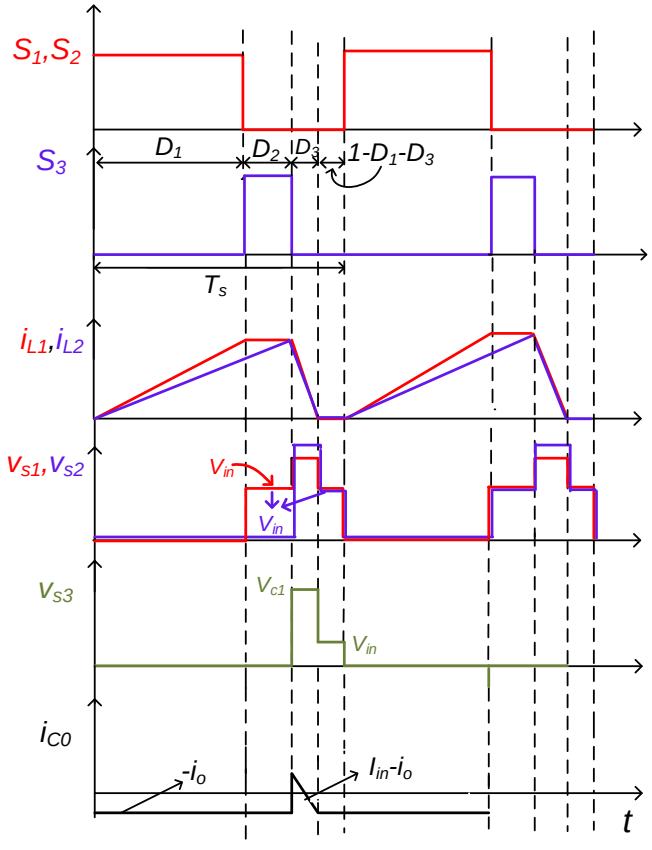

Figure 5.7: Steady state waveform during DCM.

$$I_{C0} = \frac{\frac{1}{2}(D_3 T_s I_{L2_{max}}) - I_0 T_s}{T_s} \tag{5.18}$$

In steady state I_{CO} equals to zero,

$$I_{C0} = \frac{(D_1+D_2)^2 V_{in}^2 T_s}{(V_{C1}+V_{C2}-V_0)2L} - \frac{V_0}{R} = 0 \tag{5.19}$$

Solving eq (5.19) voltage gain during DCM operation can be given by,

$$\frac{V_0}{V_{in}} = \frac{1}{2}A + \frac{1}{2}\sqrt{A^2 + \frac{2(D_1+0.5D_2)^2}{\tau}} \tag{5.20}$$

Where, $\tau = \frac{L}{RT_s}$, and $A = \left(\frac{3+D_1-D_2}{1-D_1-D_2}\right)$. The boundary condition for developed converter can be found as:

$$\tau_{BCM} = \frac{(1-D_1-D_2)^2(D_1+0.5D_2)}{2(3-2D_2)} \tag{5.21}$$

However, to operate the converter in CCM, the eq. (5.22) is necessary to be satisfied.

$$\tau > \frac{(1-D_1-D_2)^2(D_1+0.5D_2)}{2(3-2D_2)} \tag{5.22}$$

The boundary condition of proposed converter for different value of D_2 is shown in Figure 5.8 and for each value of D_2 (DCM region are below curve). Figure 5.8 illustrated

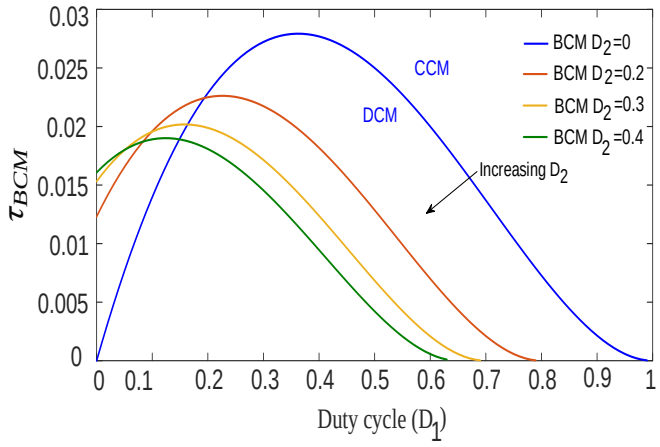

Figure 5.8: Proposed converter-5 boundary condition.

τ_{BCM} versus D_1 based on the different value of D_2. Moreover, CCM and DCM regions are shown for each value of D_2. As can be seen, the increase in the duty cycle D_2 expands the CCM region of the proposed converter.

5.3 Device stress and design equations

Device stress and degin equations are analysed by applying kirchhoff current law (KCL) in a Figure 5.3, Figure 5.4 and Figure 5.5, current stress through capacitor, diodes and

Table 5.1: Current stress of capacitor and diodes

Devices	Mode 1	Mode 2	Mode 3
C_1	$\frac{-I_0}{D_1}$	0	$\frac{I_0}{(1-D_1-D_2)}$
C_2	$\frac{I_0}{D_1}$	0	$\frac{-I_0}{(1-D_1-D_2)}$
C_0	$-I_0$	$-I_0$	$\frac{I_0(D_1+D_2)}{(1-D_1-D_2)}$
D_1	0	$\frac{2I_0}{(1-D_1-D_2)}$	0
D_2	0	0	$\frac{I_0}{(1-D_1-D_2)}$
D_3	$\frac{I_0}{D_1}$	0	0
D_4	0	0	$\frac{I_0}{(1-D_1-D_2)}$
S_1	$\frac{(1+D_1-D_2)I_0}{(1-D_1-D_2)D_1}$	0	0
S_2	$\frac{(1-D_2)I_0}{(1-D_1-D_2)D_1}$	$\frac{I_0}{(1-D_1-D_2)}$	0
S_3	0	$\frac{2I_0}{(1-D_1-D_2)}$	0

switches can be derived and reported in Table 5.1. Similarly like current stress voltage stress across diodes and switches can be examined in Table 5.2.

Inductor and capacitor design

For proposed converter-5 to operate in CCM, the inductor current must be higher than half of their ripple current, $(2I_{Lx} \geq \Delta i_L, x = 1, 2)$.

Table 5.2: Voltage stress across diodes and switches CCM operation

Devices	Mode 1	Mode 2	Mode 3
D_1	V_{in}	0	0
D_2	$\frac{(2-D_2)}{(1-D_1-D_2)}V_{in}$	$\frac{(1+D_1)}{(1-D_1-D_2)}V_{in}$	0
D_3	0	V_{in}	$\frac{(2-D_2)}{(1-D_1-D_2)}V_{in}$
D_4	$\frac{(1-D_2)}{(1-D_1-D_2)}V_{in}$	$\frac{D_1V_{in}}{(1-D_1-D_2)}$	0
S_1	0	V_{in}	$\frac{(1-D_2)}{(1-D_1-D_2)}V_{in}$
S_2	0	0	$\frac{V_{in}}{(1-D_1-D_2)}$
S_3	0	0	$\frac{(1+D_1)V_{in}}{(1-D_1-D_2)}$

$$-i_{c2}D_1 + 0.D_2 + i_{L2}(1-D_1-D_2) = 0$$
$$I_{C2} = \frac{I_{L2}}{D_1}(1-D_1-D_2) \tag{5.23}$$

Applying Mode 1, Mode 2, and Mode 3 for charge-balance across, C_2. Similarly, applying charge balance law across C_0 gives following result,

$$-I_0.D_1 - I_0.D_2 + i_{C0}(1-D_1-D_2) = 0$$
$$I_{C0} = \frac{I_0}{1-D_1-D_2}(D_1+D_2) \tag{5.24}$$

Similarly the expression of C_1, for Mode 1 and Mode 3 can be deduced;

$$I_{C1} = \frac{-I_0}{D1}, \quad I_{C2} = \frac{-I_0}{1-D_1-D_2} \tag{5.25}$$

Using Mode 3 and average current flowing through both inductor is given as:

$$I_{L2} = I_{C1}, \quad I_{L1} = I_{L2} - I_{C2} \tag{5.26}$$

$$I_{L1} = \frac{2I_0}{(1-D_1-D_2)}, \qquad I_{L2} = \frac{I_0}{(1-D_1-D_2)} \tag{5.27}$$

The inductance can be calculated as;

$$L_1 \geq \frac{V_{in}^2(3-2D_2)D_1}{4P_0 f_s}, \qquad L_2 \geq \frac{V_{in}^2(3-2D_2)D_1}{2P_0 f_s} \tag{5.28}$$

The capacitance selection is based on voltage ripple in the capacitors and assuming 2-3% of average voltage.

$$C_1 = C_2 = \frac{I_0}{\Delta v_{c1} f_s}, \qquad C_0 = \frac{I_0 D_1}{\Delta v_{c0} f_s} \tag{5.29}$$

Where Δv_{c1} %, Δv_{c2} % and Δv_{c0} are the percentage voltage ripple and f_s = switching frequency of converter.

5.4 Comparison and analysis of converter

Voltage gain comparison with other topologies

In order to clearly demonstrate the benefits of the proposed converter, Table 5.3 compares similar topologies in terms of voltage gain, number of device utilized and switch as well as diode stress. ASL network in converter [62],[63] needs high duty cycle to

achieve higher voltage conversion ratio. Three switch based ASL converter is reported in [71] with low component to achieve high gain however the voltage stress across auxiliary switch is equal to output voltage. Improved version of converter is presented in [72] with more switch stress across auxiliary switch. Converter [73] achieves high gain but all switches encounter high voltage stress compared to the proposed converter. Converter [70] and [74] is reported with slightly low gain and more voltage stress across output diode. Converter [75] is reported by the authors with more gain as compared to the proposed converter but output diode is having more voltage stress. Compared converters are presented in Figure 5.9. Except the proposed converter rest do not have common ground. Zoomed voltage gain of Figure 5.9 is shown in Figure 5.10 at low range of duty cycle.

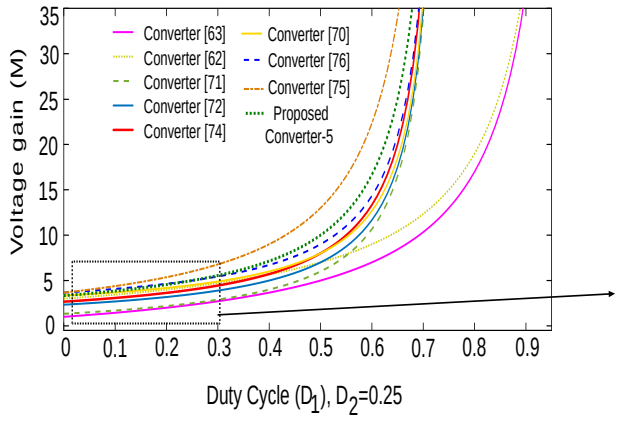

Figure 5.9: Comparison of voltage gain of various converter for $D_2 = 0.25$.

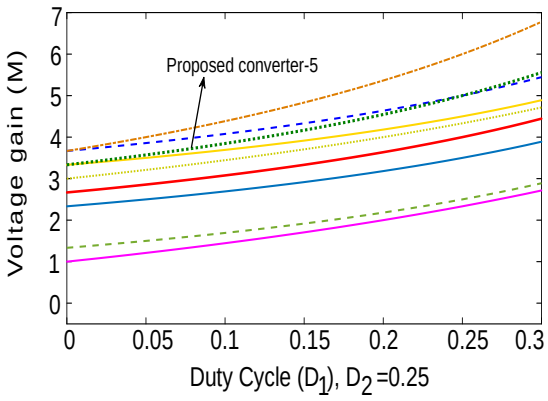

Figure 5.10: Zoomed plot of voltage gain.

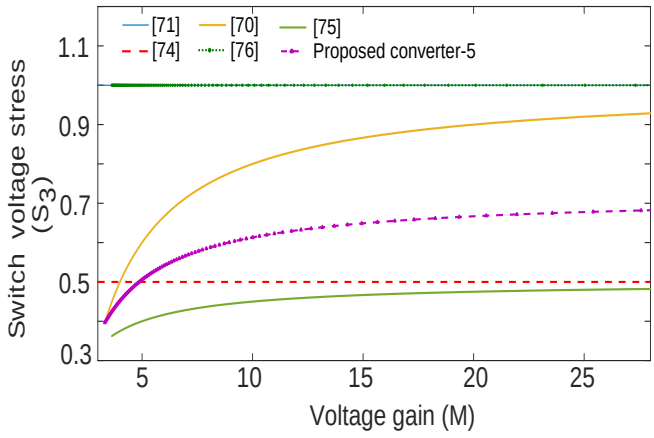

Figure 5.11: Normalized switch stress across S_3.

Table 5.3: Comparison of proposed converter-5 with existing topologies

Topology	*L*	*C*	*S*	*Di*	TC	*Gain*	*Maximum Switch stress*	*Maximum Diode stress*	Efficiency	input current	Common ground
[63]	3	3	2	2	10	$\frac{1+3D}{1-D}$	$V_{S1}=V_{S2}=\frac{V_0}{1+3D}$	$V_{D1}=V_{D1}=\frac{2}{1+3D}V_0$	95.9%	continuous	NO
[62]	2	3	2	3	10	$\frac{3+D}{1-D}$	$V_{S1}=V_{S2}=\frac{V_0}{3+D}$	$V_{D1}=V_{D2}=\frac{2V_0}{3+D}$ $V_{D0}=\frac{2V_0}{3+D}$	96%	continuous	NO
[71]	2	1	3	2	8	$\frac{1+D_1}{1-D_1-D_2}$	$V_{S1}=V_{S2}=\frac{2-D_2}{2(1+D_1)}V_0$ $V_{S3}=V_0$	$V_{D1}=\frac{1-D_1-D_2}{1+D_1}V_0$ $V_{D2}=\frac{2-D_2}{1+D_1}V_0$	95%	continuous	NO
[72]	2	2	3	3	10	$\frac{2-D_2}{1-D_1-D_2}$	$V_{S1}=V_{S2}=\frac{1-D_1-D_2}{2(2-D_2)}V_0$ $V_{S3}=\frac{1+D_1}{1-D_1-D_2}V_0$	$V_{D1}=\frac{V_0}{2}$ $V_{D2}=\frac{1+D_1}{1-D_1-D_2}V_0$	96%	continuous	NO
[74]	2	2	3	3	10	$\frac{2}{1-D_1-D_2}$	$V_{S1}=V_{S2}=\frac{V_0}{2}$ $V_{S3}=\frac{V_0}{2}$	$V_{D1}=V_{D2}=\frac{V_0}{2}$ $V_{D0}=V_0$	95%	continuous	NO
[70]	2	3	2	2	10	$\frac{3-D_1-2D_2}{1-D_1-D_2}$	$V_{S1}=\frac{(2-D_2)}{2(3-D_1-2D_2)}V_0$ $V_{S2}=\frac{(2-D_2)}{2(3-D_1-2D_2)}V_0$ $V_{S3}=\frac{(1+D_1)}{3-D_1-2D_2}V_0$	$V_{D1}=\frac{(2-D_2)}{2(3-D_1-2D_2)}V_0$ $V_{D2}=\frac{(2-D_2)}{2(3-D_1-2D_2)}V_0$ $V_{D0}=\frac{(2-D_2)}{3-D_1-2D_2}V_0$	93.2%	continuous	NO
[76]	2	3	3	4	12	$\frac{3-D_1-D_2}{1-D_1-D_2}$	$V_{SX}=V_{SY}=\frac{V_0}{3-D_1-D_2}$ $V_{SZ}=V_0$	$V_{DX}=V_{DY}=\frac{V_0}{3-D_1-D_2}$ $V_{DZ}=V_0$	95.1%	continuous	NO
[75]	2	3	3	4	12	$\frac{3+D_1-D_2}{1-D_1-D_2}$	$V_{S1}=V_{S2}=\frac{2-D_2}{2(3+D_1-D_2)}V_0$ $V_{S3}=\frac{1+D_1}{(3+D_1-D_2)}V_0$	$V_{D2}=V_{D3}=\frac{2-D_2}{(3+D_1-D_2)}V_0$ $V_{D0}=\frac{2-D_2}{(3+D_1-D_2)}V_0$	96.8%	continuous	NO
Proposed converter-5	2	3	3	4	12	$\frac{3-2D_2}{1-D_1-D_2}$	$V_{S1}=\frac{1-D_2}{3-2D_2}V_0$ $V_{S2}=\frac{V_0}{3-2D_2}$ $V_{S3}=\frac{1+D_1}{3-2D_2}V_0$	$V_{D1}=\frac{1-D_1-D_2}{3-2D_2}V_0$ $V_{D2,D3}=\frac{2-D_2}{3-2D_2}V_0$ $V_{D4}=\frac{1-D_2}{3-2D_2}V_0$	97.1%	continuous	YES

Note1: In this table L=number of inductor, C=number of capacitor, S=number of switches, Di= number of diodes, TC= total count, D=Duty cycle of converter

Note2: Efficiency number calculated for 400 W power rating and Switching frequency $f_s = 40\ kHz$

Normalized voltage stress and analysis

The normalized voltage across auxiliary Switch S_3 is illustrated in Figure 5.11. It can be seen that voltage across Switch S_3 is in the acceptable range with respect to other topologies. Similarly, the voltage and current stress of the Switch are shown in Figure 5.12 for different values of D_2. It can be seen that the optimal value of voltage and current stress for Switch is near $D_1 = 0.45-0.5$ and $D_2 = 0.15-0.3$. Based on the above analysis, we designed a converter for $D_1 = 0.5$ and $D_2 = 0.25$ to achieve the desired gain with minimal device stress.

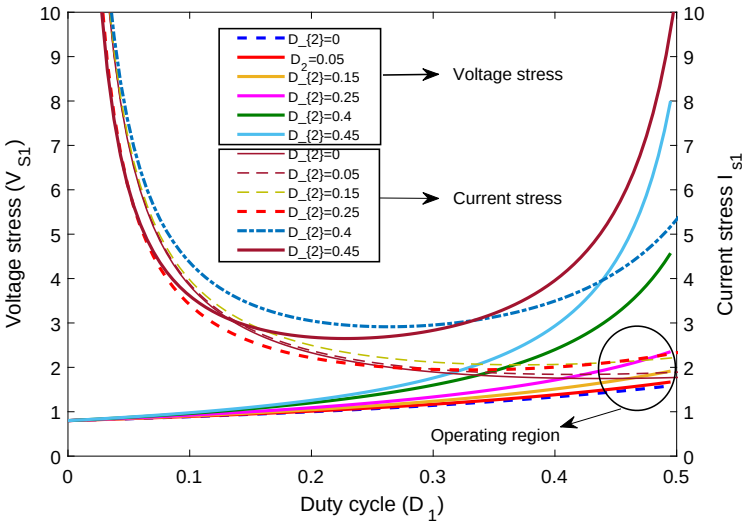

Figure 5.12: Voltage and current stress of switch.

5.5 Experimental validation

To validate the theoretical analysis, a laboratory prototype of the proposed converter is built and a photograph of the prototype as shown in Figure 5.13. The design of storing element for rated power is discussed below. The design of storing element is calculated for $P_0 = 400\ W$ of load power keeping the load resistance $R = 400\ \Omega$, switching frequency f_s=40 kHz and input voltage fixed to 40 V. The duty cycle both Switches fixed to 0.5 (main switch) and 0.25 (auxiliary switch), respectively. The calculation of both inductance can be done using eq. (5.1).

$$L = L_1 = L_2 = \left(\frac{V_{in}}{\Delta I_L}\right) D_1 T_s, \implies L = \frac{40 \times 0.5}{40k \times 0.15} = 420\ \mu H \tag{5.30}$$

Similarly the capacitance calculation is performed using eq. (5.29).

$$C_1 = \frac{I_0 T_s}{\Delta V_{C1}}, \implies C_1 = \frac{1}{0.02 \times 40k} = 15\ \mu F \tag{5.31}$$

$$C_2 = \frac{I_0 T_s}{\Delta V_{C2}}, \implies C_2 = \frac{1}{0.02 \times 40k} = 12\ \mu F \tag{5.32}$$

$$C_0 = \frac{I_0 D_1 T_s}{\Delta V_{C0}}, \implies C_0 = \frac{1 \times 0.5}{0.02 \times 40k} = 8\ \mu F \tag{5.33}$$

The specification and used final value of storing elements for the developed converter is listed in Table 5.4. Moreover, to validate converter-5 components with the manufacturer's name as listed in Table 5.5. For validation of the analytical expression, the converter is tested, and the measured value of input-output parameters for the

proposed converter is V_{in}, I_{in} and V_0 are captured with value 40 V, 10.2 A, 394 V respectively, as shown in Figure 5.14.

Table 5.4: Specification and parameter of converter

Specification	
Input Voltage V_{in}	40 V
Output Voltage V_0	400 V
Output Power P_0	400 W
Switching frequency f_{sw}	40 kHz
Parameter	
Inductance L_1,L_2	420 μH
All Capacitance	47μF

Table 5.5: Device and components used in experimental setup

Component/Device	**Part Number and Manufacturer**
DC Source	H3010, Aplab
MOSFET	IPW60R017C7XKSA1, Infineon
Diode	STPS60SM200CW, STElectectrnoics STTH6004W, STElectectrnoics
Gate driver	HCPL3120 Avago Technology
Inductor	MCAP115018077A-561LU, Multicomp Pro
Capacitor	450QXW47MEFC10X45, Rubycon
Control board	eZdsp F28335 DSP board, Texas

The inductors current profile with an of average value $I_{L1} = 7.95\ A$ and $I_{L2} = 3.8\ A$ presented in Figure 5.15. The inductor current shape of I_{L1} follows eq. (5.5) and acquires a flat shape for a little duration due to a specific current path in the circuit. The measured current ripple of I_{L1} and I_{L2} are 24% and 16%, respectively, which is more than the design guidelines. The maximum value of measured voltage across switch $S_1 \approx 120\ V$ and Switch $S_2 \approx 160\ V$ as shown in Figure 5.16. This is close in agreement with the theoretical one. The measured peak voltage across Diodes $D_1 \approx 42\ V$, $D_2 = 230\ V$ and $D_3 = 270\ V$ as shown in Figure 5.5. All these values

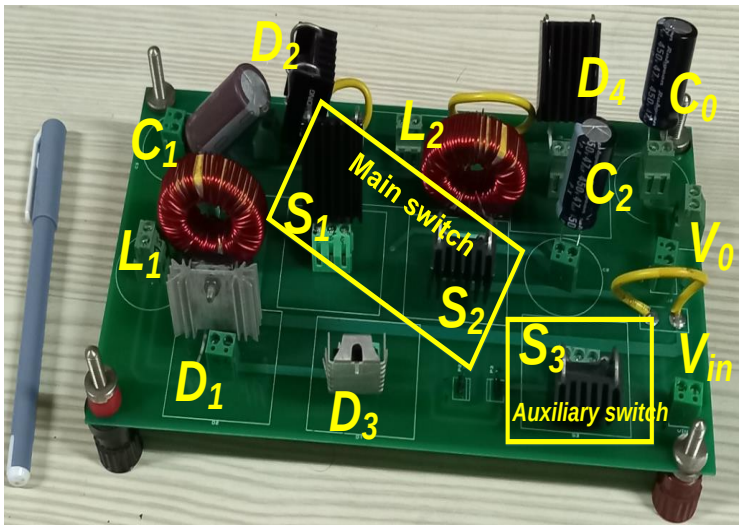

Figure 5.13: Photograph of the proposed converter-5.

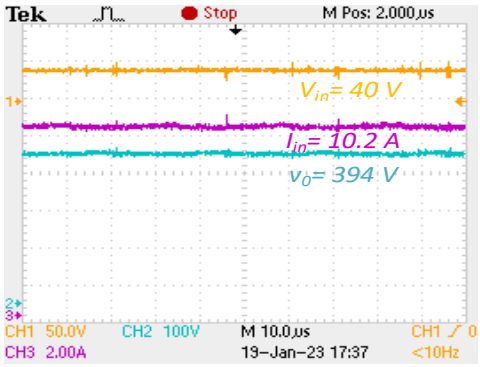

Figure 5.14: Measured steady state input-output waveform.

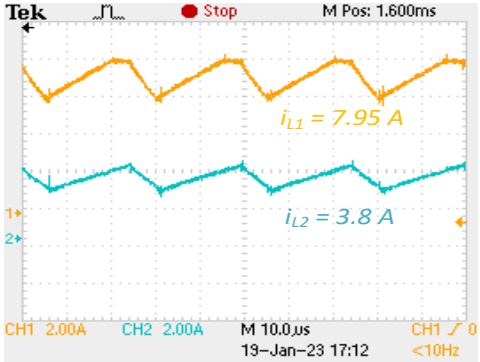

Figure 5.15: Measured inductor current profile for proposed converter

are closer to analytical values presented in Table 5.2. The voltage stress across output Diode $D_4 \approx 140\ V$ and auxiliary Switch $S_3 = 230\ V$ as reported in Figure 5.18. The measured mean voltage across capacitor C_1 and C_2 are 230 V, 250 V, respectively as shown in Figure 5.19.

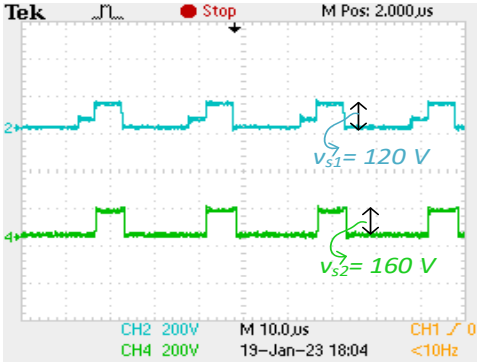

Figure 5.16: Switch stress of main switch S_1 and S_2.

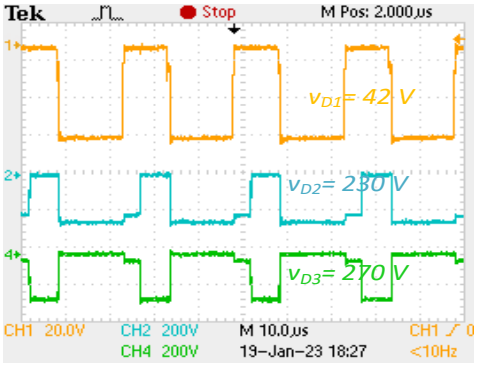

Figure 5.17: Voltage stress across diodes D_1, D_2 and D_3

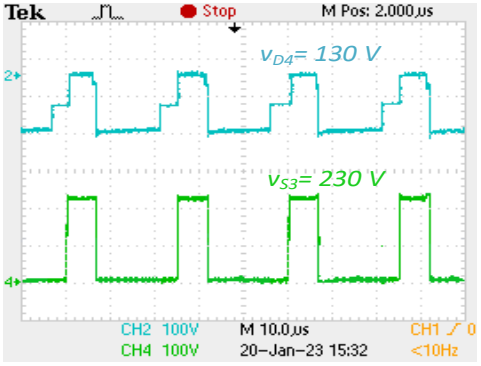

Figure 5.18: Voltage stress across output diode D_4 and auxiliary switch S_3.

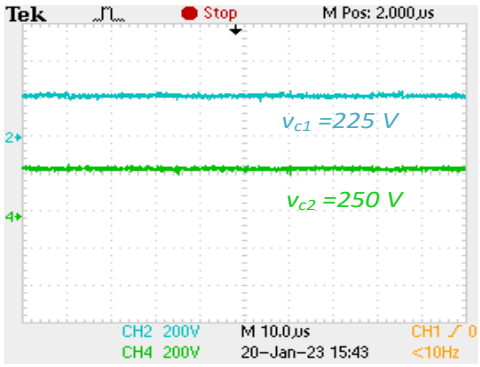

Figure 5.19: Voltage stress across capacitors C_1 and C_2.

5.6 Loss calculation

The proposed converter uses storing elements (L, C), diodes, and power switches. To evaluate the converter's efficiency, calculation of the loss contributed by each device is critical. The analysis of loss for components is given below.

Inductor loss (P_L)

The inductor loss is due to the current flowing through it.

$$P_L = I_{L1}^2 r_{L1} + I_{L2}^2 r_{L2} \tag{5.34}$$

$$P_L = \frac{I_0^2}{(1-D_1-D_2)^2}(4r_{L1} + r_{L2}) \tag{5.35}$$

where, r_{L1} and r_{L2} are the DC resistance of inductor.

Capacitor loss (P_C)

Capacitor loss is due to the equivalent series resistance (ESR) of capacitance. The loss contributed by the capacitor is given in eq. (5.36). The rms value of current (I_{Crms}) in various capacitor is given as,

$$P_C = I_{C1}^2 r_{c1} + I_{C3}^2 r_{c3} + I_{C4}^2 r_{c4} + I_{C0}^2 r_{c0} \tag{5.36}$$

$$I_{C1} = \sqrt{\left(\frac{-I_0}{D_1}\right)^2 D_1 + \left(\frac{I_0}{1-D_1-D_2}\right)^2 (1-D_1-D_2)} \tag{5.37}$$

$$I_{C1} = I_0 \sqrt{\frac{(1-D_2)}{D_1(1-D_1-D_2)}} \tag{5.38}$$

In the same way rms value of capacitor C_2 is given by,

$$I_{C2} = I_0\sqrt{\frac{(1-D_2)}{D_1(1-D_1-D_2)}} \tag{5.39}$$

Finally, rms current of output capacitor is calculated as,

$$I_{C0} = \sqrt{((-I_0)^2D_1+(-I_0)^2D_2)+\left(\frac{I_0(D_1+D_2)}{(1-D_1-D_2)}\right)^2(1-D_1-D_2)} \tag{5.40}$$

$$I_{C0} = I_0\sqrt{\frac{(D_1+D_2)}{(1-D_1-D_2)}} \tag{5.41}$$

Diode loss (P_D)

The loss occurs in the diode due to forward voltage drop and due to conduction. The diode loss is given by,

$$P_D = V_D I_{D1_{avg}} + V_D I_{D2_{avg}} + V_D I_{D3_{avg}} + V_D I_{D0_{avg}} + I^2_{D1_{rms}} r_d + I^2_{D2_{rms}} r_d + I^2_{D3_{rms}} r_d + I^2_{D0_{rms}} r_d \tag{5.42}$$

$$I_{D1,avg} = \frac{2I_0}{(1-D_1-D_2)}D_2 \tag{5.43}$$

$$I_{D2,avg} = I_{D3,avg} = I_{D0,avg} = I_0 \tag{5.44}$$

The rms value of current through each diodes calculated as,

$$I_{D1} = \frac{2I_0}{(1-D_1-D_2)}\sqrt{D_2} \tag{5.45}$$

$$I_{D2} = I_0\sqrt{\frac{1}{(1-D_1-D_2)}} \tag{5.46}$$

$$I_{D3} = I_0\sqrt{\frac{1}{(D_1}} \tag{5.47}$$

$$I_{D0} = I_0\sqrt{\frac{1}{(1-D_1-D_2}} \tag{5.48}$$

Switch loss (P_S)

The switches loss is divided into two parts: one is due to the conduction P_{CSW} process, and the other is due to the switching behavior of switches. The calculation for switch loss can be given as

$$P_{CSW} = (I^2_{S1rms} + I^2_{S2rms} + I^2_{S3rms}) r_{dsON} \tag{5.49}$$

The rms value of current through switches is given by the following formulas,

$$I_{S1} = I_0\sqrt{\left(\frac{1+D_1-D_2}{(1-D_1-D_2)D_1}\right)^2 D_1} \tag{5.50}$$

$$I_{S2} = I_0\sqrt{\left(\frac{1-D_2}{(1-D_1-D_2)D_1}\right)^2 D_1 + \left(\frac{1}{(1-D_1-D_2)}\right)^2 D_2} \tag{5.51}$$

$$I_{S3} = 2I_0\sqrt{\left(\frac{1}{1-D_1-D_2}\right)^2 D_2} \tag{5.52}$$

The switching loss can be given by using mention formula,

$$P_{SW} = \frac{1}{6}V_S I_S(t_{on}+t_{off})f_{sw} \tag{5.53}$$

For power loss distribution parasitic effect of each component is considered: Inductors resistance $r_{L1} = r_{L2} = 0.08\ \Omega$, capacitor resistance $r_{C1} = r_{C2} = 0.15\ \Omega$ and $r_{C0} = 0.3\ \Omega$, MOSFET ON-state resistance $r_{dson} = 0.015\ \Omega$, diode drop $V_f = 0.58$ V for Diode D_1 and $V_f = 0.8\ V$ for remaining diodes, diode resistance $r_d = 0.003\ \Omega$ and switching frequency $f_{sw} = 40$ kHz. The power loss distribution is depicted in

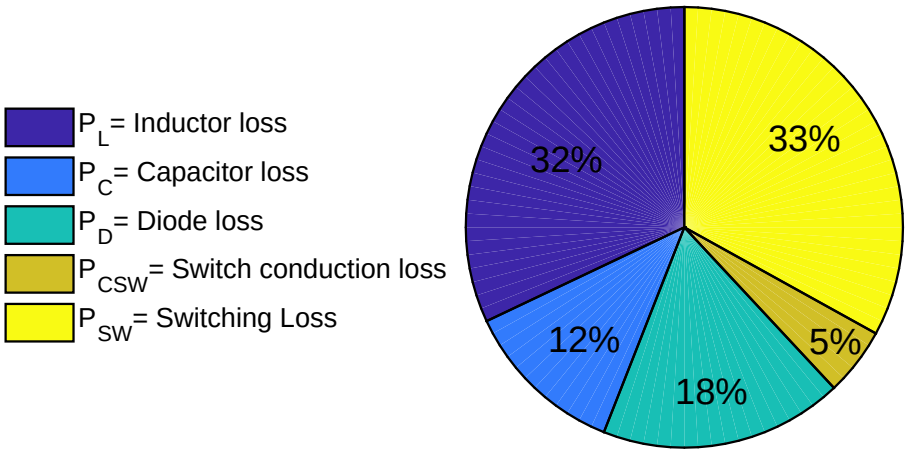

Figure 5.20: Power loss distribution for proposed converter at 400 W.

Figure 5.20. According to specification listed ib Table 5.4, the losses contributed by inductors $P_L = 6.8\ W$, capacitor $P_C = 2.5\ W$, diode loss $P_D = 3.6\ W$, Mosfet conduction loss $P_{s,conducction} = 1.2\ W$ and switching loss $P_{s,swtching} = 6.6\ W$. From the power distribution curve, the measured efficiency of the converter is 95.1%. According to the estimated values, the switch losses present the most significant impact on the converter efficiency followed by the inductors, diodes, and capacitors.

The proposed converter is also tested experimentally at different power levels. The efficiency achieved in the experiment is slightly lower than the theoretical efficiency due to parasitics present in the designed setup. At 400 W, the experimental efficiency is 95.1%, which is lower than the theoretical efficiency. Figure 5.21 shows the theoretical and experimental efficiency for input voltage $V_{in} = 40\ V$.

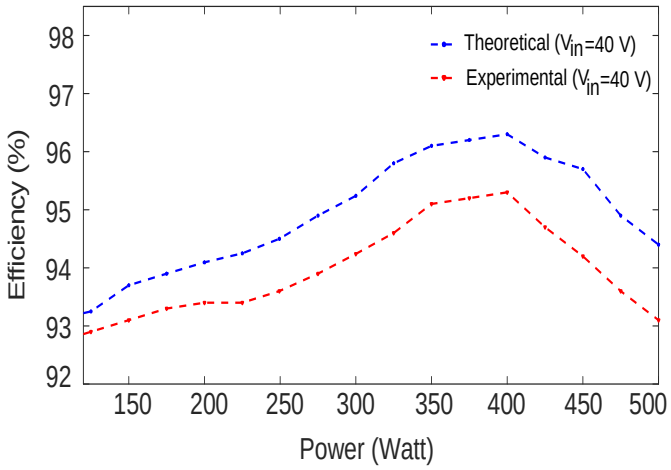

Figure 5.21: Comparison of theoretical and measured efficiency.

5.7 Conclusion

This chapter gives a solution to improving the limitations of the voltage gain of the ASL network by using a limited number of power devices for a high voltage conversion ratio. Based on the idea of the triple switch with ASL structure, a modification is made to achieve the new configuration of the converter. While analyzing the operation of the proposed converter, the output voltage is governed by the two duty cycles, which make the converter operate with a flexible range of duty cycles. The proposed converter achieves more than ten times gain at low-duty operation of the main switches.

Furthermore, the suggested converter provides high-quality input and output waveforms, immunity to EMI noise, flexibility in control, and control voltage. With these features, the proposed converter can be a potential candidate in the line of existing topologies.