Design and Performance Investigation of SiO_2/HfO_2 Gate Stacked Ge/Si Heterojunction TFET on SELBOX Substrate (GSHJ-STFET)

2.1 Introduction

Increased static power dissipation in integrated circuits (ICs) using sub-50 nm channel length MOS transistors is a serious concern due to short channel effects (SCEs) [8]-[13], [153]-[154]. To overcome the situation, TFET is projected as an alternate MOS transistor for low-power VLSI circuits owing to its inherently lower OFF-state current and smaller subthreshold swing (SS), which is below the minimum *SS* value of the Boltzmann limit of 60 mV/dec obtained in conventional MOSFETs [22]-[25] as previously discussed in Chapter 1. However, the major drawbacks of TFETs are their low ON-state current and ambipolar conduction [41]-[45]. There are several ways, which have been explored for improving the ON-state current of the TFETs such as gate engineering [74], work function engineering and gate dielectric engineering [64]-[66], negative capacitance engineering [36]-[37], [67]-[71], low band gap engineering [78]-[82], source/drain doping engineering [155]-[156], heterojunction source (drain)/channel engineering [79]-[81], substrate engineering [72]-[77] and *etc.* In this chapter, to increase the drive current and I_{ON}/I_{OFF} ratio of the device, I have used Si/Ge heterojunction (HJ) engineering and gate stacked (GS) SiO_2/HfO_2 oxide structure engineering [65]-[66]. The SOI substrate engineering is explored in TFETs for reducing the SCEs, improving vertical and lateral isolations to minimize the leakage current, and enhancing the speed of operation by reducing parasitic capacitances of the device [72]-[74]. However, SOI TFETs suffer from poor thermal insulation and high OFF-state current [70]-[72]. Barah *et al*. 2018, [76] have

reported a SELBOX structure in the SOI substrate to improve the thermal insulation and I_{ON}/I_{OFF} ratio in the conventional TFET. The SELBOX structure has been created by removing some selective portion of the buried oxide in the SOI TFET as shown in Figure 2.2 (b). The SELBOX structure also reduces the leakage current by trapping some electrons through the gap which is difficult to pull for the low drain field under the subthreshold regime of operation [72] [76]. Further, the floating body effect of conventional SOI TFET is eliminated in GSHJ-STFET structures [70]-[72].

Therefore in this chapter, to highlight the importance of SELBOX structure, we have used both Ge/Si heterojunction engineering at the source-channel junction and gate oxide engineering by replacing convention SiO_2 gate oxide with SiO_2/HfO_2 gate stacked (GS) and hence applied them to both FD-SOI and SELBOX structure. Further we have performed extensive electrostatic analysis of both the proposed novel TFET structures (i.e., GSHJ-FD-SOI TFET and GSHJ-STFET). Figures 2.1 (a), and (b) demonstrate the conventional fully depleted (FD) SOI TFET (FD-SOITFET) and TFET on the SELBOX substrate (STFET), respectively.

According to the discussion so far, the present chapter aims to investigate the DC and RF/analog performance analysis, the DC and RF/analog parameters are I_{ON} current, I_{OFF} current, I_{ON}/I_{OFF} ratio, subthreshold swing (SS), transconductance (g_m), parasitic capacitances (C_{gs}, C_{gd}, C_{gg}), cutoff frequency (f_t), gain-bandwidth product (GWB), transconductance generation factor (TGF), and transconductance frequency product (TFP) are investigated using TCAD simulations and compared between the GSHJ-FD-SOI TFET and GSHJ-STFET devices. At the end of this chapter, we evaluated the effects of temperature (250 K - 400 K) on some essential DC parameters of the studied TFET devices. The layout of the present Chapter is as follows:

Section 2.2 deals with the schematic structures and simulation methodologies of the proposed TFET using the SILVACO ATLAS^{TM} TCAD tool [157]. The possible fabrication steps to realize the proposed structure has been presented in Section 2.3. In Section 2.4, a device-level performance comparison has been made for GSHJ-FD-SOI TFET and GSHJ-STFET. Finally, Sec.2.5 includes the summary and conclusion of the present chapter.

2.2 TCAD Simulation Framework

The schematic structure of the proposed TFET and its various parameters used for the TCAD simulation studies are discussed. The possible fabrication feasibility of the proposed device structure is also discussed. Different models used in the TCAD simulation are briefly discussed in this section.

2.2.1 2-D Schematic Structures of the Proposed TFETs

Figure 2.1 (a) and Figure 2.1 (b) show the schematic view of GSHJ-FD-SOITFET and GSHJ-STFET, respectively. Aluminum (Al) has been considered in the whole thesis work as electrode material. Table 2.1 shows the device parameter values and symbols employed throughout the simulation analysis.

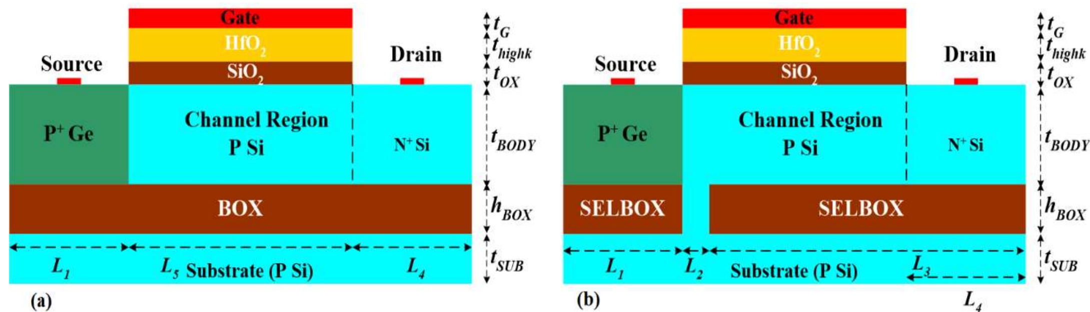

Figure 2.1: 2D cross-sectional view of (a) GSHJ-FD-SOITFET, and (b) GSHJ-STFET.

TABLE 2.1: Studied devices parameters.

Parameters	GSHJ-SOITFET	GSHJ-STFET
Source doping concentration (N_S)	1×10^{19} cm^{-3}	$1\times10^{19}cm^{-3}$
Channel doping concentration (N_{CH})	1×10^{16} cm^{-3}	1×10^{16} cm^{-3}
Drain doping concentration (N_D)	5×10^{18} cm^{-3}	5×10^{18} cm^{-3}
The thickness of the channel (t_{Si})	15 nm	15 nm
The thickness of SiO_2 gate oxide (t_{ox})	1 nm	1 nm
The thickness of High-k gate oxide (t_{ox})	2 nm	2 nm
Effective Oxide Thickness (t_{EOT})	1.312 nm	1.312 nm
SiO_2 gate dielectric permittivity (ε)	3.8	3.8
HfO_2 gate dielectric permittivity (ε)	25	25
Gate length (L_G)	40 nm	40 nm
Source length (L_S)	30 nm	30 nm
Drain length (L_D)	30 nm	30 nm
The thickness of buried oxide (BOX), (t_{BOX})	10 nm	10 nm
Length of SELBOX gap (L_{BOX})	2 nm	2 nm
Hole tunnel mass in silicon (m_{htSi})	$0.24m_o$	$0.24m_o$
Hole tunnel mass in germanium (m_{htGe})	$0.044m_o$	$0.044m_o$
Electron tunnel mass in silicon (m_{etSi})	$0.20m_o$	$0.20m_o$
Electron tunnel mass in germanium (m_{etGe})	0.082mo	0.044mo
Lattice constant of Ge	5.656 ^{0}A	5.656 ^{0}A
Lattice constant of Si	5.429 ^{0}A	5.429 ^{0}A
Bandgap energy Ge	0.70 eV	0.70 eV
Bandgap energy Si	1.12 eV	1.12 eV
Electron affinity Ge	4.01 eV	4.01 eV
Electron affinity Si	4.05 eV	4.05 eV

2.2.2 Possible Fabrication Steps

The fabrication process steps of the proposed device (GSHJ-STFET) are depicted in Figure 2.2, which is based on the approach given in ref. [109]. Starting with a p-type substrate, the SiO_2 layer can be grown via a thermal oxidation technique, as shown in Figure 2.2 (a). The SELBOX structure is then created by removing a portion of the SiO_2 layer near the source region (Figure 2.2 (b)). The source (Ge), channel (Si), and drain (Si) regions will next be formed on the SELBOX substrate using the molecular beam epitaxy (MBE) technique (Figure 2.2 c, and d). The SiO_2/HfO_2 stacked gate-oxide structure can be formed using the oxidation method by first growing SiO_2 and then deposition of HfO_2 into the channel region (Figure 2.2 (e). Finally, the electrode terminals for the source, gate, and drain can be made by depositing metals in the appropriate regions by using the vacuum evaporation method, as shown in Figure 2.2 (f).

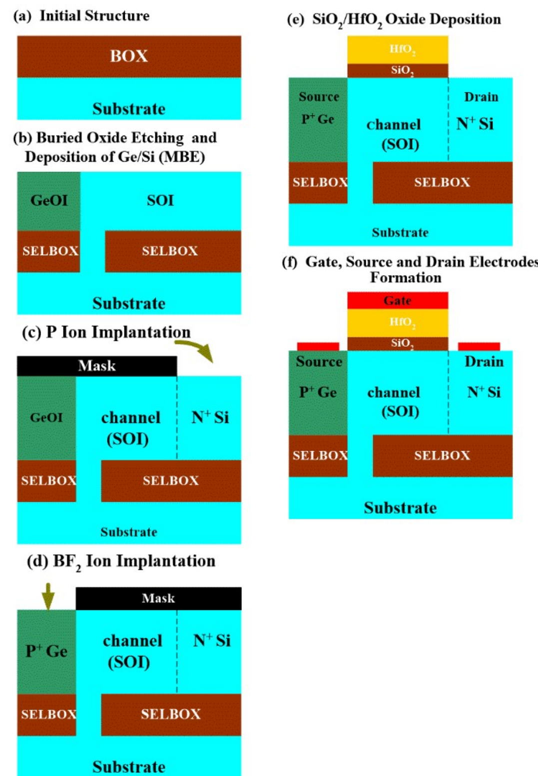

Figure 2.2: Possible fabrication steps for the proposed structure GSHJ-STFET [109].

2.3 TCAD Simulation Methodology and Description of Models

In this section, the objective of using various models for simulating the proposed TFETs using SILVACO ATLAS TCAD has been briefly discussed [157]. The non-local band-to-band tunneling model is mostly used where the tunneling process is needed with the utmost accuracy. The local band-to-band tunneling model based on Kane's work is used to calculate the generation and recombination rate at each point solely based on a constant local electric field in the tunneling path of the carriers. This does not consider the spatial variation in the energy band profile. On the other hand, the non-local band-to-band tunneling model (BBT.NONLOCAL) of the SILVACO ATLAS TCAD allows the modeling of the forward and reverse biased tunneling currents. In the non-local BTB tunneling model, tunneling is assumed to take place on a series of 1D slices through the tunneling junction. Here each of the slices is locally perpendicular to the junction and they are approximately parallel to each other. ATLAS has two methods of setting up these areas of slices. At the time of simulation of the proposed device structures, the tunneling area has been set up by specifying the number of tunneling slices and the number of mesh points along the slices using the QTX.MESH and QTY.MESH statements. In addition, the tunneling direction has been using QTUNN.DIR in the model statement. In the case of a highly doped tunneling junction, the BTB tunneling current can be very high depending on the energy band profile of the junction. This in turn creates a charge dipole and affects the potential to a greater extent. Consequently, the band energies at and near the junction get affected and this type of coupling may create convergence issues. This problem can be resolved using BBT.NLDERIVS in the model statement uses non-local coupling to resolve the convergence issues. Effective mass models (ME. TUNNEL and MH. TUNNEL) of the carriers have been used with the values of the effective masses of carriers listed in Table 2.1 [157]. Moreover, gate

material with higher work function (tungsten) has been considered in the control gate region (Region 1) and lower work function gate material (copper) in the screen gate region (Region 2). The graded channel can be fabricated using asymmetric halo-doping as used in (Pavanello *et al.*, 2001) Oxide thickness t_{ox} has been taken to be 2 nm. Due to very heavy doping in the source-drain region, depletion region extension in the source and drain region is negligible, hence being neglected in the model formulation (Najmzadeh *et al.*, 2012; Gupta, 2015). The numerical method "NEWTON" is used in the METHOD statements of the input file. The NEWTON method solves the total number of systems of unknowns together. It is believed to be a very effective method of strongly coupled system equations with quadratic convergence. Meshing plays an important role in the TCAD simulation of TFETs using the non-local BTB model. The various important regions like the electrodes, junctions, interface between semiconductor and oxide layer, etc. of the device must be accurately represented by the meshing. The finer the meshing, the more accurate the result. We have used fine rectangular meshing for the simulation of our proposed vertical TFETs to achieve optimum results.

2.3.1 Calibration of the Models

The TCAD tool has been first calibrated by comparing the simulation data with the experimental data for a known device structure [158]. We have considered the SOI TFET structure [158] for calibration purposes due to its closeness to the proposed structure. The experimental and TCAD simulation data for the transfer characteristic and output chararacteristics of the SOI TFET used for calibration is shown in Figure 2.3 for V_{DS} = 0.5 and 1.0 V (transfer characterisctics) and for V_{GS} = 1.5 V, 2 V and 2.5 V (output characterisctics). We find a reasonable matching but with a little difference between the experiment and TCAD results possibly due to the non-ideal factors of the experimental device.

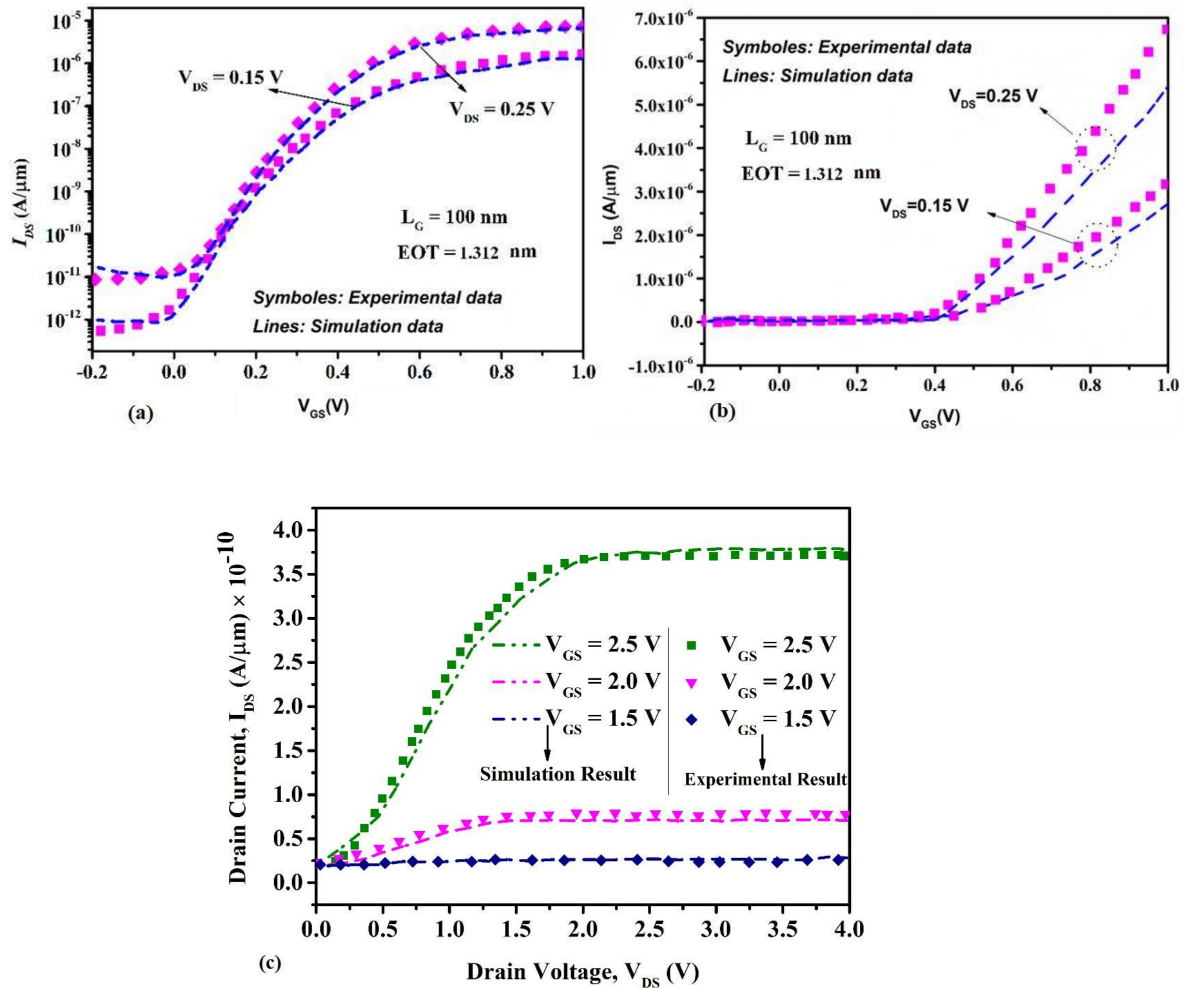

Fig. 2.3 Calibration of used model using SILVACO ATLAS™ TCAD tool: comparison of simulation data with experimental result of a SOI TFET (a) linear-linear scale, (b) log-linear scale, and (c) Simulated and measured output characteristics. Symbols indicate measured data and solid lines the corresponding simulation.

2.4 Results and Discussion

In this section, we have studied TCAD-based device-level performance analysis of GSHJ-STFET and GSHJ-FD SOITFET, respectively.

2.4.1 DC Performance Analysis

The TFET structure on the SELBOX substrate is optimized to achieve a lower OFF-state current and improved I_{ON}/I_{OFF} ratio. The optimization is carried out sequentially by varying different dimensional parameters, namely the position of the gap, the length of the SELBOX gap (W_{gap}), the thickness of the SELBOX gap (h_{BOX}), the thickness of the

silicon body (t_{Body}), and the channel length (L_{ch}) while keeping the drain terminal voltage, V_{DS} = 0.5 V throughout all simulations process. The optimized structure is compared with GSHJ-FD-SOITFETs by varying SELBOX gap length and position. There are different DC figure of merits (FOMs) that has been taken for the analysis in this section such as gate leakage current, drain current, I_{ON}, I_{OFF}, I_{ON}/I_{OFF} ratio, subthreshold swing (SS), threshold voltage (V_T), surface potential, transconductance (g_m), BTB tunneling rate, and absolute electric field.

To start our discussions, the advantage of vertical gate stacking in the proposed TFET has been presented in the beginning. The effective oxide thickness expression (EOT) (t_{EOT} = 1.312 nm) for vertical SiO_2/HfO_2 gate stacked is given as [66], [160],

$$t_{EOT} = t_{SiO_2} + t_{high-k}\frac{k_{SiO_2}}{k_{high-k}} \tag{2.1}$$

where t_{SiO2} is the SiO_2 oxide thickness, $t_{high\text{-}k}$ is the high-k oxide thickness, k_{SiO2} is the SiO_2 dielectric constant, and $k_{high\text{-}k}$ is the high-k (HfO_2) dielectric constant.

The gate leakage current plots for both vertical SiO_2/HfO_2 gate stacked and without gate stacked are shown in Figures 2.4 (a) and (b), respectively. Figures 2.4 (a) and (b) show that the proposed TFET has a significant reduction in gate leakage current due to the vertical SiO_2/HfO_2 gate stacking, this raises the gate oxide layer's physical thickness [66], [160]. As a result, the gate leakage current is reduced [161]. Figure 2.5 (a) shows the logarithmic drain current plots of GSHJ-STFET and GSHJ-FD SOITFET. The electrostatic performance of the GSHJ-STFET has been improved, including a reduction in OFF-state current, an increase in ON-state current, and a steeper subthreshold slope. Figure 2.5 (b) shows the energy band diagram of the proposed GSHJ-STFET for both ON and OFF-state conditions. Misalignment of the source's valence band and the channel's

conduction band during the OFF-state (zero gate bias) prevents electrons from tunneling through the source-channel junction. Due to considerable band bending with the application of positive gate bias in the ON-state, the electron-occupied valence band of the source aligns with the empty states of the channel's conduction band. This causes electrons to tunnel from the source's valence band to the channel's conduction band [41]-[45].

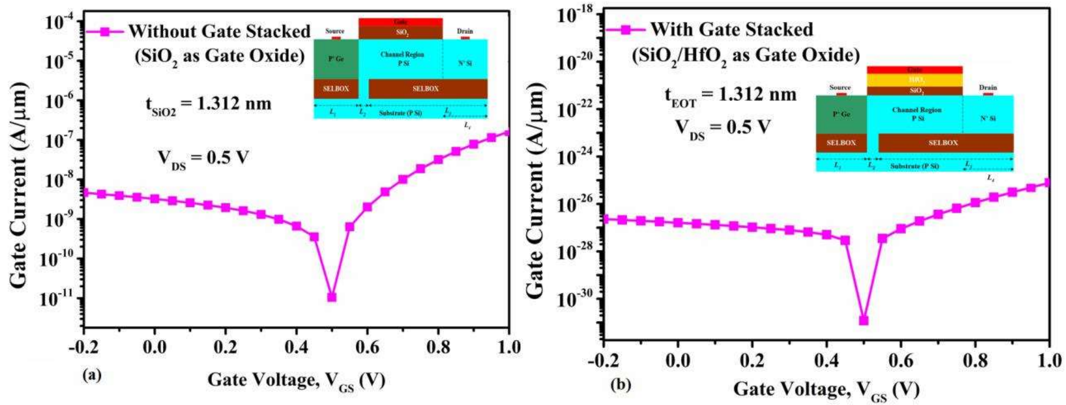

Figure 2.4 Plots of gate leakage current for (a) without gate stacked i.e., SiO_2 as the gate oxide, and (b) with gate stacked i.e., SiO_2/HfO_2 as gate oxide of the HJ-STFET at t_{EOT} = 1.312 nm.

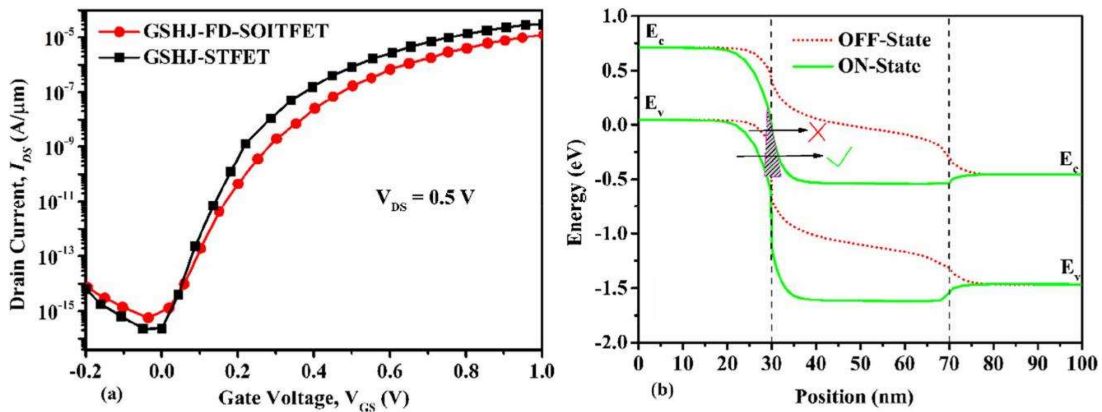

Figure 2.5 Plots of (a) I-V characteristics of both the presented TFETs and (b) energy band diagram for on and off state of the GSHJ-STFET.

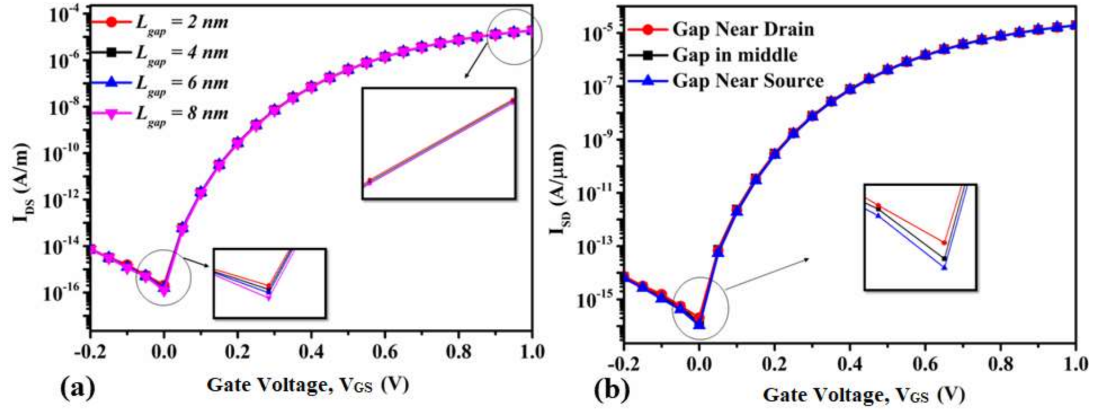

Figure 2.6 Plots of (a) drain current for different values of SELBOX gap length and (b) drain current with the different positions of SELBOX gap of GSHJ-STFET.

Figure 2.6 (a) shows the logarithmic drain current graphs of Ge/Si heterojunction TFETs on SELBOX substrate (HJ-STFET) for different SELBOX gap length values. The optimized SELBOX gap length value is considered to be 2 nm by considering both ON and OFF-state current. The main reason to consider 2 nm as optimized SELBOX length is to retain the properties of both SOI and SELBOX structures. Figure 2.6 (b) shows the logarithmic drain current plots of GSHJ-STFET for the different positions of the SELBOX gap. On the side of the source region, as demonstrated in Figure. 2.6 (b), the SELBOX gap position is more responsible for reducing leakage current than the drain region and the middle of the channel region.

Figures 2.7 (a) and (b) show the contour plots of the non-local BTB e-tunneling rate of GSHJ-FD-SOITFET, and GSHJ-STFET respectively. The non-local BTBT of GSHJ-STFET is higher than GSHJ-FD-SOITFET at the source-channel junction as shown in Figures 2.7. A higher conduction current and a steeper subthreshold slope are caused by a higher BTBT rate [44]. Figures 2.8 shows the plots of absolute electric field of the proposed TFET structure for different SELBOX gap length. At the source-channel junction, the absolute electric field of the GSHJ-STFET is larger for the gap length of 2

nm as shown in zoomed subfigure 2.8. Figure 2.9 shows the plots of surface potential of the proposed TFET structure for different SELBOX gap length, in the source region surface potential is zero and it increases from junction and become saturated in the channel region, the zoomed diagram of surface potential shown in the same Figure 2.9, where FD-SOISTFET shows higher surface potential because of inversion layer already forms in the channel due to the “drain” in your FD-SOITFET device.

Figure 2.10 (a) shows the drain current vs. drain voltage plots for both studied TFETs, with the recommended TFET (GSHJ-STFET) having a higher drain current than the GSHJ-FD-SOITFET. Figure 2.10 (b) shows the output transconductance plots for both TFETs, with GSHJ-STFET providing higher output transconductance than SOITFET's output transconductance. Table 2.2 includes some DC parameter values from both investigations TFETs and previous work for comparison.

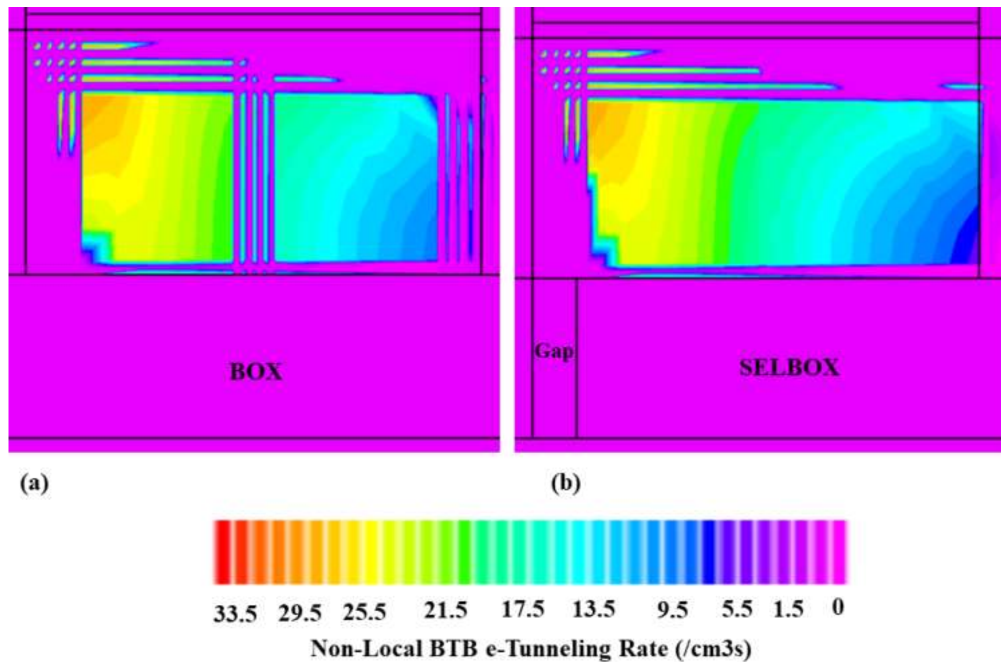

Figure 2.7 Contour plots of non-local BTB e- tunneling rate of (a) GSHJ-FD-SOITFET, (b) GSHJ-STFET $V_{DS} = 0.5$ V.

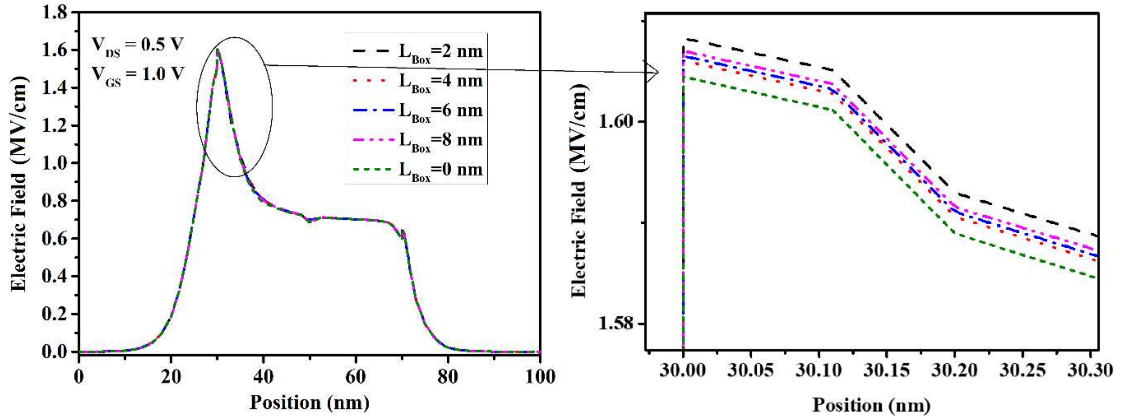

Figure 2.8 Plots of absolute electric field of proposed TFETs structures for SELBOX gap length at V_{DS} = 0.5.

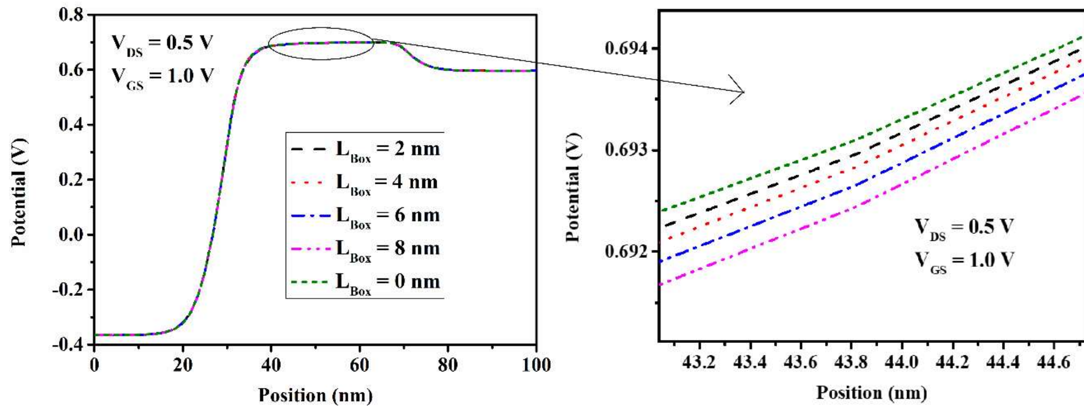

Figure 2.9 Plots of surface potential of proposed TFETs structures for SELBOX gap length at V_{DS} = 0.5 V.

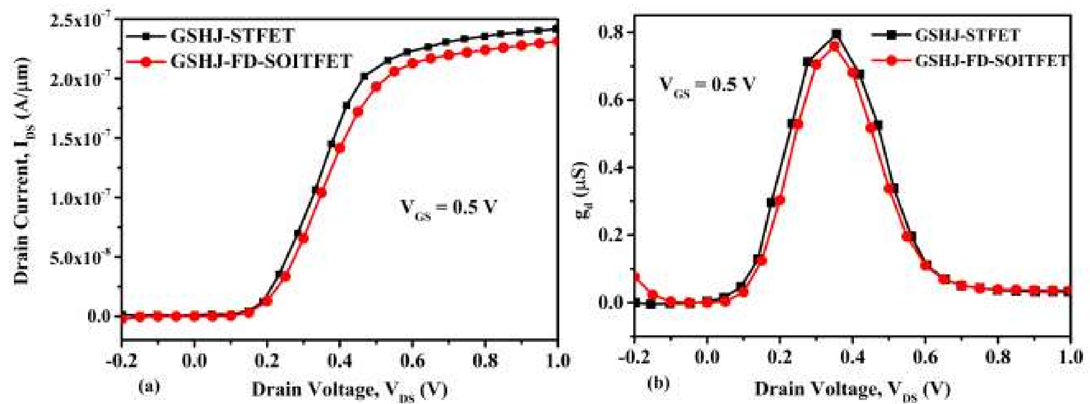

Figure 2.10 (a) Drain current versus and (b) output transconductance plots of both GSHJ-FD-SOITFET, and GSHJ-STFET at V_{DS} = 0.5 V.

TABLE 2.2 Values of DC parameters of the studied TFETs structures.

Parameters	GSHJ-FD-SOITFET	GSHJ-STFET	GU-ED TFET Structure [160]
V_T(V)	0.418	0.434	0.9
Avg.(SS, mV/dec)	41.5	38.1	49.6
I_{ON} (A/µm)	9.2x10^{-6}	1.2x10^{-5}	2.21x10^{-7}
I_{OFF} (A/µm)	1.22x10^{-15}	1.254x10^{-16}	1.6 x10^{-15}
I_{ON}/I_{OFF}	7.54x10^{9}	9.566x10^{10}	1.381x10^{8}

2.4.2 RF/Analog Performance Analysis

In the design of RF applications, the parameters f_T (cut-off frequency) and GWB (gain-bandwidth product) are primary figures of merits (FOMs). Figure 2.11shows the plots of the transconductance of both studied TFETs, in which the suggested TFET has higher transconductance all over the range of gate voltage because of a higher ON-state current. Figure 2.12 illustrates the parasitic capacitance of the studied TFETs, the parasitic capacitances are, the gate to source capacitance (C_{gs}), gate to drain capacitance (C_{gd}), and total gate capacitance (C_{gg}), where $C_{gg} = C_{gs} + C_{gd}$ [162]. The parasitic capacitances of the proposed TFET for different gap lengths such as (0 to 8 nm), and we can see that as the gap length increases, the capacitances decrease, as shown in Figure 2.12. Higher intrinsic hampers the circuit-level performance as it increases the propagation delays [162]. The f_T is the frequency at which the device's circuit current gain falls to unity, which is determined by the g_m/total capacitance ratio. f_T is expressed by Eqn: 2.2 in the case of conventional MOSFETs [72], [74]- [67].

$$f_T = \frac{g_m}{2\pi C_{gg}} \tag{2.2}$$

where g_m represents transconductance and C_{gg} represents total gate capacitance.

Figure 2.13 shows the plots of cut-off frequency for different gap lengths such as (0 to 8 nm), and we can see that as the gap length increases, the cut-off frequency decreases. As

a result, in order to maintain both the bulk and SOI natures of my device, I considered a gap length of 2 nm.

Figure 2.14 shows the plots of f_T (cut-off frequency) vs. gate voltage. Gain bandwidth product is another critical RF parameter (GWB) as shown in Figure 2.14 (b). For TFETs, GWB is written as [74]-[76]:

$$GWB = \frac{g_m}{2\pi C_{gd}} \tag{2.3}$$

where C_{gd} is the gate to drain capacitance.

Figure 2.14 (b) depicts the GWB of both studied TFETs and GSHJ-STFET has better GWB as compared to GSHJ-FD-SOITFET. Again, the higher value of f_T and GWB is because of higher transconductance in the proposed structure [75].

The transit time (τ) of the device is calculated using the expression [76],

$$\tau = \frac{1}{2\pi 10 f_T} \tag{2.4}$$

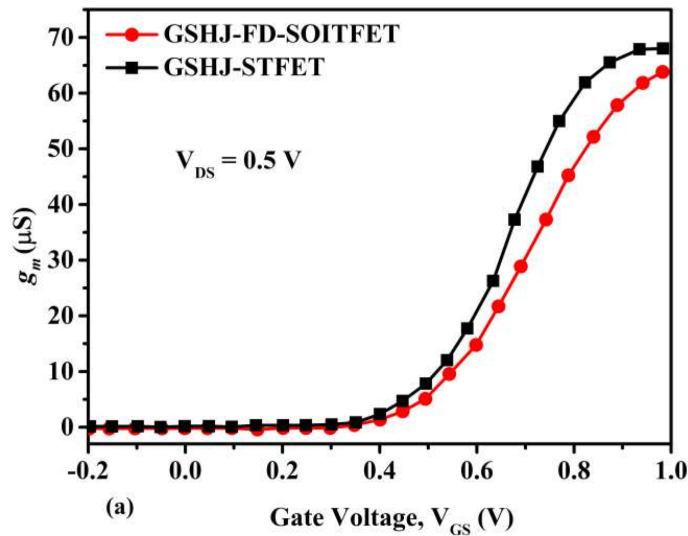

Figure 2.11 Transconductance plots of both GSHJ-FD-SOITFET, and GSHJ-STFET.

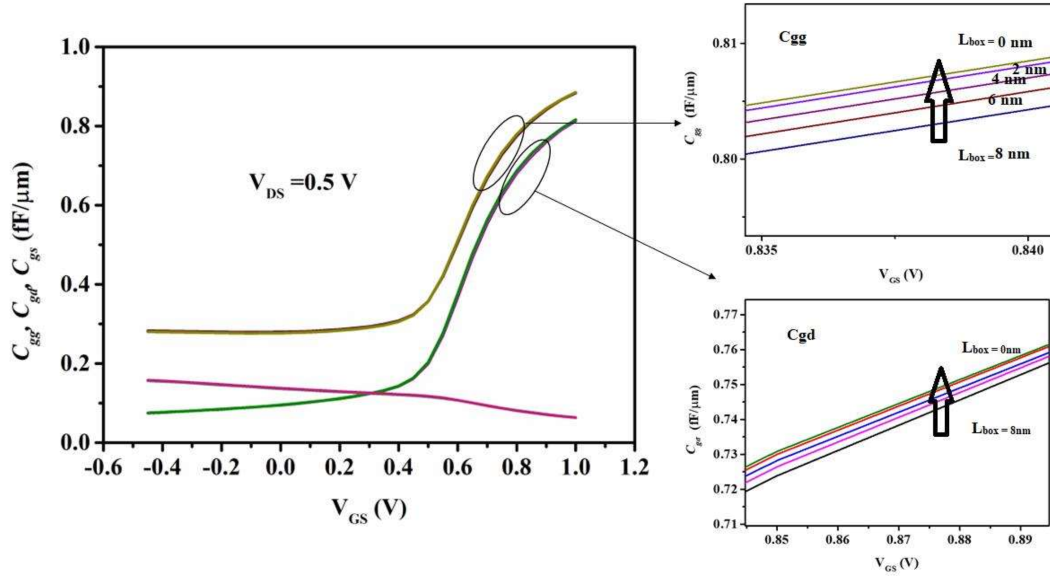

Figure 2.12 Plots of Cgg, Cgd and Cgs for SELBOX gap length of the proposed TFET.

Figure 2.15 (a) depicts transit time plots for both studied TFETs, demonstrating that the GSHJ-STFET has a lower value of transit time than the GSHJ-FD-SOITFET across the entire V_{GS} range. Figure 2.15 (b) depicts the comparative TGF variation vs. V_{GS}. GSHJ-STFET exhibits higher TGF at lower V_{GS} than GSHJ-FD-SOITFET, according to the findings. Because the variance in I_{DS} is modest, TGF begins to diminish when the gate voltage reaches more beyond 0.2 V. The TGF can be made in the following way [163]:

$$TGF = \frac{g_m}{I_{DS}} \tag{2.5}$$

The comparative variation of TFP with V_{GS} at V_{DS} = 0.5 V is shown in Figure 2.16 (a). The results show that GSHJ-STFET has a higher TFP due to the high value of g_m and f_T. The TFP is obtained in the following manner [164]:

$$TFP = \frac{g_m}{I_{DS}} f_T \tag{2.6}$$

The maximum oscillation frequency (f_{MAX}) is described as the frequency at which unilateral power gain is equal to one. The expression of f_{MAX} is given below [163] [164]:

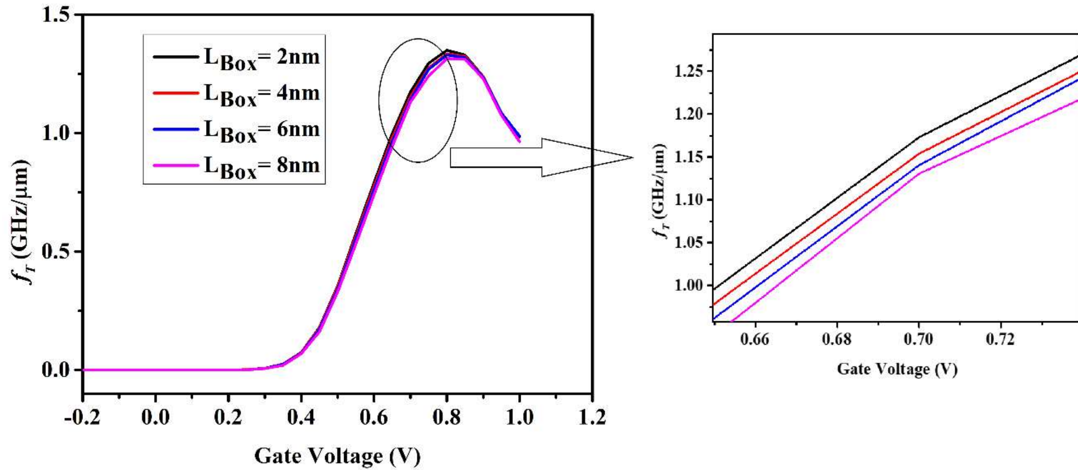

Figure 2.13 Plots of cut-off frequency SELBOX gap length of the proposed TFET.

$$f_{MAX} = f_o\sqrt{\frac{|Y_{21}-Y_{12}|^2}{4[Re(Y_{11})Re(Y_{22})-Re(Y_{12})Re(Y_{21})]}} \quad (2.7)$$

where $Y_{i,\,j}$ (i, j = 1, 2) are the device's Y-parameters at applied frequency f_0, which is assumed to be 1 MHz for all Y parameter extraction from Eqn: (2.7).

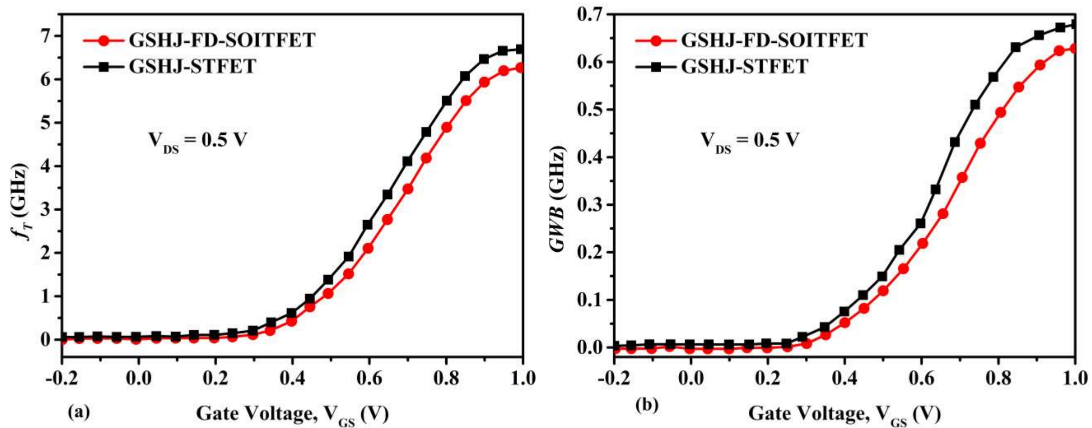

Figure 2.14 (a) Cut-off frequency and (b) GWB plot of both GSHJ-FD-SOITFET, and GSHJ-STFET.

Figure 2.16 (b) shows that f_{MAX} follows the same trend as that of f_T. The f_{MAX} of the GS-HJ-STFET is ~37 GHz that is 1.26 times higher than that of the GSHJ-FD-SOITFET.

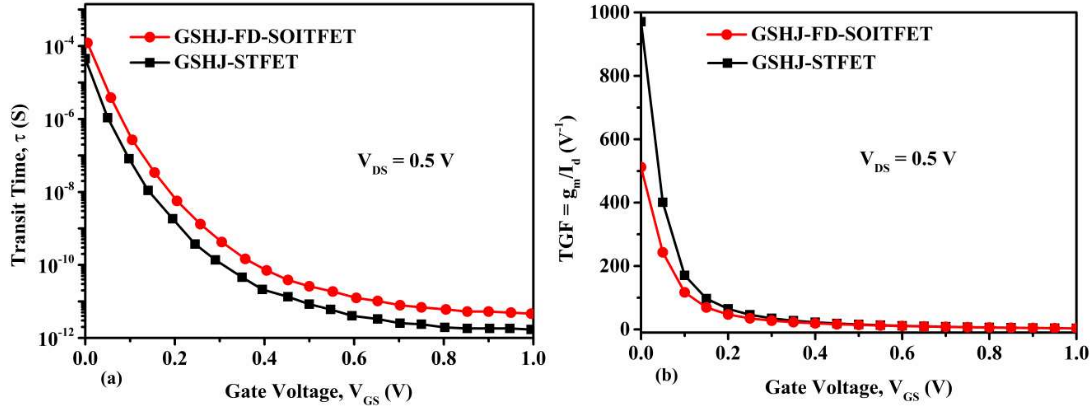

Figure 2.15 (a) Transit time plots and, (b) TGF plots of both GSHJ-FD-SOITFET, and GSHJ-STFET.

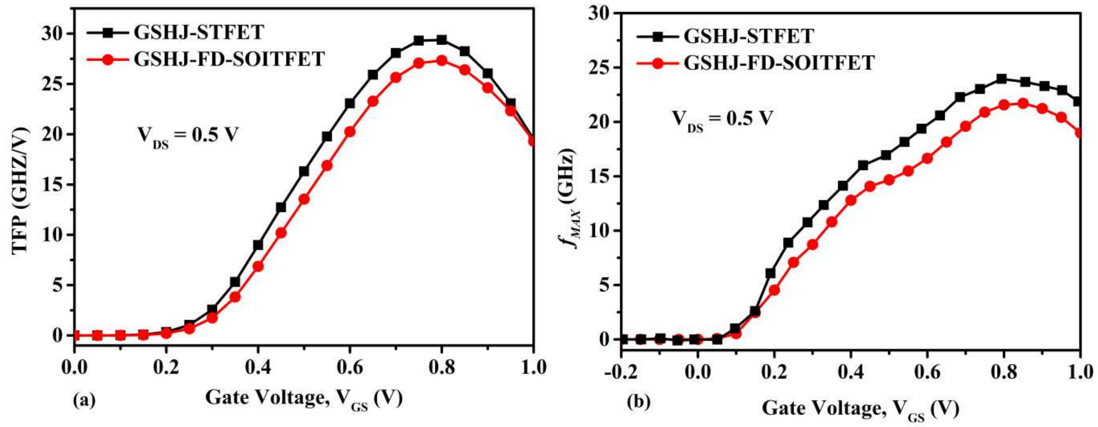

Figure 2.16 (a) TFP plots and, (b) maximum oscillation frequency plots of both GSHJ-FD-SOITFET, and GSHJ-STFET.

2.4.3 Temperature Impact Analysis

This section investigates the effect of temperature variation on various electrical parameters such as drain current, I_{ON}/I_{OFF} ratio, *SS*, and device threshold voltage. The energy bandgap (E_g) is a parameter that mainly depends upon the temperature (T), the relationship between E_g and temperature is given by Eqn: 2.8 [165]-[166].

$$E_g(T) = E_g(0) - \frac{\gamma T^2}{T + \beta} \tag{2.8}$$

TABLE 2.3 – Comparison of RF/analog parameters of all given structures.

Parameters	GSHJ-FD-SOITFET	GSHJ-STFET	Ref. [163]
f_T (GHz)	5.8	6	3
GWB (GHz)	0.63	0.65	0.60
τ (sec)	$8.243\text{x}10^{-6}$	$8.042\text{x}10^{-6}$	$8.045\text{x}10^{-6}$
TFP (GHz/V)	27.00	30.00	28.00
TGF (V^{-1})	21.00	37.00	23.00
f_{MAX} (GHz)	21.05	26.10	34.00

For a germanium semiconductor, γ and β are two fitting parameters, and $E_g(0)$ is the energy band gap at 0 K. γ = 4.77x10^4 eV/K and β = 235 K. According to the WKB approximation, the tunneling current is exponentially proportional to the bandgap, and when the bandgap lowers, the current increases [44], as shown by Eqn: (2.9).

$$I \propto T(E) \approx \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3|e|\hbar(E_g + \Delta\Phi)} \sqrt{\frac{\varepsilon_s}{\varepsilon_{ox}} t_{ox} t_s} \right) \Delta\Phi \tag{2.9}$$

where e is the single-electron charge, m^* is the charge carrier effective mass, E_g is the tunneling junction gap, ε_{si} is the semiconductor's dielectric constant, ε_{ox} gate oxide dielectric constant, t_{si} channel thickness, t_{ox} oxide thickness, ħ is modified Plank's constant and ΔΦ is the tunneling energy range. According to Eqn: 2.9, decreasing the bandgap and raising the gate dielectric constant will increase the chance of tunneling and hence the ON-state current.

The temperature dependency of the energy bandgap of Ge is expected to affect the tunneling current and other electrical characteristics of the TFET device under examination because tunneling is predominantly limited to Ge source material. Because the energy bandgap is temperature-dependent, and the drain current is temperature-dependent, Eqns. (2.8) and (2.9) demonstrate that the drain current should be temperature-dependent as well. Furthermore, as the temperature rises, the energy bandgap becomes

narrower and the drain current (I_{DS}) increases [166].

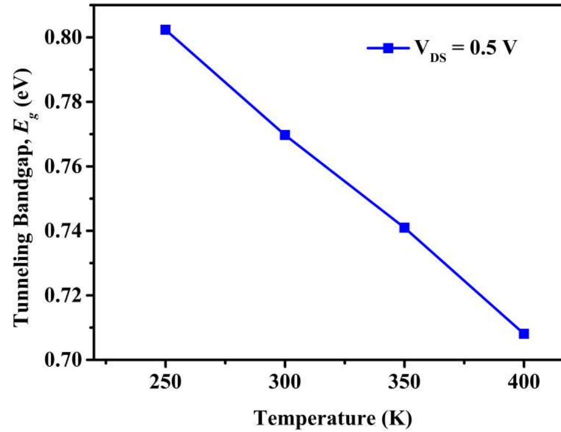

Figure 2.17 Variation of tunneling bandgap vs. temperatures at a drain voltage of 0.5 V.

Figure 2.17 shows the temperature variation of the tunneling bandgap for different drain voltages. Here the source is germanium so the tunneling bandgap is lower than silicon. According to equation (8) and in Figure 2.17, we found that the tunneling band gap is almost independent of drain voltage. In Figures 2.18 (a) & (b), we can see that with an increase in temperature the OFF-state current also increases largely but there is not much variation in ON-current [164]-[165]. The temperature variation is made from 250K to 400K, where we can reveal that the OFF-state current of our proposed device at higher temperature is not crossing the ITRS limit which is said to be 10^{-10} A/µm. That concludes the use of the proposed TFET at very high temperatures without getting much degradation in performance [165]. Figure 2.19 (a) depicts the plots of I_{ON}/I_{OFF} ratio vs. temperature, where, the I_{ON}/I_{OFF} ratio is reduced with temperature. Proposed TFET (GSHJ-STFET) has a higher I_{ON}/I_{OFF} ratio over the taken temperature range (250K-400K). The value of the threshold decreases as the temperature rises, as seen in Figure 2.19 (b) [164]. This is because more no of carriers is getting generated with an increase in temperature. Due to this phenomenon, the device is switched ON earlier which in turn decreases threshold voltage [164]-[165].

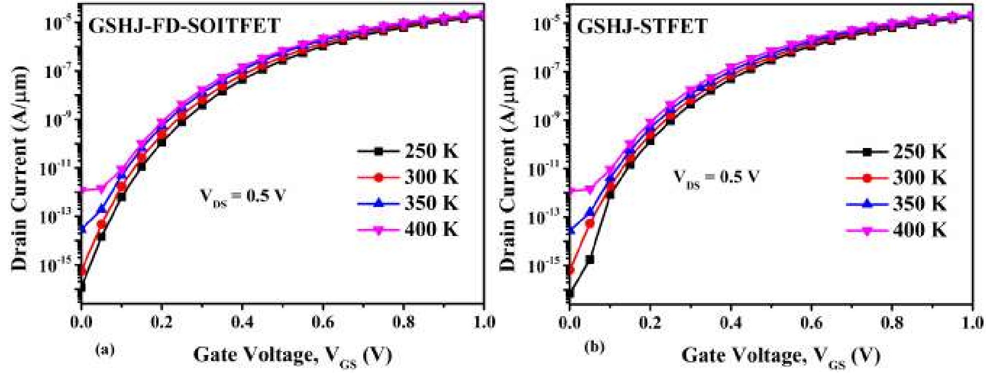

Figure 2.18 Drain current plots at different temperatures of (a) GSHJ-FD-SOITFET, and (b) GSHJ-STFET.

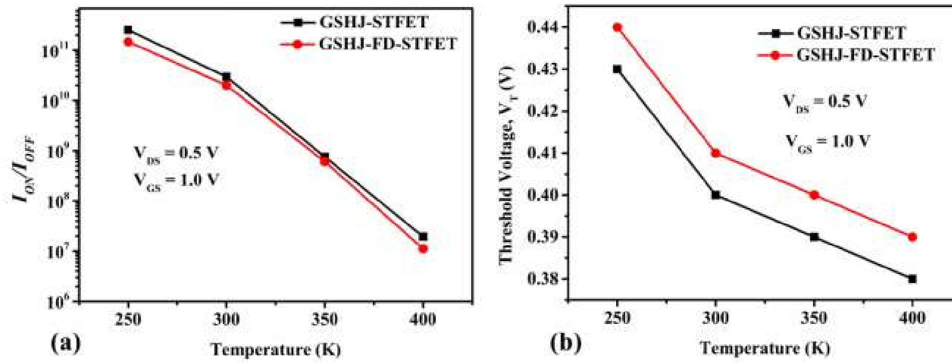

Figure 2.19 Plots of (a) I_{ON}/I_{OFF} ratio vs. temperature and, (b) threshold voltage vs. temperature of GSHJ-FD-SOITFET, and GSHJ-STFET.

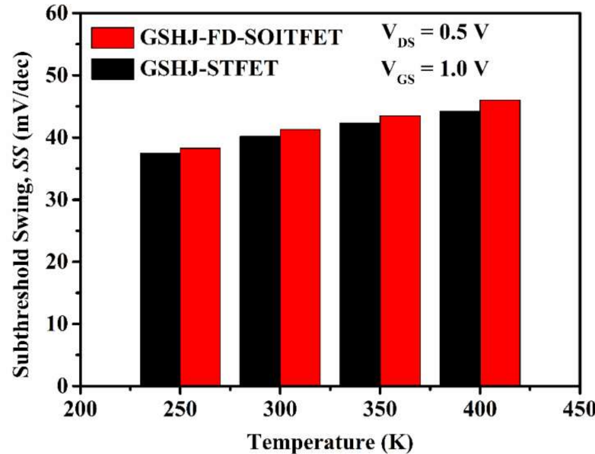

Figure 2.20 Subthreshold swing (SS) plots of GSHJSTFET and GSHJ-FD-SOITFET at various temperatures.

Figure 2.19 (b) shows that the threshold voltage of the GSHJ-STFET is lower than that of the GSHJ-FD-SOITFET, over the studied temperature range. Figure 2.20 depicts a bar

graph of subthreshold swing (SS), in which GSHJ-STFET has a smaller *SS* than GSHJ-FD-SOITFET over the temperature range 250K-400K. The subthreshold swing (SS) value increases with temperature [166] as shown in Figure 2.20.

2.5 Conclusions

This chapter investigates the DC and Analog/RF performance of a newly suggested GSHJ-STFET-based TFET structure with stacked HfO_2/SiO_2 gate and Ge (source)/Si (channel) heterojunction. The rapid rate of BTB tunneling of carriers from the source to the channel region is due to the presence of germanium (a low bandgap material) in the source region. It has been shown that the SELBOX structure demonstrates the advantages over SOI and bulk structures. So, it can be considered a good option when selecting between SOI and bulk structures. This is mainly due to the gap present in the buried oxide in the SELBOX structure. Vertical gate stacked SiO_2/HfO_2 is highly responsible for the reduction of the gate leakage current due to the higher physical thickness of the gate oxide layer. The proposed TFET structure with SELBOX improves both DC and RF characteristics. The ATLAS™ TCAD tool which is commercially available has been utilized to simulate the devices throughout a temperature range of 250 K to 400 K. The influence of temperature on the suggested GSHJ-STFET structure's performance is shown to be minimal over the GSHJ-FD-SOITFET structure.