# Chapter 5

# Grid Integration of Transformerless Interleaved Hybrid Converter with Reduced Leakage Current

## 5.1 Introduction

Chapters 2, 3 and 4 present the operations of different types of transformerless boost derived hybrid converter topologies for PV applications. In chapter 2, a transformerless minimum phase hybrid converter (TLMPHC) has been proposed to operate in stand-alone mode. Similarly, a transformerless interleaved hybrid converter (TLIHC) has been proposed and its steady-state performance is discussed in chapter 3. In chapter 4, the controller behaviour and dynamic performance of TLIHC is presented. All these PV based hybrid converters work in stand-alone/off-grid mode. The PV based hybrid converters (and inverters) generally operate in either stand-alone/off-grid mode or grid tide/grid integration mode. The grid tied mode operation of TLIHC is presented in this chapter. The detailed analysis of grid side filter inductors ($L_{g1}$ and $L_{g2}$), phase-locked loop (PLL) design and fast Fourier transform (FFT) analysis of grid current ($I_g$) of the proposed TLIHC are discussed in this chapter. Also, the closed loop control strategy of $I_g$ is discussed in this chapter. As, the DC part of the proposed TLIHC is derived from a conventional boost converter, the performance of TLIHC is studied for varying $I_g$ and duty ratio ($D$). Simulation results for the performance verifications of the grid integrated proposed TLIHC is also presented in this chapter.

## 5.2 Grid Integration of TLIHC

The grid integrated circuit diagram of the proposed TLIHC is shown in Fig. 5.1. From the grid integrated circuit, it can be observed that an LCL filter is used in the grid side of TLIHC. Among the two pairs of filter inductors of the LCL filter, one pair is connected to the inverter side and the other pair is connected to the grid side. Both in stand-alone mode and grid tied mode, the operating states of the proposed TLIHC are same. Also, the charging and discharging behaviour of all the passive components are same for both the operating conditions.

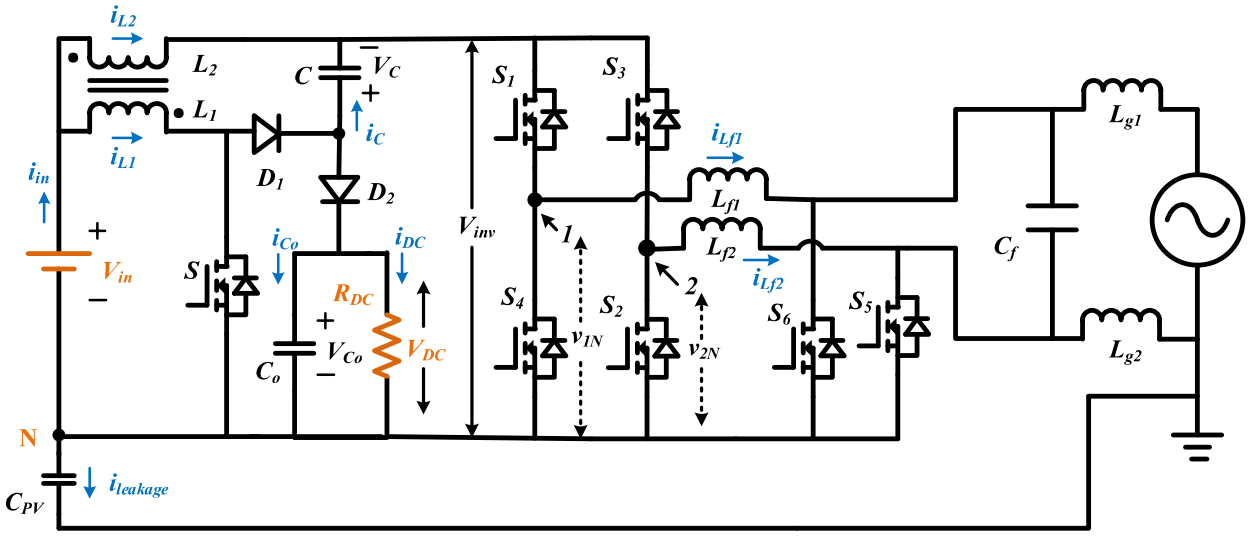



**Fig. 5.1** Circuit diagram of the proposed TLIHC in grid tied mode.

The grid connection of the proposed TLIHC allows injection of the current into the grid to leverage the monetary benefits of the solar energy obtained from the PV panel. For the proper operation of the TLIHC during the grid integration, the injected current should have lower total harmonic distortion (THD), within the specified limits of IEEE standards [101]. Since the grid is connected to the ground and there is no low frequency transformer in between the PV panel and the grid, the common mode leakage current ($I_{leakage}$) flows through the system due to the presence of stray capacitance ($C_{pv}$). The grid integration in case of the TLIHC helps in transfer of surplus amount of active power from the PV panel to the grid. Therefore, the injected $I_g$ is in the same phase with the grid voltage ($V_g$) in this case.

In the previous chapters, the proposed TLIHC has been operated in standalone mode. For the grid connected mode, the frequency of the output voltage of TLIHC is required to be synchronized with the grid frequency using a PLL. Therefore, close tracking of the grid frequency is essentially required in this case [104]. Normally, the grid frequency varies with the load variations. So, any mismatch in frequency may lead to generation of unwanted circulating currents resulting into damage of power electronic devices used in TLIHC. Also, during the grid integration of TLIHC, the grid acts as a sink for all the harmonic components (except fundamental component) present in the output voltage.

Fig. 5.2 shows the circuit diagram of inverter output voltage ($V_{o/p}$) of the TLIHC along with the grid voltage. It is observed that in between the inverter output and grid an inductor ($L_g$) is present.

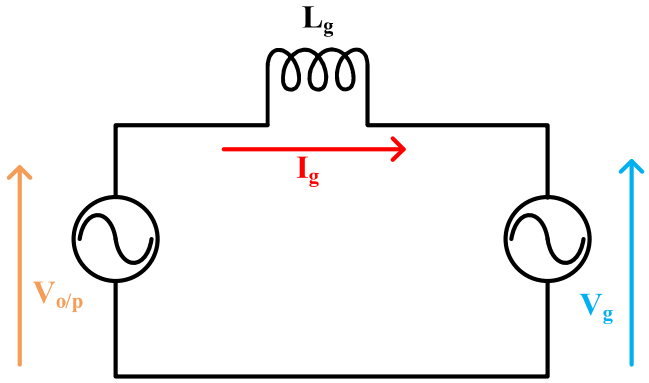



**Fig. 5.2** Circuit diagram of inverter output voltage of TLIHC along with the grid voltage.

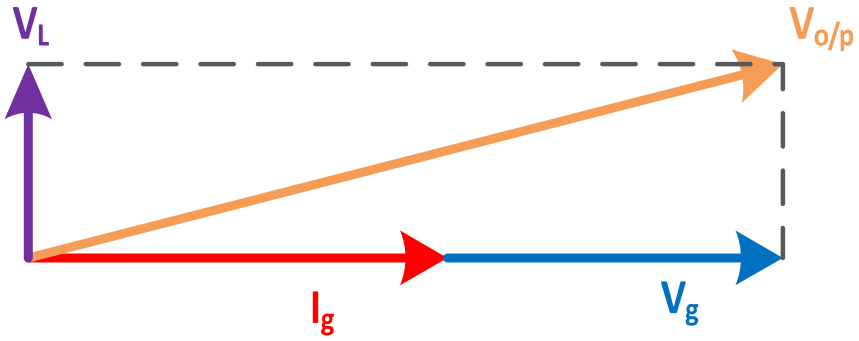



**Fig. 5.3** Phasor diagram of inverter side output of TLIHC along with the grid.

Applying KVL in Fig. 5.2

$$I_g = \frac{V_{o/p} - V_g}{Z_g} \tag{5.1}$$

where $V_{o/p}$= inverter output voltage, $Z_g = 2\pi f L_g$ and $f$ = grid frequency

The voltage across the grid side inductor ($V_L$) is

$$V_L = V_{o/p} - V_g \tag{5.2}$$

As, the value of grid side filter inductance is small, the voltage across it is less. Hence, the value of $V_g$ is close to $V_{o/p}$. Fig. 5.3 shows the phasor diagram of the inverter side output voltage of the

TLIHC along with the grid voltage. From the figure, it can be observed that the phase difference between $V_{o/p}$ and $V_g$ is small as the value of $V_L$ is very small as compared to $V_g$.

## 5.3 Closed Loop Control Strategy for Grid Current

For the grid integration, synchronous reference frame control strategy is used. During the grid integration, the inverter output voltage is more than $V_g$. So, depending upon the amount of active power transfer to the grid the value of $I_g$ is dependent. Synchronous reference frame control strategy is used to control the value of $I_g$. Fig. 5.4 shows the proposed TLIHC referred to the grid side. From the figure, it can be observed that the inverter side inductance is $L_f$ and grid side inductance is $L_g$. For synchronous reference control strategy, the total inductance referred to grid side is $L_s = L_f + L_g$. The equivalent circuit referred to the grid side is shown in Fig. 5.5 and the current flowing through the inductor is $I_s$.

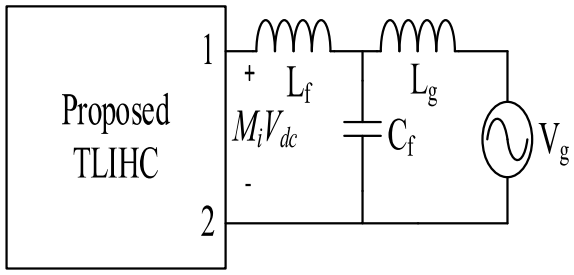



**Fig. 5.4** Proposed TLIHC referred to grid.

Applying KVL in Fig. 5.5

$$M_i V_{dc} = L_s \frac{di_s}{dt} + r i_s + V_g \tag{5.3}$$

$$\frac{di_s}{dt} = -\frac{r}{L_s} i_s - \frac{V_g}{L_s} + \frac{M_i}{L_s} V_{dc} \tag{5.4}$$

The expression given in (5.4) can be written in $\alpha\beta$ matrix form as follows:

$$\frac{d}{dt}\begin{bmatrix} i_{s\alpha} \\ i_{s\beta} \end{bmatrix} = -\frac{r}{L_s}\begin{bmatrix} i_{s\alpha} \\ i_{s\beta} \end{bmatrix} - \frac{1}{L_s}\begin{bmatrix} V_{g\alpha} \\ V_{g\beta} \end{bmatrix} + \frac{V_{dc}}{L_s}\begin{bmatrix} M_{i\alpha} \\ M_{i\beta} \end{bmatrix} \tag{5.5}$$

After applying $\alpha\beta - dq$ transformation, (5.5) can be written as

$$\frac{d}{dt}[T]^{-1}\begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} = -\frac{r}{L_s}[T]^{-1}\begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} - \frac{1}{L_s}[T]^{-1}\begin{bmatrix} V_{gd} \\ V_{gq} \end{bmatrix} + \frac{V_{dc}}{L_s}[T]^{-1}\begin{bmatrix} M_{id} \\ M_{iq} \end{bmatrix} \tag{5.6}$$

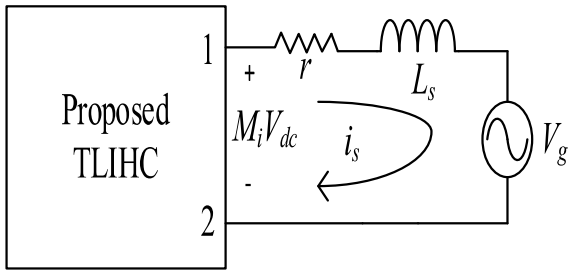



**Fig. 5.5** Equivalent circuit referred to grid side.

Differentiating the left-hand side of (5.6), the simplified expression is written as

$$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}\frac{d}{dt}\begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} = \begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix}\begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} - \frac{r}{L_s}\begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} - \frac{1}{L_s}\begin{bmatrix} V_{gd} \\ V_{gq} \end{bmatrix} + \frac{V_{dc}}{L_s}\begin{bmatrix} M_{id} \\ M_{iq} \end{bmatrix} \tag{5.7}$$

Taking Laplace transform of (5.7)

$$sI_{sd}(s) = \omega I_{sq}(s) - \frac{r}{L_s}I_{sd}(s) - \frac{V_{gd}}{L_s} + M_d\frac{V_{dc}}{L_s} \tag{5.8}$$

$$sI_{sq}(s) = -\omega I_{sd}(s) - \frac{r}{L_s}I_{sq}(s) - \frac{V_{gq}}{L_s} + M_q\frac{V_{dc}}{L_s} \tag{5.9}$$

The expressions given in (5.8) and (5.9) represent the mathematical model of grid side of the proposed TLIHC. Fig 5.6 shows the signal flow graph of the mathematical model of the grid side current controller of the proposed TLIHC. A proportional integral (PI) controller is used in the current control loop to control the value of $I_g$.

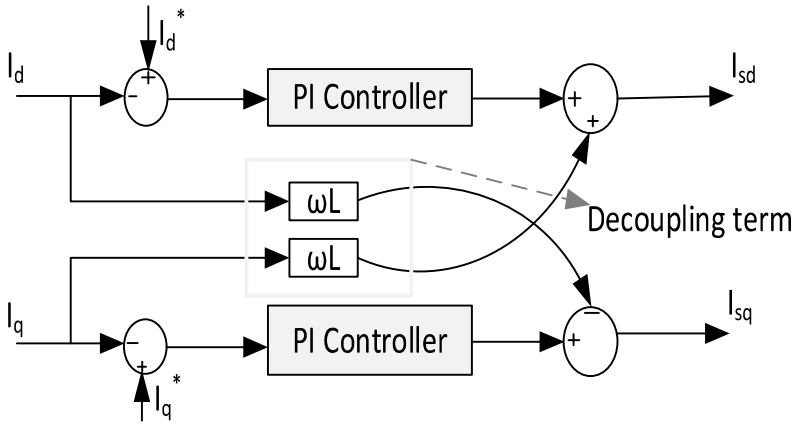



**Fig. 5.6** Signal flow graph of Current controller model of grid side.

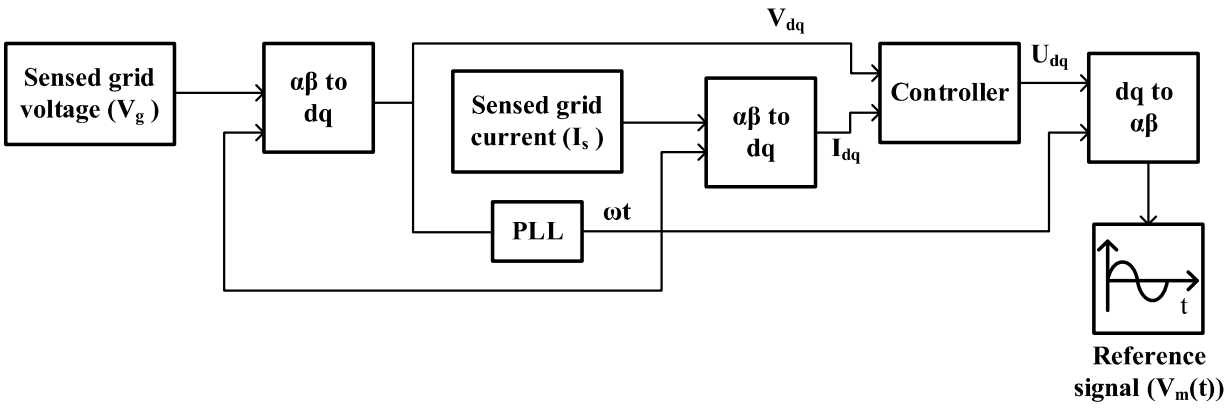



**Fig. 5.7** Schematic of overall control structure of grid integrated TLIHC.

The schematic of the overall control structure of grid integrated TLIHC is shown in Fig. 5.7, where two $\alpha\beta - dq$ and one $dq - \alpha\beta$ transformation matrices are used. The $\alpha\beta - dq$ transformation matrix is used to convert the sensed time-variant $V_g$ and $I_s$ into their time-invariant synchronous reference frame quantities. The $dq - \alpha\beta$ transformation matrix is used to convert the controlled time-invariant form of reference signal $V_m(t)$ into its time variant form. The PLL is used to track the grid frequency.

## 5.4 Phase Locked Loop (PLL)

In this work, PLL is used to control the variation in frequency and phase of the grid voltage. A PLL is a vital control loop in grid connected systems. The PLL is required to synchronize the inverter to the grid and to keep it locked to the grid frequency. As, in the grid connected mode, the inverter output of the proposed TLIHC is synchronized with the single-phase grid, the grid frequency tracking is the main objective of PLL in this work. The PLL consists of a voltage-controlled oscillator (VCO), whose transfer function is $\frac{1}{s}$ (integrator). The PLLs take sensed grid voltage as the input. They estimate the grid frequency, phase and provide unit amplitude sine and cosine signals. These sine and cosine signals are known as unit vectors and they are used for the reference signal generation for the closed loop control. The $\alpha\beta$ components of the input signal are considered as

$$\left.\begin{aligned} V_\alpha &= V_g \sin\omega t \\ V_\beta &= V_g \sin\left(\omega t - \frac{\pi}{2}\right) \end{aligned}\right\} \tag{5.10}$$

The $dq$ components of the input signal are represented as

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \tag{5.11}$$

where $\theta$ is the rate at which synchronous reference frame rotates.

Substituting, $V_d = V_g$ and $V_q = 0$ in (5.11), the expression is rewritten as

$$\begin{bmatrix} V_g \\ 0 \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} V_g \sin\omega t \\ V_g \sin\left(\omega t - \frac{\pi}{2}\right) \end{bmatrix} \tag{5.12}$$

From (5.12)

$$V_g = V_g \cos\theta \sin\omega t - V_g \sin\theta \cos\omega t \tag{5.13}$$

By simplifying (5.13)

$$1 = \cos\left(\omega t - \theta\right) \tag{5.14}$$

From (5.14)

$$\theta = \omega t + 2n\pi \tag{5.15}$$

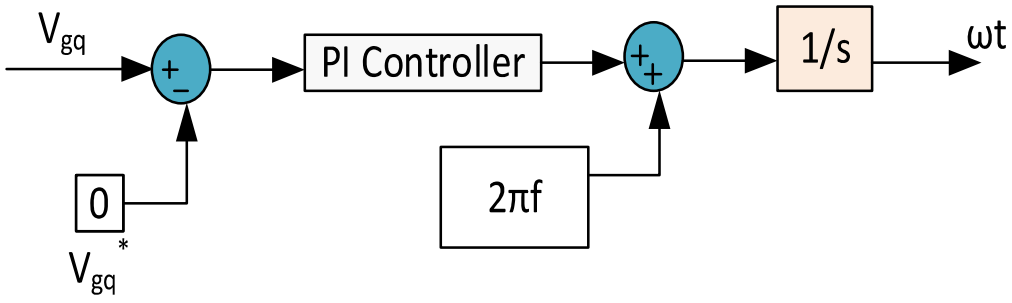



**Fig. 5.8** Phase locked loop (PLL).

Fig. 5.8 shows the PLL circuit which is used for grid integration of TLIHC. The magnitude of $q$-component of the reference signal is zero in the control loop. This is done in order to obtain $\theta$ in

phase with $\omega t$. The PLL is designed to obtain the phase and track the frequency of the reference voltage ($V_g$). It can be observed from Fig. 5.8 that the PLL circuit takes $V_{gq}$ ($q$- component of grid voltage after $dq-$ transformation) and subtracts it from 0 (reference value of $V_{gq}^{*}$) to make the phase output voltage equal to the grid voltage. Then, the PI controller takes the error signal and passes it through the VCO to obtain the phase of the voltage signal. Fig. 5.9 shows the phase tracking of the PLL. It can be observed from this figure that the performance of the PLL is good as it tracks the grid voltage signal within a 0.02 sec.

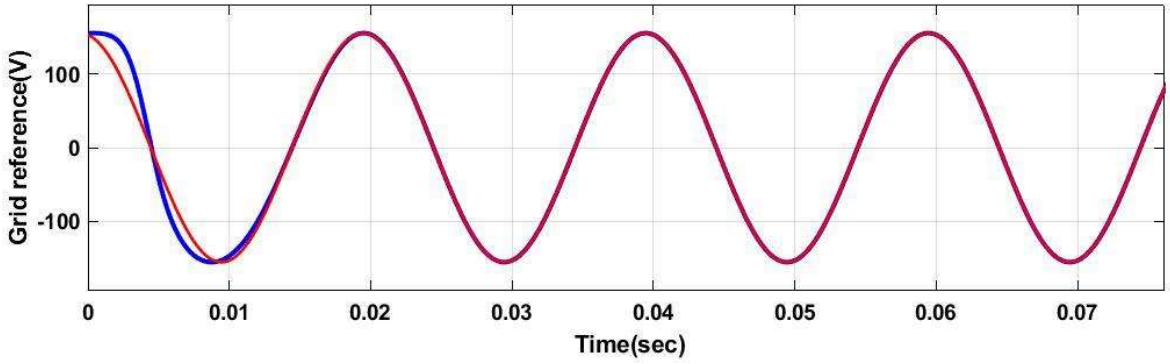



**Fig. 5.9** Phase tracking of the PLL.

The PLL technique used for the grid integration of TLIHC is known as T/4 delay technique, because the $\beta$- signal is obtained by using T/4 time delay (where T is the time period of the grid voltage). Since, this PLL technique is a delay based PLL technique (depends on time period/frequency), it is mostly suitable for the systems where the frequency of the grid voltage is not varying.

## 5.5 LCL Filter Design

The LCL filters are required in grid integrated inverters to attenuate the harmonic currents injected into the grid. Basically, the sinusoidal pulse width modulation (SPWM) driven inverters with high carrier frequencies have high frequency ripple components at and around their switching frequency ($f_{sw}$). So, to remove these ripple components, filters are required. In the grid integrated mode of TLIHC, an LCL filter is used. Fig. 5.10 shows the LCL filter referred to the grid side.

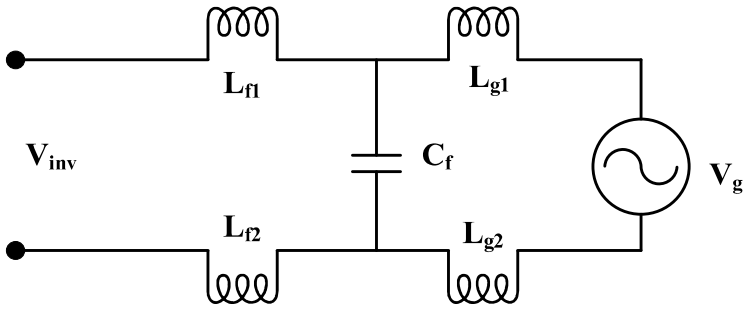



**Fig. 5.10** LCL filter referred to grid side.

For the calculation of LCL filter parameters, the considerations are

Filter capacitance is limited to a maximum value of $x_{cf}\% \leq 5\ \%$, to limit the decrease in power factor [113].

For the calculation of $C_f$, the expression $0 < C_f < x_{cf}\%$ is used [114]. So, $C_f$ is calculated as

$$C_f < 0.05 \frac{P_g}{V_g^2 \omega_g} \tag{5.16}$$

where $V_g$ = Grid voltage (rms value), $P_g$ = Active power flow into the grid and $\omega_g$ = Grid frequency in (rad / sec).

In Fig. 5.10, $L_{f1}$ and $L_{f2}$ represent the inverter side inductance ($L_f$), whereas $L_{g1}$ and $L_{g2}$ represent the grid side inductance ($L_g$). So, the total inductance $L_T = L_f + L_g$ and the inductance co-efficient $\Delta = \frac{L_g}{L_f}$.

From the inductance and capacitance parameters, the resonant frequency ($f_{res}$) can be calculated as follows

$$f_{res} = \frac{1}{2\pi} \sqrt{\left(\frac{L_f + L_g}{L_f L_g C_f}\right)} \tag{5.17}$$

By simplifying (5.17), the obtained total inductance ($L_T$) expression can be written as

$$L_T = \frac{1}{4\pi^2 f_{res}^2 C_f} \frac{(1+\Delta)^2}{\Delta} \tag{5.18}$$

Substituting $\Delta = 1$, $L_T$ can be written as

$$L_T = \frac{1}{\pi^2 f_{res}^2 C_f} \tag{5.19}$$

For better performance of the filter, $f_{res}$ must satisfy the following criteria

$$10f_g < f_{res} < 0.5f_{sw} \tag{5.20}$$

where $f_g$ is the grid frequency and $f_{sw}$ is the switching frequency of the proposed TLIHC.

From the above expressions, the filter inductance values are obtained as $L_f = L_g = \frac{L_T}{2}$. The obtained filter parameters are given in Table 5.1.

**Table 5.1** Filter Parameter Values

| Filter parameters | Values |
|---|---|
| $L_{f1}$ | 3 mH |
| $L_{f2}$ | 3 mH |
| $C_f$ | 2.5 μF |
| $L_{g1}$ | 3 mH |
| $L_{g1}$ | 3 mH |

## 5.6 Simulation Results of Grid Integrated TLIHC

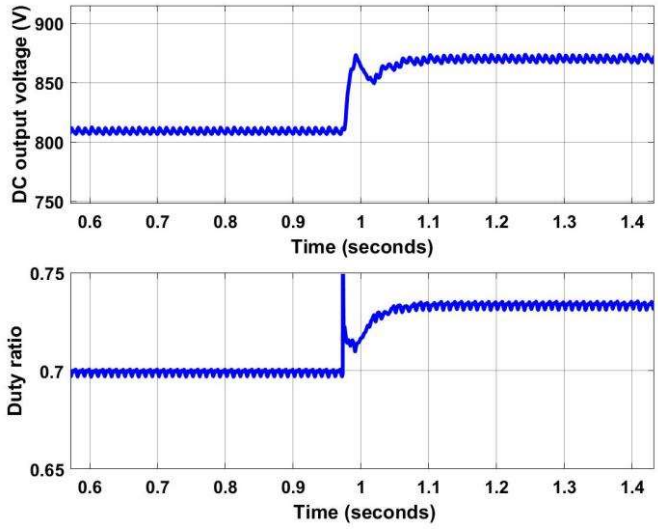
The simulation studies of the proposed TLIHC for the dynamic response are carried out using MATLAB/SIMULINK. The various operating parameters of TLIHC and their attributes for simulation studies are given in Table 5.2.

In this chapter, the grid tied mode operation of the proposed TLIHC is discussed. As in the proposed TLIHC, both DC and AC outputs are obtained from a single DC source, the simulation studies are carried out for both the cases (i.e., behaviour of grid current, grid voltage, DC link capacitor voltage, coupled inductor currents and reference signal $V_m(t)$ for change in both DC reference voltage and grid current). The robustness of the grid side controller and the DC side controller are verified in this work.

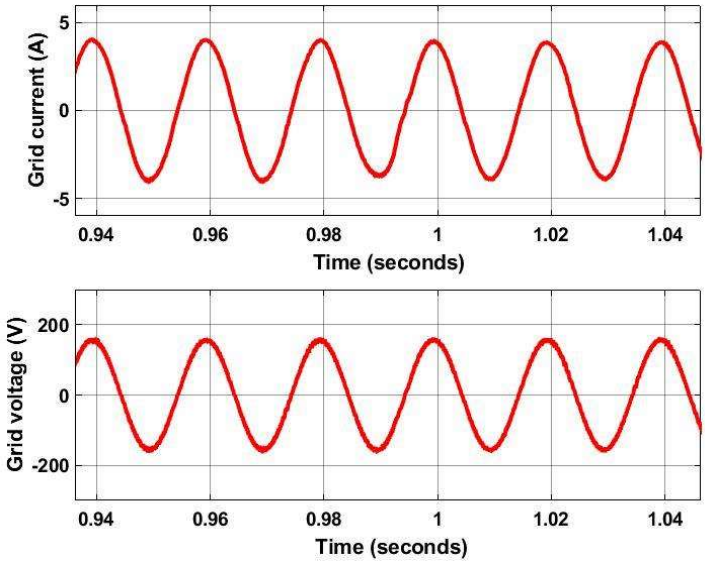
**Table 5.2** List of Parameters and Attributes for Grid Integrated TLIHC

| Parameters | Attributes |
|---|---|
| $L_1$ | 2.82 mH |
| $L_2$ | 2.04 mH |
| $C$ | 360 µF |
| $C_0$ | 400 µF |
| $R_{DC}$ | 700 Ω |
| $V_{in}$ | 170 V |
| $V_g$ | 110 V (rms value) |

Figs. 5.11, 5.12 and 5.13 show the dynamic response of duty ratio ($D$), grid current, grid voltage, DC link capacitor voltage, coupled inductor currents and the reference signal for the step-up operation of DC reference voltage. Fig 5.11 (a) shows the DC output voltage and $D$ tracking during the step-up operation of DC reference voltage. The DC output voltage has been stepped up from 809 V at 0.98 sec and settles at 870 V within 0.2 sec, which verifies the fast dynamic response of the type 3 controller used for DC output voltage control. Also, it can be noticed from Fig. 5.11 (a) that in the grid connected mode, there is no transient undershoot and ringing, when the value of $D$ is increased. Fig. 5.11 (b) shows the grid voltage and grid current of TLIHC during the step-up condition. From the Fig 5.11 (b), it can be observed that the grid current (2.83 A rms value) is in phase with the grid voltage (unity power factor) and there is only slight disturbance in grid current at 0.99 sec which settles down quickly.



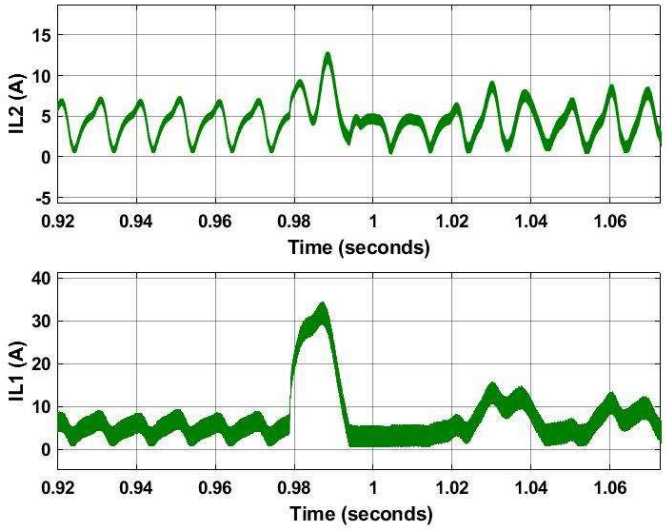

**(a)**



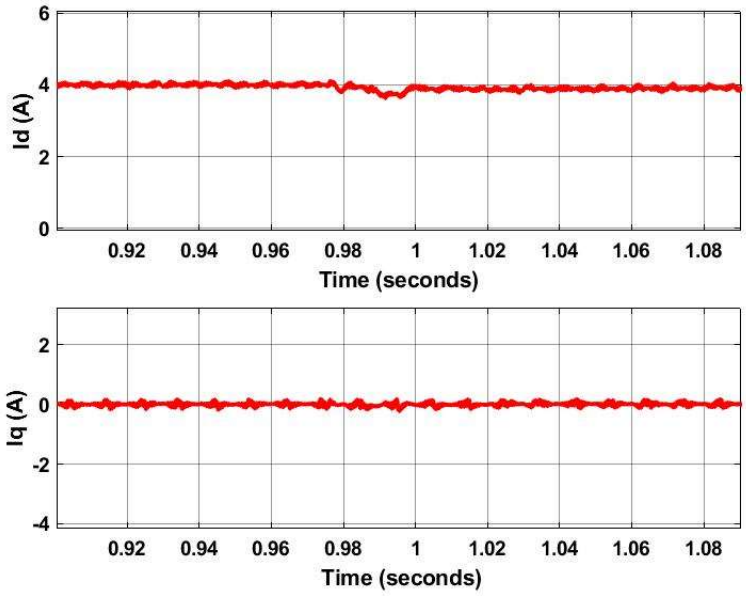

**(b)**

**Fig. 5.11** Step-up operation of DC reference voltage. **(a)** Tracking of duty ratio with DC output voltage and **(b)** Grid voltage and grid current.

Fig 5.12 (a) shows current across the coupled inductors $L_1$ and $L_2$ during the step-up condition of $D$. From this figure, it can be observed that both the currents $I_{L1}$ and $I_{L2}$ increase during the transition, but it settles once the value of $D$ is settled. Fig. 5.12 (b) shows the behaviour of $I_d$ and $I_q$ during the step-up condition of $D$. From Fig. 5.12 (b), it can be observed that the value of $I_d$ is slightly disturbed at 0.99 sec and it settles quickly, whereas $I_q$ is undisturbed.



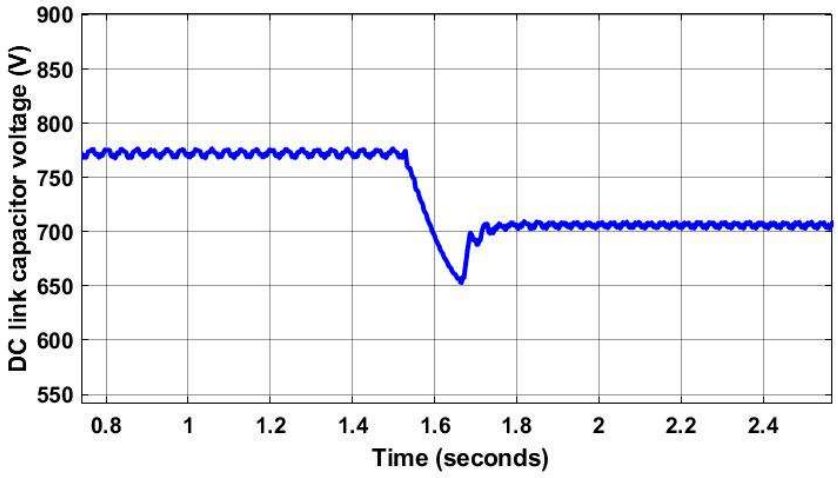

**(a)**



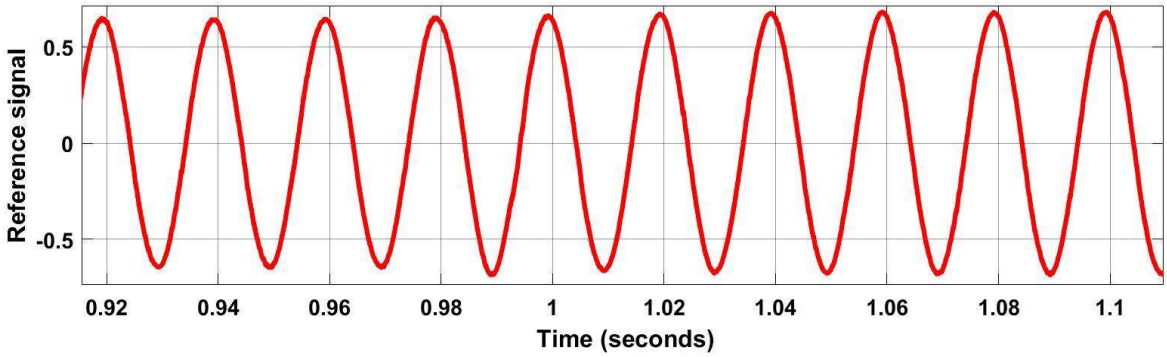

**(b)**

**Fig. 5.12** Step-up operation of DC reference voltage. **(a)** Coupled inductor current $I_{L1}$ and $I_{L2}$ and **(b)** Small fluctuation in $I_d$ and $I_q$.

Fig. 5.13 shows the DC link capacitor voltage and $V_m$ (t) for the step-up operation of $D$. From Fig. 5.13 (a), it can be observed that the DC link capacitor voltage is stepped down at 1.68 sec and settled down to 709 V within 0.2 sec. Since the inverter input voltage $V_{inv} = \frac{V_{in}}{D}$ decreases due to increase in $D$, peak value of reference signal $M_i$ of the grid connected TLIHC slightly increases to make the grid current undisturbed as observed from Fig. 5.13 (b).



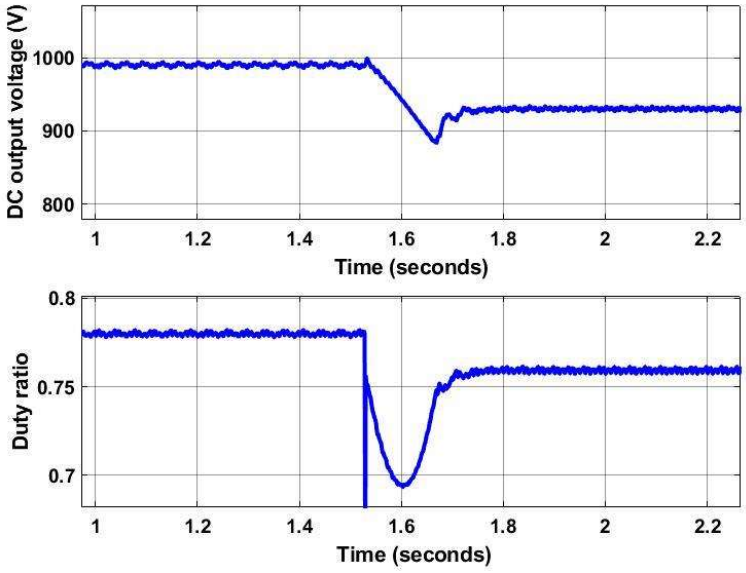

**(a)**



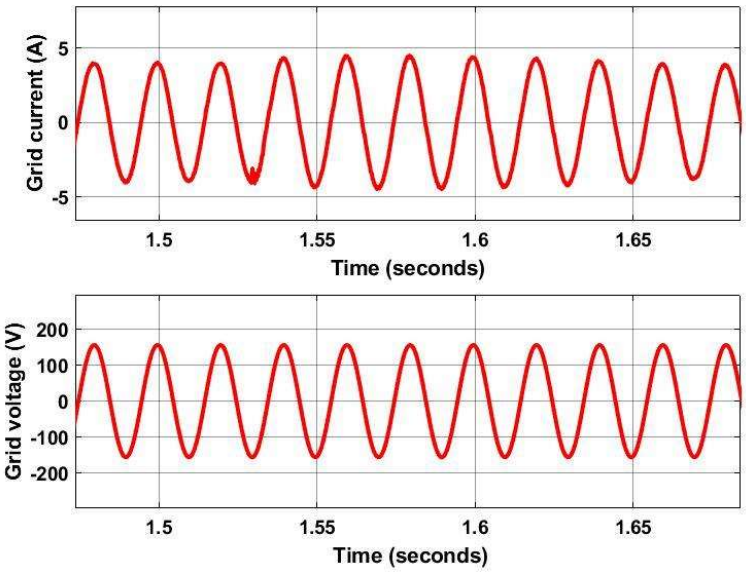

**(b)**

**Fig. 5.13** Step-up operation of DC reference voltage. **(a)** DC link capacitor voltage and **(b)** Reference signal for SPWM.

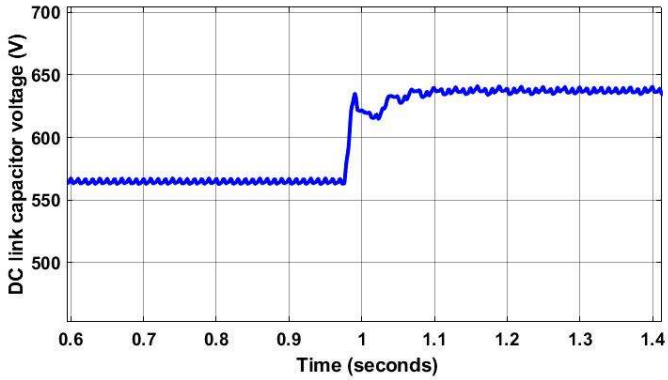
The DC output voltage for step-down in $D$ is shown in Fig. 5.14 (a). From Fig. 5.14 (a), it can be observed that the DC output voltage has been stepped down at 1.53 sec and settles at 930 V within 0.2 sec, which verifies the fast dynamic response of the DC side controller during the step-down operation of $D$. Also, it can be noticed from Fig. 5.14 (a) that the proposed TLIHC has no transient overshoot and ringing, when $D$ is decreased and it verifies the minimum phase behaviour of the grid integrated TLIHC. Fig. 5.14 (b) shows the grid voltage and grid current of TLIHC during the step-down condition of $D$ from 0.78 to 0.76. From Fig. 5.14 (b), it can be noticed that the grid current is disturbed only at the instant of step changing and it is settles quickly, whereas the grid voltage remains the same. Fig. 5.14 (c) shows the DC link voltage variation due to sudden change in $D$. It can be observed from Fig. 5.14 (c) that the DC link voltage has been increased to 635 V within 0.25 sec. Fig. 5.14 (d) shows the reference signal for the generation of switching pulses of the inverter side switches of TLIHC. As, the inverter input voltage ($V_{inv} = \frac{V_{in}}{D}$) is increased due to decrease in $D$, the modulation index ($M_i$) of TLIHC is slightly decreased to keep the AC output voltage same. From Fig. 5.14 (d), it can be noticed that the reference signal is slightly decreased due to increase in $D$ or DC reference voltage in case of the proposed TLIHC.


DC output voltage (V)
1000
900
800
1
1.2
1.4
1.6
1.8
2
2.2
Time (seconds)
Duty ratio
0.8
0.75
0.7
1
1.2
1.4
1.6
1.8
2
2.2
Time (seconds)

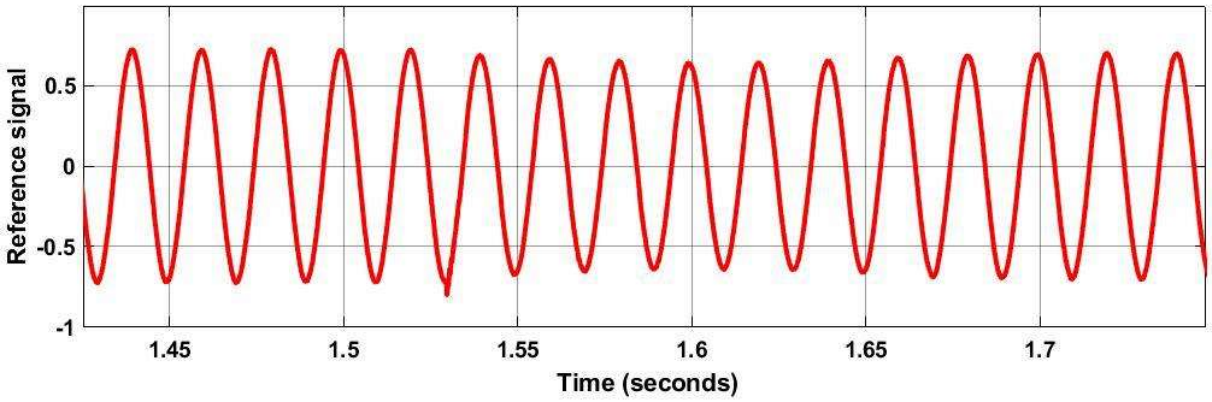
**(a)**


Grid current (A)
5
0
-5
1.5
1.55
1.6
1.65
Time (seconds)
Grid voltage (V)
200
100
0
-100
-200
1.5
1.55
1.6
1.65
Time (seconds)

**(b)**

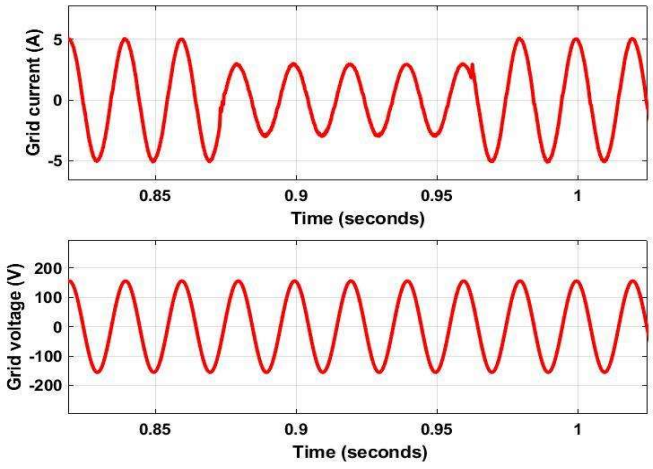



**(c)**

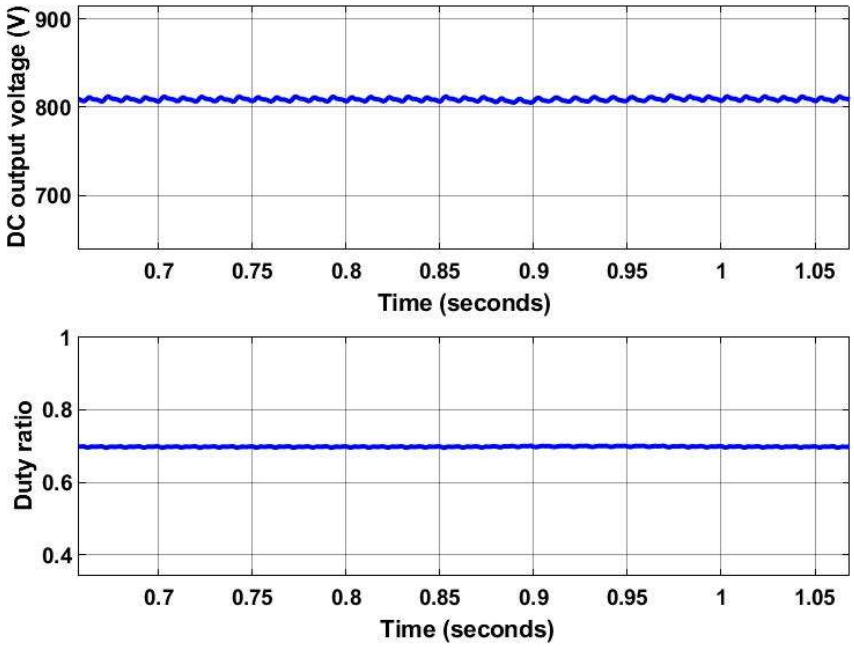



**(d)**

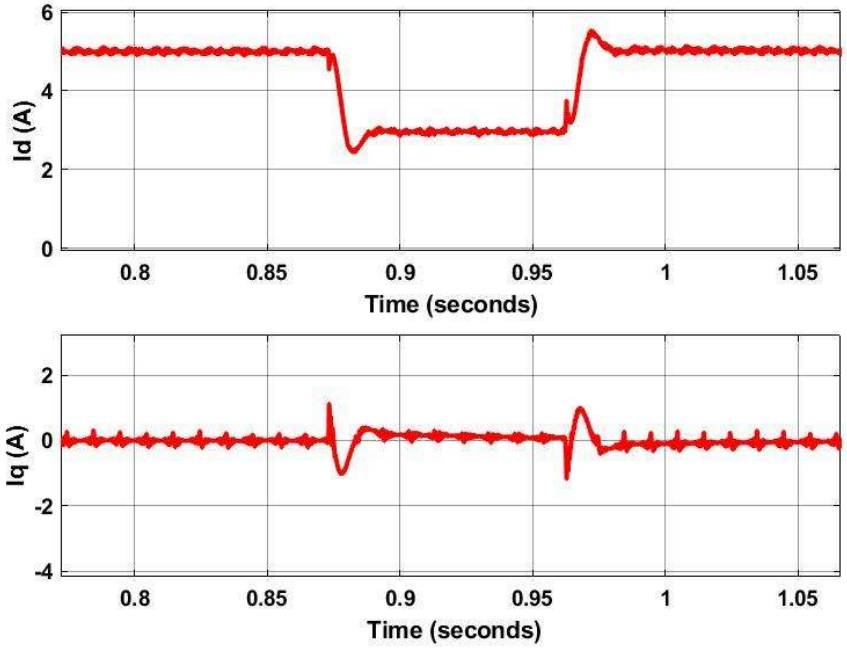
**Fig. 5.14** Response to step-down in duty ratio. **(a)** DC output voltage with respect to change in duty ratio, **(b)** Grid voltage and grid current, **(c)** DC link voltage and **(d)** Reference signal for SPWM implementation.



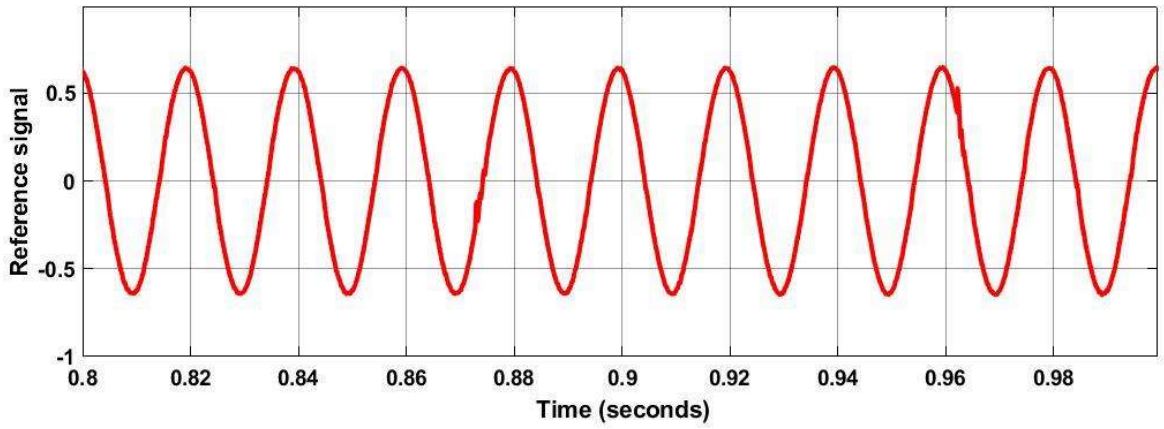

**(a)**


DC output voltage (V)
900
800
700
0.7
0.75
0.8
0.85
0.9
0.95
1
1.05
Time (seconds)
Duty ratio
1
0.8
0.6
0.4
0.7
0.75
0.8
0.85
0.9
0.95
1
1.05
Time (seconds)

**(b)**


Id (A)
6
4
2
0
0.8
0.85
0.9
0.95
1
1.05
Time (seconds)
Iq (A)
2
0
-2
-4
0.8
0.85
0.9
0.95
1
1.05
Time (seconds)

**(c)**



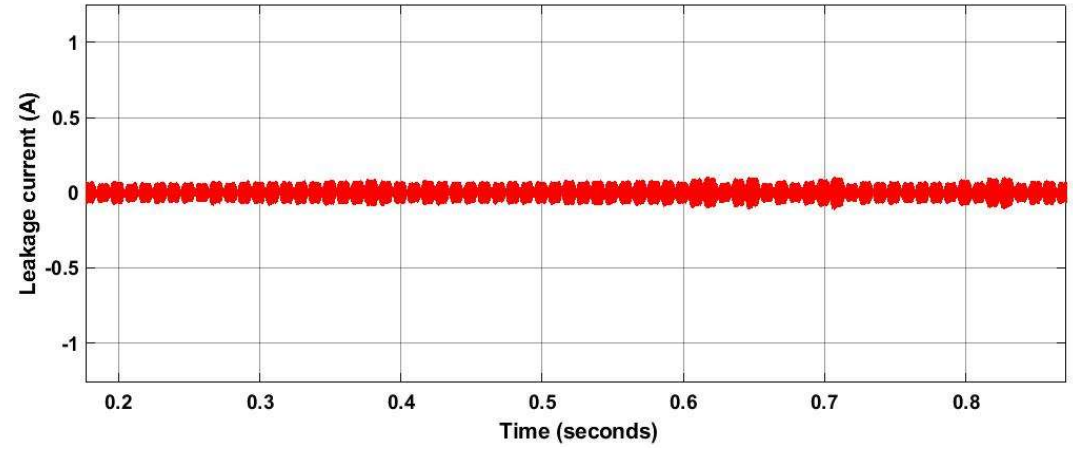

**(d)**

**Fig. 5.15** Step-down in grid current from 5A to 3A, then step-up from 3A to 5A. **(a)** Grid voltage and grid current, **(b)** DC output voltage and duty ratio, **(c)** $I_d$ and $I_q$ components of current and **(d)** Reference signal for SPWM.

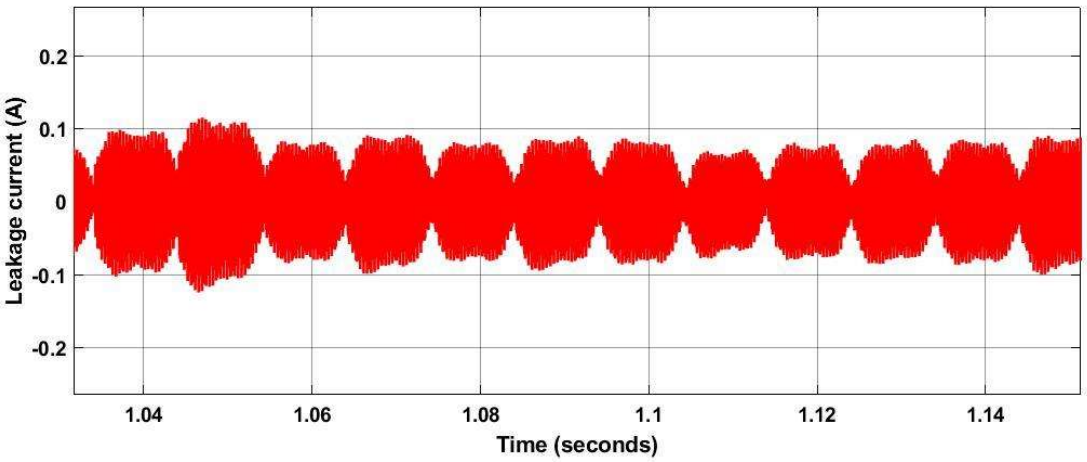
Fig. 5.15 shows the changes in the DC output voltage, duty ratio, grid voltage, $I_d$ and $I_q$ components of current and reference signal by changing the grid current using the synchronous reference frame control strategy. It can be observed from Fig. 5.15 (a) that as soon as the grid current is stepped down from 5 A to 3 A after 0.87 sec, it takes less than 0.02 sec to settle at 3 A. Fig. 5.15 (b) shows the DC output voltage ($V_{DC}$) and $D$ for both step-down and step-up in grid current. From Fig. 5.15 (b), it can be observed that $V_{DC}$ and $D$ are unchanged in either of the cases. Fig. 5.15 (c) shows $I_d$ and $I_q$ components of current during both step-down and step-up condition of grid current. It can be observed from Fig. 5.15 (c) that the value of $I_d$ decreases, when the grid current is stepped-down and again increased to achieve its previous value, when the grid current is stepped-up to its initial value. In this case, the power input to the grid is decreased to 234 W from 370 W. Further, the grid current is stepped up to 5 A peak just before 2 sec and settles down quickly, whereas the power output to the grid again changes to 370 W. Once again, no change in $V_{DC}$ and current through inductors are noticed. Also, from the Fig. 5.15 (d), it can be observed that no change in the value of the reference signal can be noticed once the inverter voltage is synchronized to the grid voltage. Further, it can be noticed that there is not much effect on inverter voltage due to change in grid current during the active power flow.

Fig. 5.16 shows the leakage current profile of the TLIHC for grid tied mode of operation. From the figure, it can be observed that the average leakage current is 70 mA and it never exceeds 110

mA during the grid integration. Thus, the TLIHC effectively mitigates the leakage current for both island mode and grid connection mode. It also follows the specification of VDE 0126-1-1 to maintain the leakage current below 300 mA. The value of parasitic capacitance has been taken 100 nF during the simulation of island mode as well grid connected mode. The Fig. 5.16 (b) shows the zoomed view of leakage current profile during the grid integration which does not exceed 110 mA.




**(a)**

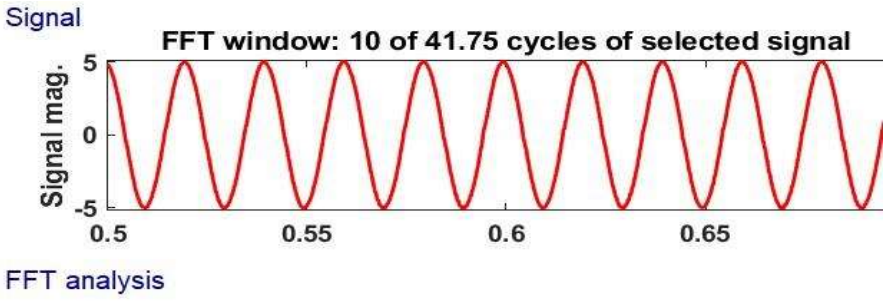



**(b)**

**Fig. 5.16** Leakage current profile. **(a)** Leakage current in grid integrated mode of TLIHC and **(b)** Zoomed view of leakage current profile.

## 5.7 FFT Analysis of Grid Current

The total harmonic distortion (THD) is reduced and the reliability is improved in case of the proposed TLIHC. As the two switches are placed at the grid side to isolate the DC part and grid/AC part during the freewheeling period and also as the dead-time of the switching pulses are eliminated, the quality of the grid current is improved. Fig 5.17 shows the FFT analysis of the grid current. It can be observed that the THD is equal to 1.68%, which is within limits of the recommended IEEE-519- 2014 standards. Also, the grid current is in phase with grid voltage as observed from Fig. 5.16. The FFT analysis of grid current is also be carried out by injecting it into the grid (at 156 V peak, 110V rms). It has been observed that the THD of the injected grid current is very low and equal to 1.96%.




FFT analysis

```
Fundamental          = 5 peak (3.535 rms)
THD                  = 1.68%

      0 Hz   (DC):          0.01%     90.0°
      5 Hz                  0.03%    249.4°
     10 Hz                  0.02%    -43.0°
     15 Hz                  0.04%     15.3°
     20 Hz                  0.01%     29.3°
     25 Hz                  0.01%    175.9°
     30 Hz                  0.02%     18.5°
     35 Hz                  0.02%    229.8°
     40 Hz                  0.03%    -44.4°
     45 Hz                  0.03%     91.0°
     50 Hz   (Fnd):        100.00%    102.7°
```

**Fig. 5.17** FFT analysis for 5 A grid current.

## 5.8 Summary

In this chapter, the dynamic response of TLIHC during the grid integrated condition has been verified to check performance of the controller. A $\frac{T}{4}$ delayed PLL technique is implemented to synchronize the inverter output voltage of TLIHC with the grid. Detailed mathematical analysis for the state space model of synchronous reference frame strategy has been carried out in this chapter. Further, the effect of step-down and step-up in $D$ or DC reference voltage on grid current

is also discussed. The robustness of the controller has been checked by instantly stepping-up and stepping-down the grid current. Also, to check the functionality of DC side controller, the behaviour of coupled inductor currents, DC output voltage, DC link capacitor voltage and duty ratio has been verified during the step-up and step-down conditions of the grid current. The FFT analysis of the grid current has been carried out to check the amount of harmonics injected into the grid current.