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High gain bipolar converter with reduced input current ripple for fuel cell integrated DC microgrid

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Abstract

The key characteristics of a DC-DC converter for a fuel cell (FC) application include higher voltage gain for DC-link voltage, the continuous and ripple-free source current that is beneficial for FC. This paper proposes a high-gain DC-DC converter with continuous and ripple-free input current. The proposed converter is suitable for integrating fuel cell and photovoltaic (PV) power into an isolated DC microgrid. Modified boost converter with an intermediate capacitor integrated with the cuk converter to achieve high voltage gain and low voltage stress across switches, which also reduces the reverse recovery problem of diodes. A prototype of a 1 kW converter is designed, developed, and analyzed to verify its working principle. The simulation and experimental results for high gain 40/400 V and 1 kW load power, with a DC microgrid of 400 V connected to the proposed converter, are in good harmony and are conforming to the theoretical analysis. The maximum obtained converter efficiency is 96.13%.

KEYWORDS

DC-DC converter, DC microgrid, fuel cell, high gain, reduced voltage stress

1 | INTRODUCTION

The pollution caused by greenhouse gas emissions has compelled the power industries to shift from fossil fuel to renewable energy based power generation. The fuel cell has a strong potential to replace fossil fuel based electrical energy. However, the fuel cell output voltage is low, thereby requiring a high gain converter for integration with the DC microgrid. DC-DC converters serve an important role in extracting power from low-voltage renewables, such as PV and FC, to meet load demand.[1–3] The adoption of unconventional energy sources like solar photovoltaic (PV) and fuel cells has raised awareness of the idea of microgrids. Microgrids appear promising for both islanded and grid-connected modes of operation because they are situated near the consumers and have the potential to increase the reliability, security, and quality of electrical power.[4–6] Figure 1 illustrates the basic structure of a microgrid. FC has some drawbacks despite offering benefits including zero emissions, quiet operation, superior dependability, and quick refueling times. Furthermore, FC voltage is strongly influenced by the loading conditions, and it falls as the load current rises. To increase the working life of fuel cells, it is also essential to ensure the suppression of ripples in the source current.[7]

In addition, the DC-DC converter for FC needs to have continuous input with the ripple-free current. In the past 10 years, a number of isolated and non-isolated high step-up DC-DC converters have been reported.[8] For isolated DC/DC converters, increasing the transformer turns can produce a significant voltage gain. However, as the number of turns increases, there is a corresponding increase in the leakage inductance. This leads to a decrease in voltage, the

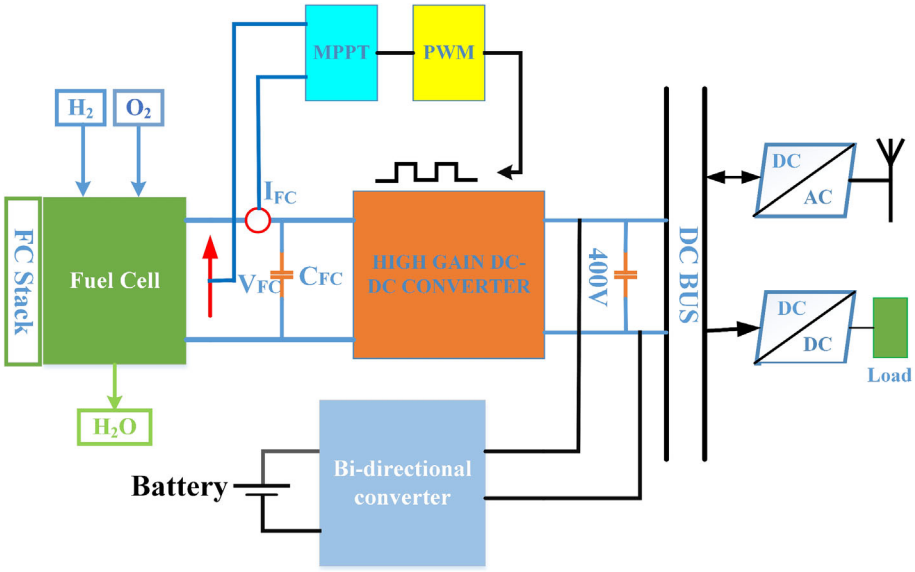

FIGURE 1 Integration of high gain converter with DC bus.

occurrence of excessive voltage spikes, and a reduction in efficiency.[9] Furthermore, it should be noted that the RMS value of current through switches and diodes tends to be larger in isolated DC-DC converters. The size of an isolated DC-DC converter is increased by the transformer's presence and the increased number of switching components. As a result, the utility of these converters is useless in applications where isolation is not necessary.

Non-isolated high-gain DC/DC converters are more affordable and efficient, and they offer a high boost voltage in a single stage. Moreover, the converters are separated into two groups: coupled type inductors and non-coupled type inductors. Isolated converters and coupled inductor-type converters have a lot of similarities.[10] Due to leakage inductance, coupled inductor converters also cause voltage spikes. There are several clamping and snubber circuits that have been required to reduce voltage spikes and recover energy.[11] However, these additional circuits increase the system's complexity, making it large and expensive.[12] As a result, non-coupled type inductor based converters are a good option for FC DC microgrid applications.

There are many non-isolated high-gain DC-DC converters being developed and constructed. A traditional boost converter is the name of the fundamental topology. Nevertheless, it is known that the conventional boost converter attains a high voltage gain for a high duty ratio, which results in greater conduction loss and more voltage stress on the switch and diode. In addition to that, working at a higher duty ratio raises the possibility of inductor core saturation. Consequently, reducing voltage stress and attaining better voltage gain at a reduced duty ratio becomes the motivating factor for future research. In Ahmed et al,[13] a cascaded boost converter configuration is proposed, where multiple individual units of traditional converters are connected in series. This design achieves higher gain through a high duty ratio, leading to diminished efficiency due to considerable conduction losses. The topology outlined in Muhammad et al[14] adopts an interleaved structure incorporating two coupled inductors and four switches lead to increased complexity. The literature[15–17] discusses a voltage lift technique that enhances the converter's gain. However, this method places substantial voltage and current stresses on the intermediate capacitor. DC-DC converters are cascaded with a clamped circuit to achieve high voltage, but it draw more current through input diodes.[18] Voltage multiplier cells[19–21] achieve significant voltage gain, but this comes at the cost of reduced efficiency due to the higher number of components, especially when employing multiple voltage multiplier cells. Moreover, managing the converter operation becomes challenging as the number of stages increases. In Karthikeyan et al,[22] hybridization of boost and cuk is reported to achieve voltage gain by a factor (1+D)/(1-D) where D is the duty cycle. However, this converter suffers low gain and high voltage stress across the switch. A switch inductor based converter is presented in Tang et al.[23] This converter has lower gain and high-frequency pulse width modulation (HF PWM) voltage, which increases the radiated EMI and requires additional periodic maintenance. The converter in Banaei and Bonab[24] presents a buck-boost based topology that achieved a gain of 3D/(1-D) with a drawback of discontinuous input current with high voltage and current stress through the devices. The converter in Saravanan and Babu[25] achieves a gain of (3+D)/2(1-D) but high current stress through the switch, which causes a reduction in the overall efficiency of the converter.[26] proposes a converter

with a single switch with low gain and more voltage stress across devices. Buck-boost integrated with zeta converter is presented in Banaei and Bonab[27] and has a discontinuous input current. The converters in the literature[28,29] both have the same gain in comparison with the proposed converter, but one has a higher component count, and the other one has a pulsating input current. The configuration in the literature[30,31] are based on the switched capacitors (SC). These converters involve parallel charging of capacitors followed by series discharging. However, this approach leads to inadequate voltage regulation and necessitates in integration with other techniques to ensure proper output voltage control, resulting in high current spikes. Active passive inductor cell based topology is reported in Tang et al[32] with a gain of (1+3D)/(1-D), this configuration utilizes switched inductor arrangement to achieve this voltage gain. However, converter switches are under a high current stress, and high-frequency pulse width modulation (HF PWM) voltage, which increases the radiated EMI and requires additional periodic maintenance.

This study proposes a high-gain DC-DC converter that has been shown to work well as a bridge to integrating FC output with a standalone DC microgrid. Key characteristics of the proposed converter achieved a high voltage gain with a moderate number of components, minimizing current ripple at the input side, reducing voltage stress on semiconductor devices, and ensuring a constant voltage from source to load ports to eliminate high-frequency PWM voltage. This design also prevents leakage current and minimizes radiated electromagnetic interference (EMI).

The manuscript is organized as follows: The circuit description and its operational aspects are explained in Section 2. The design parameters of the proposed converter, dynamic analysis, and efficiency calculation are presented in Section 3. Section 4 discusses the comparative analysis of the converter. Simulation and experimental verification are discussed in Section 5, and Section 6 concludes the paper.

1.1 | Topological evolution of high gain DC-DC converter

To improve the conversion ratio of a boost converter, by cascading two boost converters with an intermediate capacitor, achieving a gain of 2/(1-D) as shown in Figure 2B, where the capacitor exhibits a voltage of 2D/(1-D) and corresponding

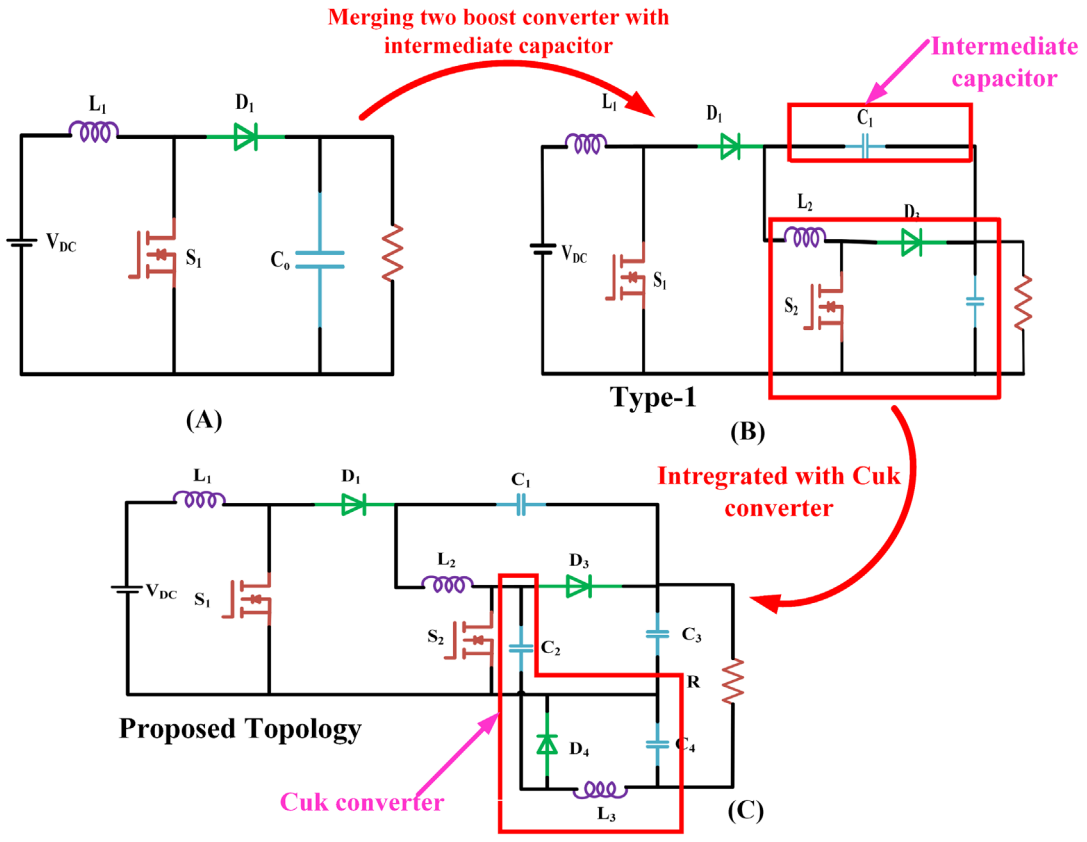

FIGURE 2 Evalution of proposed converter: (A) Boost converter. (B) Type-1. (C) Proposed (type-2).

reduces the stress across the switch S_1 and diode D_1, But switch S_2 and diode D_2 bear the same stress equal to output voltage. So, the Type-1 configuration can be further modified into the proposed topology, and this modified setup is integrated with a cuk converter (utilizing a CD cell with an inductor) as shown in Figure 2C. The resulting proposed topology gain is expressed as 2(1+D)/(1-D), and correspondingly reduces the voltage stress across the switch and diode. This modified circuit of the proposed converter is shown in Figure 2.

2 | CIRCUIT DESCRIPTION AND OPERATING PRINCIPLE OF PROPOSED CONVERTER

The proposed high gain converter consists of switches-(S_1, S_{11} & S_2), inductors-($L_1, L_{11}, L_2, \& L_3$), diodes-($D_1, D_2, \& D_3$) with a common coupling capacitor C_1 and an output filter capacitor C_3 and C_4. The working of the converter in continuous inductor current mode (CICM) is described in modes of operation. Figure 3 represents an expanded iteration of Figure 4 achieved through the implementation of interleaving principles. For interleaving, both switches S_1 and S_{11} operate at 50% duty cycle in opposite phases to mitigate the ripple at the source side. Modifications in the boost converter and cuk converter integrate with each other to obtain a high voltage gain, low voltage stress, and minimized

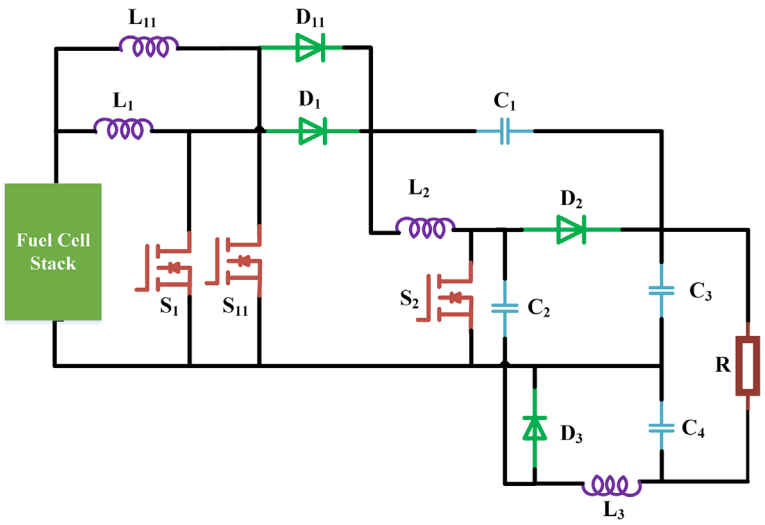

FIGURE 3 Proposed converter interleaved circuit configuration.

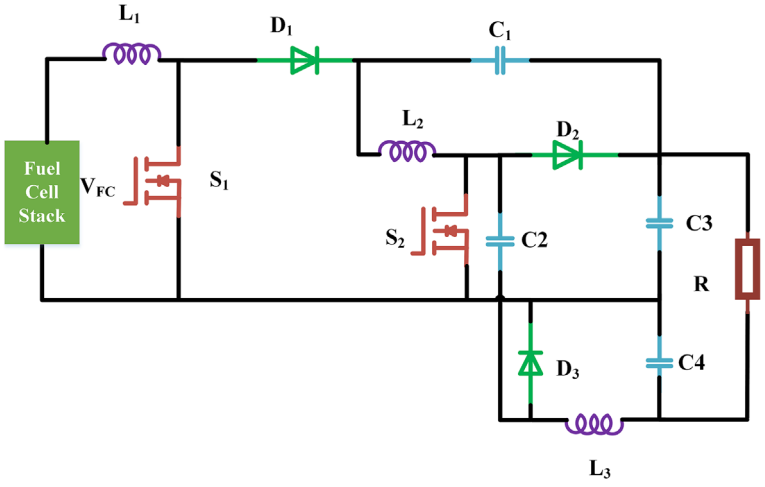

FIGURE 4 Proposed converter circuit configuration.

ripple at the source side. The main operating waveforms of the proposed converter in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are depicted in Figure 5 over a switching period.

2.1 | Modes of operation

2.1.1 | Mode-1

In this mode, the switches S_1 and S_2 are in an "ON" state. Thus, input inductor L_1 is charging through S_1 and inductor L_2 is charging through switch S_2, C_3 and C_1. The inductor L_3 is discharging through C_2 and C_4. Output capacitor C_3 and C_4 discharge through load as shown in Figure 6.

For t = 0 to D_2T_s (both S_1 and S_2 are "ON"),

$$v_{L_1} = v_{in} \tag{1}$$

$$v_{L_2} = v_{c_3} - v_{c_1} \tag{2}$$

$$v_{L_3} = v_{c_4} - v_{c_2} \tag{3}$$

$$i_{c_3} + i_{c_1} + i_0 = 0 \tag{4}$$

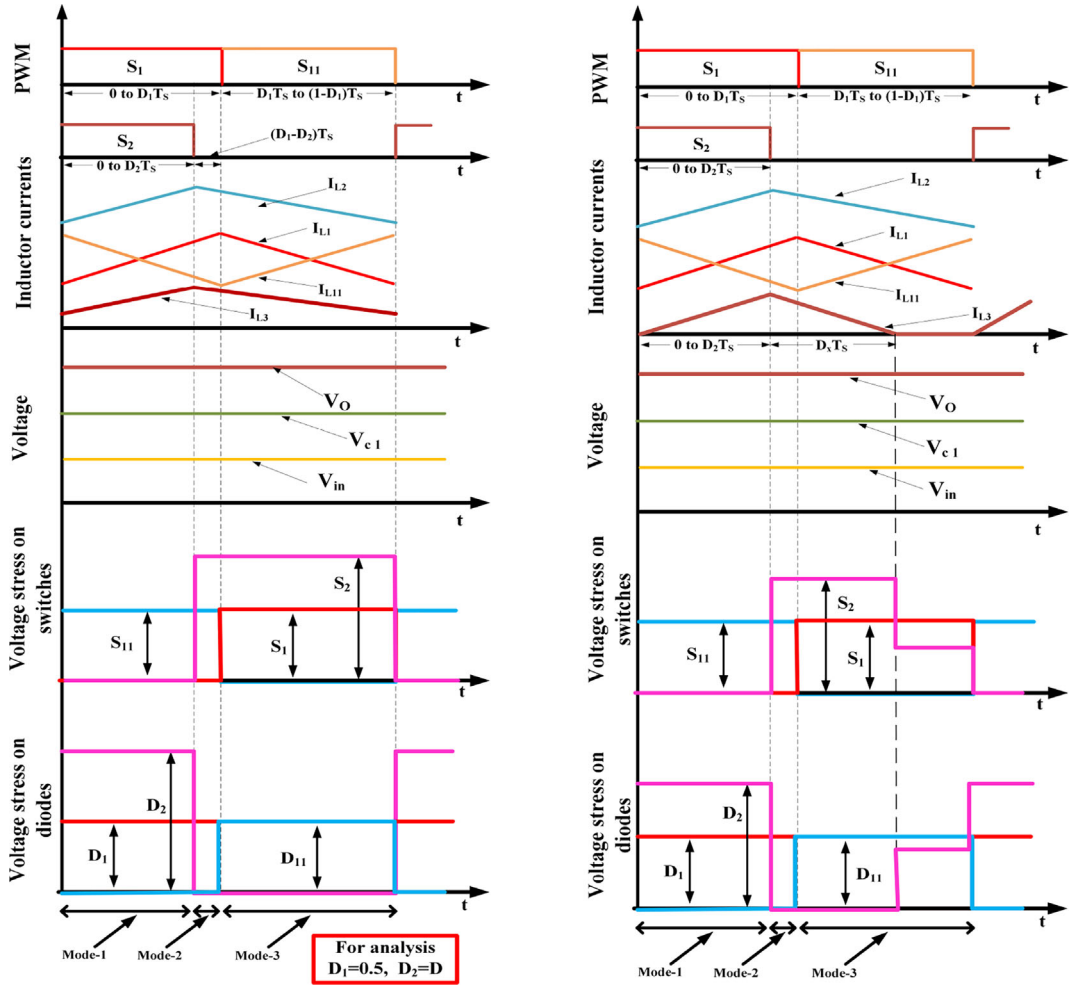

FIGURE 5 Key waveform of the proposed converter: (A) CCM and (B) DCM.

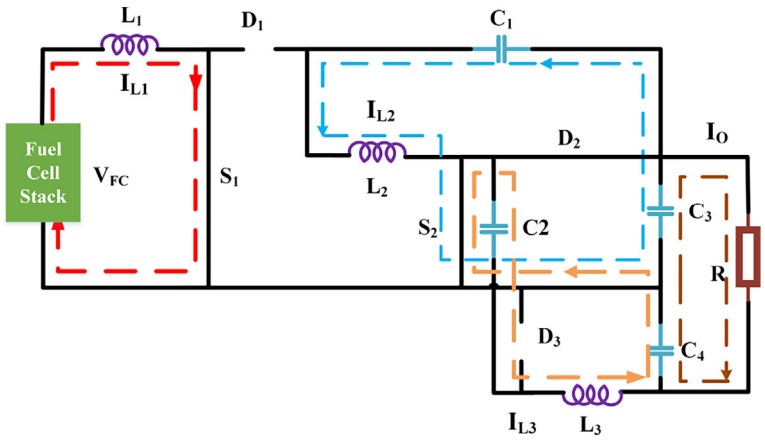

FIGURE 6 Basic circuit operation in mode-1.

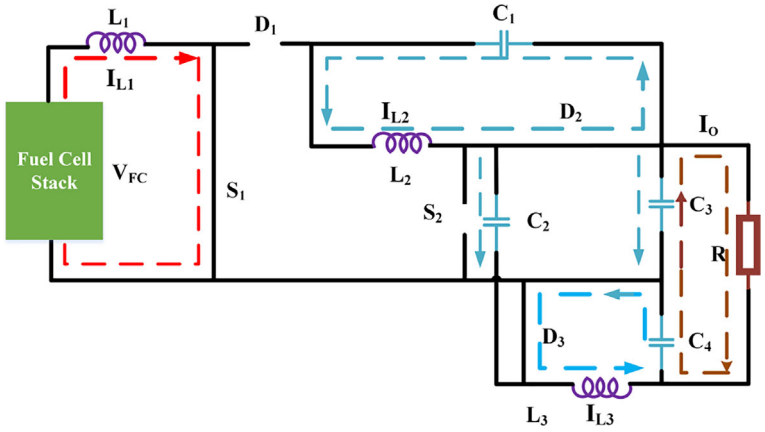

FIGURE 7 Basic circuit operation in mode-2.

$$i_{c_1} = i_{L_2} \tag{5}$$

$$i_{c_2} = i_{L_3} \tag{6}$$

$$i_{c_3} + i_{c_1} + i_0 = 0 \tag{7}$$

2.1.2 | Mode-2

For this mode, the converter operation is explained in Figure 7. In this mode of operation, switch S_1 is ON, and S_2 is in "OFF" state. Input inductor L_1 is still charging through S_1. Then, inductor L_2 discharges through capacitor C_1, and inductor L_3 charges through C_4, which is shown in Figure 7.

For t = D_2T_s to $(D_1 - D_2)T_s$ (S_1 is "ON" and S_2 is "OFF"),

$$v_{L_1} = v_{in} \tag{8}$$

$$v_{L_2} = -v_{c_1} \tag{9}$$

$$v_{L_3} = v_{c_4} \tag{10}$$

$$i_{c_1} = i_{L_2} \tag{11}$$

$$i_{c_3} + i_{c_2} + i_0 = 0 \tag{12}$$

$$i_{c_4} + i_{L_3} + i_0 = 0 \tag{13}$$

$$i_{c_2} + i_{c_3} = i_{L_3} + i_{c_4} = 0 \tag{14}$$

2.1.3 | Mode-3

The converter operation for this mode is depicted in Figure 8. In this mode, the switches S_1 & S_2 both are OFF and inductor L_1 discharge through diode D_1, C_1 and C_3. In this mode of operation, D_1, D_2, and D_3 all are ON. Inductor L_2 discharge through C_1 and inductor L_3 charge through D_3 and C_4.

For t $= D_1 T_s$ to $(1 - D_1) T_s$ (both S_1 and S_2 are "OFF"),

$$v_{L_1} = v_{in} + v_{c_1} - v_{c_3} \tag{15}$$

$$v_{L_2} = -v_{c_1} \tag{16}$$

$$v_{L_3} = v_{c_4} \tag{17}$$

$$-i_{c_2} + i_{L_3} - i_{c_3} + i_{c_4} + i_{L_1} = 0 \tag{18}$$

$$i_{L_2} = i_{L_1} + i_{c_1} \tag{19}$$

$$i_{c_3} + i_0 + i_{c_2} = i_{L_1} \tag{20}$$

$$i_{c_4} + i_{L_3} + i_0 = 0 \tag{21}$$

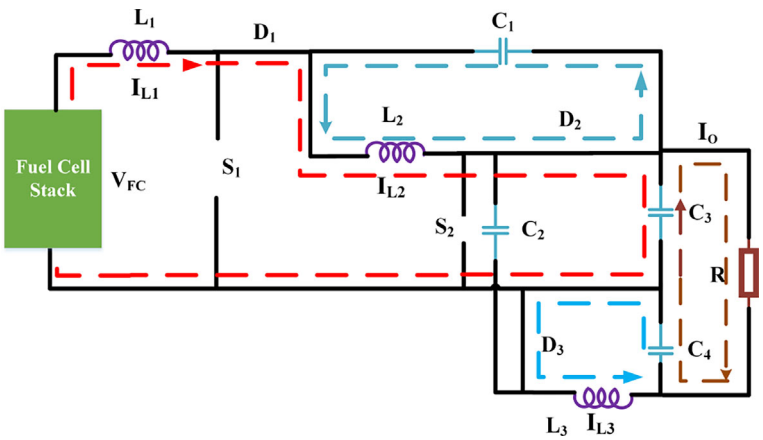

FIGURE 8 Basic circuit operation in mode-3.

2.2 | Voltage gain

Applying volt-second balance on inductor L_1 by Equations (1), (8), and (15)

$$D_2V_{in}+(D_1-D_2)V_{in}+(1-D_1)(V_{in}+V_{c_1}-V_{c_3})=0$$

$$V_{in}+V_{c_1}(1-D_1)-V_{c_3}(1-D_1)=0 \tag{22}$$

Applying volt-sec balance on inductor L_2 by Equations (2), (9), and (16)

$$D_2(V_{c_3}-V_{c_1})+(D_1-D_2)(-V_{c_1})+(1-D_1)(-V_{c_1})=0$$

$$V_{c_1}=V_{c_3}D_2 \tag{23}$$

Applying volt-sec balance on inductor L_3 by Equations (3), (10), and (17)

$$D_2(V_{c_4}-V_{c_2})+(D_1-D_2)(V_{c_4})+(1-D_1)V_{c_4}=0$$

$$V_{c_4}=V_{c_2}D_2 \tag{24}$$

By Equations (22) and (23), we get V_{c_3}

$$V_{c_3}=\frac{V_{in}}{(1-D_1)(1-D_2)} \tag{25}$$

$$V_o=V_{c_3}+V_{c_4} \tag{26}$$

By using the above equations to obtain a final output voltage:

$$V_o=\frac{V_{in}(1+D_2)}{(1-D_1)(1-D_2)} \tag{27}$$

Note: Both D_1 and D_2 are variable duty cycle. For interleaving, both switches S_1 and S_{11} operate at a D_1=50% duty cycle in opposite phases to mitigate the ripple at the source side. The switch S_2 is set to a duty cycle represented by D_2 =D (variable duty) to regulate the gain of the proposed converter.

$$V_o=\frac{2V_{in}(1+D)}{(1-D)} \tag{28}$$

2.3 | Non-ideal gain calculation

In practical applications, the performance of a converter is significantly impacted by parasitic elements, necessitating an analysis of the proposed converter under non-ideal characteristics, as illustrated in Figure 9. Understanding how these elements influence voltage gain and efficiency is crucial. Here, r_s denotes the on-state resistance of the active switch, whereas $r_{D1}-r_{D3}$ and $V_{D1}-V_{D3}$ represent the forward resistance and voltage drop of diodes, respectively.

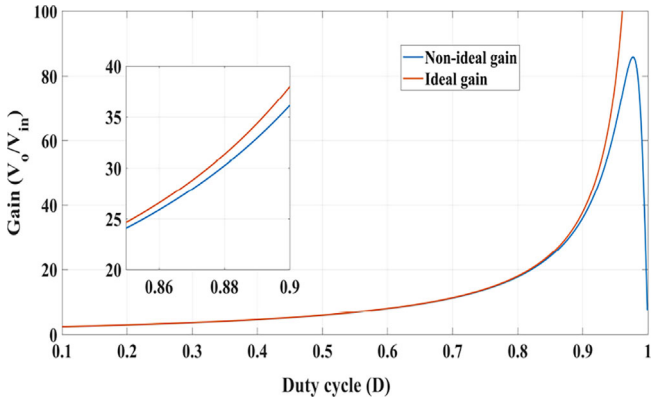

FIGURE 9 Impact of parasitic parameters on voltage gain.

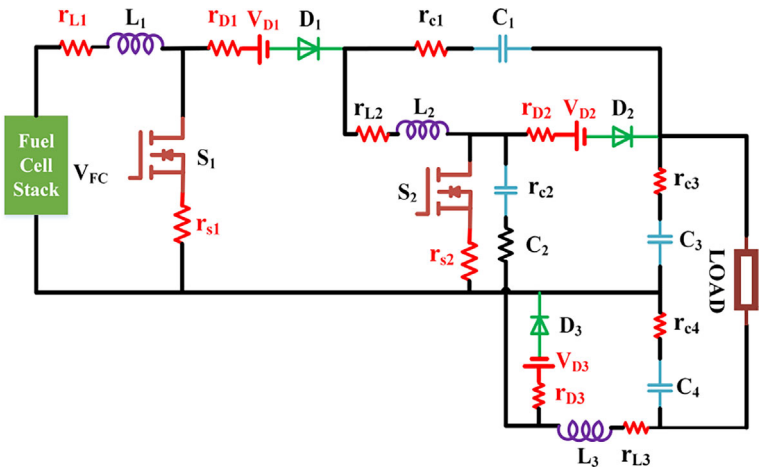

FIGURE 10 Non-ideal circuit of the proposed converter.

Additionally, r_{L1}-r_{L3} indicates the internal resistance of the inductors, and $r_{c_1} - r_{c_4}$ represents the equivalent series resistance of capacitors as shown in Figure 10.

The actual voltage gain of the proposed converter can be calculated by applying the volt-sec balance on the inductor when the switch is ON and OFF condition. Applying Kirchhoff's Voltage Law (KVL) to the inductor voltage results in the following equations:

Equations for mode-I

$$\left.\begin{aligned} V_{L_1} &= V_{in} - I_{L_1}(r_{L_1} - r_s) \\ V_{L_2} &= V_{c_3} - V_{c_1} - I_{L_2} r_{L_2} - r_{s_2}(I_{L_2} - I_{c_2}) + r_{c_3} I_{c_3} - r_{c_1} I_{L_2} \\ V_{L_3} &= V_{c_4} - V_{c_2} - I_{c_2} r_{c_2} - r_{L_3} I_{L_3} + r_{c_4} I_{c_4} - r_{s_2}(I_{L_2} - I_{c_2}) \end{aligned}\right\} \quad (29)$$

Equations for mode-II

$$\left.\begin{aligned} V_{L_1} &= V_{in} - I_{L_1}(r_{L_1} - r_{s_1}) \\ V_{L_2} &= -V_{c_1} - I_{c_1} r_{L_2} - V_{D_2} - r_{D_2}(I_{c_1} - I_{c_2}) + r_{c_1} I_{c_1} \\ V_{L_3} &= V_{c_4} - I_{L_3} r_{L_3} + r_{c_4} I_{c_4} + V_{D_3} - r_{D_3}(I_{c_2} - I_{L_3}) \end{aligned}\right\} \quad (30)$$

Equations for mode-III

$$\left.\begin{aligned} V_{L_1} &= V_{in} - I_{L_1} r_{L_1} + V_{c_1} + I_{c_1} r_{c_1} - V_{c_3} - I_{c_3} r_{c_3} \\ V_{L_2} &= -V_{c_1} - r_{L_2}(I_{L_1} + I_{c_1}) - V_{D_2} - r_{D_2}(I_{L_1} + I_{c_1} - I_{c_2}) - r_{c_1} I_{c_1} \\ V_{L_3} &= V_{c_4} - I_{L_3} r_{L_3} + r_{c_4} I_{c_4} + V_{D_3} - r_{D_3}(I_{c_2} - I_{L_3}) \end{aligned}\right\} \tag{31}$$

$$\left.\begin{aligned} L_1 : [V_{in} - I_{L_1}(r_{L_1} + r_{s_1})]D_2 + [V_{in} - I_{L_1}(r_{L_1} + r_{s_1})](D_1 - D_2) + [V_{in} - I_{L_1} r_{c_1} + V_{c_1} + I_{c_1} r_{c_1} - V_{c_3} - I_{c_3} r_{c_3})](1 - D_1) \\ V_{c_3} + I_{c_3} r_{c_3} = \frac{1}{(1 - D_1)}[V_{in} - I_{L_1}(2 r_{L_1} D_1 - r_{L_1} + r_{s_1 D_1}) + V_{c_1} + r_{c_1 I_{c_1}}] \end{aligned}\right\} \tag{32}$$

$$\left.\begin{aligned} L_2 : [V_{c_3} - V_{c_1} - r_{s_2}(I_{L_2} - I_{c_2}) + r_{c_3 I_{c_3}} - r_{c_1} I_{L_2}]D_2 + [-I_{c_1} r_{c_1} - V_{D_2} - r_{D_2}(I_{c_1} - I_{c_2}) - \\ I_{c_1} r_{c_1} - V_{c_1}](D_1 - D_2) + [-I_{c_1} r_{c_1} - V_{D_2} - r_{D_2}(I_{c_1} - I_{c_2}) - I_{c_1} r_{c_1} - V_{c_1}](1 - D_1) \\ V_{c_1} + I_{c_1} r_{c_1} = (V_{c_3} - I_{c_3} r_{c_3})D_2 - [I_{L_2} r_{L_2} + r_{s_2}(I_{L_2} - I_{c_2})]D_2 \\ -[I_{c_1} r_{L_2} - V_{D_2} - (I_{c_1} - I_{c_2}) r_{D_2}](1 - D_2) \end{aligned}\right\} \tag{33}$$

putting Equation (33) into Equation (32)

$$\left.\begin{aligned} V_{c_3} + r_{c_3} I_{c_3} = \frac{1}{(1 - D_1)(1 - D_2)}[V_{in} - I_{L_1}(2 r_{L_1} D_1 - r_{L_1} + r_{s_1} D_1)] - [r_{L_2} I_{L_2} + r_{s_2}(I_{L_2} - I_{c_2})]\frac{D_2}{1 - D_2} \\ -[r_{L_2} I_{c_1} - V_{D_4} - r_{D_2}(I_{c_1} - I_{c_2}] \end{aligned}\right\} \tag{34}$$

$$\left.\begin{aligned} L_3 : [V_{c_4} - V_{c_2} - r_{c_2 I_{c_2}} - r_{L_3} I_{L_3} + r_{c_4 I_{c_4}} + r_{s_2}(I_{L_2} - I_{c_2})]D_2 + [V_{c_4} - I_{L_3} r_{L_3} + I_{c_4} r_{c_4} + V_{D_3} \\ - r_{D_3}(I_{c_2} - I_{L_3})](D_1 - D_2) + [V_{c_4} - I_{L_3} r_{L_3} + r_{c_4 I_{c_4}} + V_{D_3} - r_{D_3}(I_{c_2} - I_{L_3})](1 - D_1) \\ V_{c_4} + r_{c_4} I_{c_4} = [V_2 + r_{c_2 I_{c_2}} - r_{s_2}(I_{L_2} - I_{c_2})]D_2 - [V_{D_3} - r_{D_3}(I_{c_2} - I_{L_3})(1 - D_2) \\ + r_{L_3} I_{L_3} + r_{L_3} I_{L_3}(1 - D_2)] \end{aligned}\right\} \tag{35}$$

$$V_o = V_{c_3} + r_{c_3} I_{c_3} + V_{c_4} + r_{c_4} I_{c_4} \tag{36}$$

By using Equations (34), (35), and (36)

$$G_{practical} = \frac{\frac{2(1+D)}{(1-D)} - \frac{K_p}{V_{in}}}{1 + \frac{1}{R_L}\left[\frac{4(1+D)}{1-D} K_{L_1} + \frac{1+D}{1-D}(K_{L_2} + K_{c_1}) + K_{L_3} - K_{c_2}\right]} \tag{37}$$

$$\begin{aligned} &where\, K_p = 1.5 V_{D_1} + V_{D_2}(1+D) + V_{D_3} \\ &K_{L_1} = (r_{s_1}(1+D))/(1-D) \\ &K_{L_2} = (r_{L_2} + r_{s_2})(D(1+D)/(1-D) + r_{s_2} D) \\ &K_{L_3} = (r_{D_3}(1-D) + r_{L_3} + r_{L_3}(1-D)) \\ &K_{c_1} = (r_{L_2} + r_{D_2})(1+D) \\ &K_{c_2} = r_{s_2} D(1+D)/(1-D) - r_{D_2}(1+D) + r_{s_2} D + r_{D_3}(1-D) \end{aligned}$$

Equations (28) and (37) provide the ideal and non-ideal voltage gains of the proposed converter, as illustrated in Figure 9. This figure demonstrates that at duty ratios (up to 0.75), the ideal and practical voltage gains are nearly identical due to the minimal impact of component nonidealities. At higher duty ratios, a clear difference between the non-ideal and ideal voltage gains becomes apparent, as shown in Figure 9. Nonidealities significantly impact the converter's performance, especially at higher duty ratios.

Similarly, non-idealities impact on efficiency of the proposed converter. To investigate this impact, the actual output voltage and load resistance to calculate the output power (P_o). However, this computation does not initially consider switching losses, which are significant in high-frequency power converters. Thus, we subtract switching losses from the

output power expression, as outlined in Equation (38). Likewise, the expression for input power (P_{in}) can be formulated in relation to the real output voltage, as described in Equation (38).

$$\left.\begin{aligned} P_o &= \frac{V_o^2}{R} - P_{sw} \\ P_{in} &= \frac{G_{ideal} V_{in} V_o}{R} \end{aligned}\right\} \tag{38}$$

Here, P_{sw} denotes the switching losses of the proposed converter, and these losses can be computed using the specified method or formula.

$$P_{sw} = V_S I_S (t_r + t_f) f_s \tag{39}$$

The efficiency Equation (40) presents a comprehensive evaluation of the converter's performance by accounting for all component losses, including the switching frequency (f_s), peak voltage (V_S), peak current (I_S), rise time (t_r), and fall time (t_f) of the active switches, as presented in Equations (39) and (40).

$$\left.\begin{aligned} \frac{P_o}{P_{in}} = \frac{\frac{V_o^2}{R} - P_{sw}}{P_{in}} = \frac{G_{ideal} V_{in} V_o}{R} - \frac{P_{sw}}{P_{in}} \\ \eta = \frac{P_o}{P_{in}} = \chi - \frac{P_{sw}}{P_{in}} \end{aligned}\right\} \tag{40}$$

The conduction loss equivalent of the converter, denoted as χ, can be determined using Equation (41).

$$\chi = \frac{1 - \frac{(1-D)}{2(1+D)} \frac{(1.5V_{D_1} + V_{D_2}(1+D) + V_{D_3})}{V_{in}}}{1 + \frac{1}{R_L}\left[\frac{4(1+D)}{1-D} K_{L_1} + \frac{1+D}{1-D}(K_{L_2} + K_{c_1}) + K_{L_3} - K_{c_2}\right]} \tag{41}$$

Figure 11 illustrates the efficiency plotted against various duty ratios, utilizing the analytical expressions provided in Equations (40) and (41). It is evident from the graph that the proposed converter theoretically attains a peak efficiency and then decreases with the duty cycle. However, efficiencies significantly drop at higher duty ratios due to increased input current required to support rated output power. The converter operates at higher duty ratios when

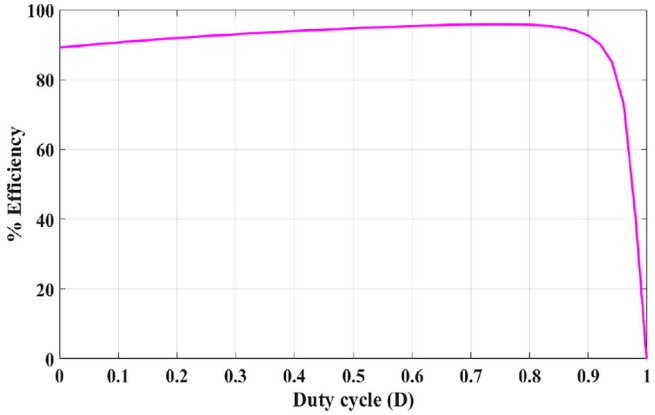

FIGURE 11 Theoretical efficiency curves with respect to duty ratio.

operating at lower input voltages for a given output voltage and power. Consequently, higher input currents are necessary to maintain constant power, leading to observed efficiency decreases, as depicted in Figure 11.

2.3.1 | DCM operation of proposed topology

In Figure 12, the analytical waveforms during the steady state of the DCM operation are depicted in Figure 6B. In this illustration, it is evident that the inductor current reaches zero states at time $D_x T_s$. The DCM operation observed here can be categorized into three modes. As per the described operating principle, the inductor currents exhibit linear increase within the time interval $[0, D_2 T_s]$. The expression for the ripple currents across each inductor is provided as follows:

$$\Delta I_{L1} = \frac{DV_{in}}{L_1 f_s}, \Delta I_{L_2} = \frac{D(V_{c_3} - V_{c_1})}{L_2 f_s}, \Delta I_{L_3} = \frac{D(V_{c_4} - V_{c_3})}{L_3 f_s}, \tag{42}$$

DCM takes place when the average current of the inductor is less than its ripple current. The following are the conditions that could allow the proposed converter to function under DCM operation:

$$I_{L_1 avg} - \Delta I_{L1} \leq 0,\ I_{L_2 avg} - \Delta I_{L2} \leq 0,\ I_{L_3 avg} - \Delta I_{L3} \leq 0 \tag{43}$$

Therefore, based on the information provided in relation Equation (43), it can be stated that the current through inductor L_3 reaches the boundary condition for the DCM earlier than that of L_1 and L_2.

During DCM mode operation, switches are turned off, and the circuit configuration is shown in Figure 12. At this point, the energy stored in inductor L_3 is reduced to zero, leaving only the energy stored in capacitors C_3 and C_4 available to discharge through the load.

$$\int_0^{D_2 T_s} V_{L3} dt + \int_{D_2 T_s}^{D_1 T_s} V_{L3} dt + \int_{D_1 T_s}^{T_s} V_{L3} dt = 0 \tag{44}$$

$$D_2 (V_{C_4} - V_{C_2}) + D_x V_{C_4} + 0 = 0 \tag{45}$$

$$V_{C_4} (D_2 + D_x) = V_{C_2} D_2 \tag{46}$$

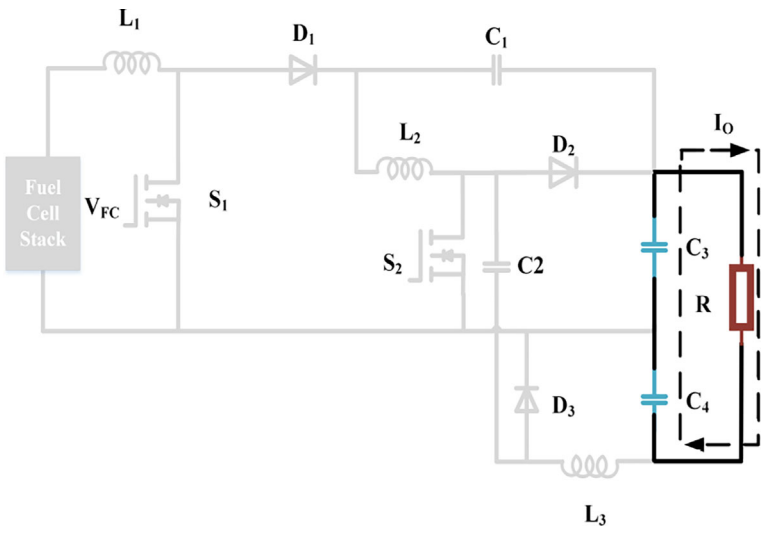

FIGURE 12 Converter operation in DCM.

$$V_{C_1} = V_{C_3} D_2 \tag{47}$$

$$V_{C_3} = \frac{V_{in}}{(1-D_1)(1-D_2)} \tag{48}$$

$$V_{C_4} = V_{C_2} \frac{D_2}{D_2 + D_x} \tag{49}$$

$$V_{C_4} = \frac{V_{in} D_2}{(1-D_1)(1-D_2)(D_2+D_x)} \tag{50}$$

$$V_o = V_{c_3} + V_{c_4} \tag{51}$$

$$V_o = \frac{V_{in}}{(1-D_1)(1-D_2)} \left[1 + \frac{D_2}{(D_2+D_x)}\right] \tag{52}$$

$$V_o = \frac{2V_{in}}{(1-D)} \left[1 + \frac{D}{(D+D_x)}\right] \tag{53}$$

$$D_x = D \frac{4V_{in} - V_o(1-D)}{V_o(1-D) - 2V_{in}} \tag{54}$$

The average current of the output capacitor for each switching period is calculated as follows:

$$I_{co} = \frac{(1/2) D_x T_s I_{LPeak} - I_o T_s}{T_s} \tag{55}$$

For mode-1, the peak value of the inductor current can be written as

$$I_{L3_{peak}} = \frac{2V_{in} D}{L_3 f_s} \tag{56}$$

Upon substituting Equations (54) and (56) into Equation (55), considering that I_{co} equals zero in steady-state conditions, the expression for I_{co} can be derived as follows:

$$I_{co} = \frac{1}{2} D \frac{4V_{in} - V_o(1-D)}{(V_o(1-D) - 2V_{in})} \frac{2V_{in} D}{L_3 f_s} - \frac{V_o}{R} = 0 \tag{57}$$

Hence, the voltage gain can be determined by

$$G_{dcm} = \frac{V_0}{V_{in}} = \frac{1}{2} \left[\frac{2}{1-D} - \frac{D^2}{K} + \sqrt{\left(\frac{2}{1-D}\right)^2 - \left(\frac{D^2}{K}\right)^2 + \frac{16D^2}{K(1-D)}} \right] \tag{58}$$

When the proposed Converter is operated in Boundary Conduction Mode (BCM), the voltage gain in CCM becomes equivalent to the voltage gain in DCM.

$$K_{critical} = \frac{D(1-D)(2-D)}{2(1+D)} \tag{59}$$

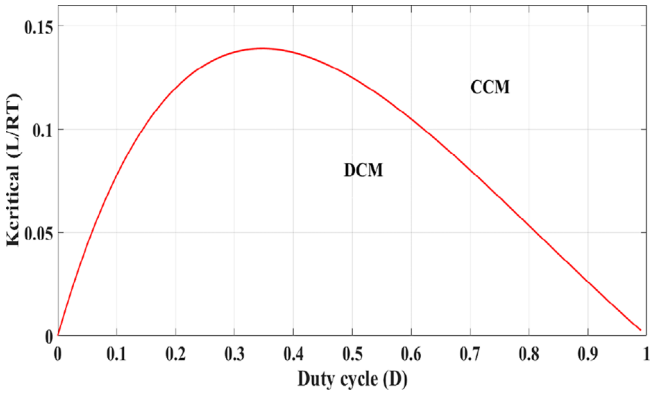

FIGURE 13 Normalized boundary time constant versus duty cycle.

Figure 13 illustrates the curve of $K_{critical}$. When the value of $K > K_{critical}$ value, the proposed converter is operating in CCM, where the value of K is L/RT_s.

3 | DESIGN AND ANALYSIS OF THE PROPOSED CONVERTER

The output terminal of the proposed converter is connected to a DC microgrid and its a design calculation is provided. The requirements for the design study are as follows:

3.1 | Calculation of parameters

3.1.1 | Duty cycle selection

The duty ratio is determined by putting the input and output voltage values into Equation (28) as follows.

$$D = \frac{V_o - 2V_{in}}{2V_{in} + V_o}$$

3.1.2 | Inductor selection

The switch on the input side, denoted as S_1, operates with a constant 50% duty cycle for interleaving to mitigate ripple at the source side, while S_2 operates with a variable duty cycle. The input inductor's estimated value is 431.80μH by considering 40% ripple in inductor current. In this study, the closest readily available inductor value is 470μH.

$$L_1 = \frac{D_1 V_{in}}{f \Delta I_{L_1}} \tag{60}$$

It can be seen from Equation 23 and Equation 25 that the obtained value of $(V_{c_3} - V_{c_1})$ is equal to $2V_{in}$. So, the inductance value is to be 545.80μH for a 20% ripple in the current. In this study, the closest possible value of 564 μH is chosen.

$$L_2 = \frac{D_2 (V_{c_3} - V_{c_1})}{f \Delta I_{L_2}} \tag{61}$$

Similarly, using equations 23,24, and 25, the value of inductance L_3 is 220μH for 20% ripple in current. In the hardware analysis, closed value of 270μH is selected:

$$L_3 = \frac{D_2(V_{c_4} - V_{c_2})}{f\Delta I_{L_3}} \tag{62}$$

3.1.3 | Capacitor selection

The capacitance of the device depends upon the allowable voltage ripple (Δvc), average voltage (V_C), switching frequency (fs), and the current flow through the capacitor. By applying Kirchhoff's Current Law (KCL) during Mode-1, given equations in Appendix A, the following design equations are

$$C_1 = \frac{(1+D_2)D_2T_sI_0}{(1-D_2)\%\Delta V_{C_1}}, \quad C_2 = \frac{D_2T_sI_0}{\%\Delta V_{C_2}}$$
$$C_3 = \frac{2I_0D_2T_s}{(1-D_2)\%\Delta V_{C_2}}, \quad C_4 = \frac{4I_0D_2T_s}{(1-D_2)\%\Delta V_{C_4}}$$

By maintaining the voltage ripple under 2% for all capacitors. The value of capacitor C_1, C_2, C_3 and C_4 is estimated to have a value of 17.15 μF, 35.35 μF, 125.07 μF and 110.23 μF but for this work, a higher available value of capacitors C_1=22μF, C_2= 47μF, C_3=160μF and C_4=160μF are selected.

A DC microgrid is connected to the output of the proposed converter. Thus, the amount of the output capacitor is irrelevant. To filter the output current, a capacitor with a value of 160 μF can be attached to the output. In Table 1, the design parameters are listed. The chosen values of reactive components are given in Table 2.

3.2 | Dynamic analysis of proposed converter

Figure 14 provides the converter state symbols and polarity indicators for small signal analysis. The output of the converter is connected to a DC microgrid. As a result, for state-space analysis, a resistive DC microgrid resistance of 1.5Ω is taken into account.[33] Hence, the following equations describe the converter operation given below:

For t = 0 to DT_s (both S_1 and S_2 are "ON"),

TABLE 1 Design parameters.

Power	1000 W
Input voltage	95 V
Output voltage	350 V
Switching frequency	40 kHz

TABLE 2 Reactive components.

Input inductor value (L_1)	470 μH
Value of Inductor (L_2)	564 μH
Value of Inductor(L_3)	270 μH
Intermediate capacitor (C_1)	22 μF
Capacitor value (C_2)	47 μF
Output filter capacitor (C_3)	160 μF
Output filter capacitor (C_4)	160 μF

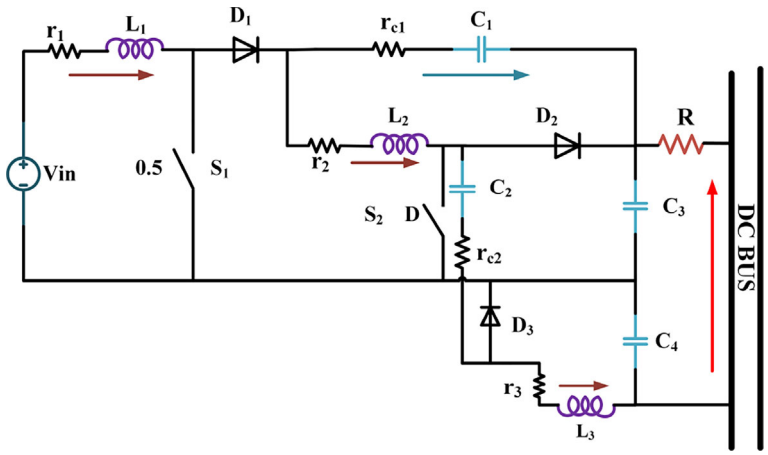

FIGURE 14 Circuit diagram with a parameter for small signal analysis.

$$L_1\dot{i}_1 = V_{in} - I_1 r_1 \tag{63}$$

$$L_2\dot{i}_2 = V_{c_3} - V_{c_1} - I_2(r_{c_1} - r_{c_3} + r_2) - I_o r_{c_3} \tag{64}$$

$$L_3\dot{i}_3 = V_{c_4} - V_{c_2} - I_3(r_{c_4} + r_{c_2} + r_3) - I_o r_{c_4} \tag{65}$$

$$C_1\dot{v}_{c_1} = I_2 \tag{66}$$

$$C_2\dot{v}_{c_2} = -I_3 \tag{67}$$

$$C_3\dot{v}_{c_3} = -I_o - I_2 \tag{68}$$

$$C_4\dot{v}_{c_4} = -I_o + I_3 \tag{69}$$

For t = DT_s to (0.5-D)T_s (S_1 is "ON" and S_2 is "OFF"),

$$L_1\dot{i}_1 = V_{in} - I_1 r_1 \tag{70}$$

$$L_2\dot{i}_2 = -V_{c_1} - I_2(r_2 + r_{c_1}) \tag{71}$$

$$L_3\dot{i}_3 = V_{c_4} + I_3(r_3 + r_{c_4}) - I_o r_{c_4} \tag{72}$$

$$C_1\dot{v}_{c_1} = I_2 \tag{73}$$

$$C_2\dot{v}_{c_2} = (V_o - V_{c_2} - V_{c_4})/r_{c_2} \tag{74}$$

$$C_3\dot{v}_{c_3} = -I_o \tag{75}$$

$$C_4\dot{v}_{c_4} = -I_o + I_3 \tag{76}$$

For t = 0.5T_s to T_s (both S_1 and S_2 are "OFF"),

$$L_1\dot{i}_1 = V_{in} + V_{c_1} - V_{c_3} + I_1(r_{c_1} - r_1) - I_2 r_{c_1} + I_o r_{c_3} \tag{77}$$

$$L_2\dot{i}_2 = -V_{c_1} - I_2(r_{c_1} + r_2) + I_1 r_{c_1} \tag{78}$$

$$L_3\dot{i}_3 = V_{c_4} - I_3(r_3 + r_{c_4}) + I_o r_{c_4} \tag{79}$$

$$C_1\dot{v}_{c_1} = I_2 - I_1 \tag{80}$$

$$C_2\dot{v}_{c_2} = (V_{c_3} - V_{c_2})/r_{c2} \tag{81}$$

$$C_3\dot{v}_{c_3} = -I_o \tag{82}$$

$$C_4\dot{v}_{c_4} = -I_o + I_3 \tag{83}$$

The equivalent ESR value of the series resistance of all passive components is shown in Figure 14. The voltage V_d is constant DC grid voltage, and R is grid resistance. The state-space matrix is calculated by introducing small perturbations and assuming V_d is grid voltage which is constant so $\hat{V}_d = 0$ and the average value of $V_d = V_o$.

$$\begin{array}{llllll} v_{in} & = V_{in} + \hat{v}_{in} & i_1 & = I_1 + \hat{i}_1 & i_2 & = I_2 + \hat{i}_2 \\ i_3 & = I_3 + \hat{i}_3 & v_{c_1} & = V_{c_1} + \hat{v}_{c_1} & v_{c_2} & = V_{c_2} + \hat{v}_{c_2} \\ v_o & = V_o + \hat{v}_o & d & = D + \hat{d} & & \end{array}$$

$$A = \begin{bmatrix} 0 & 0 & 0 & \frac{1}{2L_1} & 0 & -\frac{1}{2L_1} & 0 \\ 0 & 0 & 0 & k_1 & 0 & \frac{D}{L_2} & 0 \\ 0 & 0 & 0 & 0 & -\frac{D}{L_3} & 0 & k_2 \\ -\frac{1}{2C_1} & k_3 & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{2C_2} & 0 & \frac{D}{C_2} & 0 & 0 & \frac{(D-1/2)}{2C_2R} & \frac{(D-1/2)}{2C_2R} \\ 0 & -\frac{D}{C_3} & 0 & 0 & 0 & k_4 & k_5 \\ 0 & 0 & k_6 & 0 & 0 & k_7 & k_8 \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{D}{L_1} + \frac{1}{2L_1} & -\frac{D-0.5}{L_1} \\ 0 & \\ 0 & \\ 0 & \\ 0 & \\ 0 & \\ 0 & \end{bmatrix}, X = \begin{bmatrix} \hat{i}_1 \\ \hat{i}_2 \\ \hat{i}_3 \\ \hat{V}_{c_1} \\ \hat{V}_{c_2} \\ \hat{V}_{c_3} \\ \hat{V}_{c_4} \end{bmatrix}, U = \begin{bmatrix} \hat{V}_{in} \\ \hat{d} \end{bmatrix}$$

$$
\begin{aligned}
&\text{where value of } k_1, k_2, k_3 \ldots\ldots k_8\\
&k_1 = (D-1/2)/L2 - 1/(2*L2) - D/L2\\
&k_2 = -D/L3 + D/L3 + 1/(2*L3) - (D-1/2)/L3\\
&k_3 = D/C1 + 1/(2*C1) - (D-1/2)/C1\\
&k_4 = (D-1/2)/(2*C3*R) - 1/(2*C3) - D/(C3*R)\\
&k_5 = (D-1/2)/(2*C3*R) - 1/(2*C3) - D/(C3*R)\\
&k_6 = (D/C4 + 1/(2*C4)) - (D-1/2)/C4\\
&k_7 = (D-1/2)/(C4*R) - 1/(2*C4*R) - D/(C4*R)\\
&k_8 = (D-1/2)/(C4*R) - 1/(2*C4*R) - D/(C4*R)
\end{aligned} \tag{1}
$$

$\dot{X} = A[X] + B[U]$

The matrices A, B, X, and U can be used to find the current to duty transfer functions for $|\hat{i}_1/\hat{v}_{in}, |\hat{i}_1/\hat{d}, |\hat{i}_2/\hat{v}_{in}, |\hat{i}_2/\hat{d}, |\hat{v}_c/\hat{v}_{in}, |\hat{v}_c/\hat{d}, |\hat{v}_o/\hat{v}_{in}$, & $|\hat{v}_o/\hat{d}$. The transfer function for the magnitude of the current $\hat{i}_2$ divided by the input disturbance $\hat{d}$ can be determined by summing the design values of passive components and the resistance of the DC microgrid, denoted as $R = 1.5$.[34]

$$
= \frac{\widehat{i_2(s)}}{\widehat{d(s)}}
$$

$$
= \frac{2.6\times10^{14}s^4 + 4.1\times10^{19}s^3 - 3.5\times10^{28}s^2 - 4.72\times10^{35}s + 2.9\times10^{39}}{1.65\times s^7 + 2.8\times10^{9}s^6 + 4.1\times10^{14}s^5 + 3.1726\times10^{23}s^4 + 6.6\times10^{26}s^3 + 9.5\times10^{29}s^2 + 5.2\times10^{32}s + 5\times10^{35}} \tag{84}
$$

3.3 | Efficiency of the proposed converter

The efficiency of the proposed converter is computed by considering both conduction losses and switching losses. Specifically, the root mean square (RMS) value of device currents is utilized in this computation[35] as given below:

RMS current through switches:

$$
\begin{aligned}
I_{s1,rms} &= \sqrt{\frac{1}{T_s}\int_0^{D_1T_s} \imath_s^2 dt}, \quad I_{s1,rms} = \frac{(1+D_2)I_0}{(1-D_2)(1-D_1)}\sqrt{D_1}\\
I_{s2,rms} &= \sqrt{\frac{1}{T_s}\int_0^{D_2T_s} \imath_s^2 dt}, \quad I_{s2,rms} = \frac{(1+D_2)I_0}{(1-D_2)}\sqrt{D_2}
\end{aligned}
$$

RMS current through diodes:

$$
\begin{aligned}
I_{D_1,rms} &= \sqrt{\frac{1}{T_s}\int_0^{(1-D_1)T_s} \imath_{L_1}^2 dt}, \quad I_{D_1,rms} = \frac{(1+D_2)I_0}{(1-D_2)(1-D_1)}\sqrt{1-D_1}\\
I_{D_2,rms} &= \sqrt{\frac{1}{T_s}\int_0^{(1-D_2)T_s} \imath_{L_2}^2 dt}, \quad I_{D_2,rms} = \frac{(1+D_2)I_0}{(1-D_2)}\sqrt{1-D_2}\\
I_{D_3,rms} &= \sqrt{\frac{1}{T_s}\int_0^{(1-D_2)T_s} \imath_{L_3}^2 dt}, \quad I_{D_3,rms} = I_0\sqrt{1-D_2}
\end{aligned}
$$

Similarly RMS currents $I_{c_1}, I_{c_2}, I_{c_3}$ and I_{c_4} through capacitors are given equations in Appendix A:

The equation $P_s^{con}=I_{s,rms}^2.r_{on}$ is used to compute the device conduction losses. Power loss is estimated by substituting the values of inductor currents, internal resistance, and duty ratios:

$$\begin{aligned} I_{s_1,rms} &= 5.36A & I_{s_{11},rms} &= 5.72A & I_{s_2,rms} &= 4.97A \\ I_{D_1,rms} &= 3.20A & I_{D_{11},rms} &= 3.21A & I_{D_2,rms} &= 4.17A \\ I_{D_3,rms} &= 3.043A & D_1, D_{11} &= 50\% & D_2 &= 29.6\% \end{aligned}$$

The r_{on} of MOSFET and diode are 45 mΩ and 40 mΩ, respectively. For that conduction, losses are

$$\begin{aligned} P_{s_1} &= 1.415W & P_{s_{11}} &= 1.510W & P_{s_2} &= 0.816W \\ P_{D_1} &= 1.10W & P_{D_{11}} &= 1.10W & P_{D_2} &= .695W \\ P_{D_3} &= .3704W \end{aligned}$$

The equation for switching loss calculation:

$$P_{sw}=\frac{1}{2}V_s.I_s(t_r+t_f)f_s$$

Switching loss is calculated by substituting average values of currents for switch ON and OFF periods.

$$\begin{aligned} I_{s_1} &= 5.40A & I_{s_{11}} &= 5.72A & I_{s_2} &= 10.1A \\ T_{on} &= 40nsec & T_{off} &= 115nsec & F_s &= 40KHz \end{aligned}$$

$$P_{s_1} = 4.20W \qquad P_{s_{11}} = 4.10W \qquad P_{s_2} = 10.3W$$

Power loss on passive component:

$$\begin{aligned} P_{L_1} &= 5.81W & P_{L_{11}} &= 5.78W & P_{L_2} &= 1.46W \\ P_{L_3} &= .396W & P_{C_1} &= .695W & P_{C_2} &= .3704W \\ P_{C_3} &= .3704W & P_{C_4} &= .3704W \end{aligned}$$

The efficiency is calculated as :

$$\eta = \frac{P_o}{P_o + P_{losses}}$$

Total $P_{losses} = 40.15$ W, when $P_o = 1000$ W. As a result, the proposed converter's efficiency at the rated load condition is 96.13%, and distribution losses are depicted in Figure 15.

4 | COMPARATIVE ANALYSIS

A detailed comparative analysis of the proposed converter and the recent high-gain converters is provided in Table 3. This analysis includes crucial performance metrics, including component count, voltage gain in CCM, voltage stress on power devices, and current stress on semiconductor devices (switches and diodes), as well as additional features such as efficiency, small signal order (SSO), and input current.

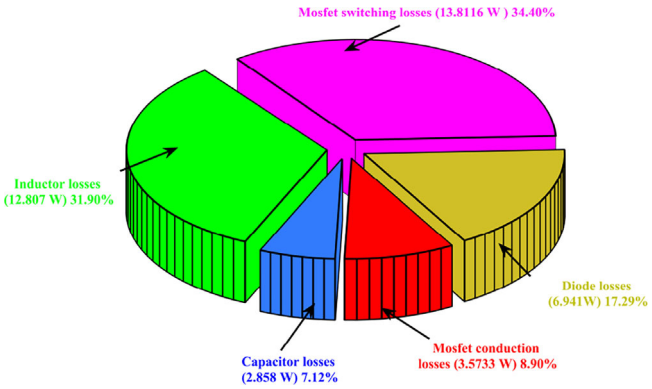

FIGURE 15 Percentage loss distribution of switches, diodes and passive components.

4.1 | Comparison of voltage gain

By using the gain formula provided in Table 3, a graph depicting the voltage gain versus duty cycle is plotted for different converters, including conventional boost converters. The proposed converter exhibits a high voltage gain in comparison to all converters. But only the converter in Alilou et al[15] shows better gain for less than 50% duty cycle as shown in graphical form Figure 16A. Table 3 indicates that topology in previous works[28,29] attain the same voltage gain as the proposed topologies, but topology in Shanthi et al[28] shares the same component count while exhibiting pulsating input current, and topology in Elsayad et al[29] utilizes more components to achieve the same gain.

4.2 | Comparison of voltage and current stress

Figure 16B makes it evident that the voltage stresses on switches in converters,[15,24,25,28] and Elsayad et al[29] are reduced when operating with duty cycles below 50%. However, when duty cycles exceed 50%, the proposed converter shows lower voltage stress compared to the other converters. Similarly, the normalized voltage stress across diodes, as shown in Figure 17A, indicates that converters in previous works[15,28] and Elsayad et al[29] experience lower voltage stress across diodes at duty cycles below 50%. When duty cycles surpass 50%, the proposed converter shows lower voltage stress across the diode. Figure 17B illustrates the normalized current stress across the switch. Converters in the literature[22–24,26,27] and the boost converter exhibit lower current stress on the switch, but it is important to note that these converters also have lower gain when compared to the proposed converter.

5 | SIMULATION AND EXPERIMENTAL VERIFICATION AND DISCUSSION

5.1 | Simulation test

The proposed converter is validated through Matlab/Simulink with 40 V input supply, a duty cycle of S_1,=S_{11}= 50% and S_2 = 66.66% as shown in Figure 18B. The measured voltage gain is V_0/V_{in}=10. Figure 18A shows the current behavior I_{L1}, I_{L11} of both inductors. During mode-1 and mode-2, I_{L1} increase from 5.82A to 7.05A, while I_{L11} decreases from 7.05A to 5.82A. So the ripple content on the source side is minimized which improves the performance of FC. Figure 18C and Figure 19A show the simulated waveform result and depict voltage stress across switches and diodes in less compared to the output voltage. A new simulation was conducted with an imbalanced resistive load to assess how effectively the proposed converter can distribute power asymmetrically to the two poles in an unbalanced scenario. The circuit with a balanced load of 500Ω is initially considered for this simulation. For this test, resistance is of 500Ω distributed according to the output voltage [V_{co3}=260V, R_{O3}=300Ω], [V_{co4}=140V, R_{O4}=200Ω]. Suddenly, the

TABLE 3 Comparison of proposed topology with existing topologies.

Topology	S/D/L/C/TC	I.C. nature	O.P.	SSO	Gain	Switch stress	Diode stress	Switch current	Diode current	Efficiency @ 1 kW
Boost converter	1/1/1/1/4	Continuous	Unipolar	2	$\frac{1}{1-D}$	$V_S = V_0$	$V_D = V_0$	$I_S = \frac{I_0}{1-D}$	$I_D = I_0$	88%
Hybridization of Boost-cuk converter[22]	1/2/2/3/8	Continuous	Bipolar	5	$\frac{1+D}{1-D}$	$V_S = \frac{V_0}{1+D}$	$V_{D1,2} = \frac{V_0}{1+D}$	$I_S = \frac{2I_0}{1-D}$	$I_{D1,2} = \frac{I_0}{1-D}$	90.68%
Converter[23]	2/2/2/4/10	Continuous	Bipolar	6	$\frac{1+D}{1-D}$	$V_{S1,2} = \frac{V_0}{1+D}$	$V_{D1,2} = \frac{V_0}{1+D}$	$I_{S1,2} = \frac{I_0}{1-D}$	$I_{D1,2} = \frac{I_0}{1-D}$	94.18%
Combined cuk[26] +SEPIC converter	1/2/3/4/10	Continuous	Bipolar	7	$\frac{2D}{1-D}$	$V_S = \frac{V_0}{D}$	$V_D = \frac{(2-D)V_0}{2D}$	$I_S = \frac{2DI_0}{1-D}$	I_0	91.50%
Buck[27] boost based Zeta	1/2/3/4/10	Discontinuous	Unipolar	7	$\frac{2D}{1-D}$	$V_S = \frac{V_0}{2D}$	$V_{D1,2} = \frac{V_0}{2D}$ $V_{D0} = \frac{2V_0}{3+D}$	$I_S = \frac{2I_0}{1-D}$	$I_{D1,2} = \frac{I_0}{1-D}$	95.22%
Converter[25]	1/4/2/4/11	Continuous	Unipolar	6	$\frac{3+D}{2(1-D)}$	$V_S = \frac{2V_0}{3+D}$	$V_{D_{1,0}} = \frac{2V_0}{1+3D}$ $V_{D_{2,3}} = \frac{V_0}{3+D}$	$I_S = \frac{(3+D)I_o}{1-D}$	$I_D = \frac{(3+D)I_o}{1-D}$	92.13%
Converter[24]	1/3/3/5/12	Discontinuous	Unipolar	8	$\frac{3D}{1-D}$	$V_S = \frac{V_0+3}{3}$	$V_{D1,3} = \frac{V_0}{3D}$ $V_{D2} = \frac{(1-2D)V_0}{3D}$	$I_S = \frac{3I_0}{1-D}$	$I_{D1-3} = \frac{I_0}{1-D}$	94%
Converter[32]	2/7/4/1/14	Continuous	Unipolar	5	$\frac{1+3D}{1-D}$	$V_{S1,2} = \frac{1+D}{1+3D}$	$V_{D1-4} = \frac{DV_0}{1+3D}$ $V_{D5,6} = \frac{(1-D)V_0}{1+3D}$ $V_D = \frac{2(1+D)V_0}{1+3D}$	$I_{S1,2} = \frac{(2+D)I_0}{D(1-D)}$	$I_{D1-7} = \frac{I_0}{1-D}$	94.86%
Converter[15]	1/5/2/6/14	Pulsating	Bipolar	8	$\frac{3}{1-D}$	$V_S = \frac{V_0}{3}$	$V_{D1,2} = \frac{V_0}{3}$ $V_{D3,4,5} = \frac{V_0}{3}$	$I_S = \frac{(2+D)I_0}{D(1-D)}$	$I_{D1-5} = \frac{2I_0}{1-D}$	91.26%
Converter[28]	1/6/2/3/12	Pulsating	Unipolar	5	$\frac{2(1+D)}{1-D}$	$V_S = \frac{V_0}{2}$	$V_{D1-6} = \frac{V_0}{2}$	$I_S = \frac{2(1+D)I_0}{1-D}$	$I_{D1-3} = \frac{2I_0}{1-D}$ $I_{D3-6} = \frac{I_0}{1-D}$	91.05%
Converter[29]	1/5/3/7/16	Continuous	Unipolar	10	$\frac{2(1+D)}{1-D}$	$V_S = \frac{V_0}{2(1+D)}$	$V_{D1-5} = \frac{V_0}{2(1+D)}$	$I_S = \frac{(1+3D)I_0}{D(1-D)}$	$I_{D1-4} = \frac{I_0}{1-D}$ $I_{D5} = \frac{I_0}{D}$	96%
Proposed converter	2/3/3/4/12	Continuous	Bipolar	7	$\frac{2(1+D)}{1-D}$	$V_{S1} = \frac{(1-D)V_0}{1+D}$ $V_{S2} = \frac{V_0}{1+D}$	$V_{D_1} = \frac{(1-D)V_0}{1+D}$ $V_{D2,3} = \frac{V_0}{1+D}$	$I_{S1} = \frac{2(1+D)I_0}{(1-D)}$ $I_{S2} = \frac{(1+D)I_0}{(1-D)}$	$I_{D1} = \frac{2(1+D)I_0}{(1-D)}$ $I_{D2} = \frac{(1+D)I_0}{1-D}$ $I_{D3} = I_0$	96.13%

Note: Calculated % (analytical) efficiency for 1 kW load and operating switching frequency = 40 kHz.

Abbreviations: C, number of capacitor; D, number of diodes; D, duty cycle of converter; I.C. nature, input current nature; L, number of inductor; O.P., output polarity; S, number of switches; SSO, small signal order; TC, total count.

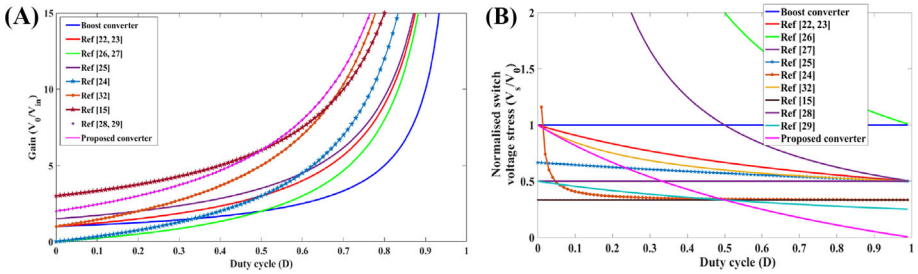

FIGURE 16 Comparison of proposed topology: (A) Voltage gain. (B) Switch voltage stresses.

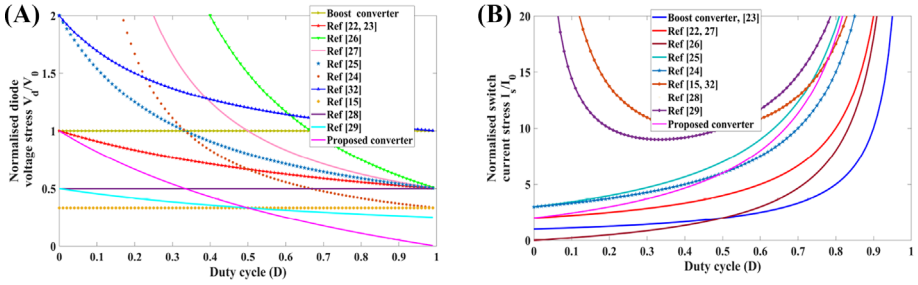

FIGURE 17 Comparison of proposed topology: (A) Diode voltage stresses. (B) Switch current stresses.

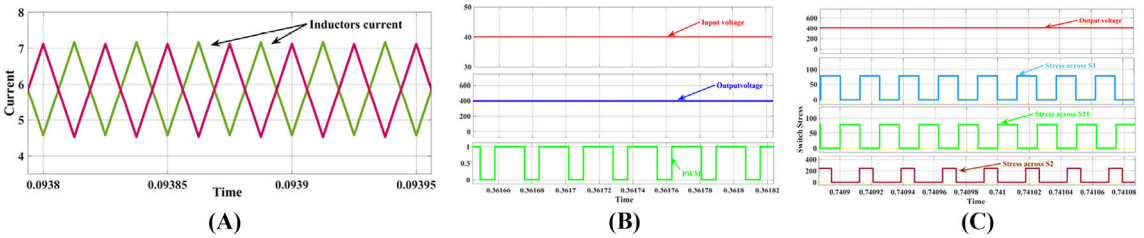

FIGURE 18 Matlab simulation based result. (A) Current ripple cancelation. (B) S_2 control duty to control the output voltage. (C) Voltage stress across switches S_1, S_{11} and S_2

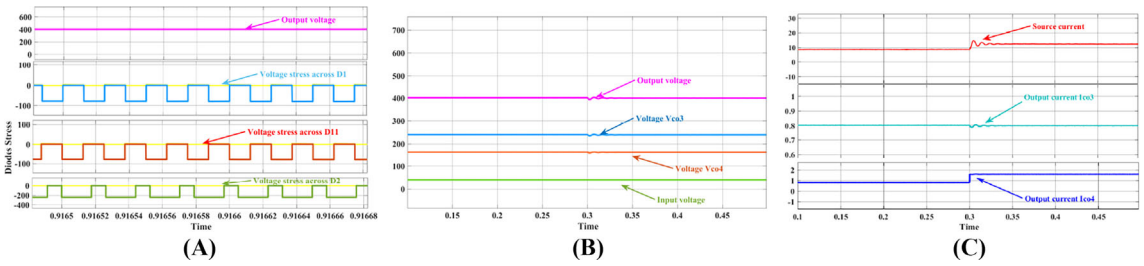

FIGURE 19 Simulation result. (A) Voltage stress across diodes D_1, D_{11} and D_2. (B) The input (V_i) and output (V_o, V_{Co3} and V_{Co4}) voltages during a simulation of a sudden shift in the load of the negative pole. (C) Waveforms for the output currents (i_{o3} and i_{o4}) in a simulation for a scenario where the load on the negative pole changes.

resistance attached to the negative pole is changed to 100Ω, leading to an imbalance in the circuit's output as shown in Figure 19B,C. This result demonstrates that the output pole voltages stay balanced even when the load becomes unbalanced.[36]

5.2 | Experimental test

The prototype of the proposed converter is designed and developed as shown in Figure 20. The specification of switches S_1, S_{11} are STW56N60M2, which work on 50% opposite duty for ripple cancelation, and the diodes with specification BYV60W-600PT2 are selected for the hardware study. The parameters chosen for the hardware result are the same as the parameters for the simulation as given in Table 2 with device specification in Table 4. The DSP-TMS320F28379D digital signal processor is used to produce the control signals.

The proposed converter was experimentally verified in the following cases:

5.2.1 | Case [1]: High duty cycle (66.66%)

Figure 21A illustrates the inductor's current behavior. Here, 50% duty cycle is applied to both switch S_1, S_{11}. When S_1 is in "ON," I_{L_1} is charging and $I_{L_{11}}$ is discharging. For the remaining duty cycle, I_{L_1} is discharging and $I_{L_{11}}$ is charging this

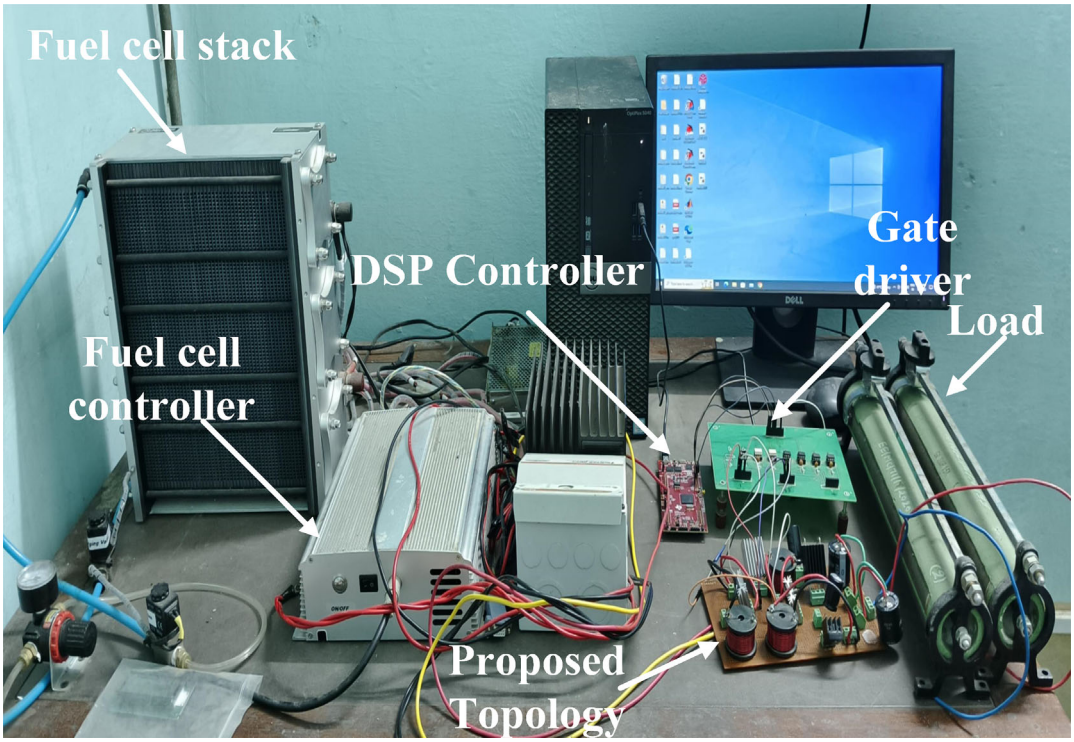

FIGURE 20 Experimental setup of fuel cell with proposed converter.

TABLE 4 Device specifications.

Component	Number	Specification
MOSFETs	2	STW56N60M2
Diodes	3	BYV60W-600PT2
Inductor	2	PCV-2-473-10
Inductor	1	PCV-2-564-08
Capacitor (C_1)	1	ECA2EHG220
Capacitor (C_2)	1	MCKSK400M101K32S
Capacitor (C_3), (C_4)	2	LGU2G181MELB
Fuel cell stack	1	FCS-C2000

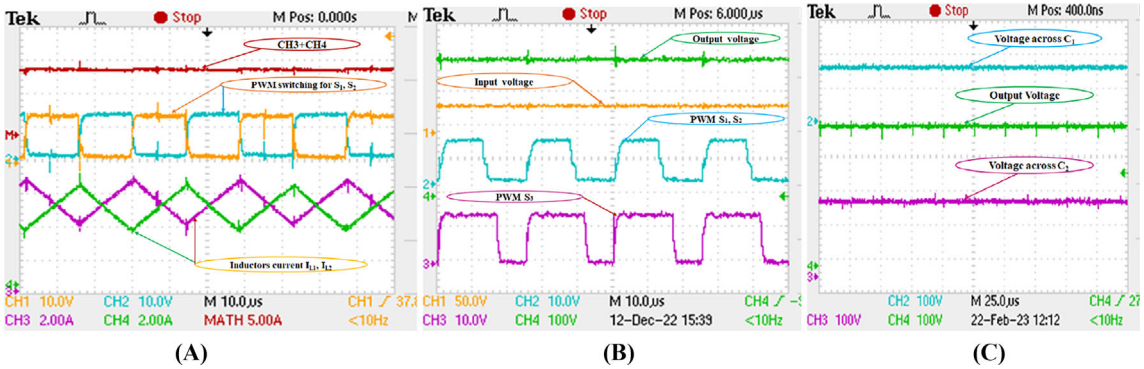

FIGURE 21 Experimental result. (A) Current ripple cancelation. (B) S_1 and S_2 fixed duty (ripple cancelation) and S_3 control duty to control the output voltage shown in channel CH4, input voltage shown in CH1. (C) CH3-capacitor voltage C_2, CH2-capacitor voltage C_1, CH4-Output voltage.

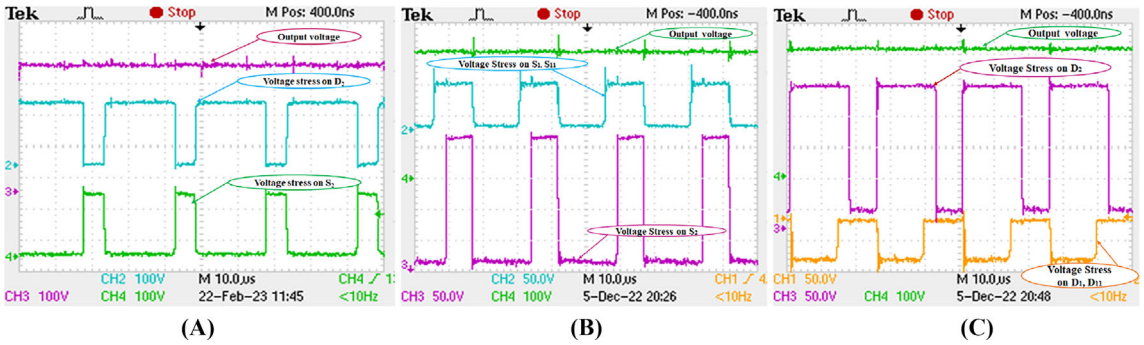

FIGURE 22 Experimental result show stress across switches and diodes in comparison of output voltage.

behavior almost cancels the ripple content in the input current which is shown in red color. Figure 21B shows the duty cycle of switch S_2 which is measured as 66.66%. For 40 V input, the obtained output voltage is 400 V which is nearly equal to the theoretical value given in Equation (28). Capacitors C_1 and C_2 voltage stress are measured as 160 V and 240 V, respectively, which are depicted in Figure 21C. Figure 22A shows voltage stress across switch S_2, and diode D_2 are measured as 240 V. Figure 22B shows voltage stress across remaining switches S_1 and S_{11} are measured as 40 V. In the same manner, Figure 22C measured voltage stress across diodes D_1 and $D_{11} = 80$ V. : Low duty cycle (29.6%)].

5.2.2 | Case [11]: Low duty cycle (29.6%)

The proposed converter examined for 1 kW power at 29.6% duty ratio. The corresponding waveforms are shown in Figure 23C. Inductor currents I_{L1}, I_{L11} have a peak-to-peak ripple value of 4.3 A, which is almost canceled in the input current ripple as shown in Figure 23A. Figure 23B shows voltage stress across switches and diodes.

Figure 24 shows the dynamic performance of the proposed converter when it is connected to 400 V DC grid, for t < 50 ms only the battery maintains the grid voltage. At t = 50 ms, the proposed converter connected to the grid and started feeding power to the stand-alone grid, input current, and voltage increased gradually and reached steady ≈ 250 ms. The further proposed converter is tested for sudden changes in load across the pole voltage V_{co4}. For this test, resistance of 500Ω distributed according to the output voltage [V_{co3} =260 V, R_{co3} =300 Ω], [V_{co4}=140V, R_{co4}=200Ω]. Figure 25 shows the grid voltage maintains balanced voltage under unbalanced load conditions (negative pole load changed from 200 Ω to 100 Ω). The theoretical and measured efficiency of the proposed converter is observed by changing load power from 200 W to 1.4 kW. At 1 kW load power, theoretical and measured efficiencies are achieved at a maximum value of 96.13% and 96%, respectively, as shown in Figure 26.

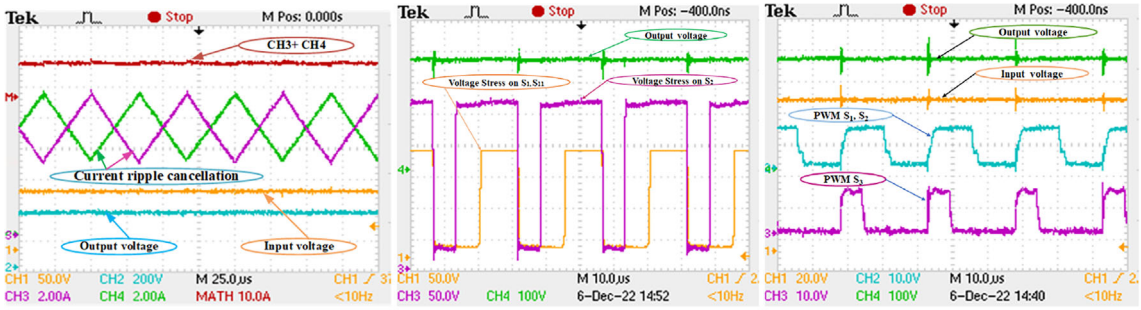

FIGURE 23 Experimental result of the proposed converter at 1 kW. (A) Current ripple cancelation. (B) Voltage stress across switches S_1, S_{11} and S_2, input voltage shown in CH1. (C) CH4-output, CH2, and CH3 show duty cycle.

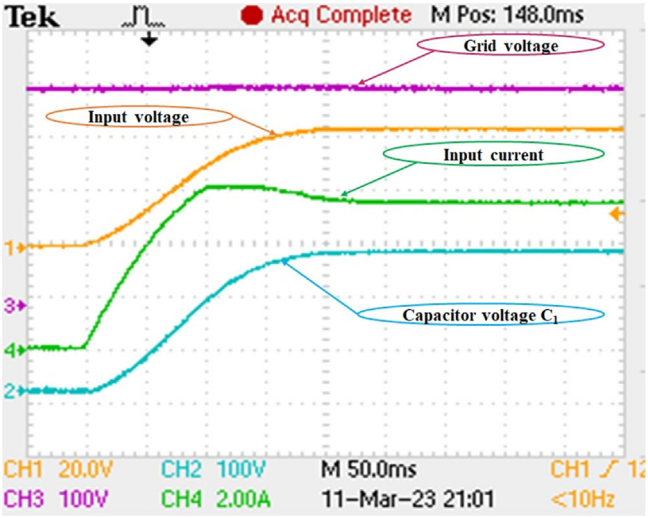

FIGURE 24 Dynamics of fuel cell connected with grid system.

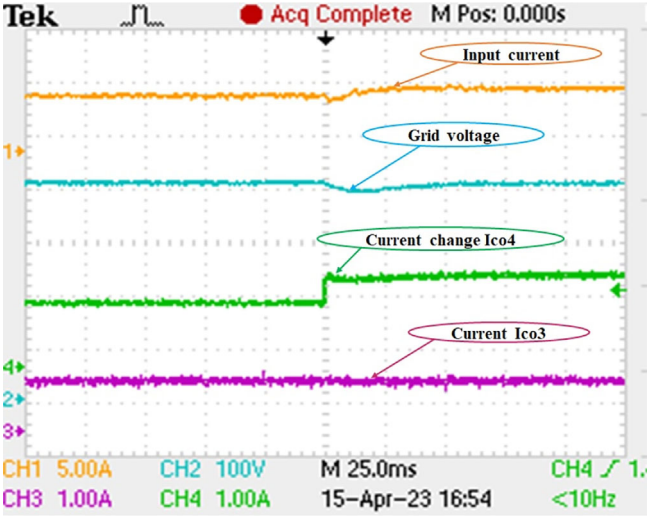

FIGURE 25 Waveforms for the output currents (i_{o3} and i_{o4}) scenario where the load on the negative pole changes.

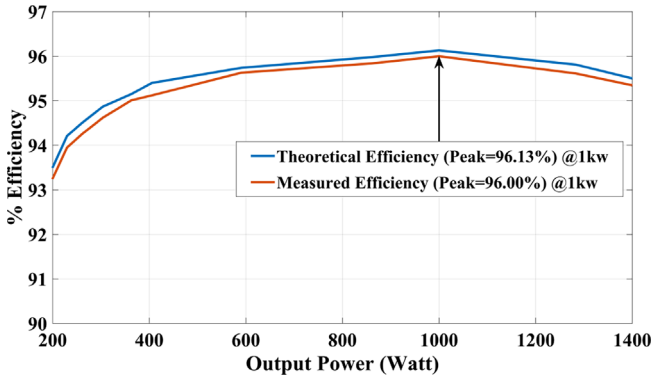

FIGURE 26 Efficiency curve with output power.

6 | CONCLUSION

The continuous ripple-free input current and high voltage gain are essential requirements for FC integration with a DC microgrid. This paper presents a high-gain DC-DC converter with reduced ripple in source current and reduced voltage stress across the devices. This proposed topology is suitable for transformerless grid-connect fuel cell generator systems to DC microgrids. This analysis covers the 1 kW output power and the voltage gain of 40/400 volts under continuous conduction mode (CCM). It explores the steady-state analysis and comprehensive comparisons. The proposed converter's operation is validated by using a Matlab/Simulink and experimental results. Compared to the existing converters, the proposed topology has low voltage stress on switches and diodes. The theoretical and measured efficiency of the proposed converter is observed by changing load power from 200 W to 1.4 kW. At 1 kW load power, theoretical and measured efficiencies are achieved at a maximum value of 96.13% and 96%, respectively. The results obtained confirm the converter's suitability for integrating FC output into an isolated DC microgrid.

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APPENDIX A

Apply KCL on Capacitor C_1

$$\left.\begin{aligned} &i_{C_1(Mode-1)} \times D_2 T_s + i_{C_1(Mode-2)} \times (D_1 - D_2) T_s + i_{C_1(Mode-3)} \times (1 - D_1) T_s = 0 \\ &i_{C_2(Mode-1)} \times D_2 T_s + i_{C_2(Mode-2)} \times (D_1 - D_2) T_s + i_{C_2(Mode-3)} \times (1 - D_1) T_s = 0 \\ &i_{C_3(Mode-1)} \times D_2 T_s + i_{C_3(Mode-2)} \times (D_1 - D_2) T_s + i_{C_3(Mode-3)} \times (1 - D_1) T_s = 0 \\ &i_{C_4(Mode-1)} \times D_2 T_s + i_{C_4(Mode-2)} \times (D_1 - D_2) T_s + i_{C_4(Mode-3)} \times (1 - D_1) T_s = 0 \end{aligned}\right\} \tag{A1}$$

where D is the duty cycle and T_s is the switching period.

Apply KCL on Equations (5), (11), and (19)

$$i_{C_1(Mode-1)} \times D_2 T_s + i_{C_1(Mode-2)} \times (D_1 - D_2) T_s + i_{C_1(Mode-3)} \times (1 - D_1) T_s = 0 \tag{A2}$$

$$i_{L_2} \times D_2 T_s + i_{L_2} \times (D_1 - D_2) T_s + (i_{L_2 - i_{L_1}}) \times (1 - D_1) T_s = 0 \tag{A3}$$

$$I_{L_1} = \frac{I_{L_2}}{1 - D_1} \tag{A4}$$

$$I_{L_1} = \frac{(1 + D_2) I_0}{(1 - D_1)(1 - D_2)} \tag{A5}$$

$$i_{C_1(Mode-1)} \times D_2 T_s + i_{C_1(Mode-2)} \times (D_1 - D_2) T_s + i_{C_1(Mode-3)} \times (1 - D_1) T_s = 0 \tag{A6}$$

$$(-i_0 - i_{C_3} \times D_2 T_s + i_{L_2} \times (D_1 - D_2) T_s + i_{L_2 - L_1} \times (1 - D_1) T_s = 0 \tag{A7}$$

$$i_{C_1, Mode-1} = \frac{(1 + D_2) I_0}{1 - D_2} \tag{A8}$$

$$\left.\begin{aligned} i_{C_1, Mode-1} &= \frac{(1 + D_2) I_0}{1 - D_2}, & i_{C_2, Mode-1} &= -I_0 \\ i_{C_3, Mode-1} &= \frac{2 I_0}{1 - D_2}, & i_{C_4, Mode-1} &= \frac{4 I_0}{1 - D_2} \end{aligned}\right\} \tag{A9}$$

RMS current through capacitors for loss calculation:

$$I_{c_{1,2,3,4},rms} = \sqrt{\frac{1}{T_s}\int_0^{D_2T_s} \iota_{c_1{}^2_{(mode-1)}} + \int_{D_1T_s}^{D_2T_s} \iota_{c_1{}^2_{(mode-2)}} + \int_0^{1-D_1T_s} \iota_{c_1{}^2_{(mode-3)}} dt}$$

$$I_{c_1,rms} = \sqrt{\frac{((1+D_2)I_0)^2}{(1-D_2)^2}D_2 + \frac{((1+D_2)I_0)^2}{(1-D_2)^2}(D_1-D_2) + \frac{(((1+D_2)D_1)I_0)^2}{((1-D_2)(1-D_1))^2}(1-D_1)}$$

$$I_{c_2,rms} = \sqrt{(-I_0)^2D_2 + \frac{(D_2I_0)^2}{(D_1-D_2)^2}(D_1-D_2) + \frac{(I_0D_1)^2}{(D_1-D_2)^2}(1-D_1)}$$

$$I_{c_3,rms} = \sqrt{\frac{(2I_0)^2}{(1-D_2)^2}D_2 + \frac{(2I_0D_2)^2}{(1-D_2(D_1-D_2))^2}(D_1-D_2) + \frac{((4I_0D_2))^2}{((1-D_2)(1-D_1))^2}(1-D_1)}$$

$$I_{c_4,rms} = \sqrt{\frac{(4I_0)^2}{(1-D_2)^2}D_2 + \frac{((1+3D_2)I_0)^2}{((D_1-D_2)(1-D_2))^2}(D_1-D_2) + \frac{(I_0)^2}{(1-D_1)^2}(1-D_1)}$$