CHAPTER 5

Single-Phase Enhanced High Gain SLC-ZSI

5.1 Introduction

Chapter 4 discusses two single-phase SLC-ZSIs for the single-stage AC system. Although the two SLC-ZSIs are capable of connecting low voltage DC sources to AC grid/loads through single-stage power conversion, they also have few disadvantages such as moderate ripple in input current and moderate voltage/current stresses on the elements. To take care of these issues, a single-phase enhanced high gain SLC-ZSI (eSLC-ZSI) is presented in this chapter for the single-stage AC system. The eSLC-ZSI is an improved version of Type 2 SLC-ZSI, by reorganizing elements between the input DC source and HB circuit with the addition of one capacitor and one diode to it. Detailed mathematical modeling of the eSLC-ZSI is carried out in this chapter. Simulation and experimental results are included in this chapter to investigate the performance of eSLC-ZSI.

5.2 Single-Phase eSLC-ZSI

Fig. 5.1 shows a proposed single-phase eSLC-ZSI [118]. As shown in Fig. 5.1, the eSLC-ZSI consists of one additional switch (S) along with HB circuit switches ($S_1 - S_4$), five diodes ($D_1 - D_5$), two inductors ($L_1$and L_2), three capacitors ($C_1 - C_3$) and a second-order low pass filter (L_f and C_f) along with a resistive load (R_{ac})The salient features of eSLC-ZSI are as follows.

- The eSLC-ZSI has higher voltage gain at low values of D_{st} as compared to SLC-ZSIs.
- It has continuous input current with lesser ripple at lower values of passive elements as compared to SLC-ZSIs.
- It gives high gain inversion at reduced harmonic distortion similar to SLC-ZSIs.
- It has lesser voltage/current stresses on the elements as compared to some reported high gain ZSIs.
- As it has lesser number of elements and reduced energy storage elements, the volume of overall system is reduced which results in better power density.

As it is an improved version of the Type 2 SLC-ZSI, its operation is similar to SLC-ZSIs. The shoot-through period (i.e., D_{st}) of HB switches is the ON-period of S. Due to presence of L_1 at the input side, it gives continuous input current with less ripple as compared to SLC-ZSIs. It can be observed from Fig. 5.1 that the input DC source and HB circuit of eSLC-ZSI has a common ground terminal.

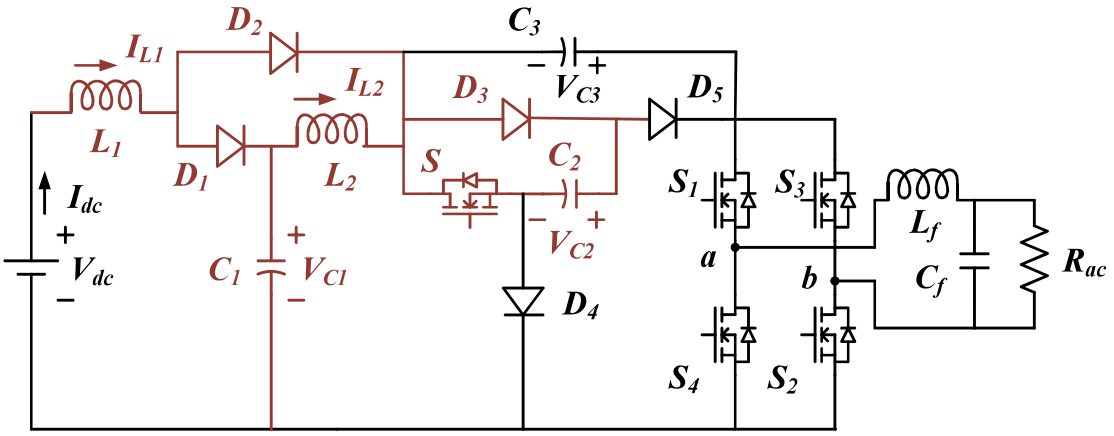


Fig. 5.1. A single-phase enhanced high gain SLC-ZSI.

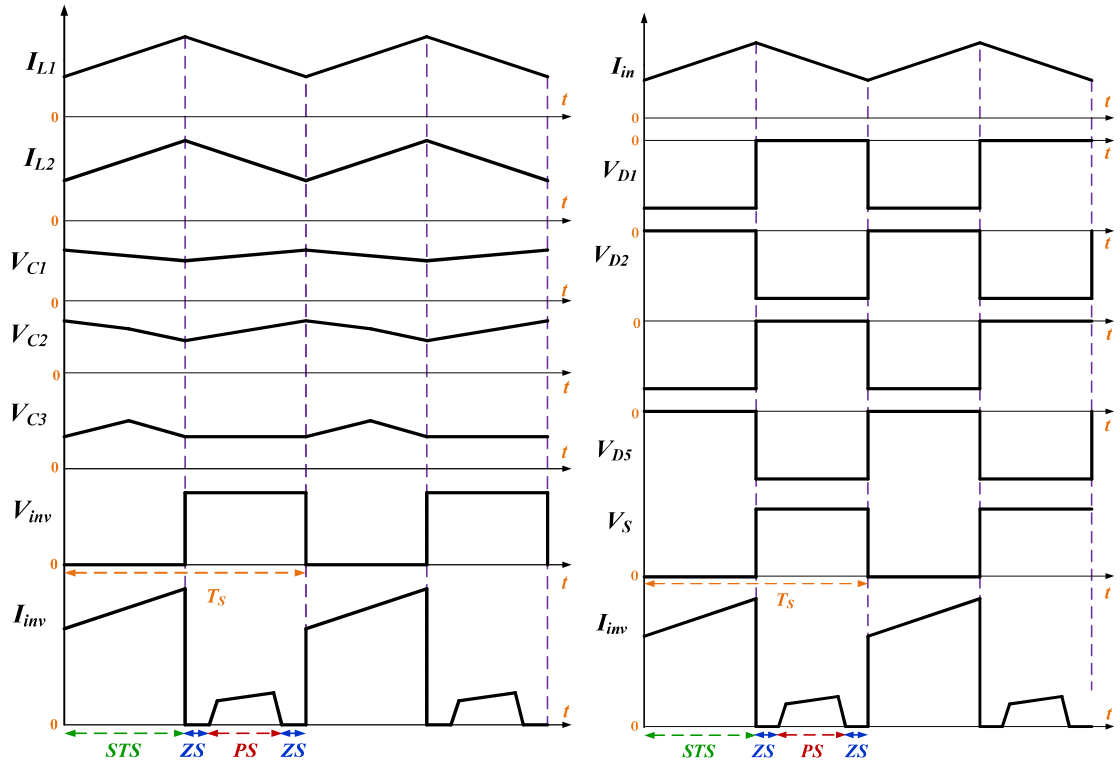


Fig. 5.2. Operating waveforms of eSLC-ZSI.

5.2.1 Operation of eSLC-ZSI

The operating waveforms of eSLC-ZSI are shown in Fig. 5.2. It can be observed from Fig. 5.2 that the eSLC-ZSI has three operating states (power, shoot-through, and zero states). However, the operation of eSLC-ZSI in the three states can be explained in two operating modes; shoot-through and non-shoot-through operations similar to SLC-ZSIs. The non-shoot-through operation consists of power and zero states (PS and ZS). Further, the non-shoot-through operation of eSLC-ZSI is same as that of conventional VSI for giving AC output. The shoot-through operation consists of shoot-through state (STS) only, which is used to boost the input DC voltage for achieving high gain AC output. For investigating the operation of eSLC-ZSI easily, the HB circuit ($S_1 - S_4$), $L_f C_f$ filter and R_{ac} of eSLC-ZSI are replaced by a parallel combination of a single switch S_{inv} and an equivalent resistance R_{eq}. The simplified circuit of eSLC-ZSI is shown in Fig. 5.3. Further, the switching period T_s of eSLC-ZSI is divided into two periods; shoot-through period ($D_{st}T_s$) and non-shoot-through period ($(1 - D_{st})T_S$).

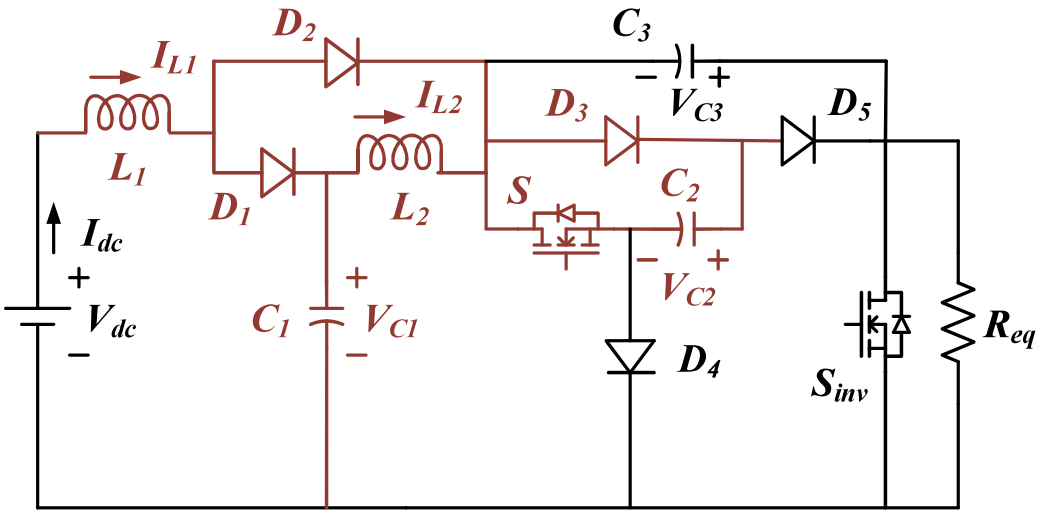


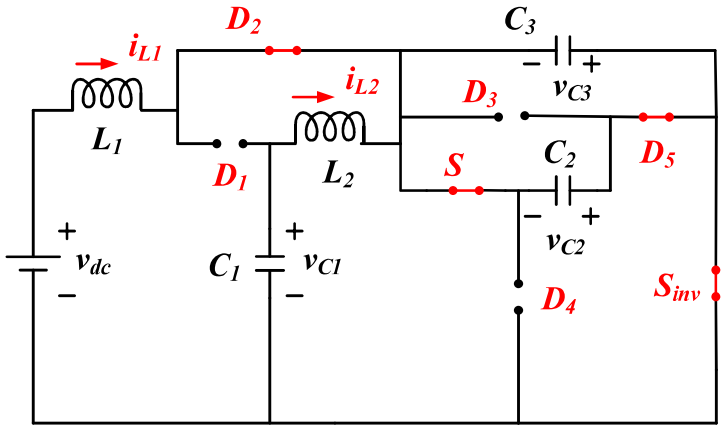
Fig. 5.3: Simplified circuit of eSLC-ZSI for investigating its operation.

(a) Shoot-Through Operation of eSLC-ZSI

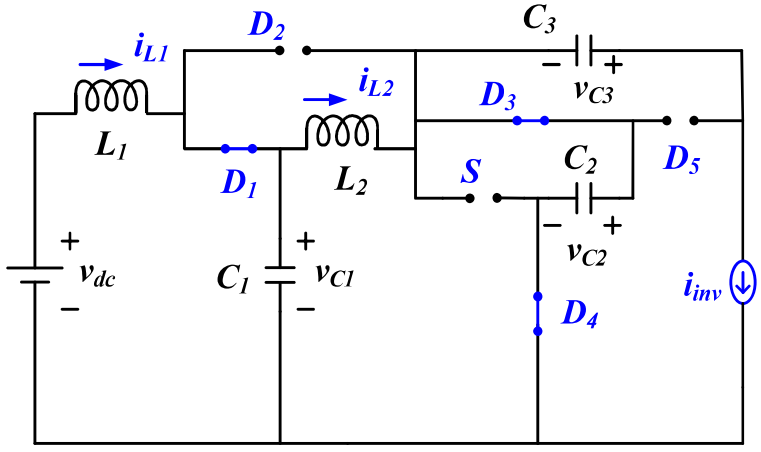
The equivalent circuit of eSLC-ZSI during shoot-through operation is shown in Fig. 5.4(a). The shoot-through operation (i.e., S_{inv} ON) is realized by turning-on of switches in the same leg of HB circuit at same instant. During this operation, S and S_{inv} are turned-on to achieve boosted voltage across the HB circuit. And the inductors (L_1 and L_2) are charged from the

input DC source and capacitors. The diodes (D_1, D_3 and D_4) are reverse biased and diodes (D_2 and D_5) are forward biased during this operation. Further, no power is transferred to AC load in this operation, but the switches experience a high value of shoot-through current. The KCL and KVL expressions of eSLC-ZSI during this operation are given in (5.1).

$$\left.\begin{aligned} v_{L1} = L_1\frac{di_{L1}}{dt} &= v_{dc} + v_{C2} \\ v_{L2} = L_2\frac{di_{L2}}{dt} &= v_{C1} + v_{C2} \\ v_{C2} &= v_{C3} \\ i_{C1} = C_1\frac{dv_{C1}}{dt} &= -i_{L2} \\ i_{C2} + i_{C3} = C_2\frac{dv_{C2}}{dt} + C_3\frac{dv_{C3}}{dt} &= -i_{L1} - i_{L2} \end{aligned}\right\} \quad (5.1)$$



(a)



(b)

Fig. 5.4. Equivalent circuits of eSLC-ZSI **(a)** during shoot-through operation **(b)** during non-shoot-through operation.

(b) Non-Shoot-Through Operation of eSLC-ZSI

The equivalent circuit of eSLC-ZSI during non-shoot-through operation is shown in Fig. 5.4(b). During this operation, S and S_{inv} are turned-off to allow load and circulating currents through HB switches. The inductors L_1 and L_2 discharge their stored energy into the capacitors and load. The diodes (D_1, D_3 and D_4) are forward biased and diodes (D_2 and D_5) are reverse biased during this operation. The KCL and KVL equations of eSLC-ZSI during this operation are given in (5.2).

$$\left.\begin{aligned} v_{L1} &= L_1 \frac{di_{L1}}{dt} = v_{dc} - v_{C1} \\ v_{L2} &= L_2 \frac{di_{L2}}{dt} = v_{C1} - v_{C2} \\ v_{inv} &= v_{C2} + v_{C3} \\ i_{C1} &= C_1 \frac{dv_{C1}}{dt} = i_{L1} - i_{L2} \\ i_{C2} &= C_2 \frac{dv_{C2}}{dt} = i_{L2} - i_{inv} \\ i_{C3} &= C_3 \frac{dv_{C3}}{dt} = -i_{inv} \end{aligned}\right\} \tag{5.2}$$

5.2.2 Steady-State Analysis of eSLC-ZSI

After applying volt-second balance principle of inductor to L_1, $\int_0^{D_{st}T_s} v_{L1}\, dt + \int_{DT_s}^{(1-D_{st})T_s} v_{L1}\, dt = 0$, the obtained steady-state relation is given in (5.3).

$$V_{dc} + D_{st}V_{C2} = V_{C1}(1 - D_{st}) \tag{5.3}$$

Similarly, by applying volt-second balance principle to L_2, the obtained steady-state relation is given in (5.4).

$$V_{C1} = V_{C2}(1 - 2D_{st}) \tag{5.4}$$

From (5.3) and (5.4), the obtained steady-state voltage across C_1 is given in (5.5).

$$V_{C1} = \frac{1-2D_{st}}{1-4D_{st}+2{D_{st}}^2} V_{dc} \tag{5.5}$$

From (5.4) and (5.5), the obtained steady-state voltage across C_2 is given in (5.6).

$$V_{C2} = \frac{1}{1-4D_{st}+2{D_{st}}^2} V_{dc} \tag{5.6}$$

From (5.1) and (5.6), the steady-state voltage across C_3 is derived and is given in (5.7).

$$V_{C3} = \frac{1}{1-4D_{st}+2{D_{st}}^2} V_{dc} \tag{5.7}$$

The voltage appearing across the HB circuit of eSLC-ZSI, V_{inv} is determined and is given in (5.8).

$$V_{inv} = V_{C2} + V_{C3} = \frac{2}{1-4D_{st}+2D_{st}^2} V_{dc} \tag{5.8}$$

The boosting ability, B of eSLC-ZSI can be written as given in (5.9).

$$B = \frac{V_{inv}}{V_{dc}} = \frac{2}{1-4D_{st}+2D_{st}^2} \tag{5.9}$$

The fundamental peak AC voltage ($V_{ac(pk)}$) of eSLC-ZSI can be written as given in (5.10).

$$V_{ac(pk)} = MV_{inv} = MBV_{dc} \tag{5.10}$$

The voltage gain, G of eSLC-ZSI can be written as given in (5.11).

$$G = \frac{V_{ac(pk)}}{V_{dc}} = MB = \frac{2M}{1-4D_{st}+2D_{st}^2} \tag{5.11}$$

Further, by applying charge-second balance principle of capacitor to C_1, $\int_0^{DT_s} i_{C1}\, dt + \int_{DT_s}^{(1-D)T_s} i_{C1}\, dt = 0$, the obtained steady-state relation is given in (5.12).

$$I_{L2} = (1 - D_{st})I_{L1} \tag{5.12}$$

Similarly, after applying charge-second balance to C_2 and C_3, the obtained steady-state relation is given in (5.13).

$$I_{L2}(1 - 2D_{st}) - I_{L1}(D_{st}) = 2(1 - D_{st})I_{inv} \tag{5.13}$$

From (5.12) and (5.13), the obtained steady-state average currents through L_1 and L_2 are given in (5.14).

$$\left.\begin{aligned} I_{L1} &= \frac{2(1-D_{st})}{1-4D_{st}+2D_{st}^2} I_{inv} \\ I_{L2} &= \frac{2(1-D_{st})^2}{1-4D_{st}+2D_{st}^2} I_{inv} \end{aligned}\right\} \tag{5.14}$$

where I_{inv} is current flowing through HB circuit of eSLC-ZSI and its expression is given in (5.15).

$$I_{inv} = \frac{1-4D_{st}+2D_{st}^2}{2(1-D_{st})} I_{dc} \tag{5.15}$$

The voltage gain of eSLC-ZSI is plotted based on an operating condition $D_{st} + M \leq 1$ (similar to SLC-ZSIs) and are shown in Fig. 5.5. As the D_{st} and M are interdependent and their relation is plotted as shown in Fig. 5.5(a). The relation among G, D_{st} and M of eSLC-ZSI is plotted in 3D-surface plot as shown in Fig. 5.5(b). The variation in G with respect to M and D_{st} are shown in Figs. 5.5(c) and 5.5(d) respectively.

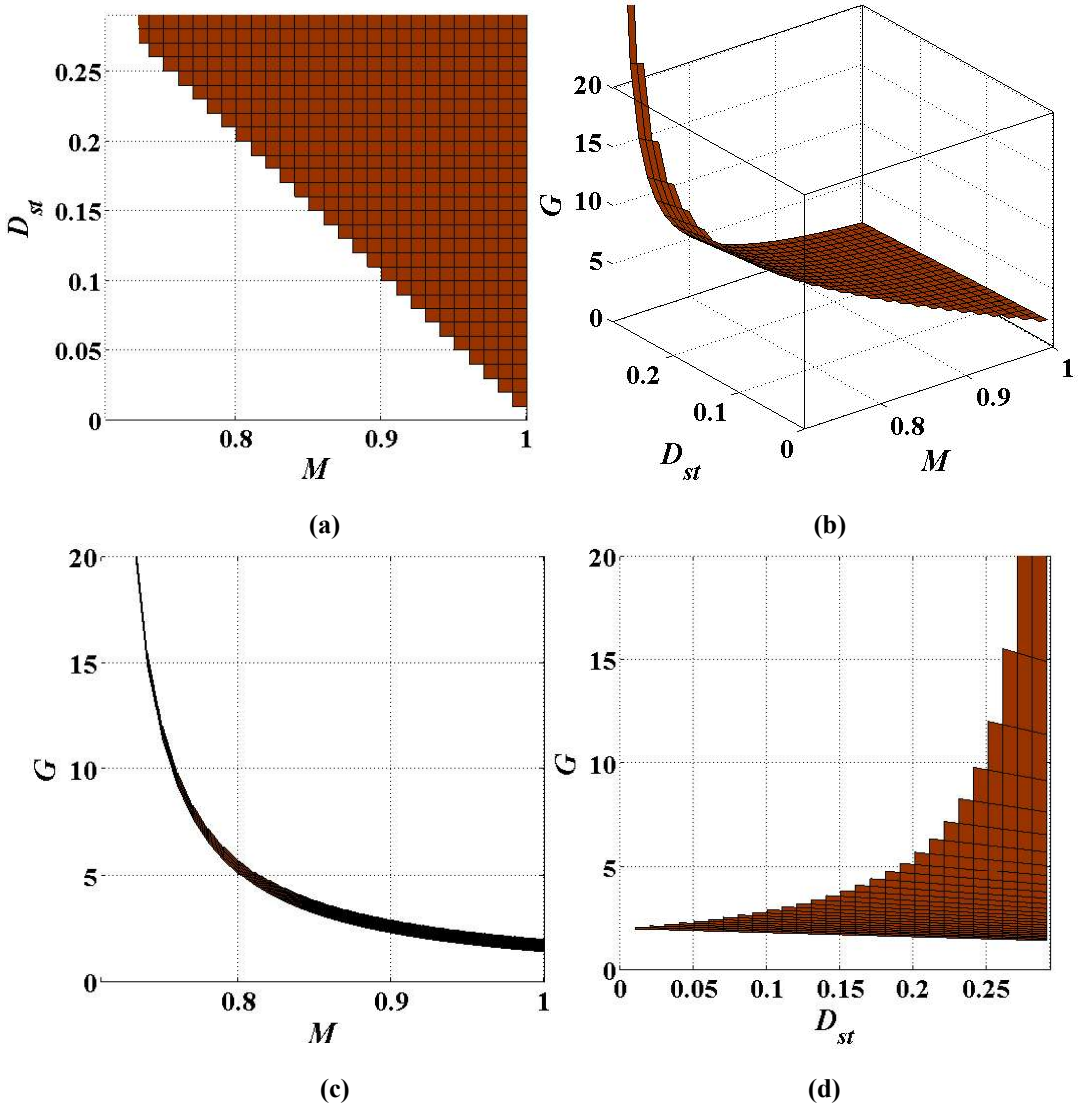
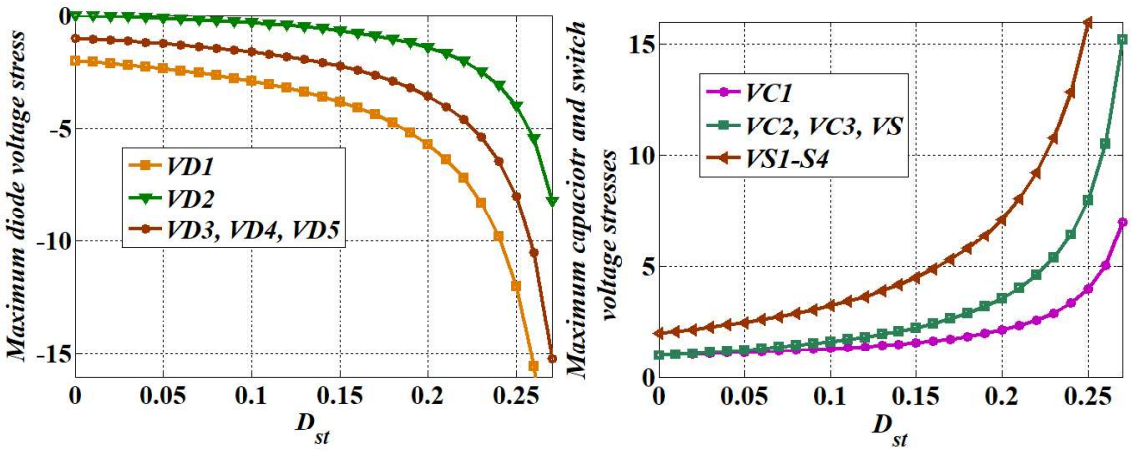


Fig. 5.5. Graphical representation of the correlation among G, D_{st} and M of eSLC-ZSI **(a)** D_{st} versus M **(b)** 3D-surface plot representing the relation among G, D_{st} and M **(c)** G versus M **(d)** G versus D_{st}.

The maximum current and voltage stresses on the elements of eSLC-ZSI are given in Table 5.1. The normalized (by V_{dc}) maximum voltage stresses are plotted with respect to D_{st} as shown in Fig. 5.6. The maximum voltage stresses on the diodes ($D_1 - D_5$) with respect to D_{st} is shown in Fig. 5.6(a). It can be observed from Fig. 5.6(a) that D_1 has higher voltage stress and D_2 has lesser voltage stress among all diodes of eSLC-ZSI. Fig. 5.6(b) shows maximum voltage stresses on the capacitors ($C_1 - C_3$) and switches (S and $S_1 - S_4$) with respect to D_{st}. It can be observed from Fig. 5.6(b) that the HB switches have higher voltage stress which is equal to boosting ability of eSLC-ZSI and the elements (S, C_2 and C_3) have equal voltage stress.

Table 5.1. Maximum voltage stresses on the elements of eSLC-ZSI.

	Maximum voltage stress
C_1	$\frac{(1-2D_{st})V_{dc}}{(1-4D_{st}+2{D_{st}}^2)}$
C_2	$\frac{V_{dc}}{(1-4D_{st}+2{D_{st}}^2)}$
C_3	$\frac{V_{dc}}{(1-4D_{st}+2{D_{st}}^2)}$
D_1	$\frac{(2-2D_{st})V_{dc}}{(1-4D_{st}+2{D_{st}}^2)}$
D_2	$\frac{(2D_{st})V_{dc}}{(1-4D_{st}+2{D_{st}}^2)}$
D_3	$\frac{V_{dc}}{(1-4D_{st}+2{D_{st}}^2)}$
D_4	$\frac{V_{dc}}{(1-4D_{st}+2{D_{st}}^2)}$
D_5	$\frac{V_{dc}}{(1-4D_{st}+2{D_{st}}^2)}$
S	$\frac{V_{dc}}{(1-4D_{st}+2{D_{st}}^2)}$
$S_1 - S_4$	$\frac{2V_{dc}}{(1-4D_{st}+2{D_{st}}^2)}$



(a) **(b)**

Fig. 5.6. Normalized maximum voltage stresses on the elements of eSLC-ZSI **(a)** voltage stresses on the diodes **(b)** voltage stresses on the capacitors and switches.

5.2.3 Design of Passive Elements of eSLC-ZSI

For CCM operation of eSLC-ZSI, minimum values of passive elements can be determined from the inequalities given in (5.16).

$$\left.\begin{aligned} L_1 &\geq \frac{(2-4D_{st}+2{D_{st}}^2)D_{st}T_S V_{dc}}{(x_{I_{L_1}}\%)(1-4D_{st}+2{D_{st}}^2)I_{dc}} \\ L_2 &\geq \frac{2D_{st}T_S V_{dc}}{(x_{I_{L_1}}\%)(1-4D_{st}+2{D_{st}}^2)I_{dc}} \\ C_1 &\geq \frac{D_{st}(1-D_{st})(1-4D_{st}+2{D_{st}}^2)T_S I_{dc}}{(x_{V_{C1}}\%)(1-2D_{st})V_{dc}} \\ C_2 &\geq \frac{I_{dc}(1-4D_{st}+2{D_{st}}^2)T_S}{(x_{V_{C2}}\%)2V_{dc}} \\ C_3 &\geq \frac{(1-4D_{st}+2{D_{st}}^2)^2 T_S I_{dc}}{(x_{V_{C3}}\%)2V_{dc}} \end{aligned}\right\} \quad (5.16)$$

where $x_{I_{L1}}\%$ and $x_{I_{L2}}\%$ are percentage ripple in inductor currents; $x_{V_{C1}}\%, x_{V_{C2}}\%$ and $x_{V_{C3}}\%$ are percentage ripple in capacitor voltages; T_S is the switching period; V_{dc} is the input voltage and I_{dc} is the input current.

The ripple in inductor currents (ΔI_L) of eSLC-ZSI can be calculated from the expression given in (5.17).

$$\Delta I_L = \int_0^{D_{st}T_s} \frac{di_L}{dt}\,dt \quad (5.17)$$

By using (5.17), the obtained ripples in inductor currents are given in (5.18).

$$\left.\begin{aligned} \Delta I_{L1} &= \frac{V_{L1}}{L_1} D_{st}T_s \\ \Delta I_{L2} &= \frac{V_{L2}}{L_2} D_{st}T_s \end{aligned}\right\} \quad (5.18)$$

where V_{L1} and V_{L2} are voltages across L_1 and L_2 during shoot-through period, $D_{st}T_s$.

The ripple in capacitor voltages (ΔV_C) of eSLC-ZSI can be determined from the expression given in (5.19).

$$\Delta V_C = \int_0^{D_{st}T_s} \frac{dV_C}{dt}\,dt \quad (5.19)$$

By using (5.19), the obtained ripples in capacitor voltages are given in (5.20).

$$\left.\begin{aligned} \Delta V_{C1} &= \frac{I_{C1}}{C_1} D_{st}T_s \\ \Delta V_{C2} &= \frac{I_{C2}}{C_2} D_{st}T_s \\ \Delta V_{C3} &= \frac{I_{C3}}{C_3} D_{st}T_s \end{aligned}\right\} \quad (5.20)$$

where $I_{C1,}I_{C2}$ and $I_{C3}$are currents through C_1, C_2 and C_3 during shoot-through period, $D_{st}T_s$.

Further, the design criteria of second-order low-pass filter (C_f and L_f) which gives sinusoidal AC output across load terminals, is discussed here. The cutoff frequency (f_c) of low-pass filter should be chosen one decade below switching frequency of eSLC-ZSI, to obtain a 40-dB attenuation for voltage components at switching frequency and unity gain at frequency of AC output. As per the said statements and assuming the value of C_f, value of L_f can be determined from the equation given in (5.21).

$$L_f = \frac{1}{(2\pi f_c)^2 C_f} \tag{5.21}$$

5.2.4 Modified Unipolar SPWM Technique of eSLC-ZSI

A modified unipolar SPWM technique is derived from conventional unipolar SPWM technique to operate the proposed eSLC-ZSI and it is similar to the SPWM technique of SLC-ZSIs [115]-[117]. Further, it has an operating condition $D_{st} + M \leq 1$. The SPWM technique of eSLC-ZSI is implemented in FPGA digital domain for generating gating pulses of eSLC-ZSI and its equivalent analog representation is shown in Fig. 5.7. It can be observed from Fig. 5.7(a) that the SPWM logic consists of modulating signal $V_m(t)$, constant signal (V_{st}) and carrier signal $V_{tr}(t)$ for generating gating pulses. The peak of $V_m(t)$ determines M, which decides fundamental peak AC output voltage of single-phase eSLC-ZSI. The value of V_{st} determines D_{st} of switches (S and $S_1 - S_4$), which decides equivalent DC voltage appeared across the HB circuit of eSLC-ZSI. The frequency of $V_{tr}(t)$ determines switching frequency of eSLC-ZSI. The gating pulses obtained by the SPWM logic are shown in Fig. 5.7(b). The relation among D_{st}, V_{st}, $V_{tr}(t)$ and M, $V_m(t)$, $V_{tr}(t)$ are given in (5.22).

$$\left.\begin{aligned} D_{st} &= 1 - \frac{V_{st}}{V_{tr}} \\ M &= \frac{V_m}{V_{tr}} \end{aligned}\right\} V_{st} \geq V_m \; and \; D_{st} + M \leq 1 \tag{5.22}$$

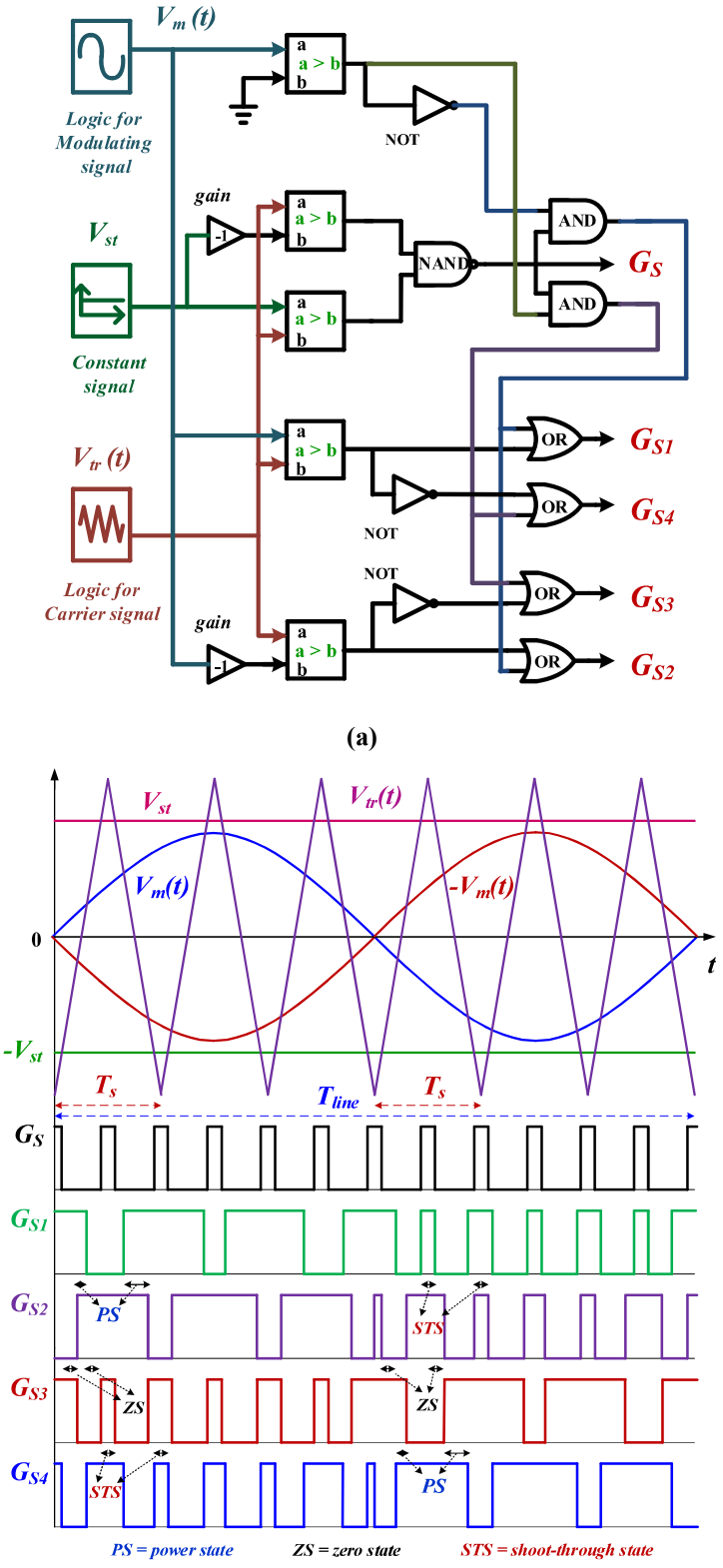
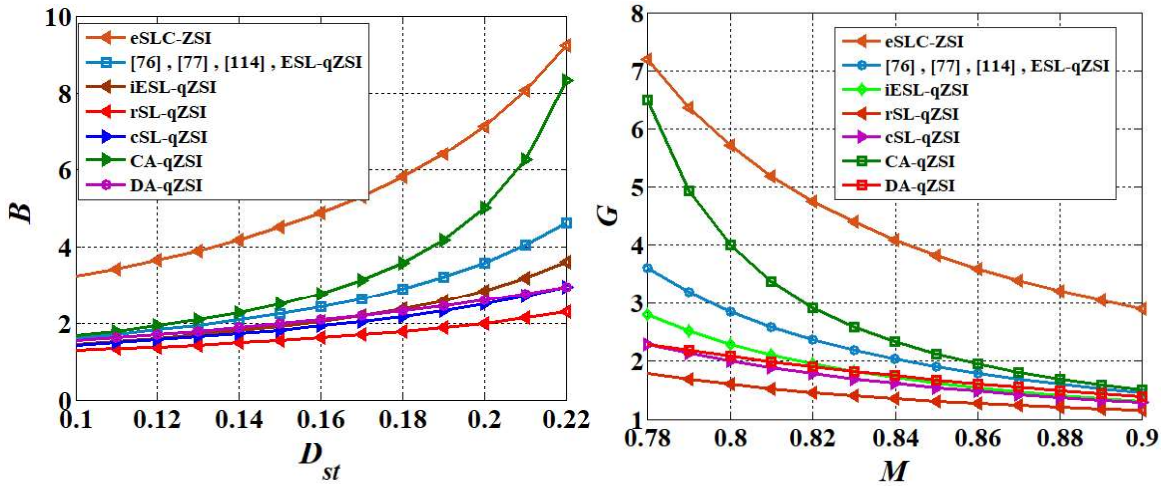
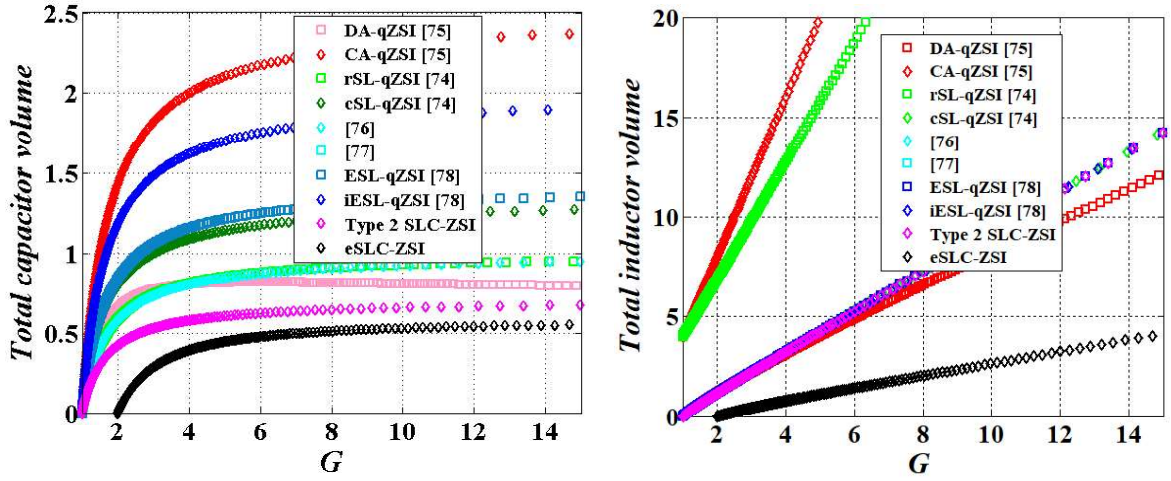


Fig. 5.7. Modified unipolar SPWM technique of eSLC-ZSI **(a)** analog representation of SPWM switching logic which is implemented in FPGA digital domain **(b)** gating pulses of eSLC-ZSI.



(a) (b)

Fig. 5.8. Boosting ability and voltage gain of eSLC-ZSI in comparison to some reported high gain ZSIs **(a)** B versus D_{st} **(b)** G versus M.



(a) (b)

Fig. 5.9. Comparison between eSLC-ZSI and reported ZSIs in terms of volume of energy storage elements **(a)** total volume of capacitors **(b)** total volume of inductors

5.3 Comparison Between eSLC-ZSI and Some Reported High Gain ZSIs

As stated earlier that B of eSLC-ZSI is decided by D_{st}, variation in B of eSLC-ZSI is plotted with respect to D_{st} in comparison to some reported high gain ZSIs [74]-[78], [114] and is shown in Fig. 5.8(a). It can be observed from Fig. 5.8(a) that the eSLC-ZSI has higher boosting ability as compared to reported ZSIs. Further, variation in G of eSLC-ZSI with respect to M is plotted under the operating condition $D_{st} + M \leq 1$ as compared to reported ZSIs. The

variation in G is shown in Fig. 5.8(b). It can be noticed from Fig. 5.8(b) that the eSLC-ZSI has higher voltage gain at higher values of M as compared to reported ZSIs.

Further, the comparison is extended in terms of a number of elements, input current ripple and voltage/current stresses on the elements. Table 5.2 gives a comparison in terms of number of elements and input current ripple along with the relations of B and M. It can be noticed from Table 5.2 that the eSLC-ZSI has two extra elements as compared to Type 2 SLC-ZSI [114] and lesser number of elements as compared to ZSIs [74]-[78] to achieve high voltage gain at low values of D_{st}. Also, Table 5.3 shows total voltage stresses on the elements (C, $Di.$ and $Sw.$) and Table 5.4 shows total current stresses on the elements (L, $Di.$ and $Sw.$) of eSLC-ZSI and reported ZSIs. The size of energy storage elements of eSLC-ZSI for analyzing their volume is plotted with respect to G as compared to reported ZSIs and its comparison is shown in Fig. 5.9. It can be observed from Fig. 5.9(a) that the total capacitor size of eSLC-ZSI is lesser than the reported ZSIs. Fig. 5.9(b) shows the total inductor size of eSLC-ZSI is lesser than the reported ZSIs. Hence, it can be concluded from Fig. 5.9 that the overall volume of eSLC-ZSI is lesser than the reported ZSIs. Further, voltage and current stresses on the elements of eSLC-ZSI and reported ZSIs are derived and are given in Tables 5.3 and 5.4, respectively. The stresses are plotted with respect to G as shown in Fig. 5.10. Moreover, the device voltage stresses of all ZSIs (eSLC-ZSI and reported ZSIs) are determined as a ratio of voltage appearing across them and equivalent DC voltage ($G.V_{in}$). Fig. 5.10(a) shows total capacitor voltage stress of all ZSIs with respect to G. It can be observed from Fig. 5.10(a) that the total capacitor voltage stress of eSLC-ZSI is greater than cSL-qZSI [74] and ESL-qZSI [78], and lesser than other ZSIs [75]-[78], [114]. Fig. 5.10(b) shows total diode voltage stress of all ZSIs with respect to G. As shown in Fig. 5.10(b), for the same G, the eSLC-ZSI has lesser diode voltage stress as compared to reported ZSIs. It can be noticed from Fig. 5.10(c) that total switch voltage stress of eSLC-ZSI is greater than ZSIs reported in [74]-[78], and lesser than ZSI reported in [75] and Type 2 SLC-ZSI [114]. The total inductor current stress of all ZSIs is shown in Fig. 5.10(d). As shown in Fig. 5.10(d), for the same G, the inductors of eSLC-ZSI experience lesser current stress as compared to ZSIs reported in [74]-[78], [114] and greater/equal current stress as compared to iESL-qZSI [78]. It can be observed from Fig. 5.10(e) that total diode current stress of eSLC-ZSI is lesser than ZSIs reported in [74], [76]-[78] and greater than ZSIs reported in [75], [114]. As shown in Fig. 5.10(f), the total switch

current stress of eSLC-ZSI is lesser than reported ZSIs. It can be concluded from Fig. 5.10 that the eSLC-ZSI has lesser device voltage and current stresses as compared to reported ZSIs, which results in economical prototype design.

Table 5.2. Comparison between proposed eSLC-ZSI and some reported high gain ZSIs.

ZSIs	***Sw.***	***Di.***	***L***	***C***	**Total elements**	**Boost factor *B***	**Voltage gain *G***	**Ripple in input current**
DA-qZSI [75]	4	5	4	4	17	$\frac{1}{1-4D_{st}+5{D_{st}}^2-2{D_{st}}^3}$	$\frac{1}{2M^2-M}$	low
CA-qZSI [75]	4	3	4	6	17	$\frac{1}{1-4D_{st}}$	$\frac{M}{4M-3}$	high
rSL-qZSI [74]	4	7	4	2	17	$\frac{1+D_{st}}{1-3D_{st}}$	$\frac{M^2}{3M-2}$	high
cSL-qZSI [74]	4	7	4	2	17	$\frac{1}{1-3D_{st}}$	$\frac{M}{3M-2}$	low
[76]	4	5	4	4	17	$\frac{1}{1-4D_{st}+2{D_{st}}^2}$	$\frac{M}{2M^2-1}$	very high
[77]	4	5	4	4	17	$\frac{1}{1-4D_{st}+2{D_{st}}^2}$	$\frac{M}{2M^2-1}$	very low
ESL-qZSI [78]	4	5	4	4	17	$\frac{1}{1-4D_{st}+2{D_{st}}^2}$	$\frac{M}{2M^2-1}$	low
iESL-qZSI [78]	4	5	4	4	17	$\frac{1-D_{st}}{1-4D_{st}+2{D_{st}}^2}$	$\frac{M^2}{2M^2-1}$	low
[114]	6	3	2	2	13	$\frac{1}{1-4D_{st}+2{D_{st}}^2}$	$\frac{M}{2M^2-1}$	high
Proposed eSLC-ZSI	5	5	2	3	15	$\frac{2}{1-4D_{st}+2{D_{st}}^2}$	$\frac{2M}{2M^2-1}$	very low

Note: $Sw.$ = switches, $Di.$ = diodes, L = inductors, C = capacitors

Table 5.3. Maximum total voltage stress on the elements (C, $Di.$ and $Sw.$) of eSLC-ZSI and reported ZSIs.

ZSIs	Total capacitor voltage stress	Total diode voltage stress	Total switch voltage stress
DA-qZSI [75]	$\frac{(2-3D_{st}+2{D_{st}}^2)V_{dc}}{1-4D_{st}+5{D_{st}}^2-2{D_{st}}^3}$	$\frac{3V_{dc}}{1-4D_{st}+5{D_{st}}^2-2{D_{st}}^3}$	$\frac{4V_{dc}}{1-4D_{st}+5{D_{st}}^2-2{D_{st}}^3}$
CA-qZSI [75]	$\frac{2-D_{st}}{1-4D_{st}}V_{dc}$	$\frac{3V_{dc}}{1-4D_{st}}$	$\frac{4V_{dc}}{1-4D_{st}}$
rSL-qZSI [74]	$\frac{1+D_{st}}{1-3D_{st}}V_{dc}$	$\frac{3+3D_{st}}{1-3D_{st}}V_{dc}$	$\frac{4+4D_{st}}{1-3D_{st}}V_{dc}$
cSL-qZSI [74]	$\frac{1}{1-3D_{st}}V_{dc}$	$\frac{5+6D_{st}-2{D_{st}}^2+2{D_{st}}^3}{1-2D_{st}-3{D_{st}}^2}V_{dc}$	$\frac{4}{1-3D_{st}}V_{dc}$
[76]	$\frac{4-6D_{st}+2{D_{st}}^2}{1-4D_{st}+2{D_{st}}^2}V_{dc}$	$\frac{3V_{dc}}{1-4D_{st}+2{D_{st}}^2}$	$\frac{4V_{dc}}{1-4D_{st}+2{D_{st}}^2}$
[77]	$\frac{2-2D_{st}}{1-4D_{st}+2{D_{st}}^2}V_{dc}$	$\frac{3V_{dc}}{1-4D_{st}+2{D_{st}}^2}$	$\frac{4V_{dc}}{1-4D_{st}+2{D_{st}}^2}$
ESL-qZSI [78]	$\frac{1-2D_{st}}{1-4D_{st}+2{D_{st}}^2}V_{dc}$	$\frac{3V_{dc}}{1-4D_{st}+2{D_{st}}^2}$	$\frac{4V_{dc}}{1-4D_{st}+2{D_{st}}^2}$
iESL-qZSI [78]	$\frac{1}{1-4D_{st}+2{D_{st}}^2}V_{dc}$	$\frac{3-3D_{st}}{1-4D_{st}+2{D_{st}}^2}V_{dc}$	$\frac{4-4D_{st}}{1-4D_{st}+2{D_{st}}^2}V_{dc}$
[114]	$\frac{1+2D-2D^2}{1-4D_{st}+2{D_{st}}^2}V_{dc}$	$\frac{3}{1-4D_{st}+2{D_{st}}^2}V_{dc}$	$\frac{6}{1-4D_{st}+2{D_{st}}^2}V_{dc}$
Proposed eSLC-ZSI	$\frac{(3-2D)V_{dc}}{1-4D_{st}+2{D_{st}}^2}$	$\frac{5V_{dc}}{1-4D_{st}+2{D_{st}}^2}$	$\frac{9V_{dc}}{1-4D_{st}+2{D_{st}}^2}$

Table 5.4. Maximum total current stress on the elements ($Di.$, L, and $Sw.$) of eSLC-ZSI and reported ZSIs.

ZSIs	Total inductor current stress	Total diode current stress	Total switch current stress
DA-qZSI [75]	$\frac{4-5D_{st}+2{D_{st}}^2}{1-3D_{st}+2{D_{st}}^2}I_{inv}$	$\frac{(5-3D_{st})I_{inv}}{1-3D_{st}+2{D_{st}}^2}$	$\frac{16-20D_{st}+8{D_{st}}^2}{1-3D_{st}+2{D_{st}}^2}I_{inv}$
CA-qZSI [75]	$\frac{4-4D_{st}}{1-4D_{st}}I_{inv}$	$\frac{3-3D_{st}}{1-4D_{st}}I_{inv}$	$\frac{16-16D_{st}}{1-4D_{st}}I_{inv}$
rSL-qZSI [74]	$\frac{4-4D_{st}}{1-3D_{st}}I_{inv}$	$\frac{7-5D_{st}}{1-3D_{st}}I_{inv}$	$\frac{16-16D_{st}}{1-3D_{st}}I_{inv}$
cSL-qZSI [74]	$\frac{4-4D_{st}}{1-3D_{st}}I_{inv}$	$\frac{7-5D_{st}}{1-3D_{st}}I_{inv}$	$\frac{16-16D_{st}}{1-3D_{st}}I_{inv}$
[76]	$\frac{4-6D_{st}+2{D_{st}}^2}{1-4D_{st}+2{D_{st}}^2}I_{inv}$	$\frac{5-4D_{st}}{1-4D_{st}+2{D_{st}}^2}I_{inv}$	$\frac{16-24D_{st}+8{D_{st}}^2}{1-4D_{st}+2{D_{st}}^2}I_{inv}$
[77]	$\frac{4-6D_{st}+2{D_{st}}^2}{1-4D_{st}+2{D_{st}}^2}I_{inv}$	$\frac{5-4D_{st}}{1-4D_{st}+2{D_{st}}^2}I_{inv}$	$\frac{16-24D_{st}+8{D_{st}}^2}{1-4D_{st}+2{D_{st}}^2}I_{inv}$
ESL-qZSI [78]	$\frac{4-6D_{st}+2{D_{st}}^2}{1-4D_{st}+2{D_{st}}^2}I_{inv}$	$\frac{5-4D_{st}}{1-4D_{st}+2{D_{st}}^2}I_{inv}$	$\frac{16-24D_{st}+8{D_{st}}^2}{1-4D_{st}+2{D_{st}}^2}I_{inv}$
iESL-qZSI [78]	$\frac{4-6D_{st}+2{D_{st}}^2}{1-4D_{st}+2{D_{st}}^2}I_{inv}$	$\frac{5-4D_{st}}{1-4D_{st}+2{D_{st}}^2}I_{inv}$	$\frac{16-24D_{st}+8{D_{st}}^2}{1-4D_{st}+2{D_{st}}^2}I_{inv}$
[114]	$\frac{2-3D_{st}+{D_{st}}^2}{1-4D_{st}+2{D_{st}}^2}I_{inv}$	$\frac{3-4D_{st}+{D_{st}}^2}{1-4D_{st}+2{D_{st}}^2}I_{inv}$	$\frac{10-13D_{st}+4{D_{st}}^2}{1-4D_{st}+2{D_{st}}^2}I_{inv}$
Proposed eSLC-ZSI	$\frac{4-6D_{st}+2{D_{st}}^2}{1-4D_{st}+2{D_{st}}^2}I_{inv}$	$\frac{10-10D_{st}+2{D_{st}}^2}{1-4D_{st}+2{D_{st}}^2}I_{inv}$	$\frac{8-12D_{st}+4{D_{st}}^2}{1-4D_{st}+2{D_{st}}^2}I_{inv}$

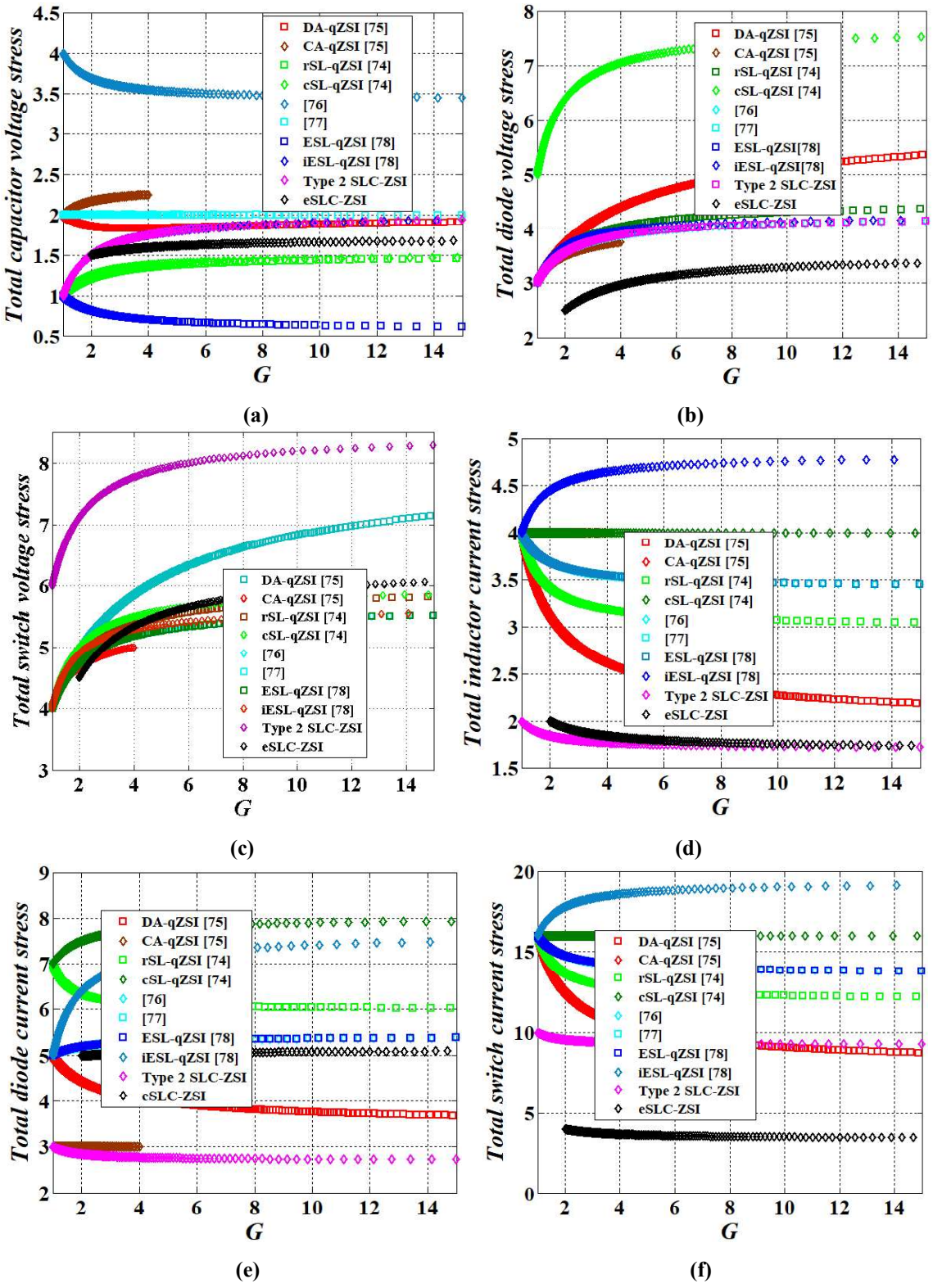


Fig. 5.10. Comparison between eSLC-ZSI and reported ZSIs in terms voltage and current stresses on the elements **(a)** total capacitor voltage stress **(b)** total diode voltage stress **(c)** total switch voltage stress **(d)** total inductor current stress **(e)** total diode current stress **(f)** total switch current stress.

5.3.1 Analysis of Ripple in Input Current and Capacitor Voltages of eSLC-ZSI as compared to Type 2 SLC-ZSI

The ripple in input current and capacitor voltages of eSLC-ZSI is determined and compared over Type 2 SLC-ZSI. The input current ripple of eSLC-ZSI and Type 2 SLC-ZSI is determined based on the procedure given in [78]. In the Type 2 SLC-ZSI, the input current is shared between two inductors during $D_{st}T_s$ period and is determined as given in (5.23).

$$\Delta i \cong \Delta i_{L1} + \Delta i_{L2} \cong \frac{D_{st}(2-4D_{st}+2{D_{st}}^2)T_s V_{inv}}{L_1} + \frac{2D_{st}(1-D_{st})T_s V_{inv}}{L_2} \tag{5.23}$$

The input current ripple of eSLC-ZSI is equal to ripple in L_1 only and it is determined during $D_{st}T_s$ period as given in (5.24).

$$\Delta i \cong \Delta i_{L1} \cong \frac{D_{st}(2-4D_{st}+2{D_{st}}^2)T_s V_{inv}}{L_1} \tag{5.24}$$

To compare the input current ripple of eSLC-ZSI and Type 2 SLC-ZSI, an input current ripple factor $rf_{in} = \frac{L\,\Delta i}{V_{inv}T_s}$ is considered. Fig. 5.11 shows variation in ripple factor (rf_{in}) with respect to D_{st}. It can be observed from Fig. 5.11 that input current ripple of eSLC-ZSI is lesser than Type 2 SLC-ZSI.

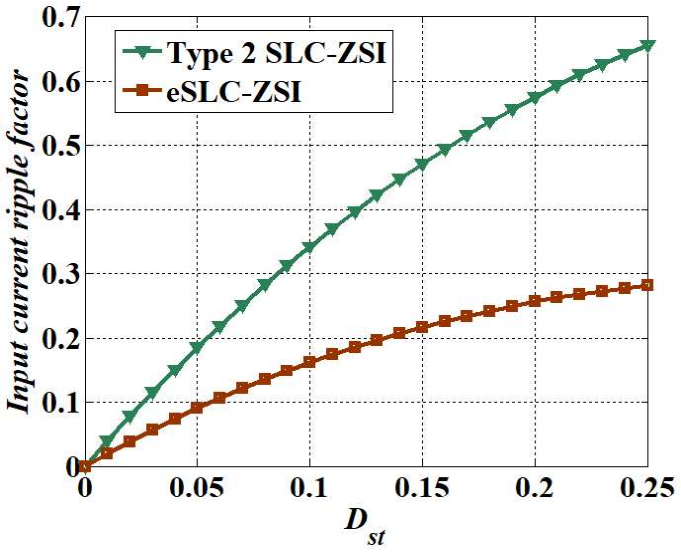


Fig. 5.11. Variation in input current ripple factor, $rf_{in} = \frac{L\,\Delta i}{V_{inv}T_s}$ with respect to D_{st}.

Further, the capacitor voltage ripples of eSLC-ZSI are determined and are given in (5.25).

$$\left.\begin{aligned}\Delta v_{C1} &= \frac{(1-2D_{st}+{D_{st}}^2)I_{dc}T_s}{C_1}\\ \Delta v_{C2} &= \frac{(1)I_{dc}T_s}{2C_2}\\ \Delta v_{C3} &= \frac{(1-4D_{st}+2{D_{st}}^2)I_{dc}T_s}{2C_3}\end{aligned}\right\} \tag{5.25}$$

Similarly, the capacitor voltage ripples of Type 2 SLC-ZSI are determined and are given in (5.26).

$$\left.\begin{aligned}\Delta v_{C1} &= \frac{(D-D^2)I_{dc}T_s}{C_1}\\ \Delta v_{C2} &= \frac{(2D-D^2)I_{dc}T_s}{C_2}\end{aligned}\right\} \tag{5.26}$$

To compare capacitor voltage ripples of eSLC-ZSI and Type 2 SLC-ZSI, a capacitor voltage ripple factor $rf_C = \frac{C\,\Delta v_C}{i_{dc}T_s}$ is considered. Fig. 5.12 show variation in ripple factor (rf_C) with respect to D_{st}. It can be observed from Fig. 5.12 that capacitor voltage ripple factors of eSLC-ZSI are marginally higher at low values of D_{st} as compared to Type 2 SLC-ZSI. However, the capacitor voltage ripple factors of eSLC-ZSI are gradually decreasing as D_{st} increases whereas the capacitor voltage ripple factors of Type 2 SLC-ZSI are increasing as D_{st} increases.

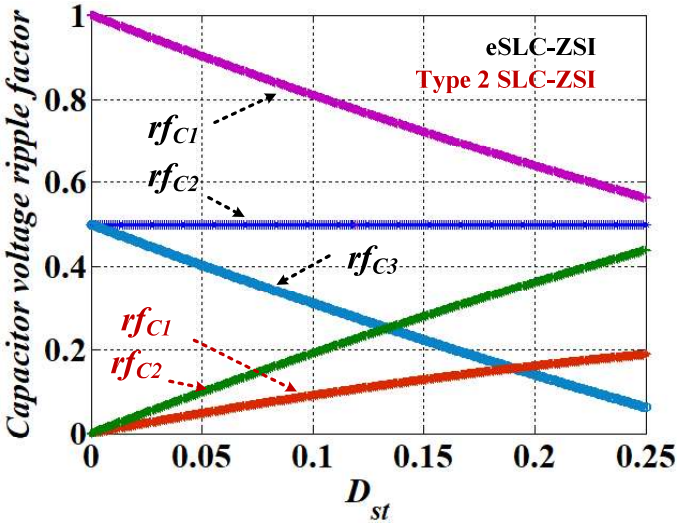


Fig. 5.12. Variation in capacitor voltage ripple factor, $rf_C = \frac{C\,\Delta v}{i_{dc}T_s}$ with respect to D_{st}.

Table 5.5. Operating conditions and list of parameters for the validation of eSLC-ZSI.

Parameter	Value
Input voltage (V_{dc})	48 V
Output power (P_{ac})	250 W
Shoot-through duty ratio (D_{st})	0.2
Modulation index (M)	0.78
Line frequency (f_{line})	50 Hz
Switching frequency (f_s)	20 kHz
Inductor (L_1)	1120 uH
Inductor (L_2)	2240 uH
Capacitor (C_1)	470 µF
Capacitor (C_2)	1800 µF
Capacitor (C_3)	2200 µF
AC filter inductor (L_f)	2 mH
AC filter capacitor (C_f)	10 µF

5. 4 Verification of eSLC-ZSI

The performance of eSLC-ZSI is verified through simulation and experimental results for the operating conditions given in Table 5.5.

5.4.1 Simulation Results of eSLC-ZSI

Simulation studies are carried out at ideal conditions of elements of eSLC-ZSI. Fig. 5.13 shows simulation results of eSLC-ZSI at $D_{st} = 0.2$ and $M = 0.78$ for R load. Further, Y-axis of Fig. 5.13 has voltage/current values having units "V" or "A" and X-axis of Fig. 5.13 has time values having a unit "s". It can be observed from Fig. 5.13(a) that voltages across capacitors are $V_{C1} = 102.85$ V, $V_{C2} = 171.42$ V and $V_{C3} = 171.42$ for an input voltage $V_{dc} =$ 48 V. It can be observed from Fig. 5.13(a) that C_2 and C_3 have equal voltages. Fig. 5.13(b) shows voltage appearing across the HB circuit of eSLC-ZSI as $V_{inv} = 342.85$ V, AC output voltage without filtering as $V_{ab(pk)} = 342.85$ V and fundamental AC output voltage as $V_{ac(rms)} = 189.1$ V along with V_{dc}. Also, THD of AC output voltage is obtained as 1.66% by using THD measurement block of PSIM simulation software. As shown in Fig. 5.13(c), fundamental AC output current as $I_{ac(rms)} = 1.32$ A along with V_{inv}, V_{ac} and V_{dc}. Fig. 5.13(d)

shows average currents flowing through inductors are $I_{L1} = 5.48$ A and $I_{L2} = 4.37$ A. The voltages experienced by power semiconductor devices of eSLC-ZSI are shown in Figs. 5.13(e) and 5.13(f). It can be noticed from Fig. 5.13(e) that maximum voltage stresses across the diodes (D_1, D_2 and D_3) are $V_{D1} = -274.28$ V, $V_{D2} = -68.57$ V and $V_{D3} = -171.42$ V along with V_{dc}. Fig. 5.13(f) shows maximum voltage stresses across the diodes (D_4, D_5 and S) are $V_{D4} = -171.42$ V, $V_{D5} = -171.42$ V and $V_S = 171.42$ V along with V_{dc}. It can be concluded that the devices (D_3, D_4, D_5 and S) have equal voltage stress as same as that of C_2 and D_2 has lesser voltage stress among all power semiconductor devices.

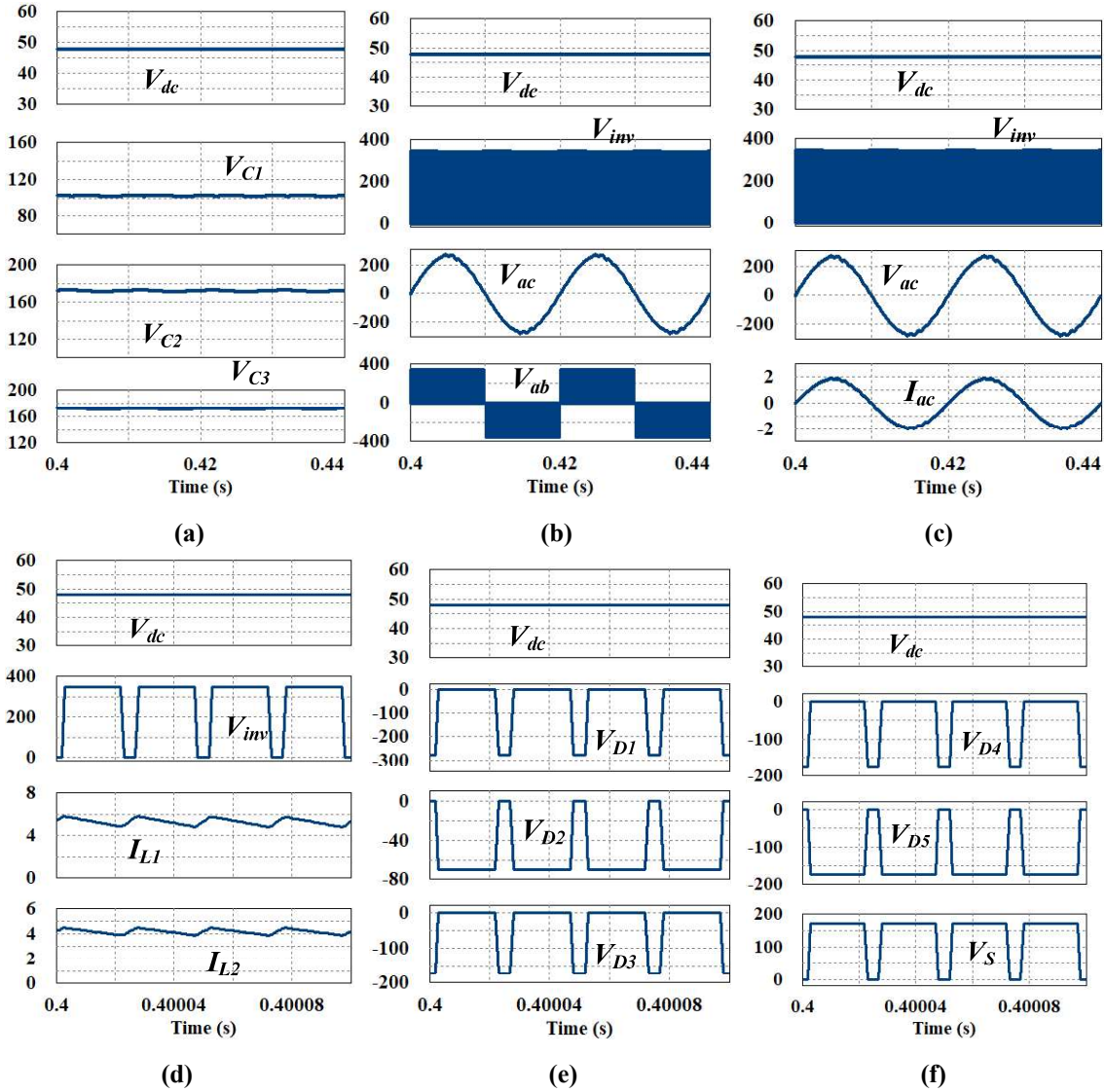


Fig. 5.13. Simulation results of eSLC-ZSI at $D_{st} = 0.2$ and $M = 0.78$ **(a)** V_{C1}, V_{C2}, V_{C3} and V_{dc} **(b)** V_{inv}, V_{ab}, V_{AC} and V_{dc} **(c)** V_{inv}, V_{AC}, I_{AC} and V_{dc} **(d)** I_{L1}, I_{L2}, V_{inv} and V_{dc} **(e)** maximum voltage stresses across the devices (D_1, D_2 and D_3) **(f)** maximum voltage stresses across the devices (D_4, D_5 and S). **[Y-axis having voltage/current values, having units "V" or "A"]**

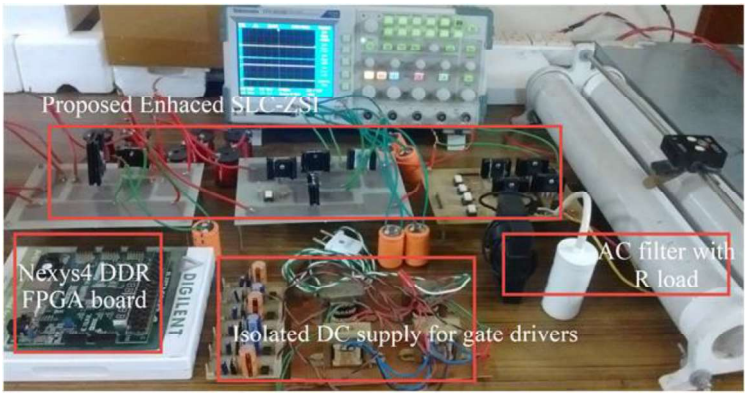


Fig. 5.14. A photograph of the experimental set-up of eSLC-ZSI.

5.4.2 Experimental Results of eSLC-ZSI

Fig. 5.14 shows a photograph of eSLC-ZSI experimental set-up. The experimental results of eSLC-ZSI are shown in Figs. 5.15 and 5.16 for the operating conditions given in Table 5.5. It can be observed from Fig. 5.15(a) that voltages across capacitors (C_1, C_2 and C_3) are V_{C1} = 99.3 V, V_{C2} = 164.1 V and V_{C3} = 165.5 V for an input voltage V_{dc} = 48 V. As shown in Fig. 5.15(a), the capacitor voltages do not have a double line frequency ripple due to high values of capacitances. Fig. 5.15(b) shows voltage appearing across the HB circuit of eSLC-ZSI as V_{inv} = 329.6 V, AC output voltage without filter as $V_{ab(pk)}$ = 329.3 V and fundamental AC output voltage as $V_{ac(rms)}$ = 181.7 V along with V_{dc}. It can be observed from Fig. 5.15(c) that fundamental AC output current as $I_{ac(rms)}$ = 1.27 A along with V_{inv}, V_{ac} and V_{dc}. As the load is resistive, I_{ac} is in phase with V_{ac} and the same can be observed from Fig. 5.15(c). The harmonic spectrum of AC output voltage is shown in Fig. 5.15(d). It can be observed from Fig. 5.15(d) that the THD of V_{AC} as 1.73%. The THD can be further reduced by proper tuning of $L_f C_f$ filter and using an optimized switching logic.

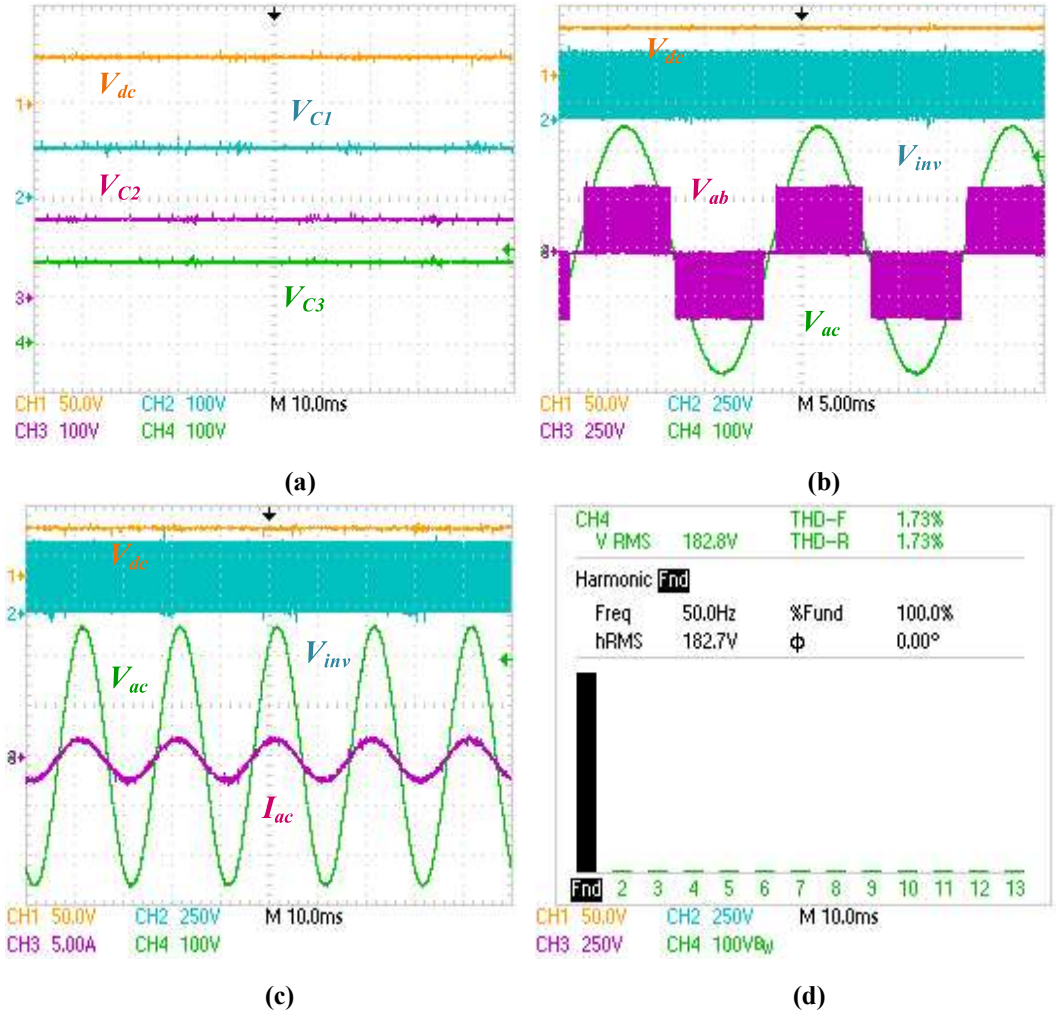
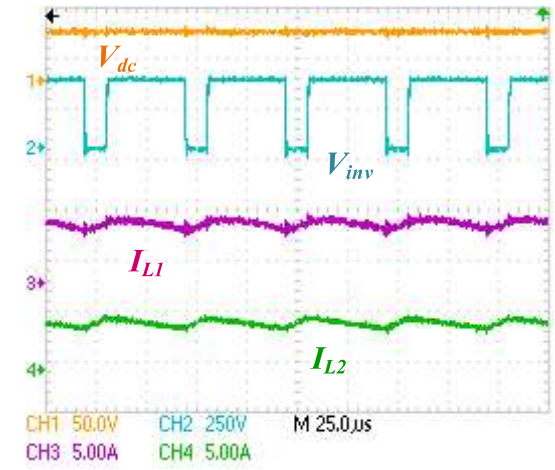
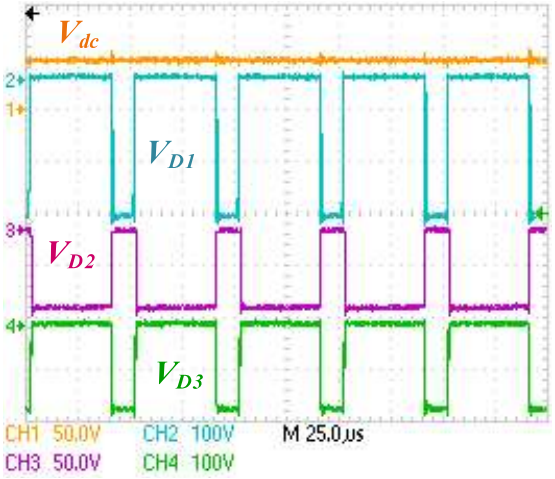


Fig. 5:15. Experimental results of eSLC-ZSI at $D_{st} = 0.2$ and $M = 0.78$ **(a)** V_{C1}, V_{C2}, V_{C3} and V_{dc} **(b)** V_{inv}, V_{ab}, V_{ac} and V_{dc} **(c)** V_{inv}, V_{AC}, I_{AC} and V_{dc} **(d)** harmonic spectrum of V_{ac}.

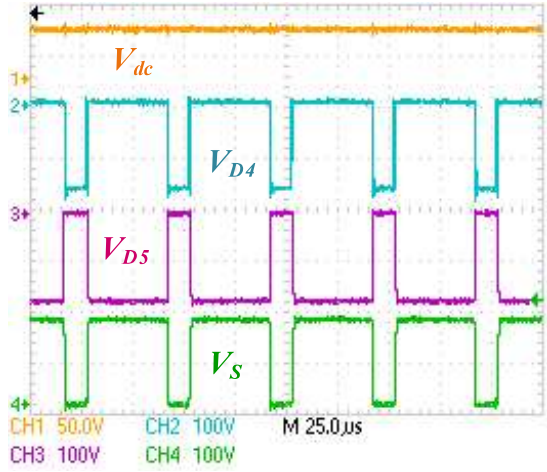
Fig. 5.16 shows average inductor currents and voltages experienced by power semiconductor devices. It can be observed from Fig 5.16(a) that average currents flowing through inductors are $I_{L1} = 5.39$ A and $I_{L2} = 4.2$ A along with V_{inv} and V_{dc} in a high-frequency region. Further, it can be observed from Fig. 5.16(a) that the input current ($\cong I_{L1}$) of eSLC-ZSI has less ripple. It can be noticed from Fig. 5.16(b) that maximum voltages appeared across the diodes (D_1, D_2 and D_3) are $V_{D1} = -262.3$ V, $V_{D2} = -67.8$ V and $V_{D3} = -164.23$ V. As shown in Fig. 5.16(c), maximum voltages across the devices (D_4, D_5 and S) are $V_{D4} = -163.9$ V, $V_{D5} = -163.7$ V and $V_S = 166.2$ V along with V_{dc}. It can be observed from Figs. 5.16(b) and 5.16(c) that D_1 has higher voltage stress and D_2 has lower voltage stress among all power semiconductor devices.



(a)



(b)



(c)

Fig. 5:16. Experimental results of the eSLC-ZSI at $D_{st} = 0.2$ and $M = 0.78$ **(a)** I_{L1}, I_{L2} and V_{inv} in high-frequency region **(b)** maximum voltages across the devices (D_1, D_2 and D_3) **(c)** maximum voltages across the devices (D_4, D_5 and S).

It is clear from experimental studies that voltage and current values are less as compared to simulation results because of ideal operating conditions in simulation studies and presence of non-idealities in the experimentation. However, this difference can be minimized by designing an optimal PCB layout and choosing optimized passive elements and power semiconductor devices.

5.4.3 Power Loss Calculations and Variation in Efficiency of eSLC-ZSI

Power losses in the elements of eSLC-ZSI occur due to switching and conduction states of the power semiconductor devices and parasitic effects of passive elements. The power losses in switches of eSLC-ZSI are calculated in power and shoot-through states only and neglected in zero states. The power losses in various elements of eSLC-ZSI are determined at rated power by considering non-idealities of elements: $r_{DCR,L1} = 180$ mΩ and $r_{L2} = 360$ mΩ; $r_{ESR,C1} = 70$ mΩ, $r_{ESR,C2} = 35$ mΩ and $r_{ESR,C3} = 40$ mΩ; $V_{DS(on)} = 1.1$ V; $r_{DS(on)} = 0.15$ Ω; $V_{F,D} = 0.8$ V and $r_{F,D} = 0.1$ Ω. The determined power losses are shown in Fig. 5.17 along with efficiency variation of eSLC-ZSI at different loading conditions [106]-[112].

(a) Power Losses in Switches of eSLC-ZSI

The switching losses in HB switches ($S_1 - S_4$) are calculated during power and shoot-through states (PS and STS). The average switching power losses in HB switches during PS, $P_{switc\_HB\_PS}$ are determined from the equation given in (5.27).

$$P_{switc\_HB\_Ps} = 4 * \frac{f_{si}*(E_{on}+E_{off})*V_{inv}*I_{inv}}{V_{ref}*I_{ref}} \tag{5.27}$$

where E_{on} and E_{off} are switching ON and OFF energies of switches at reference voltage V_{ref} and current I_{ref} (can be known from manufacturer's datasheet of switches), I_{inv} is the current flowing through HB switches, V_{inv} is the voltage appearing across HB switches and f_{eq} is the equivalent switching frequency of HB switches. The f_{eq} can be defined as $\frac{f_s}{f_{line}}$, where f_s is the frequency of carrier wave and f_{line} is the frequency of modulation wave (i.e., frequency of AC output) in the SPWM switching logic.

The required current and voltage expressions for calculating $P_{switc\_HB\_PS}$ are given in (5.28).

$$\left.\begin{aligned} V_{inv} &= \frac{2}{1-4D_{st}+2{D_{st}}^2} V_{dc} \\ I_{inv} &= \frac{1-4D_{st}+2{D_{st}}^2}{2(1-D_{st})} I_{dc} \end{aligned}\right\} \quad (5.28)$$

During the STS, each switch of the HB circuit is turned-on either in positive half or negative half cycle of AC output. Also, they are turned-on with an equal number of times as they are turned-on in PS of any half cycle of AC output. As a result, the switching frequency becomes half of f_{eq} during STS. The current flowing through HB switches during STS is I_{STS}. The average switching losses in HB switches during STS, $P_{switc\_HB\_STS}$ are determined from the expression given in (5.29).

$$P_{switc\_HB\_STS} = \frac{4*\frac{f_{eq}}{2}*(E_{on}+E_{off})*V_{inv}*I_{STS}}{V_{ref}*I_{ref}} \quad (5.29)$$

The I_{STS} is a summation of average currents flowing through inductors ($L_1$and L_2) and the required inductor currents are given in (5.30).

$$\left.\begin{aligned} I_{L1} &= \frac{2(1-D_{st})}{1-4D_{st}+2{D_{st}}^2} I_{inv} \\ I_{L2} &= \frac{2(1-D_{st})^2}{1-4D_{st}+2{D_{st}}^2} I_{inv} \end{aligned}\right\} \quad (5.30)$$

The switching losses in switch S of eSLC-ZSI during STS, $P_{switc\_S\_STS}$ are obtained from the equation given in (5.31).

$$P_{switc\_S\_STS} = \frac{2f_{si}*(E_{on}+E_{off})*V_S*I_S}{V_{ref}*I_{ref}} \quad (5.31)$$

The required current and voltage expressions for calculating $P_{switc\_S\_STS}$ are given in (5.32).

$$\left.\begin{aligned} V_S &= \frac{1}{1-4D_{st}+2{D_{st}}^2} V_{dc} \\ I_S &= I_{L1} + I_{L2} \end{aligned}\right\} \quad (5.32)$$

The obtained total switching losses in switches (S and $S_1 - S_4$) of eSLC-ZSI, P_{switc_S} are shown in Fig. 5.17(a) as a percentage of total power losses.

The conduction losses in the switches (S and $S_1 - S_4$) during PS and STS, P_{cond_S} are determined from the equation given in (5.33).

$$P_{cond\_S} = {I^2}_{S\_rms} r_{DS(on)} + I_{S\_avg} V_{DS(on)} \quad (5.33)$$

The required average and RMS currents for calculating conduction losses in switches during STS are given in (5.34)

$$\left.\begin{aligned} I_{avg\_STS} &= \frac{1}{T_s}\int_0^{T_s}(i_{L1}+i_{L2}) * \frac{D_{st}}{2}\,dt \\ I_{rms\_STS} &= \left(\frac{1}{T_s}\int_0^{T_s}(i_{L1}+i_{L2})^2 * \frac{D_{st}}{2}\,dt\right)^{\frac{1}{2}} \end{aligned}\right\} \tag{5.34}$$

The required average and RMS currents for calculating conduction losses in switches during PS are given in (5.35).

$$\left.\begin{aligned} I_{avg\_PS} &= \frac{1}{T_s}\int_0^{T_s} i_{inv}\,dt \\ I_{rms\_PS} &= \left(\frac{1}{T_s}\int_0^{T_s} i^2{}_{inv}\,dt\right)^{\frac{1}{2}} \end{aligned}\right\} \tag{5.35}$$

The obtained total conduction losses in switches (S and $S_1 - S_4$) of eSLC-ZSI, P_{cond_S} are shown in Fig. 5.17(a) as a percentage of total power losses.

(b) Power losses in Diodes of eSLC-ZSI

The conduction losses in diodes ($D_1 - D_5$) of eSLC-ZSI, P_{cond_D} are calculated from the expression given in (5.36).

$$P_{cond\_D} = V_{F,D} * I_{D\_avg} + I^2{}_{D\_rms} * r_{F,D} \tag{5.36}$$

where $V_{F,D}$ is forward voltage drop and $r_{F,D}$ is forward resistance of diodes (are known from manufacturer's datasheet of diodes), I_{D_avg} and I_{D_rms} are average and RMS current of diodes. The required currents for calculating P_{cond_D} are given in (5.37).

$$\left.\begin{aligned} i_{D1} &= i_{L1} \\ i_{D2} &= i_{L1} \\ i_{D3} &= (i_{L2} - i_{inv}) \\ i_{D4} &= (i_{L2} - i_{inv}) \\ i_{D5} &= (i_{L1} + i_{L2}) \end{aligned}\right\} \tag{5.37}$$

The calculated conduction losses in diodes ($D_1 - D_5$) of eSLC-ZSI, P_{cond_D} are shown in Fig. 5.17(a) as a percentage of total power losses.

The switching losses in diodes ($D_1 - D_5$) of eSLC-ZSI, P_{switc_D} are determined from the expression given in (5.38).

$$P_{switc\_D} = 2 * f_s * Q_{rr} * V_D \tag{5.38}$$

where Q_{rr} is reverse recovery charge of diodes (are known from manufacturer's datasheet of diodes) and V_D is the voltage across diodes during their reverse-biased condition. The required voltages for calculating P_{switc_D} are given in (5.39).

$$\left.\begin{aligned} V_{D1} &= \frac{2(1-D_{st})}{1-4D_{st}+2{D_{st}}^2}V_{dc} \\ V_{D2} &= \frac{2D_{st}}{1-4D_{st}+2{D_{st}}^2}V_{dc} \\ V_{D3} = V_{D4} = V_{D5} &= \frac{1}{1-4D_{st}+2{D_{st}}^2}V_{dc} \end{aligned}\right\} \quad (5.39)$$

The calculated switching losses in diodes ($D_1 - D_5$) of eSLC-ZSI, P_{switc_D} are shown in Fig. 5.17(a) as a percentage of total power losses.

(c) Power Losses in Inductors of eSLC-ZSI

The power losses in inductors ($L_1$and L_2) of eSLC-ZSI, P_L are occurred due to DCR of inductance (r_{DCR}) and are determined from the equation given in (5.40).

$$P_L = I_{L\_rms}^2 r_{DCR} \quad (5.40)$$

The required currents for calculating P_L are given in (5.41).

$$\left.\begin{aligned} I_{L1\_rms} &= \left(\frac{1}{T_s}\int_0^{T_s} {i^2}_{L1}\, d(t)\right)^{\frac{1}{2}} \\ I_{L2\_rms} &= \left(\frac{1}{T_s}\int_0^{T_s} {i^2}_{L2}\, d(t)\right)^{\frac{1}{2}} \end{aligned}\right\} \quad (5.41)$$

The calculated power losses in inductors ($L_1$and L_2) of eSLC-ZSI, P_L are shown in Fig. 5.17(a) as a percentage of total power losses.

(d) Power Losses in Capacitors of eSLC-ZSI

The power losses in capacitors (C_1, C_2 and C_3) of eSLC-ZSI, P_C are occurred due to ESR of capacitance (r_{ESR}) and are determined from the equation given in (5.42).

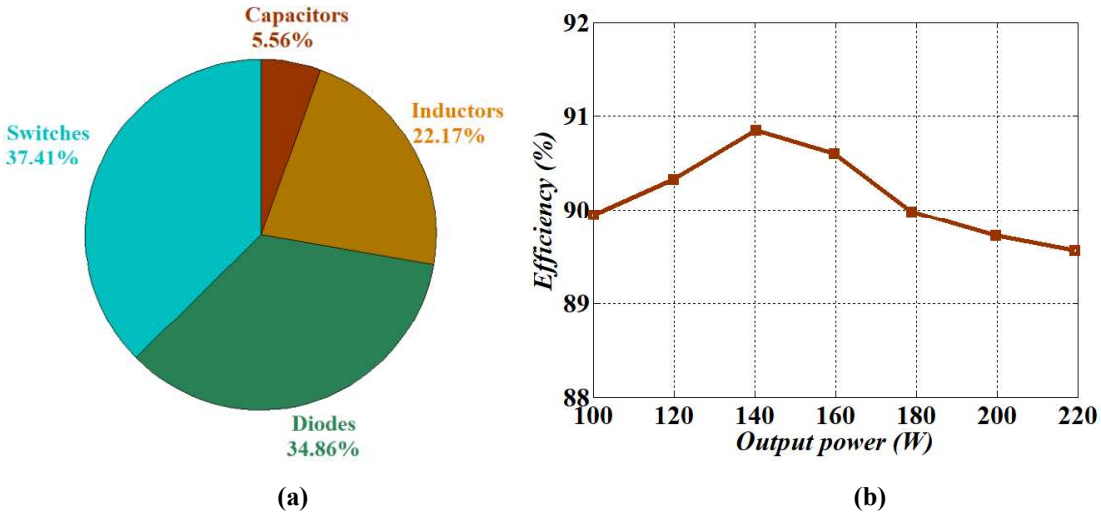
$$P_C = \frac{1}{T_s}\int_0^{T_s} i_C^2 r_{ESR} dt \quad (5.42)$$

The required currents for calculating the P_C are given in (5.43).

$$\left.\begin{aligned} i_{C1} &= \begin{cases} -i_{L2} & 0 \le t \le DT_s \quad ; STO \\ i_{L1} - i_{L2} & (1-D)T_s \le t \le T_s \quad ; nSTO \end{cases} \\ i_{C2} + i_{C3} &= \begin{cases} -(i_{L1} + i_{L2}) & 0 \le t \le DT_s \quad ; STO \\ i_{L2} - 2i_{inv} & (1-D)T_s \le t \le T_s \quad ; nSTO \end{cases} \end{aligned}\right\} \quad (5.43)$$

The calculated power losses in capacitors (C_1, C_2 and C_3) of eSLC-ZSI, P_C are also shown in Fig. 5.17(a) as a percentage of total power losses.

Further, the efficiency variation of eSLC-ZSI at different loading conditions is carried out and is shown in Fig. 5.17(b). It can be observed from Fig. 5.17(b) that the eSLC-ZSI has a maximum efficiency of 90.85% at 140W.



(a) (b)

Fig. 5.17. Power loss distribution among the elements and variation in efficiency of eSLC-ZSI (a) power losses in elements of eSLC-ZSI as a percentage of total power losses (b) variation in efficiency of eSLC-ZSI under different loading conditions.

5.6 Summary

An enhanced high gain switched LC Z-source inverter (eSLC-ZSI) is presented in this chapter. It gives high gain inversion at low values of D_{st} with reduced elements. As D_{st} is low, M increases which results in high gain inversion output with reduced harmonic distortion. Because of the inductor at input side, it has a continuous input current with a low ripple. Detailed mathematical modelling of eSLC-ZSI is carried out using developed switching logic at the operating condition $D_{st} + M \leq 1$. To show the effectiveness of eSLC-ZSI, a comparison is made between eSLC-ZSI and some reported high gain ZSIs in terms of number of elements, boosting ability, voltage gain, the volume of energy storage elements and voltage and current stresses on the elements. As the eSLC-ZSI has lesser number of elements and reduced energy storage elements, the overall volume of eSLC-ZSI is reduced as compared to reported ZSIs. Further, the performance of eSLC-ZSI is verified through simulation and experimental results. It can be observed from the results that the AC output voltage of eSLC-ZSI has low harmonic distortion. Also, the power loss calculations and efficiency variation of eSLC-ZSI are carried out to show its effectiveness. It can be found

from the efficiency variation that the eLSC-ZSI has good efficiency at different loading conditions. It can be concluded from the above discussions that the eSLC-ZSI is well suited for a single-stage AC residential system operated by low voltage DC sources due to its advantages as compared to reported ZSIs.

The eSLC-ZSI avoids the two-stage power conversion for AC residential systems. However, in recent times, DC loads are gradually increasing along with AC loads of modern residential distribution systems. To supply DC and AC loads simultaneously with the better power density and reduced volume of the overall system, the proposed converters (TSHGC, HGIBC, two SLC-ZSIs, and eSLC-ZSI) are not appropriate with their present circuit configurations. They also need additional power converters for supplying DC and AC loads which results in increased volume of the overall system. To take care of this issue, an interleaved hybrid converter (IHC) is presented in Chapter 6 to supply DC and AC loads simultaneously through a single power converter. The IHC is developed from the switching concept of HGIBC and SLC-ZSIs. The salient features and detailed operation of IHC are discussed in chapter 6.