controller used in the proposed TLIHC, for variations in passive components values are also presented. The cross-regulation behaviour of TLIHC is conferred during the dynamic loading conditions in this chapter. Leakage current comparison between the proposed TLIHC and one of the transformerless boost derived hybrid converter is also presented in this chapter.

Chapter 5 discusses the grid-tied mode operation of TLIHC. The detailed analysis of grid side filter inductors (L_{g1} and L_{g2}), phase-locked loop (PLL) design and fast Fourier transform (FFT) analysis of grid current (I_g) of the proposed TLIHC are discussed in this chapter. Also, the closed loop control strategy of I_g is discussed in this chapter. Finally, the simulation results for the performance verifications of the grid integrated proposed TLIHC is presented in this chapter.

Conclusions to the research work in the thesis and scope for the future work are discussed in Chapter 6.

In order to show the relationship among different chapters, a chapter wise block diagram representation of overall thesis is shown in Fig. 1.15. From the figure, it is observed that all the chapters are related with each other and chapter 6 shows the overall conclusion of the work.

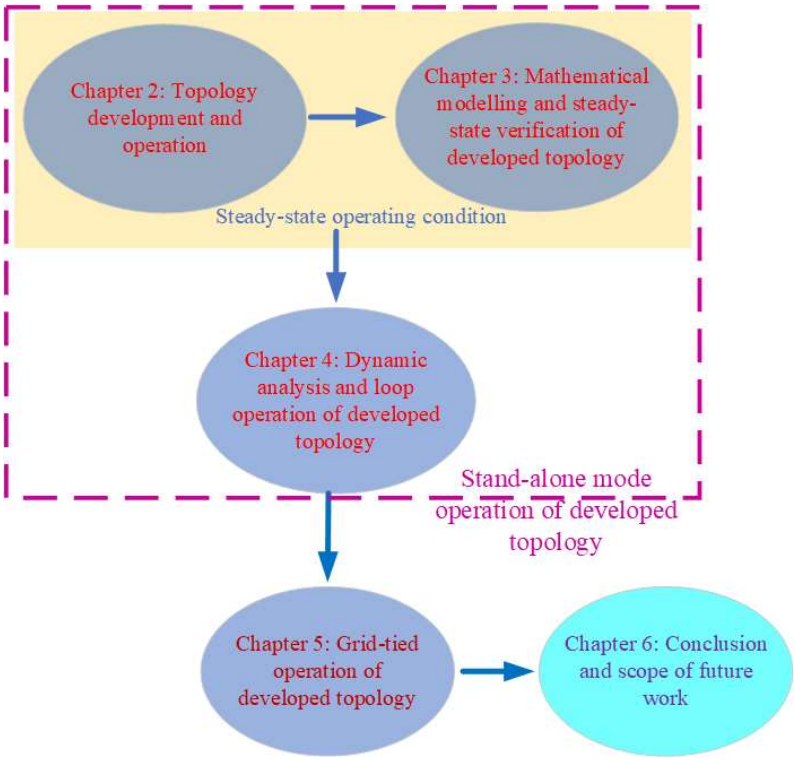


Fig. 1.15 Chapter wise block diagram representation of overall thesis.

Chapter 2

Topology Development and Operation of Wide Operating Range Transformerless Interleaved Hybrid Converter

2.1 Introduction

As discussed in the previous chapter, a simultaneous DC and AC outputs based transformerless hybrid converter (THC) is required for residential utility photovoltaic (PV) systems. However, THC has some issues, like common mode leakage current, non-minimum phase behaviour, need of deadtime circuit and shoot-through problem. In order to address all these issues, a transformerless minimum phase hybrid converter (TLMPHC) is developed. However, while investigating the developed TLMPHC, it is observed that the TLMPHC operates only in a narrow operating range of duty ratio (D) and modulation index (M_i). Thus, there is a compromise between the DC gain and better quality of AC output voltage. For achieving high DC gain along with improved AC output voltage, THC with wide operating range of D and M_i is required. This condition can only be achieved by operating the THC at $D + M_i \geq 1$. To operate the THC at this condition, both D and M_i should be controlled independently. In order to achieve wide operating range for THC, the concept of interleaved converters (interleaving of two converters) is incorporated with the developed TLMPHC in this work. The newly developed THC is termed as transformerless interleaved hybrid converter (TLIHC), which has all the advantages of TLMPHC and can also operate in wide operating range. In this chapter, the topology development and operational behaviour of both TLMPHC and TLIHC are presented. Further, two unipolar based sinusoidal pulse width modulation (SPWM) techniques are used to reduce the common mode leakage current and to regulate the power flow between the DC and AC loads in this chapter. The various features of TLMPHC and TLIHC, along with their comparison with each other and with some of the existing hybrid converter topologies is discussed in this chapter. Finally, simulation and experimental results are presented to verify the operational behaviour and salient features of the developed TLMPHC and TLIHC.

2.2 Topology Development

Both the transformerless hybrid converters TLMPHC and TLIHC are derived from the conventional DC-DC boost converter. The proposed TLMPHC is designed by replacing the controlled switch of a boost converter by a modified voltage source inverter. However, the proposed TLMPHC is incorporated with the conventional DC-DC boost converter to develop the TLIHC.

2.2.1 Topology Development of TLMPHC

In the proposed TLMPHC circuit, the boost converter control switch part and the input side inductor are modified to achieve simultaneous DC and AC outputs along with the minimum phase property. As, the controlled switch of the conventional DC-DC boost converter is replaced by a modified single phase voltage source inverter, it is capable of giving both DC and AC outputs at the same instant. The input side inductor of the boost converter is replaced by a pair of magnetically coupled inductor coils with some modification in the load side of the boost converter to achieve the minimum phase property. Fig. 2.1 shows the circuit diagram of the proposed TLMPHC. It can be observed from Fig. 2.1 that the proposed TLMPHC has six controlled switches (S_1 - S_6), one diode (D_1), two capacitors (C_d and C_0), one pair of magnetically coupled inductor (L_1 and L_2) and one filter inductor split into two equal parts (L_{f1} and L_{f2}). Among the six controlled switches, switches ($S_1 - S_4$) are operated at high switching frequencies, whereas switches S_5 and S_6 are operated at line/grid frequency (50/60 Hz). Further, switches S_5 and S_6 are placed in the AC load side/grid side to implement AC decoupling technique in the TLMPHC. So that during the freewheeling periods the AC load part/grid part is isolated from the rest of the circuit.

The salient features of TLMPHC are as follows

- It gives reduced common mode leakage current as compared to the conventional hybrid converter for PV system, when it is connected to the grid or its inverter output neutral point is grounded.
- The right half plane zero (RHPZ) is eliminated from the control-to-DC output voltage transfer function. So, it behaves as a minimum phase system.

- It gives well-regulated AC and DC outputs simultaneously from a single DC input at the operating condition of $D + M_i \leq 1$.
- It has inherent shoot-through protection capability. So, the reliability of the system is improved.
- As the deadtime is not required in the proposed TLMPHC, it improves the quality of the inverter output voltage.

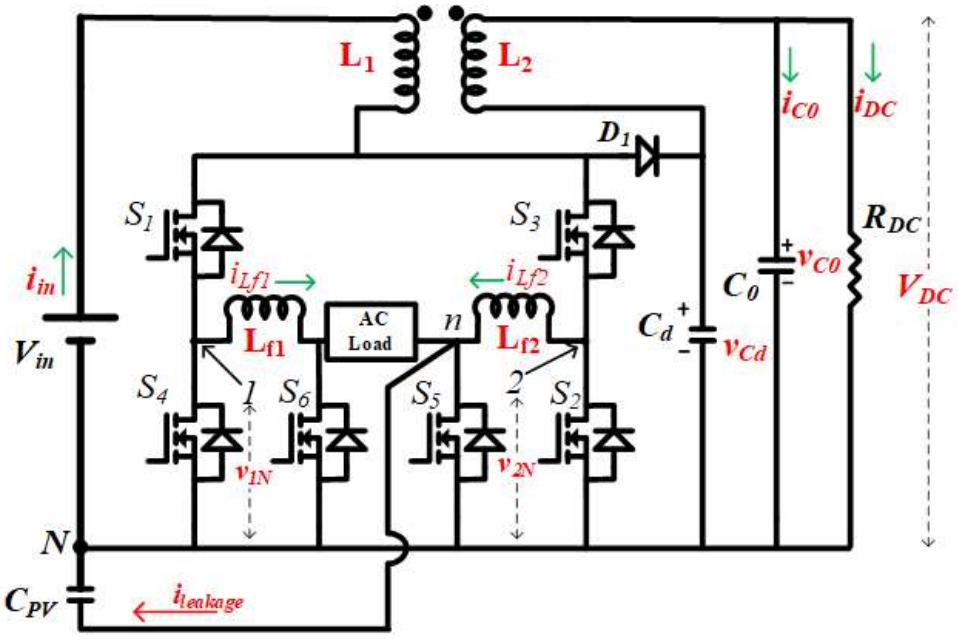


Fig. 2.1 Circuit diagram of transformerless minimum phase hybrid converter.

2.2.2 Topology Development of TLIHC

The developed TLMPHC cannot operate in wide operating range of D and M_i, as it is a boost derived type THC, where the same controlled switches are responsible for varying D and M_i. In order to achieve wide operating range of D and M_i along with all the features of TLMPHC, the developed TLMPHC is incorporated with a conventional DC-DC boost converter to develop the TLIHC. The controlled switch of the DC-DC boost converter in TLIHC is responsible for controlling the value of D and the controlled switches of TLMPHC are used for controlling the value of M_i. The inverter part and its operation are similar for both TLIHC and TLMPHC. Fig. 2.2 shows the circuit diagram of TLIHC. It can be observed from Fig. 2.2 that the proposed TLIHC

consists of seven controlled switches (S and $S_1 - S_6$), two diodes (D_1 and D_2), two capacitors (C and C_0), a pair of magnetically coupled inductors (L_1 and L_2), a filter inductor split into two equal parts (L_{f1} and L_{f2}) and an AC filter capacitor (C_f).

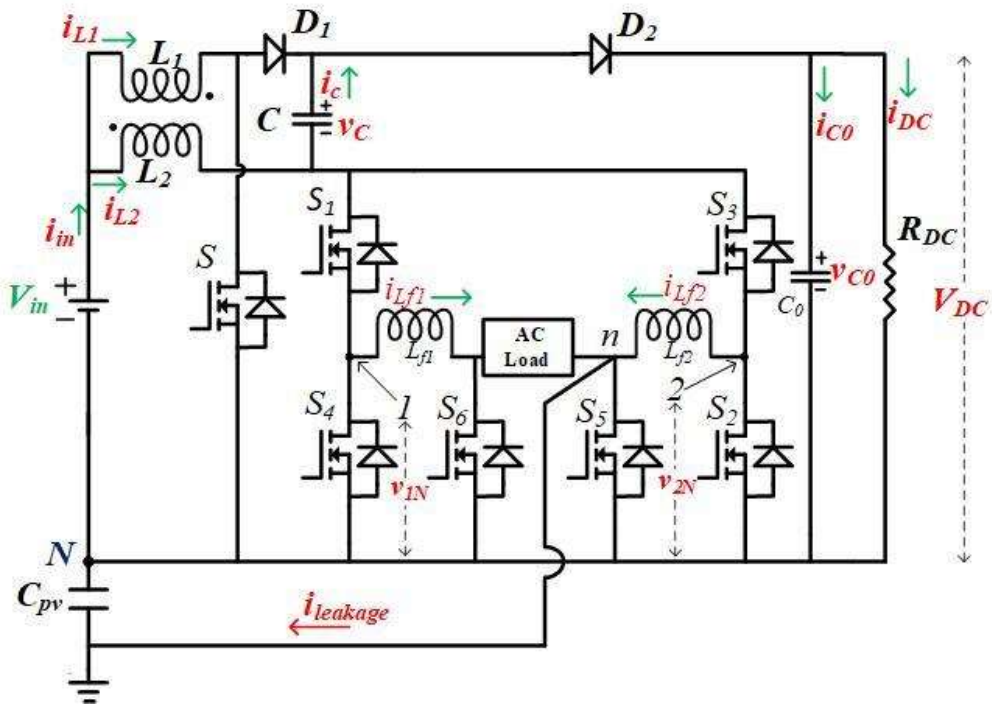


Fig. 2.2 Circuit diagram of transformerless interleaved hybrid converter.

Among the seven controlled switches, switch S and ($S_1 - S_4$) are operated at high switching frequencies, whereas switches S_5 and S_6 are operated at line/grid frequency (50/60 Hz) like the TLMPHC.

The salient features of TLIHC are as follows:

- It gives reduced common mode leakage current as compared to the conventional hybrid converter for PV system, when it is connected to the grid or its inverter output neutral point is grounded.
- The proposed TLIHC gives simultaneous DC and AC outputs for wide operating ranges of D and M_i (i. e. it can operate at both the operating conditions, $D + M_i \geq 1$ and $D + M_i \leq 1$), which results in high DC output voltage and better quality of AC output.

- The right half plane zero (RHPZ) is eliminated from the control-to-DC output voltage transfer function. So, it behaves as a minimum phase system and helps in achieving simpler controller design for wider band width. Also, an improved dynamic performance is achieved for both step-up and step-down duty ratios.
- The total harmonic distortion (THD) is reduced and the reliability is improved in case of the proposed TLIHC as the two switches (S_5 and S_6) are placed at the grid side to isolate the DC part and grid/AC output part during the freewheeling period. Also, the elimination of dead-time in the switching pulses of the proposed TLIHC helps in reducing the THD.
- In the proposed TLIHC, as the input side inductors are inverse coupled inductors, the weight and volume of the overall system is reduced.
- The DC voltage gain is increased in case of proposed TLIHC; however, the voltage stress of the switch remains the same as that of the conventional hybrid converter.

2.3 Proposed Circuit Operation and Switching Behaviour

Both the hybrid converters TLMPHC and TLIHC operate in three different operating intervals/states in both the half cycles (positive and negative half cycles) of AC output voltage and those operating intervals are shoot-through interval, power interval and zero interval.

2.3.1 Operation of TLMPHC

Different operating states of TLMPHC during positive half cycle of AC output voltage is shown in Fig. 2.3.

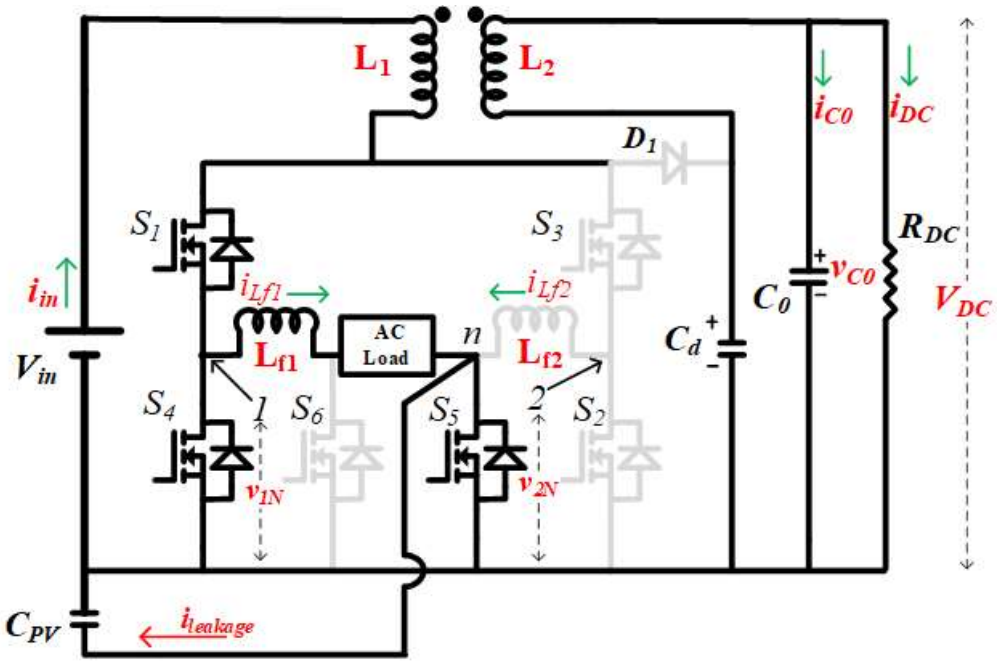
i. Shoot-through state:

During this state, both the switches of same leg (either switch S_1 and S_4 or S_3 and S_2) are in the switch-on position at the same instant. Fig. 2.3 (a) shows the operation of TLMPHC during shoot-through interval in positive half cycle of AC output voltage. It can be noticed from Fig. 2.3 (a) that switches S_1, S_4 and S_5 are kept ON and rest of the switches are kept in OFF positions. Similarly, during negative half cycle of the shoot-through state, switches S_2, S_3 and S_6 are in switch-on positions and the rest of the switches are in off positions. However, during both the

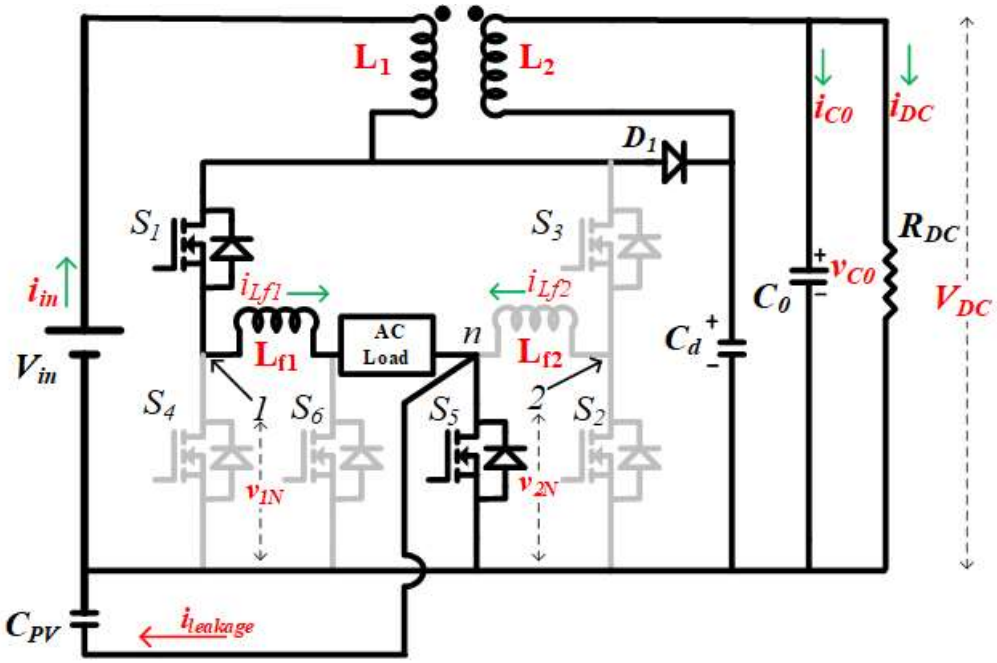
cycles of this interval, the diode D_1 is in reverse biased condition. The current I_{Lf1} freewheels through S_5 and the anti-parallel diode of S_4 during the positive half cycle, whereas current I_{Lf2} freewheels through S_6 and the anti-parallel diode of S_2 during the negative half cycle. Both the inductor coils L_1 and L_2 are in charging mode during the entire shoot-through state irrespective of positive and negative half cycles of the AC output voltage.

ii. Power state:

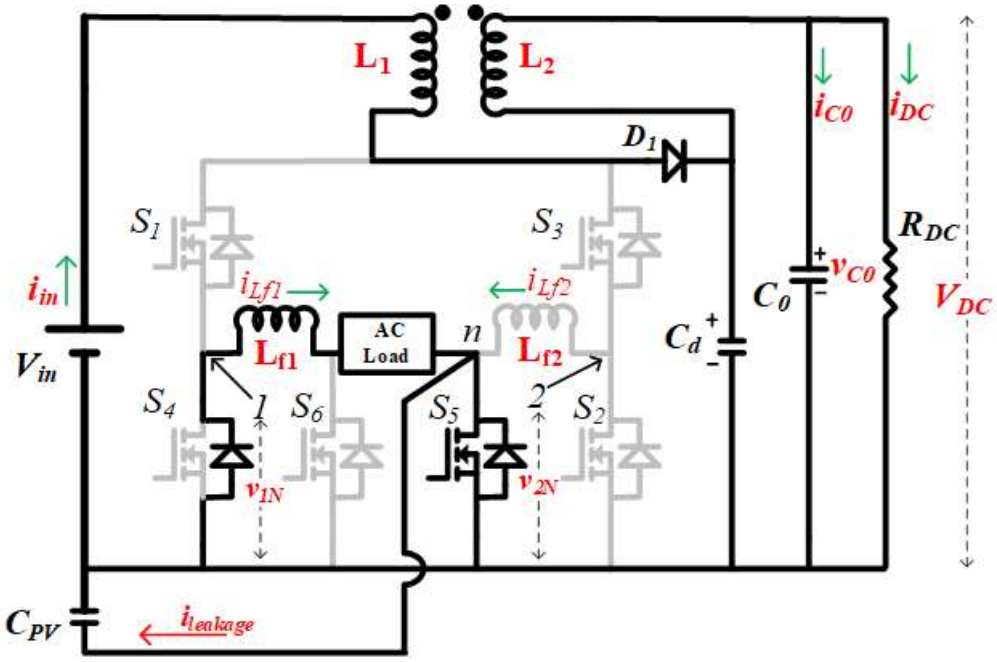
Fig. 2.3 (b) shows the operation of TLMPHC during the power interval in positive half cycle of AC output voltage. From Fig. 2.3 (b), it is observed that switches S_1 and S_5 are kept ON and the rest of the switches are in OFF positions. Similarly, during the negative half cycle of the power state, switches S_3 and S_6 are in the turn-on positions and the rest of the switches are in turn-off positions. During this interval, the stored energy of L_1 along with the input voltage is delivered to the AC load through S_1, L_{f1} and S_5 in the positive half cycle, whereas in the negative half cycle, the power is delivered through S_3, L_{f2} and S_6. However, the stored energy of L_2 along with the input voltage is delivered to the DC load through the diode D_1 in the positive and negative half cycles of this state.



(a)



(b)



(c)

Fig. 2.3 Operating states of TLMPHC. **(a)** Shoot-through interval during positive half cycle of AC output, **(b)** Power interval and **(c)** Zero interval.

iii. Zero state:

Fig. 2.3 (c) shows the operation of TLMPHC during the zero interval for the positive half cycle of AC output voltage. The switch S_5 is ON, and S_1, S_2, S_3, S_4 and S_6 are OFF during this interval. Similarly, for the negative half cycle, the switch S_6 is in ON position and the rest of the switches are kept OFF. During both the cycles of zero interval, the combined energy of L_1, L_2 and V_{in} are delivered to the DC load. However, diode D_1 is in forward biased condition during both the cycles of zero interval.

2.3.2 Switching Behaviour of TLMPHC

A hybrid unipolar based sinusoidal pulse width modulation (SPWM) technique has been developed to regulate the power flow and minimize the common mode leakage current in the proposed TLMPHC. The SPWM switching logic of TLMPHC is realized in the developed prototype using the field programmable gate array (FPGA) digital platform. The schematic of logic gate-based switching pulse generation is shown in Fig. 2.4 (a). It is observed from Fig. 2.4 (a) that the switching logic consists of constant signal (V_{st}), carrier signal ($V_{tr}(t)$) and reference signals ($V_m(t)$ and -$V_m(t)$). As the unipolar based SPWM technique is used, the reference signals have same peak magnitude and frequency, but 180^0 out of phase with respect to each other. The frequency and peak magnitude of reference signal decide the frequency of AC output and modulation index (M_i) of the TLMPHC. The switching frequency of switches (S_1 - S_4) are 20 kHz, which is same as that of the carrier signal $V_{tr}(t)$. Similarly, the switching frequency of switches S_5 and S_6 are same as that of the AC output signal. As discussed earlier, the proposed TLMPHC is operated in three different operating states in each half cycles of AC output voltage. In the shoot-through state, $V_{tr}(t)$ is compared with V_{st}, whereas in the power state $V_{tr}(t)$ is compared with $V_m(t)$ and -$V_m(t)$ during the positive and negative half cycles of the AC output voltage. For ensuring that the power state is not disturbed by the shoot-through state, it is placed within zero state of each switching cycle. As per the switching logic, the expected gating signals of TLMPHC for positive half cycle of AC output voltage are shown in Fig. 2.4 (b). From this figure, it can be observed that the duty ratio (D) of TLMPHC is decided by the shoot-through state. As during this state, both the switches of the same leg of the inverter are in switch-on position at the same instant,

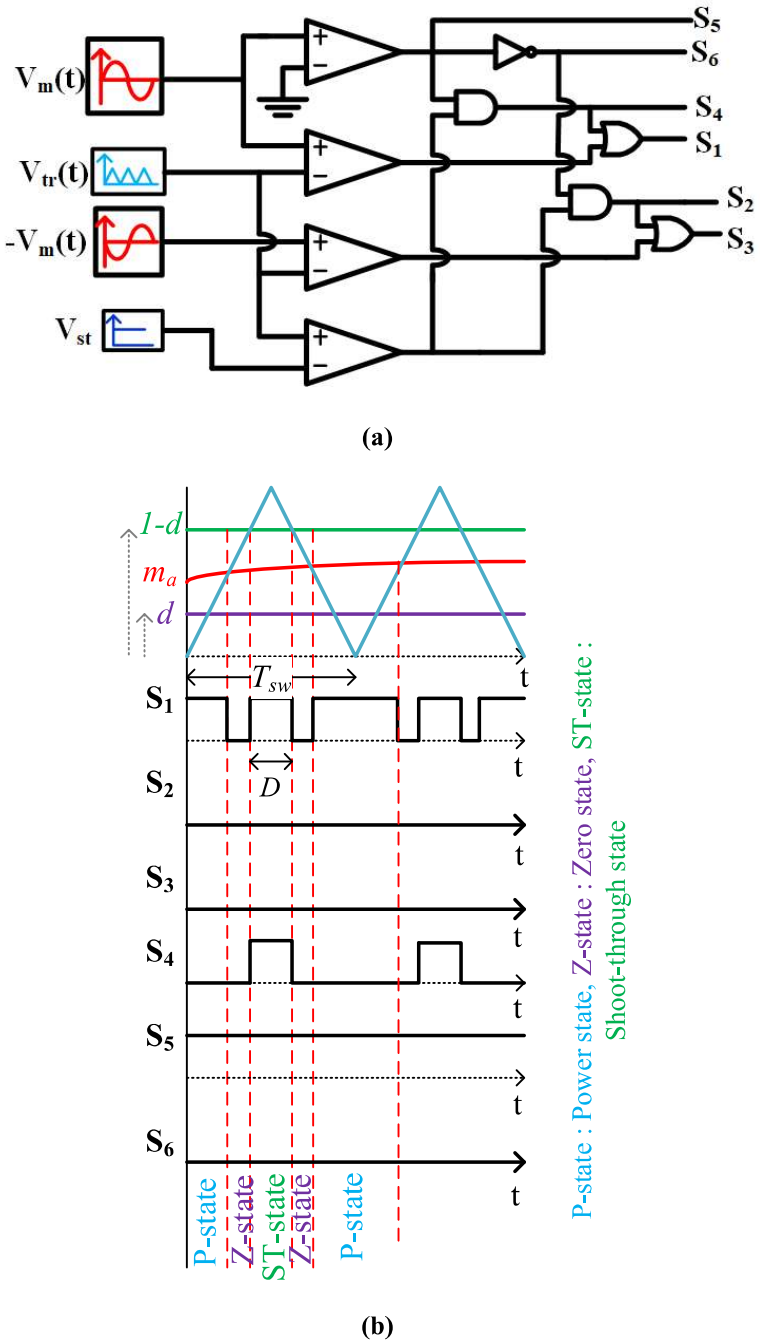


Fig. 2.4 Implementation of unipolar based switching technique of the proposed TLMPHC. **(a)** schematic of logic gate-based switching pulse generation and **(b)** Gating signals of TLMPHC for positive half cycle of AC output.

the TLMPHC operates similar to conventional boost converter in the switch-on interval. Further, as the proposed TLMPHC is derived from the conventional boost converter and the controlled switch of the boost converter is replaced by a modified transformerless voltage source inverter, the operating condition of TLMPHC is $D + M_i \leq 1$. However, the power state of TLMPHC is

decided by the modulation index (M_i) and it is obtained from the reference signal. Moreover, the switching interval of the switch S_5 is in the positive half cycle and that of S_6 in the negative half cycle of the AC output voltage as observed from Fig. 2.4 (b).

2.3.3 Operation of TLIHC

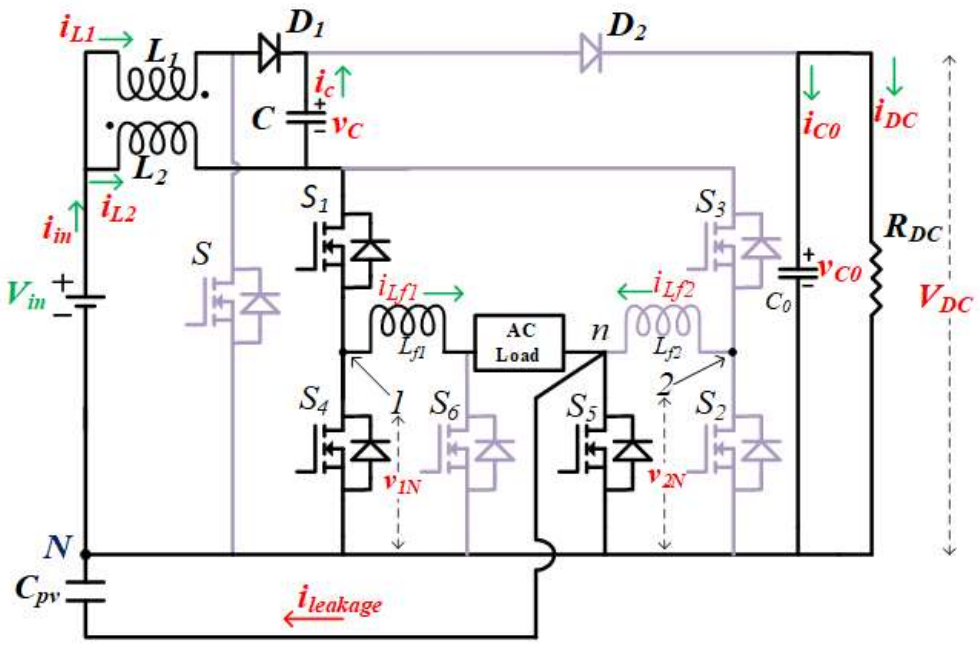
The switch-on period of switch S decides the duty ratio (D) of the proposed TLIHC, whereas switching operation of switches ($S_1 - S_4$) decide the modulation index (M_i). Fig. 2.5 shows the operating states of TLIHC during positive half cycle of AC output voltage.

i. Shoot-through state:

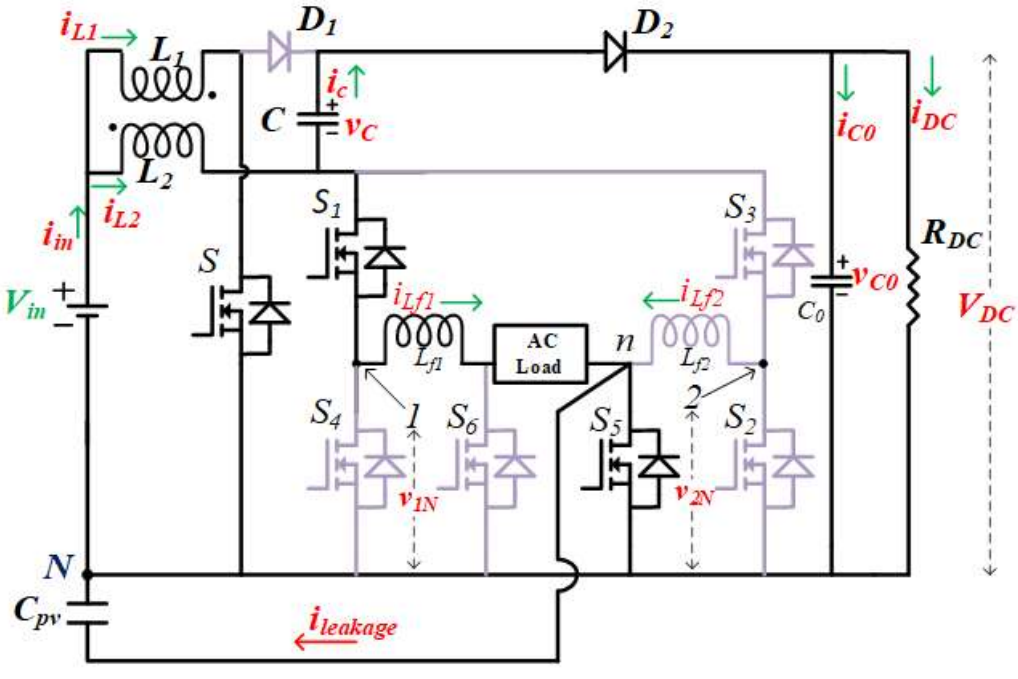
During the shoot-through state of the proposed TLIHC, both the switches of either of the legs are in switch-on position at the same instant of time alike the TLMPHC. Fig. 2.5 (a) shows the operation of the proposed TLIHC during shoot-through state for positive half cycle of AC output voltage. During this period, the switches S_1, S_4 and S_5 are in switch-on positions, and S, S_2, S_3 and S_6 are in switch-off positions. Similarly, during the negative half cycle of shoot-through state, the switches $S, S_1,\ S_4$ and S_5 are in OFF positions and S_2, S_3 and S_6 are in ON positions. The current I_{Lf1} freewheels through S_5 and anti-parallel diode of S_4 during the positive half cycle of the shoot-through state, whereas current I_{Lf2} freewheels through S_6 and anti-parallel diode of S_2 during the negative half cycle. Further, magnetically coupled coil L_2 is in charging mode during both positive as well as negative half cycle of this state.

ii. Power state:

Fig. 2.5 (b) shows the operation of the proposed TLIHC during the power state in positive half cycle of AC output voltage. It can be noticed from Fig. 2.5 (b) that switches (S, S_1 and S_5) are kept in ON positions and switches (S_2, S_3, S_4 and S_6) are kept in OFF positions.


i_{L1}
L_1
D_1
D_2
i_c
C
v_C
i_{C0}
i_{DC}
L_2
i_{L2}
i_{in}
S_1
S_3
S
R_{DC}
V_{in}
i_{Lf1}
i_{Lf2}
v_{C0}
C_0
V_{DC}
AC Load
n
L_{f1}
L_{f2}
S_4
1
S_6
S_5
2
S_2
v_{1N}
v_{2N}
N
C_{pv}
$i_{leakage}$

(a)


i_{L1}
L_1
D_1
D_2
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C
v_C
i_{C0}
i_{DC}
L_2
i_{L2}
i_{in}
S_1
S_3
S
R_{DC}
V_{in}
i_{Lf1}
i_{Lf2}
v_{C0}
C_0
V_{DC}
AC Load
n
L_{f1}
L_{f2}
S_4
1
S_6
S_5
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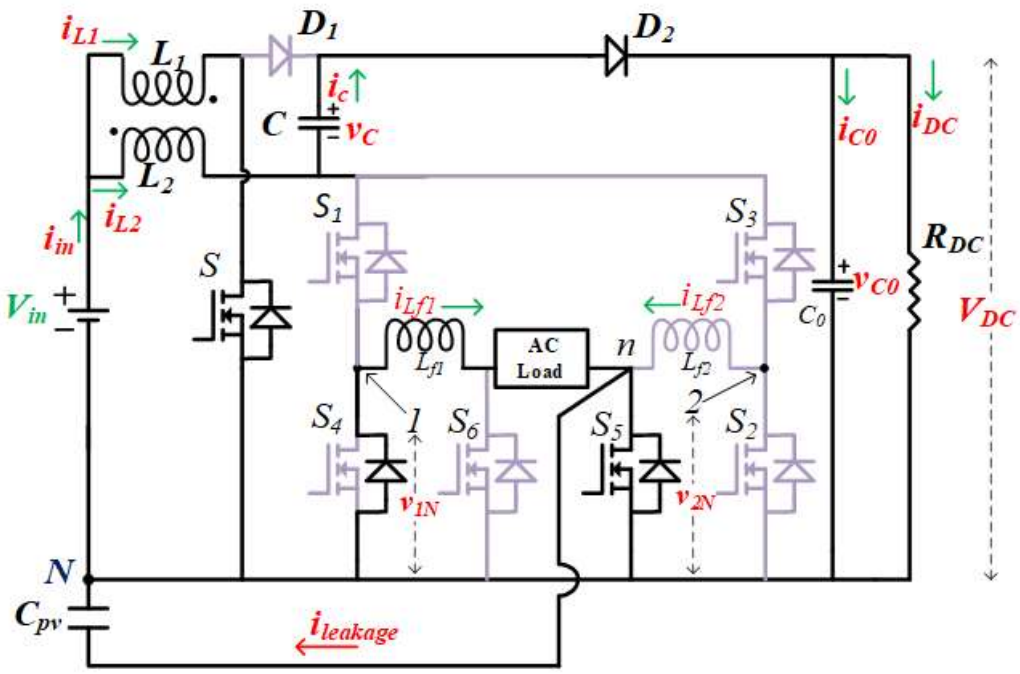
S_2
v_{1N}
v_{2N}
N
C_{pv}
$i_{leakage}$

(b)



(c)

Fig. 2.5 Operating states of TLIHC. **(a)** Shoot-through interval during positive half cycle of AC output, **(b)** Power interval and **(c)** Zero interval.

Similarly, during negative half cycle of the power interval, switches S, S_3 and S_6 are in switch-on positions and S_1, S_2, S_4 and S_5 are in switch-off positions. However, during both the cycles of the power interval, diode D_1 is in reverse biased condition and diode D_2 is in forward biased condition. At this interval, the combined energy of L_2 and V_{in} is delivered to the DC load through the DC link capacitor (C) and D_2 during both the half cycles of AC output voltage. The power is delivered to the AC load through S_1, L_{f1} and S_5 during the positive half cycle and through S_3, L_{f2} and S_6 during the negative half cycle of AC output voltage. Also, for both the cycles of the power interval, coupled inductor L_1 is in charging mode, whereas coupled inductor L_2 is in discharging mode.

iii. Zero state:

Fig. 2.5 (c) shows the operation of the proposed TLIHC during the zero state in the positive half cycle of the AC output voltage. It can be observed from Fig. 2.5 (c) that switches S and S_5 are kept in ON positions, and switches S_1, S_2, S_3, S_4 and S_6 are kept in OFF positions. During this period, no power is delivered to the AC load and i_{Lf1} freewheels through the switch S_5 and the anti-parallel

diode of S_4 in the positive half cycle of AC output voltage. Similarly, during the zero state of the negative half cycle of AC output voltage, switches S and S_6 are in switch-on positions, and S_1, S_2, S_3, S_4 and S_5 are in switch-off positions. During this interval, the filter inductor current i_{Lf2} freewheels through the switch S_6 and the anti-parallel diode of S_2. During both the half cycles of zero state, the combined energy of L_2 and V_{in} is delivered to the DC load only through C and D_2. The behaviour of L_1, L_2, D_1 and D_2 in this state are same as that of the power state.

2.3.4 Switching Behaviour of TLIHC

A unipolar sinusoidal pulse width modulation (SPWM) technique is implemented to minimize the leakage current and to regulate the power flow of the proposed TLIHC. The unipolar SPWM switching logic of TLIHC is realized for the developed prototype by using the field programmable gate array (FPGA) digital platform similar to TLMPHC switching logic. The switching pattern for one complete switching cycle of AC output voltage is shown in Fig. 2.6. It can be observed from Fig. 2.6 that the switching logic consists of constant signal (V_{st}), carrier signal ($V_{tr}(t)$) and reference signals ($V_m(t)$ and -$V_m(t)$). The frequency and peak magnitude of the reference signal decide the frequency of AC output and modulation index (M_i) of the TLIHC. The switching frequency of switches (S and S_1 - S_4) are 50 kHz, which is same as that of the carrier signal $V_{tr}(t)$. Similarly, the switching frequency of switches S_5 and S_6 are same as that of the reference signal (50/60 Hz). The proposed TLIHC is operated in three different operating states in each half cycles of AC output voltage. In the shoot-through state, $V_{tr}(t)$ is compared with V_{st}, whereas in the power state $V_{tr}(t)$ is compared with $V_m(t)$ and -$V_m(t)$ during the positive and negative half cycles of the AC output voltage. Reference signal $V_m(t)$ is responsible for all the positive half cycle switching signals except the switching signal of switch S_5. As during the entire positive half cycle switch S_5 is in turn-on position, similarly switch S_6 during the entire negative half cycle. For ensuring that the power state is not disturbed by the shoot-through state, the power state is placed within zero state of each switching cycle. Further, the duty ratio (D) and modulation index (M_i) are decided by the switching pulses of S and ($S_1 - S_4$) respectively. So, D and M_i are not interdependent on each other similar to the conventional hybrid converters and TLMPHC. The proposed TLIHC can be operated at both the operating conditions, $D + M_i \geq 1$ and $D + M_i \leq 1$.

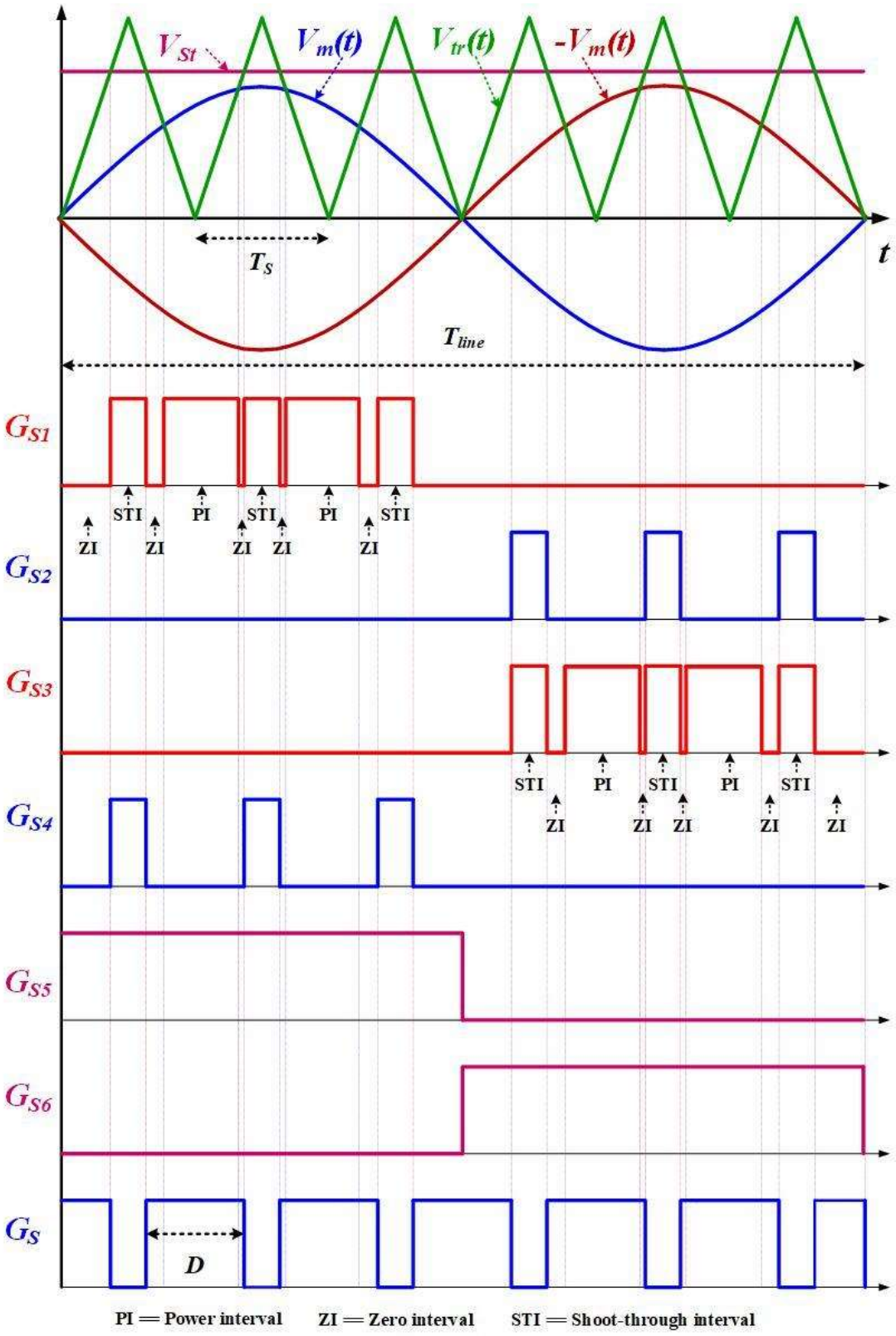


Fig. 2.6 Switching pattern for one complete cycle of AC output voltage of the proposed TLIHC.

2.4 Operational Waveforms

The operational waveforms of both the hybrid converters TLMPHC and TLIHC gives the charging and discharging behaviour of passive components, voltage stresses across the various diodes and also across the inverter bridge.

2.4.1 Operational Waveforms of TLMPHC

The operational waveforms of the TLMPHC are shown in Fig. 2.7. It can be observed from Fig. 2.7 that both the magnetically coupled inductor coils are charging and discharging simultaneously. During the shoot-through state, both the coils are in charging mode and in the non-shoot-through state (power and zero states) both the coils are in discharging mode. Further, the inverter input voltage (V_{inv}) is zero during the shoot-through state, as both the switches of either of the legs are in switch-on position at the same instant during this state as observed from Fig. 2.7. Moreover, the charging and discharging behavior of the DC link capacitor (C_d) can be observed from this figure. The capacitor is in charging mode during both the power and zero states, and in the discharging mode during the shoot-through state. However, the charging rate is faster during the zero state as compared to the power state. It can be observed that during the zero state, the inverter part is isolated from the main circuit, as all the switches except the switches S_5 and S_6 are in turn-off position. Also, both the inductor coils are in discharging mode. Moreover, the turn-on and turn-off duration of the diode (D_1) can be observed from Fig. 2.7. The peak inverse voltage of the diode same as the DC link voltage (V_{Cd}) in this duration.

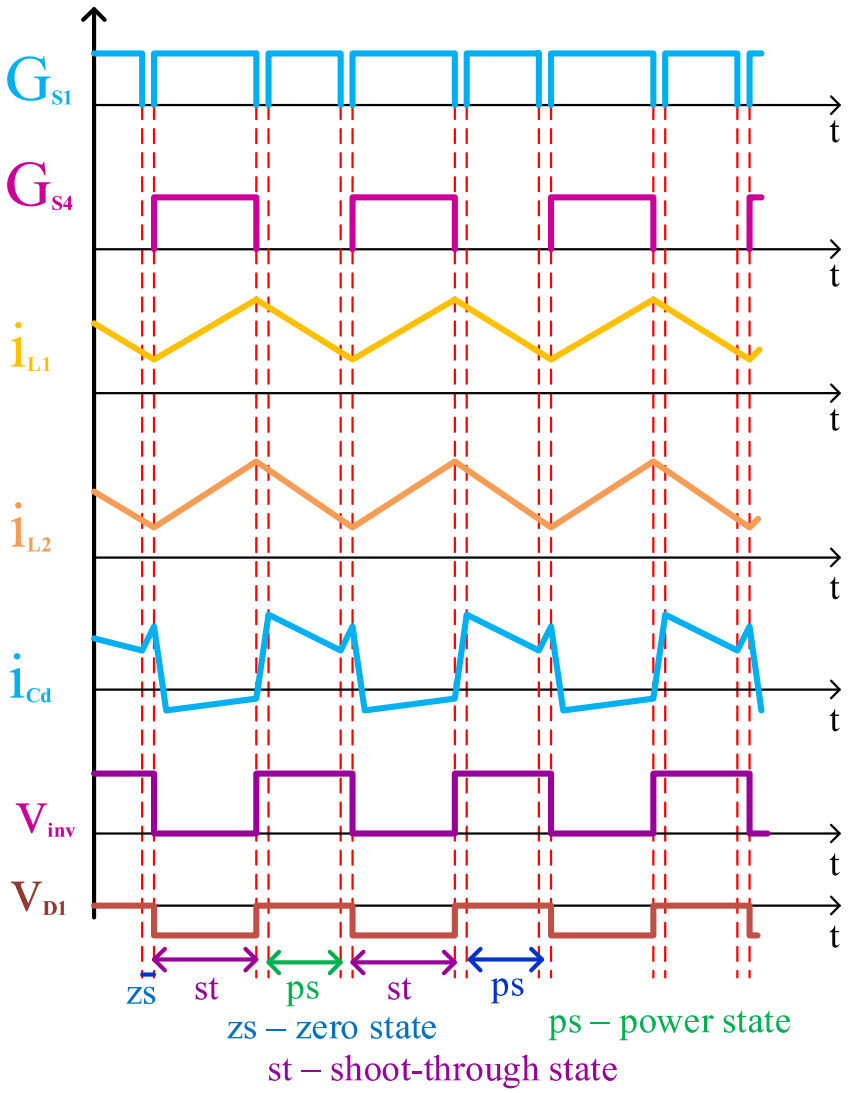


Fig. 2.7 Operational key waveforms of TLMPHC.

2.4.2 Operational Waveforms of TLIHC

The operational waveforms of the proposed TLIHC during all the three operating modes are shown in Fig. 2.8. In this figure G_s indicates the switching pulse of the switch S. It can be observed from Fig. 2.8 that the inductor L_2 is in charging mode and L_1 is in discharging mode during the shoot-through state. However, the inductor L_2 is in discharging mode and L_1 is in charging mode during both power and zero states. During the shoot-through interval, the DC-link capacitor C is in charging mode and the output capacitor C_0 is in discharging mode. Further, diode D_1 is in forward

biased condition during the shoot-through state and is in reverse biased condition during the power and zero states.

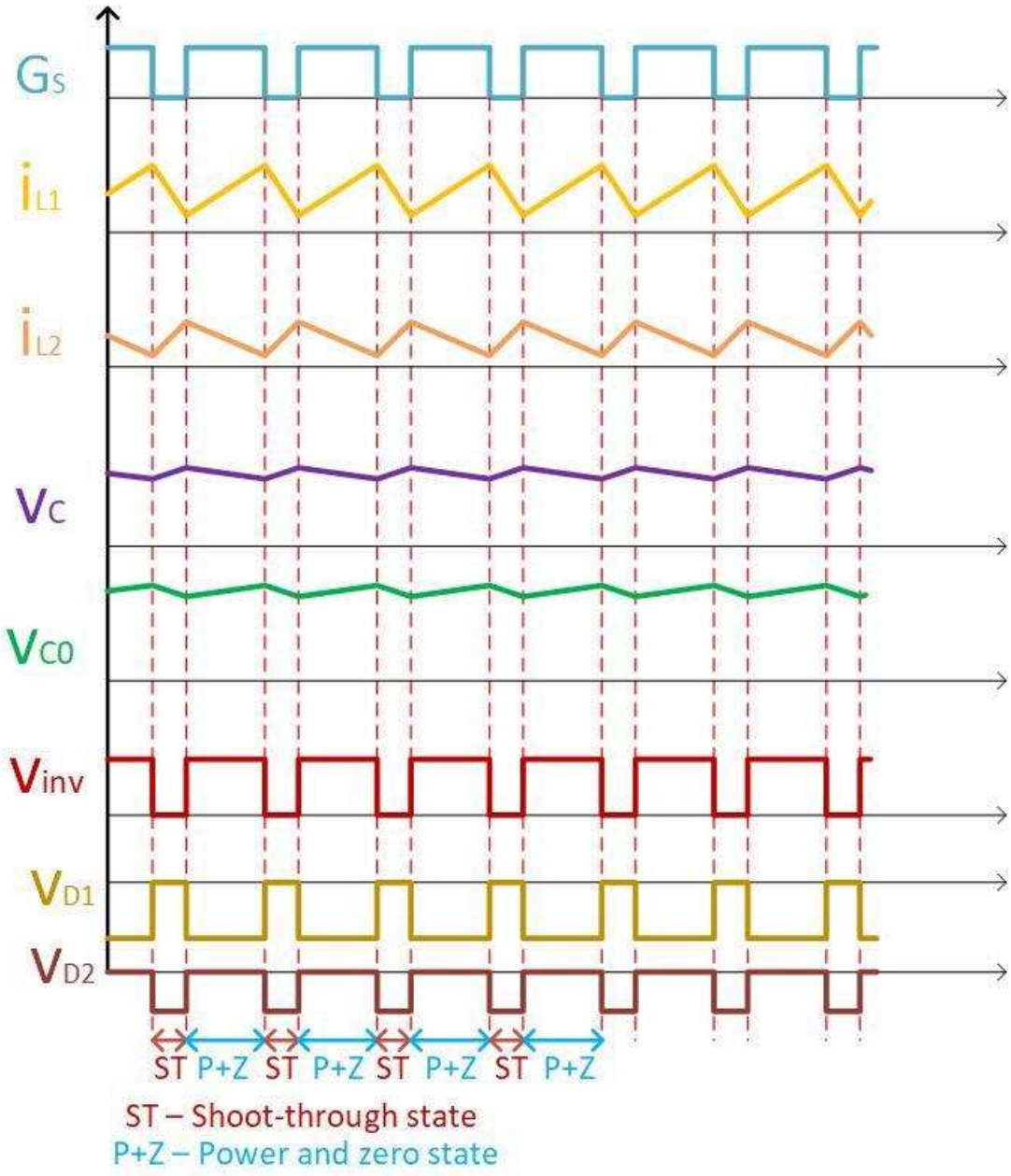


Fig. 2.8 Operational waveforms of the proposed TLIHC.

Similarly, diode D_2 is in reverse biased condition during the shoot-through state and is in the forward biased condition during the power and zero states. The peak inverse voltage (PIV) across D_1 is $\frac{V_{in}}{D(1-D)}$ and across D_2 is $\frac{V_{in}}{D}$. As, during the shoot-through state either of the switches S_1 and

S_4 or the switches S_3 and S_2 are in switch-on positions, the inverter input voltage (V_{inv}) is zero during the shoot-through state and it is $\frac{V_{in}}{D}$ during both the power and zero states.

2.5 Design of Passive Components

For continuous conduction mode of operation, the passive components of the proposed TLMPHC and TLIHC are designed. The ripple in the input inductor current ($\%x_{L1} = \Delta I_{L1}$) can be calculated by considering the waveform shown in Fig. 2.9. On the basis of charging and discharging mode of inductor (L_1), both the proposed TLMPHC and TLIHC operates in two modes (non-shoot through and shoot-through modes). During the non-shoot through mode (DT_s), L_1 is in charging mode, whereas during the shoot-through mode ($D'T_s$), L_1 is in discharging mode. So, the peak-peak current ripple is calculated as

$$2\Delta I_{L1} \geq \frac{V_{L1} DT_S}{I_{L1} L_1} \tag{2.1}$$

During the non-shoot through mode $V_{L1} = V_{in}$, so (2.1) can be written as

$$L_1 \geq \frac{V_{in} R_{DC} D(1-D) T_S}{2\Delta I_{L1} V_{DC}} \tag{2.2}$$

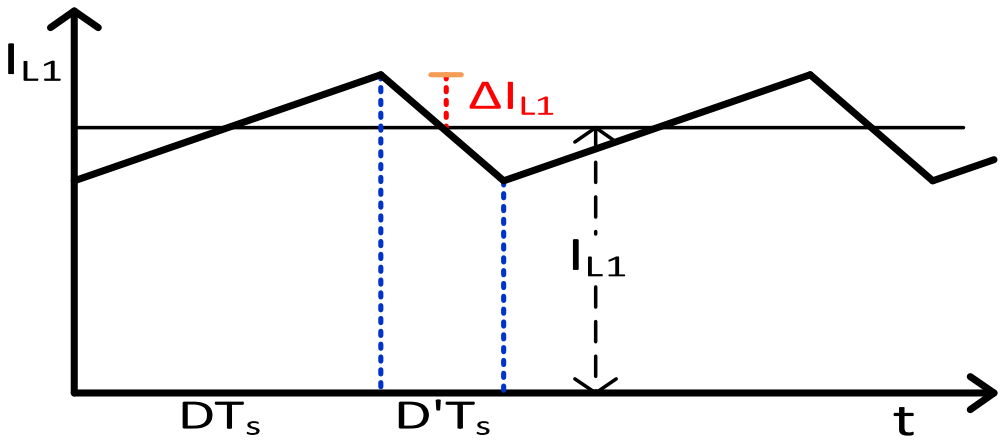


Fig. 2.9 Input inductor L_1 current ripple.

Similarly, the other passive elements of the proposed TLIHC are calculated by using the following inequality equations.

$$\left.\begin{aligned} L_2 &\geq \frac{(V_{in}+V_c-V_{C0})DT_s}{2\Delta I_{L2} I_{L2}} \\ C &\geq \frac{V_{in}\,D'^{T_s}}{2\Delta V_c * R_{DC} D(1-D)^2} \\ C_0 &\geq \frac{V_{in}(1-D)T_s}{2\Delta V_{C0}\,D(1-D)R_{DC}} \end{aligned}\right\} \quad (2.3)$$

where $x_{L1}\%$ and $x_{L2}\%$ are the percentage inductor current ripple ($\leq 10\%$), $x_C\%$ and $x_{C0}\%$ are percentage capacitor voltage ripple ($\leq 5\%$).

Further, the AC filter component values (L_{f1}, L_{f2} *and* C_f) are calculated by keeping unity gain at 50 Hz and greater than 40 dB attenuation for higher frequencies.

Table 2.1 List of Components and Ripple Percentage of TLMPHC

Parameter	**Attributes**
Coupled inductors L_1 and L_2	1.6 mH and 1.1 mH
Filter inductor $L_{f1} = L_{f2}$	2 mH
DC link capacitor (C_d)	470 µF
DC and AC filter capacitor (C_0 and C_f)	400 µF and 2.5 µF
Inductor ripple current ($x_{L1}\%$ and $x_{L1}\%$)	≤ 10 %
Capacitor ripple voltage ($x_C\%$ and $x_{C0}\%$)	≤ 5 %

Table 2.2 List of Components and Ripple Percentage of TLIHC

Parameter	**Attributes**
Coupled inductors L_1 and L_2	2.04 mH and 2.82 mH
Filter inductor $L_{f1} = L_{f2}$	2 mH
DC link capacitor (C)	360 µF
DC and AC filter capacitor (C_0 and C_f)	400 µF and 5 µF
Inductor ripple current ($x_{L1}\%$ and $x_{L1}\%$)	≤ 10 %
Capacitor ripple voltage ($x_C\%$ and $x_{C0}\%$)	≤ 5 %

The calculated passive component values and chosen ripple percentages for both TLMPHC and TLIHC are given in Table 2.1 and Table 2.2 respectively.

2.6 Comparison of some Key Features of TLIHC with TLMPHC

To authenticate the advantages of the proposed TLIHC, a comparison between the proposed TLIHC and TLMPHC are given in Table 2.3.

Table 2.3 Comparison of Some of the Key Features of TLIHC and TLMPHC

Features	**TLIHC**	**TLMPHC**
Simultaneous AC and DC outputs	Yes	Yes
Leakage current	Low	Low
Minimum phase behaviour	Achieve	Achieve
Wide operating range of D and M_i	Not satisfied	Satisfied
Requirement of Deadtime Circuit	Not required	Not required
Inherent Shoot-through Capability	Present	Present
Current stress on input side	High	Low

It can be concluded from Table 2.3 that both the hybrid converters TLMPHC and TLIHC are capable to give both DC and AC outputs simultaneously, have reduced leakage currents and satisfy the minimum phase behaviour unlike the conventional hybrid converters. From the Table 2.3, it can also be observed that the developed TLMPHC cannot operate in wide operating range of D and M_i. However, the requirement of deadtime circuit is not required for both TLMPHC and TLIHC. Also, both the transformerless hybrid converters has inherent shoot-through capability. Hence, they have self-protected from short circuit issues. In addition, from Fig. 2.3, it can be observed that both the inductor coils (L_1 and L_2) in the input side are charging and discharging in the same instant during the shoot-through and non-shoot through states in case of TLMPHC. Therefore, the developed TLMPHC has higher current stress on the input side as compared to TLIHC. So, TLMPHC is not suitable for high power applications.

To differentiate the important features of the proposed TLIHC, a comparison among the proposed TLIHC and some of the existing topologies are given in Table 2.4.

Table 2.4 Performance Comparison of the Proposed TLIHC with Other Existing Topologies

Features	**BDHC (Boost derived hybrid converter)**	**SBI (Switched boost inverter)**	**IHC (Interleaved hybrid converter)**	**Boost cascaded dual parallel buck**	**QBDHC (Quadratic boost derived hybrid converter)**	**Proposed TLIHC**
Leakage current	High	High	High	Low	High	Low
Simultaneous DC and AC outputs	Yes	Yes	Yes	Yes	Yes	Yes
Operating conditions ($\boldsymbol{D + M_i}\leq 1$ and $\boldsymbol{D + M_i}\geq 1$)	$D + M_i \leq 1$	$D + M_i \leq 1$	Both	Both	$D + M_i \leq 1$	Both
Minimum phase behavior	Not satisfied	Not satisfied	Not satisfied	Not satisfied	Not satisfied	Satisfied
Dead time requirement	No	No	No	Yes	No	No
DC gain and AC output quality	Trade-off	Trade-off	No trade-off	No trade-off	Trade-off	No trade-off
Voltage stress on inverter bridge	$\frac{V_{in}}{1 - D_{st}}$	$(\frac{1-D}{1-2D})V_{in}$	$(\frac{1-D}{1-D-D_{st}+DD_{st}})V_{in}$	$\frac{V_{in}}{1 - D}$	$\frac{V_{in}}{(1 - D_{st})^2}$	$\frac{V_{in}}{D}$

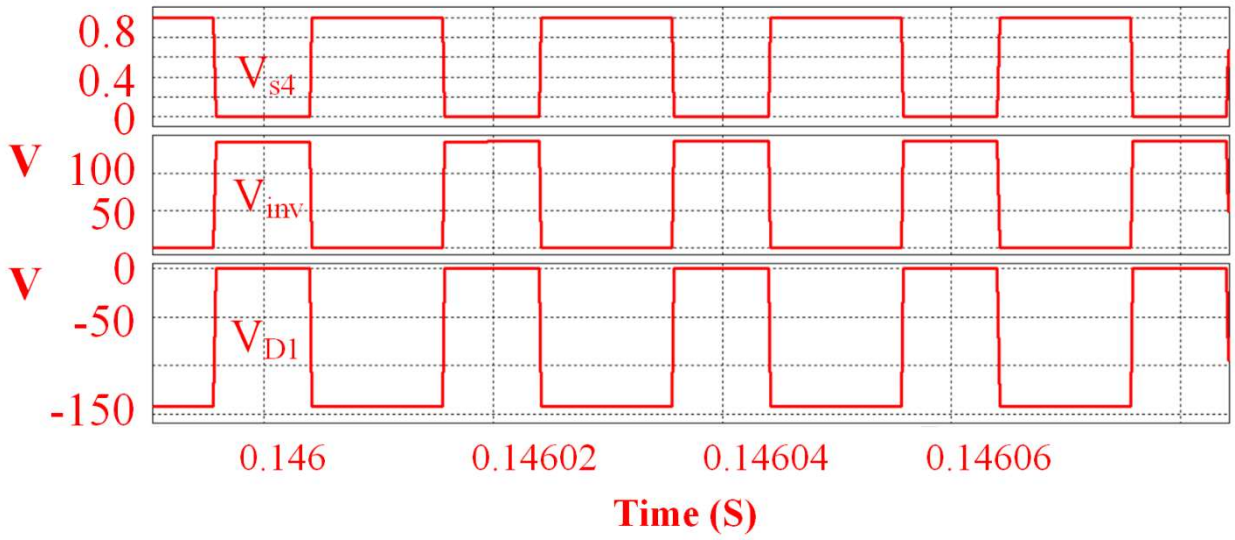
It can be concluded from Table 2.4 that the proposed TLIHC is capable of giving both DC and AC outputs simultaneously at operating conditions $D + M_i \leq 1$ and $D + M_i \geq 1$. Also, the TLIHC has reduced leakage current. The proposed TLIHC satisfies the minimum phase behaviour, unlike the other existing topologies. In addition, it does not require dead time compensation circuit, unlike the boost cascaded dual parallel buck converter (BCDPBC). Also, it can be observed from Table 2.4 that the proposed TLIHC has lower inverter bridge voltage stress at higher D as compared to the other existing topologies.

2.7 Simulation and Experimental Verifications

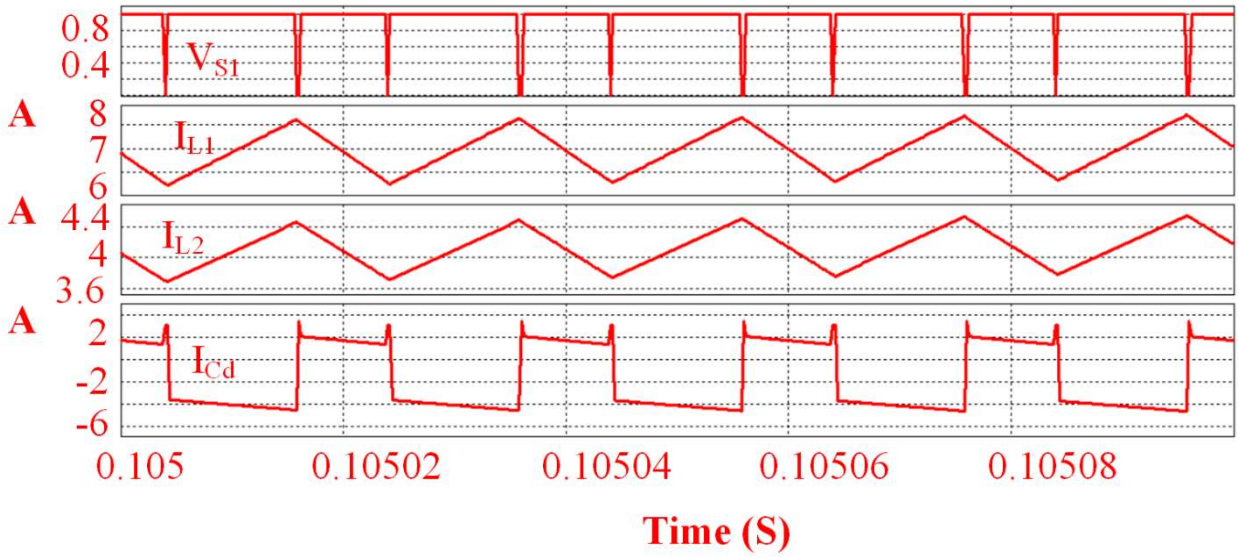
In this section, simulation and experimental verifications of operational waveforms and switching techniques of both TLMPHC and TLIHC are discussed.

2.7.1 Simulation and Experimental Verifications of TLMPHC

The simulation studies for the proposed TLMPHC are carried out using PSIM. The simulation results are shown in Fig. 2.10. Fig. 2.10 (a) shows the voltage across the diode (V_{D1}) and voltage across the inverter bridge (V_{inv}) along with the switching signal (V_{S4}) for an input voltage V_{in} = 60 V. From Fig. 2.10 (a), it can be observed that the diode D_1 is in turn-on position during both the power and zero intervals, as V_{D1} is zero during these intervals. However, during the shoot-through state, the voltage stress across the diode D_1 is maximum ≈ 142.85 V. Further, the zero-input voltage across the inverter bridge during the shoot-through state is also observed from Fig. 2.10 (a). Fig. 2.10 (b) shows the current through the coupled inductor L_1, L_2 and the DC link capacitor C_d during the switching operation of switch S_1. From Fig. 2.10 (b), it can be observed that both the inductor coils are charging simultaneously during the shoot through state and discharging during power and zero states. Similarly, the DC link capacitor is in charging mode during both the power and zero states, and in the discharging mode during the shoot-through state as observed from Fig. 2.10 (b).



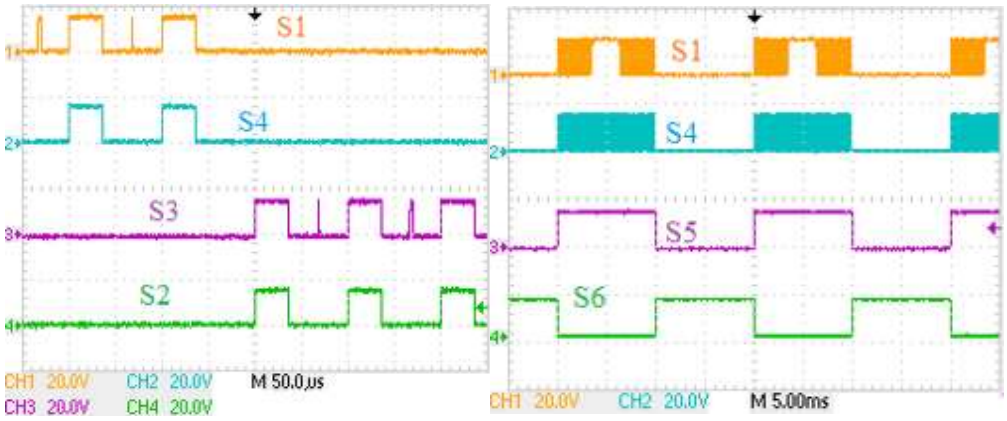
(a)



(b)

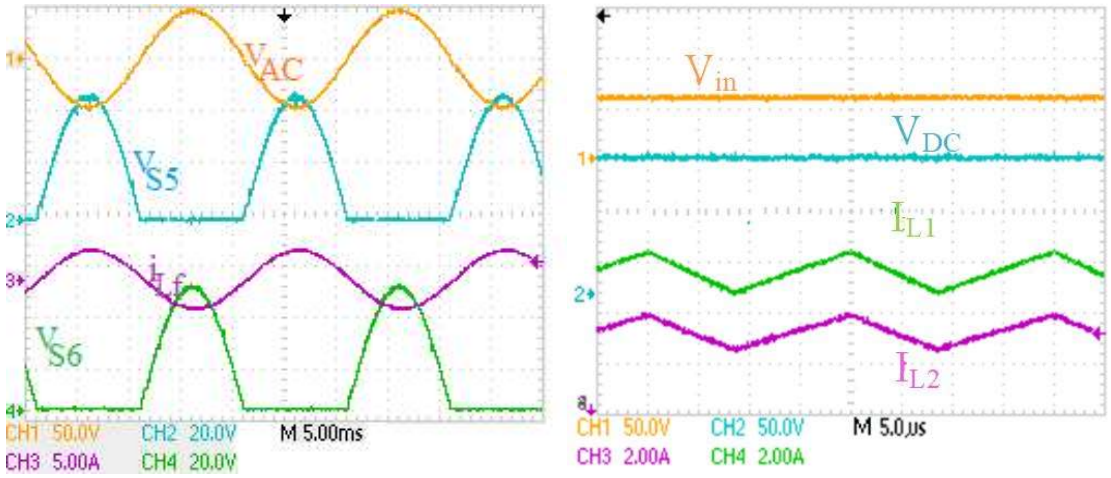
Fig. 2.10 Simulation results of TLMPHC **(a)** V_{in}, V_{AC}, I_{AC}, and $I_{leakage}$ **(b)** V_{S1}, I_{L1}, I_{L2}, and I_{Cd}. **[Y-axis has voltage/current values, having units "V" or "A"]**

The experimental results of switching pulses and operational waveforms of TLMPHC are shown in Fig. 2.11 and 2.12. The gate pulses of the controlled switches of TLMPHC are shown in Fig. 2.11 (a) and (b). Fig. 2.12 (a) shows voltage stress across the switches S_5 and S_6. As, for entire positive half cycle of the AC output voltage, S_5 is in ON position and S_6 is in OFF position and vice-versa during the entire negative half cycle, the voltage across the switch S_6 is the AC output voltage during the positive half cycle. Similarly, the voltage across the switch S_5 is the AC output voltage during the negative half cycle. Fig. 2.12 (b) shows the current through the input side magnetically coupled inductance L_1 and L_2. From the charging discharging nature of both the inductor coils, it can be observed that both the coils are charging and discharging at the same instant.



(a) **(b)**

Fig. 2.11 Switching pulses for the controlled switches of TLMPHC. **(a)** S_1, S_4, S_3, and S_4 **(b)** S_1, S_4, S_5, and S_6.



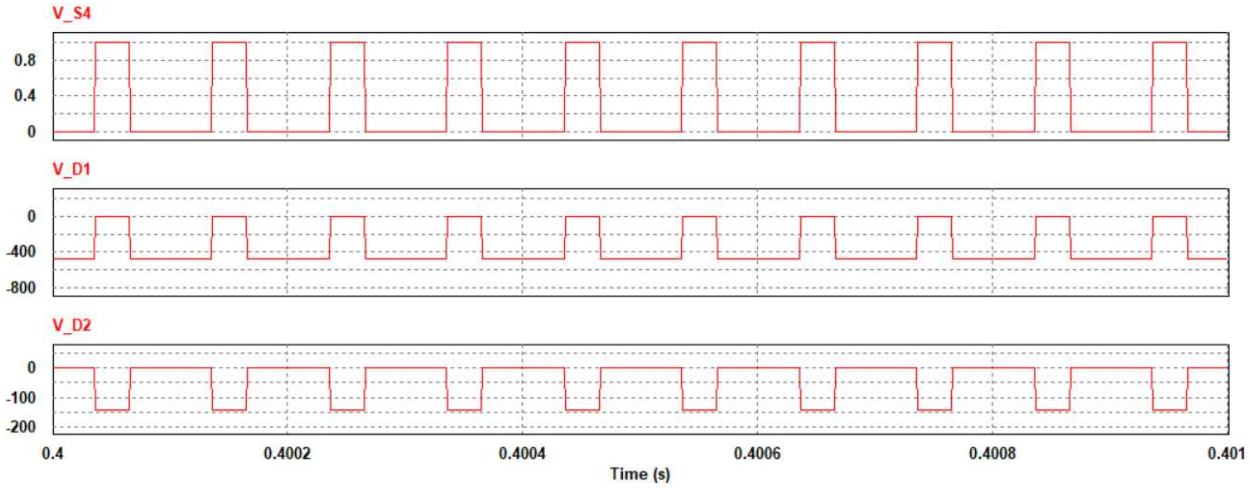
(a) **(b)**

Fig. 2.12 Experimental results of TLMPHC **(a)** V_{AC}, V_{S5}, V_{S6}, and I_{Lf} and **(b)** V_{in}, V_{DC}, I_{L1}, and I_{L2}.

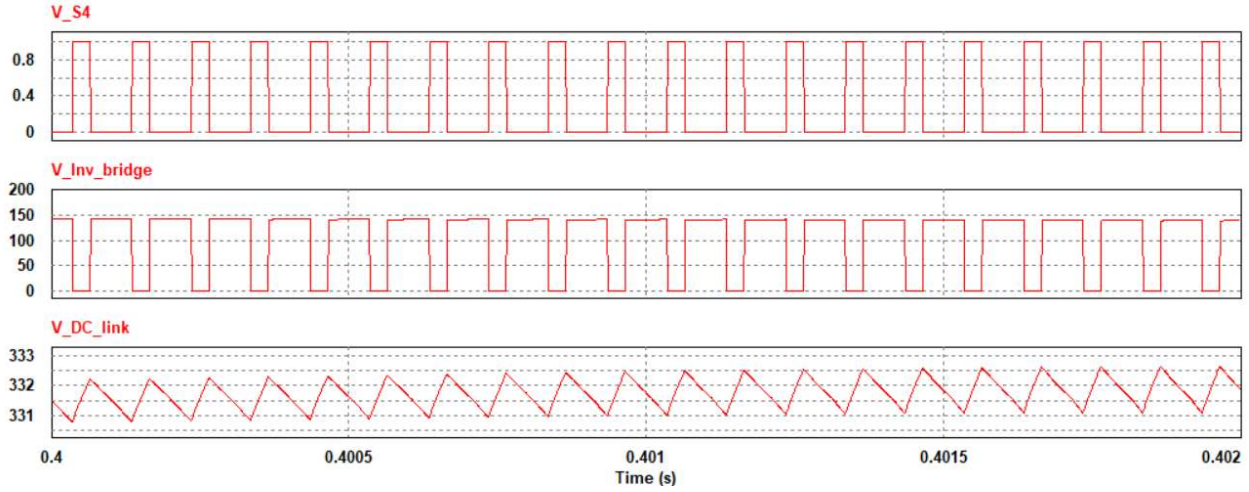
2.7.2 Simulation and Experimental Verifications of TLIHC

The simulation results of TLIHC are shown in Fig. 2.13. Fig. 2.13 (a) shows the voltage across the diode D_1 (V_{D1}) and diode D_2 (V_{D2}) along with the switching signal (V_{S4}). From Fig. 2.13 (a), it can be observed that diode D_1 is in turn-on condition during the shoot-through interval and D_2 during the non-shoot through interval. Fig. 2.13 (b) shows the voltage across the inverter bridge of TLIHC and charging discharging behaviour of DC link capacitor (C_d). It can be observed that the voltage across the inverter bridge is zero during the shoot-through interval. Similarly, from the charging

discharging profile of C_d, it can be observed that C_d is in charging mode during the shoot-through state and in discharging mode during the power and zero interval.



(a)

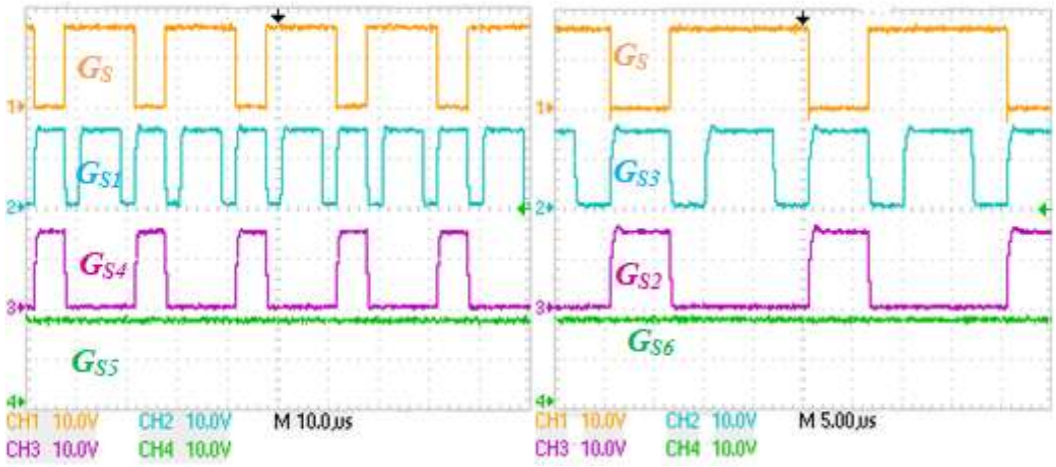


(b)

Fig. 2.13 Simulation results of TLIHC **(a)** V_{in}, V_{AC}, I_{AC}, and $I_{leakage}$ **(b)** V_{S1}, I_{L1}, I_{L2}, and I_{Cd}.

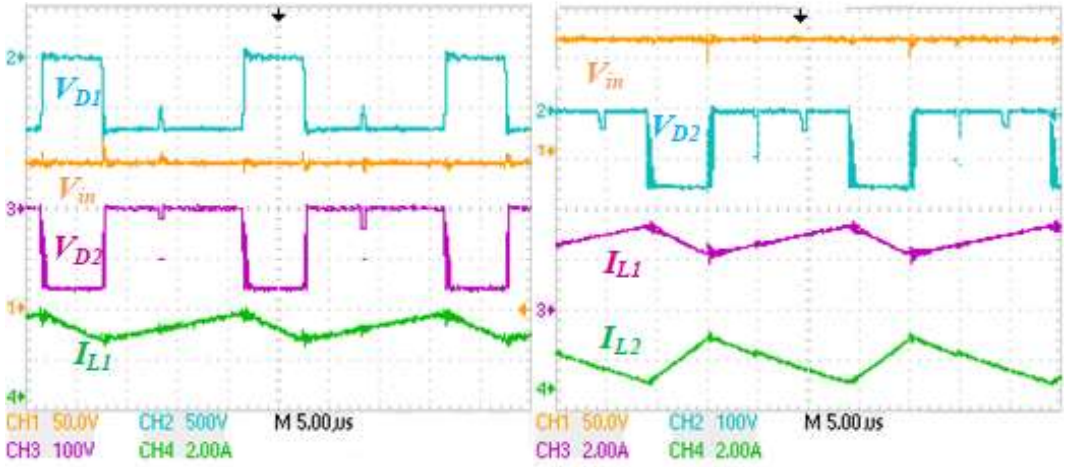
The switching pulses of the controlled switches of TLIHC are shown in Fig. 2.14. Figs. 2.14 (a) and (b) show the gate pulses of controlled switches of the proposed TLIHC during the positive and negative half cycles respectively. Fig. 2.15 (a) shows the voltage across D_1 and D_2 along with the inductor current I_{L1}, whereas Fig. 2.15 (b) shows the inductor currents (I_{L1} *and* I_{L2}). From Fig. 2.15 (a), it is observed that the voltage stress on the diode D_1 is zero during shoot-through state and that of D_2 is zero during the power and zero states. Similarly, from Fig. 2.15 (b) it is concluded that during the power and zero intervals, the inductors L_1 and L_2 are in charging and discharging

modes. Fig. 2.15 (c) shows the voltage stress across the switches S_5 and S_6 along with V_{DC} and V_{AC}.

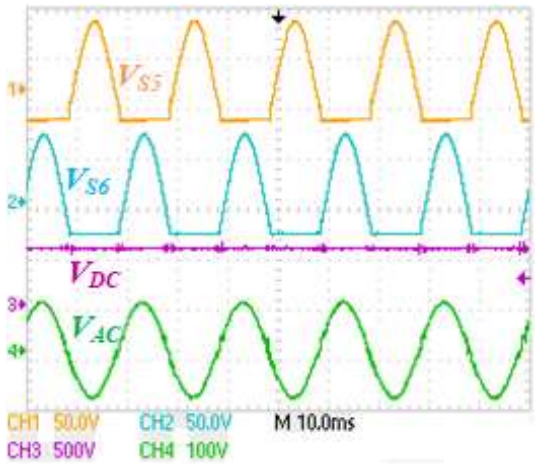


(a) **(b)**

Fig. 2.14 Switching pulses of the controlled switches of TLIHC. **(a)** Gate pulses of switches $(S, S_1, S_4$ and $S_5)$ during the positive half cycle and **(b)** Gate pulses of switches $(S, S_3, S_2$ and $S_6)$ during the negative half cycle.



(a) **(b)**



(c)

Fig. 2.15 Experimental results of the proposed TLIHC. **(a)** Voltage across diode D_1 and D_2 (V_{D1} and V_{D2}) along with $V_{in}$and I_{L1}, **(b)** inductor current I_{L1} and I_{L2} along with V_{D2} and V_{in} and **(c)** Voltage across switch S_5 and S_6 along with V_{DC} and V_{AC}.

2.8 Summary

In this chapter, the topology development along with the circuit operation of two transformerless hybrid converters named as TLIHC and TLMPHC has been presented. Both the transformerless hybrid converters give both DC and AC outputs simultaneously from a single DC source with reduced common mode leakage current. It can be observed that the inverter parts of both the converters TLIHC and TLMPHC are same. Only one extra controlled switch is added in case of TLIHC to operate the converter in wide operating range of D and M_i. Also, to increase the DC gain by a factor of $\frac{1}{D}$, a DC link capacitor is provided in case of TLIHC. Further, two hybrid unipolar based SPWM techniques are developed in this work to reduce the common-mode leakage current and to regulate the power flow between the DC and AC loads. A comparison between the proposed TLIHC and some of the existing topologies in terms of various features, such as obtaining simultaneous DC and AC outputs, achieving minimum phase behaviour, flow of harmful leakage current, operating range of the converter, inherent shoot-through capability and requirement of deadtime circuit are discussed in this chapter.