Chapter 5

Analytical Modeling for Electrical Characteristics of Double-Gate Heterojunction TFETs With a SiO_2/HfO_2 Stacked Gate-Oxide Structure

5.1 Introduction

The literature survey of Chapter-1 shows that the heterojunctions at the source/channel and drain/channel junctions can be an effective method for improving the drain current and reducing the ambipolar effect of TFETs device [Taur *et al.* (2015), Dong *et al.* (2016), Guan *et al.* (2017)]. The use of a lower band gap material than the Si at the source while maintaining Si material in both the channel and drain regions is reported to enhance the drive current and speed of the TFETs [Graef *et al.* (2014), Villani *et al*. (2015), Alam (2017), Graef *et al*. (2018)]. Thus, in the present Chapter, we will try to investigate the performance characteristics of the vertical SiO_2/high-*k* stacked gate-oxide based double-gate (DG) heterojunction (HJ) TFETs obtained by replacing the Si by Ge or any other lower bandgap materials in the source of the DG TFET structure considered in Chapter 2. Thus, the objective of the present chapter is to develop the analytical models for electrical characteristics such as surface potential, electric field, drain current and threshold voltage of the stacked gate SiO_2/HfO_2 DG HJTFETs by considering both the depletion and accumulation/inversion modes of operation of the device. Some of the results/expressions derived in Chapter 2 have been directly used in this chapter to optimize the repetition. The model results have been validated by

comparing them with the commercially available ATLAS^{TM} based TCAD simulation [ATLAS (2013)]. The layout of the present chapter can be gives as follows.

In Section 5.2, we have first developed the surface potential model for both the depletion and accumulation/inversion modes by including the source/channel and drain/channel depletion regions of the SiO_2/HfO_2 stacked gate-oxide based DG HJTFETs. The channel electric field, BTBT generation rate, drain current and threshold voltage have been modeled in the similar manner as considered in the previous chapters. The concept of TLA method has been used for developing the proposed drain current model valid for the entire (sub-threshold to strong accumulation/inversion) region of operation of the DG HJTFETs under study. Finally, threshold voltage model has been developed of the proposed device by using the shortest tunneling path concept. Section 5.3 includes some important results and discussions related to the surface potential, electric field, energy band diagram, depletion length, drain current and threshold voltage of the DG HJTFET device under study. Finally, Sec. 5.4 describes the conclusion of the present chapter.

5.2 Model Formulation

The cross-sectional view of the DG HJTFET with a SiO_2/HfO_2 stacked gate-oxide structure under study is shown in Fig. 5.1(a) where L_1, L_2 L_3, t_{ox}, t_k and t_{si} are the length of source/channel depletion region, channel length , drain/channel depletion length, SiO_2 thickness, high-*k* material (HfO_2) thickness and channel thickness of the device, respectively. The surface junction potentials ψ_0, ψ_1, ψ_2 and ψ_3 at the corresponding position $x_0 = 0$, $x_1 = L_1$, $x_2 = L_1 + L_2$ and $x_3 = L_1 + L_2 + L_3$ in the channel have also been shown in the Fig. 5.1(a). Figure 5.1(b) shows the energy band

diagram of our proposed device, where E_C and E_V represent the energy of conduction band and valance band; $E_{g,eff}$ is the effective energy band-gap at the heterojunction interface; and ΔE_C and ΔE_V are the fractions of change in the conduction and valence band appearing at Ge/Si heterojunction interface of DG HJTFET device.

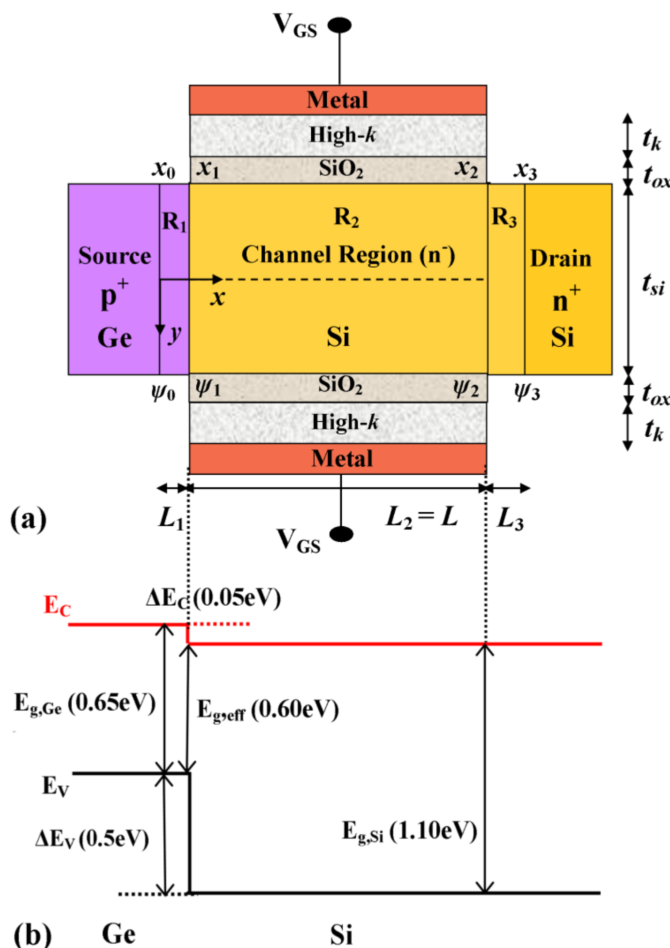

Fig. 5.1: (a) Schematic of DG HJTFET with SiO_2/HfO_2 stacked gate oxide; (b) Energy band diagram of DG HJTFET with SiO_2/HfO_2 stacked gate oxide

5.2.1 Modeling of Surface Potential

It is observed that the channel becomes either fully depleted or partially depleted and partially accumulated/inverted depending on the applied gate and drain voltages

[Lee and Choi (2011), Pal and Dutta (2016)]. We have thus derived the expressions for the surface potential separately for the two different modes in the sub-section 5.2.1.1 and 5.2.1.2, respectively.

5.2.1.1 2-D electrostatic potential in Depletion Mode

In this mode of operations, the applied gate and drain bias voltages are assumed to sufficiently low and high respectively so that channel becomes fully depleted. Thus, an expression of 2-D electrostatic channel potential $\psi_i(x,y)$ and surface potential $\psi_{s,i}(x)$ are same as discussed in the previous Chapter 2 and can be expressed as:

$$\psi_i(x,y)=\psi_{0i}(x)+\left[V_{GS}-\varphi_{FB,i}-\psi_{0i}(x)\right]\left(y/\lambda_i\right)^2 \tag{5.1}$$

$$\psi_{s,i}(x)=\psi_{0i}(x)+\left[V_{GS}-\varphi_{FB,i}-\psi_{0i}(x)\right]\left(t_{Si}/2\lambda_i\right)^2 \tag{5.2}$$

where $\psi_{0i}(x)$ is the centre potential in the channel region R_i $(i=1,2,3)$; V_{GS} is the gate-to-source voltage; $\varphi_{FB,i}=(\varphi_M-\chi_i-E_{g,i}/2)/q$ is the flat band voltage in region R_i; φ_M is the gate metal work function; q is the electronic charge; $\lambda_i=\sqrt{(1/r_i+1/4)\,t_{si}^2}$ is the characteristic length; r_i is the capacitance ratio between equivalent gate-oxide and channel region; χ_i and $E_{g,i}$ are the electron affinity and energy band gap of the materials in the region R_i $(i=1,2,3)$, respectively.

5.2.1.2 2-D Electrostatic Potential in Accumulation/Inversion Mode

In this mode of operations, the respective applied gate and drain bias voltages are assumed to be high and low so that channel becomes partially depleted and partially accumulated/inverted. Surface junction potentials in different regions R_i $\{i=1,2,3\}$ under the accumulation/inversion regions have been shown in Fig. 5.2 (a); and the

surface potential along the channel for different modes have been compared in Fig 5.2 (b). From this figure, it is observed that potential drop in the drain side is negligible (see Fig. 5.2(b)) *i.e.,* depletion length in drain side becomes zero $(L_3 = 0)$ in this mode. From the figure 5.2 (b), it is also observed that there is no difference between the surface potential for n and p-type channel materials; which means that the solution of surface potential for both type of materials is same. That is why we have used the term "accumulation/inversion" in the assumption of high gate and low drain bias.

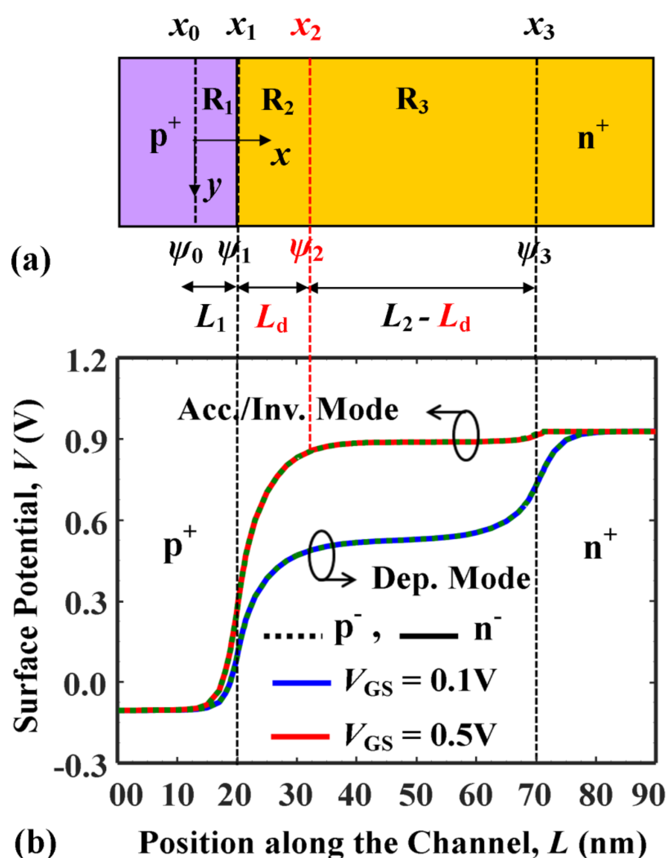

Fig. 5.2: (a) Schematic of surface junction potentials for different regions in the accumulation/inversion mode of DG HJTFET; (b) Surface potential along the channel for different mode of DG HJTFET

The surface potential in the accumulation/inversion part is pinned, and its maximum value reached at $\psi_3 = V_T \ln(N_3/n_{i,3}) + V_{DS}$ is less sensitive for V_{GS} [Lee and Young

(2011)]. Under this assumption, the electrostatic potential $\psi_i(x, y)$ in (accumulation/inversion part) region R_3 governed by 2-D Poisson's equation can be written as:

$$\frac{\partial^2 \psi_3(x, y)}{\partial x^2} + \frac{\partial^2 \psi_3(x, y)}{\partial y^2} = \frac{q n_{i,3} \exp\left((\psi_3(x, y) - V_{DS})/V_T)\right)}{\varepsilon_{i,3}} \tag{5.3}$$

where, V_{DS} is the drain-to-source voltage; V_T is the thermal voltage; N_3 is the drain doping concentration and, $n_{i,3}$ and $\varepsilon_{i,3}$ are the intrinsic carrier concentration and permittivity of the region R_3 respectively.

Using the superposition method [Dubey *et al.* (2010), Gholizadeh and Hosseini (2014), Chander and Baishya (2016)], Equation (5.3) can be solved by assuming $\psi_3(x, y) = u(y) + v(x, y)$, where $u(y)$ is due to majority charge carriers and solved by 1-D Poisson's equation; and $v(x, y)$ is obtained by solving the 2-D Laplace equation. The 1-D Poisson`s equation for $u(y)$ can be expressed as [Taur *et al.* (2004)]:

$$\frac{\partial^2 u(y)}{\partial y^2} = \frac{q n_{i,3} \exp\left((u(y) - V_{DS})/V_T)\right)}{\varepsilon_{i,3}} \tag{5.4}$$

$$u(y) = V_{DS} - 2V_T \ln\left[\frac{t_{si}}{2\eta}\sqrt{\frac{q n_{i,3}}{2\varepsilon_{i,3} V_T}} \cos\left(\frac{2\eta y}{t_{si}}\right)\right] \tag{5.5}$$

where η is satisfied the equation

$$\left(\frac{V_{GS} - \phi_{FB,3} - V_{DS}}{2V_T}\right) - \ln\left[\frac{2}{t_{si}}\sqrt{\frac{2\varepsilon_{i,3} V_T}{q n_{i,3}}}\right] = \ln\eta - \ln\left(\cos(\eta)\right) + \frac{2\eta\tan\eta}{r_3} \tag{5.6}$$

The 2-D Laplace equation for $v(x, y)$ can be written as:

$$\frac{\partial^2 v(x, y)}{\partial x^2} + \frac{\partial^2 v(x, y)}{\partial y^2} = 0 \tag{5.7}$$

and its solution is given by [Pal and Dutta (2016)]:

$$v(x,y) = f_3\left[1+(r_3/4)-(r_3 y/t_{si})^2\right]\exp\left(\sqrt{2}(x-L_d)/\lambda_3\right) \tag{5.8}$$

where r_3 and λ_3 are the capacitance ratio and characteristics length of the region R_3; N_2 is the channel doping concentration; f_3 is a constant and obtained by substituting $v(x,\pm t_{si}/2)=\psi_3$ at $x=L$ in Eq. (5.8); and L_d is the depletion length in the region R_2 and can be expressed as [Sze (1981)]:

$$L_d = \left(\frac{1}{\beta_2}\right)\cosh^{-1}\left[\frac{2\psi_o-(qN_2t_{si}^2/r_2\varepsilon_{si})-2(V_{GS}-\varphi_{FB,2}-f_3)}{u(y)-V_{GS}+\varphi_{FB,2}-(qN_2t_{si}^2/2r_2\varepsilon_{si})}\right] \tag{5.9}$$

Finally, the channel and surface potential in region R_3 can be expressed as:

$$\psi_3(x,y) = u(y)+f_3\left[1+(r_3/4)-(r_3 y/t_{si})^2\right]\exp\left(\sqrt{2}\,(x-L_d)/\lambda_3\right) \tag{5.10}$$

$$\psi_{S,3}(x) = \left[V_{DS}-2V_T\ \ln\left(\frac{t_{si}}{2\eta}\sqrt{\frac{qn_{i,3}}{2\varepsilon_{i,3}V_T}}\cos(\eta)\right)+f_3\exp\left(\frac{\sqrt{2}(x-L_d)}{\lambda_3}\right)\right] \tag{5.11}$$

The electrostatic channel potential $\psi_i(x,y)$ and surface potential $\psi_{S,i}(x)$ for regions R_i $(i=1,2)$ can be obtained in the same manner as obtained for the depletion mode including the intermediate surface junction potentials ψ_1 and ψ_2.

Note that, the primary difference between homo and heterojunction TFET devices are built-in-potential (ψ_0) and the effective energy band gap $(E_{g,eff})$ which is formed at the source/channel junction; and can be expressed as [Guan *et al.* (2017)]:

$$\psi_0 = \frac{-1}{q}\left((\chi_1-\chi_2)+0.5(E_{g,1}-E_{g,2})+qV_T\ \ln(N_1/n_{i,1})\right) \tag{5.12}$$

$$E_{g,eff} = (E_{g,2}-\Delta E_C) \tag{5.13}$$

where N_1 is source doping concentration; $n_{i,1}$ is the intrinsic carrier concentration of the region $R_i\,(i=1)$, and

$$\Delta E_C = \frac{1}{q}\left((\chi_2-\chi_1)+(E_{g,2}-E_{g,1})\right) \tag{5.14}$$

For $\chi_1=\chi_2$ and $E_{g,1}=E_{g,2}$ in homojunction TFETs, we get $\psi_0=-V_T\ln(N_1/n_{i,1})$ and $E_{g,eff}=E_g$ as discussed in Chapter 2.

5.2.2 Modeling of Drain Current

The band-to-band tunneling generation rate (G_{BTBT}) from valance band of the source to conduction band of the channel can be expressed by Kane's model, [Kane (1960)]

$$G_{BTBT} = A_{Kane}E^{\alpha}\exp\left(-\frac{B_{Kane}}{E}\right) \tag{5.15}$$

where E is the local electric field; α is a material-dependent constant parameter and, $A_{Kane}=(q^2 m_r^{1/2}/18\pi\hbar^2 E_{g,eff}^{1/2})$ and $B_{Kane}=(\pi m_r^{1/2}E_{g,eff}^{3/2}/2q\hbar)$ are process-dependent tunneling parameters [Kane (1960)], [Kao *et al.* (2014)]. $E_{g,eff}$ is the effective energy band gap ; m_r is the effective tunneling mass; The drain current (I_d) is obtained by integrating the G_{BTBT} over the entire tunneling volume and can be expressed as:

$$I_d = q\int_{Voiume} G_{BTBT}\,dV = qt_{si}\int G_{BTBT}(x)\,dx\,dw \tag{5.16}$$

Since BTBT of charge carriers mainly occurs due to lateral electric field [Vishnoi and Kumar (2014), Gholizadeh and Hosseini (2014)], Guan *et al.* (2017)] the local electric field (E) in Eq. (5.15) is replaced by the lateral electric field $E_x=-\partial\psi_i(x,y)/\partial x$ to compute the G_{BTBT}. The variation of lateral electric field (E_x) along the channel and its

corresponding G_{BTBT} have been shown in Fig. 5.3 (a) and 5.3(b) respectively. The magnitude of E_x at the drain-channel junction is observed to be neglected as compared to that of the source-channel junction for high V_{GS} values while E_x at the source/channel and drain/channel junctions are comparable for low V_{GS} values and hence its effect must be included for accurate modeling of G_{BTBT} calculation.

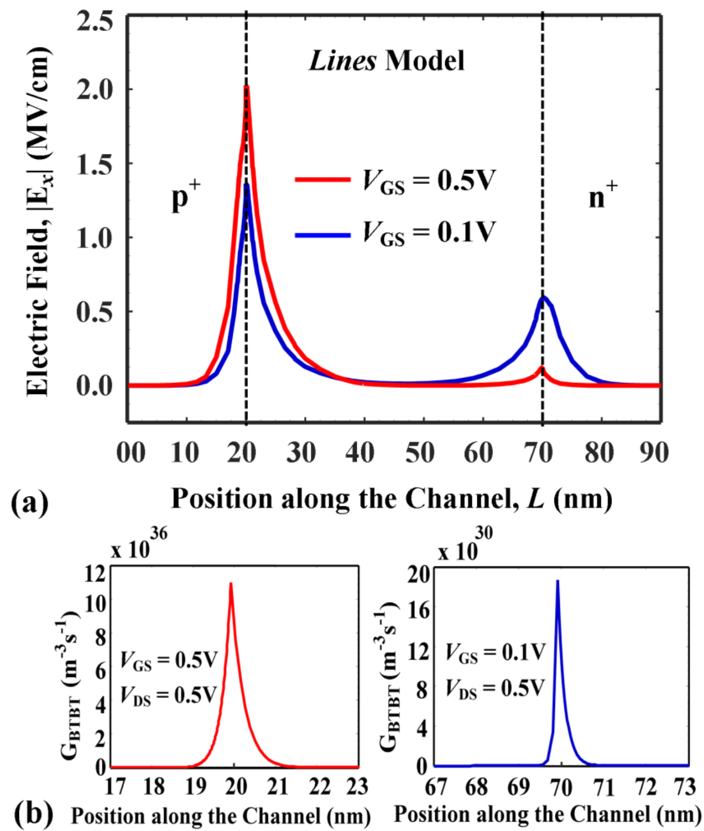

Fig. 5.3. Comparisons of (a) E_x , and (b) G_{BTBT} along the channel for different V_{GS} and constant V_{DS} = 0.5V of DG HJTFET

Magnitude of E_x at the both junction source/channel (S/Ch.) and drain/channel (D/Ch.) for different combinations of V_{GS} and V_{DS} is summarized in Table 5.1. It is observed that for $V_{GS} > 0.3\text{V}$ and different V_{DS} (*i.e.*, accumulation/inversion regime), the magnitude of E_x at drain/channel junction is negligible as compared to that of the source/channel

junction. In subthreshold regime (*i.e.,* $V_{GS} \leq 0.3\text{V}$ but for different V_{DS}), the magnitude of E_x at drain/channel junction cannot be neglected as compared to that of the source/channel junction. Thus, we have considered the effect of the subthreshold regime for accurate modeling of G_{BTBT} in the present chapter. We have obtained G_{BTBT} by assuming two different regimes: accumulation/inversion regime at high V_{GS} and subthreshold regime at low V_{GS}, each of which is described in the subsection 5.2.2.1 and 5.2.2.2, respectively.

TABLE 5.1

COMPARISONS OF BOTH JUNCTION ELECTRIC FIELDS AS A FUNCTION OF V_{GS} FOR DIFFERENT V_{DS}

	V_{GS} = 0.1V		**V_{GS} = 0.3V**		**V_{GS} = 0.5V**		**V_{GS} = 0.7V**	
V_{DS}	E_x (MV/cm)		E_x (MV/cm)		E_x (MV/cm)		E_x (MV/cm)	
	S/Ch.	D/Ch.	S/Ch.	D/Ch	S/Ch.	D/Ch	S/Ch	D/Ch
0.3V	1.40	0.38	1.70	0.10	2.00	0.02	2.20	0.01
0.5V	1.40	0.60	1.70	0.40	2.00	0.03	2.20	0.02
0.7V	1.40	0.70	1.70	0.50	2.00	0.10	2.20	0.05

5.2.2.1 BTBT Generation Rate in Strong Accumulation/Inversion Regime

The variation of G_{BTBT} along the channel of DG HJTFETs is shown in Fig. 5.4 for high gate bias voltage (*i.e.,* accumulation/inversion regime). We have used the tangent line approximation (TLA) method [Vishnoi and Kumar (2014)], [Guan *et al.* (2017)] for finding the area of G_{BTBT} curve as follows.

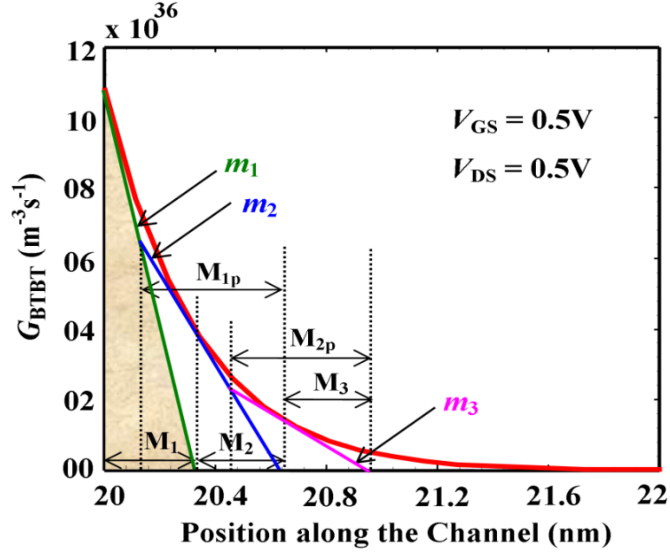

Fig. 5.4. G_{BTBT} along the channel for high V_{GS} (V_{GS} = 0.5V) of DG HJTFET with SiO_2/HfO_2 stacked gate oxide at constant $V_{DS} = 0.5$V

The areas under the tangent lines m_1, m_2 and m_3 to its x intercept M_1, $(M_1 + M_2)$ and $(M_1 + M_2 + M_3)$ as

$$G_1 = 0.5G'_{BTBT}(L_1)M_1^2 \quad (5.17)$$

$$G_2 = 0.5G'_{BTBT}(L_1 + M_1)M_{1p}^2 \quad (5.18)$$

$$G_3 = 0.5G'_{BTBT}(L_1 + M_1 + M_2)M_{2p}^2 \quad (5.19)$$

where,

$$M_1 = G_{BTBT}(L_1)/G'_{BTBT}(L_1) \quad (5.20)$$

$$M_2 = G_{BTBT}(L_1 + M_1)/G'_{BTBT}(L_1 + M_1) \quad (5.21)$$

$$M_{1p} = G'_{BTBT}(L_1)M_2/\left[G'_{BTBT}(L_1) - G'_{BTBT}(L_1 + M_1)\right] \quad (5.22)$$

$$M_{2p} = \left[\frac{G'_{BTBT}(L_1 + M_1)M_3}{G'_{BTBT}(L_1 + M_1) - G'_{BTBT}(L_1 + M_1 + M_2)} \right] \tag{5.23}$$

$$M_3 = \left[\frac{G_{BTBT}(L_1 + M_1 + M_2)}{G'_{BTBT}(L_1 + M_1 + M_2)} \right] \tag{5.24}$$

Now, the overlap area between the tangent lines m_1 & m_2 and m_2 & m_3 are given by

$$G_{1p} = 0.5G'_{BTBT}(L_1)(M_{1p} - M_2)^2 \tag{5.25}$$

$$G_{2p} = 0.5G'_{BTBT}(L_1)(M_{2p} - M_3)^2 \tag{5.26}$$

Repeating the process for n number of times, the generalized form of G_n and $G_{(n-1)p}$ are expressed as:

$$G_n = \frac{G'_{BTBT}}{2}\left[(L_1 + M_1 + M_2 + \dots\dots\dots\dots + M_{n-1})M^2_{(n-1)p}\right] \tag{5.27}$$

$$G_{(n-1)p} = \frac{G'_{BTBT}}{2}\left[(L_1 + M_1 + M_2 + \dots\dots\dots\dots + M_{n-2})(M_{(n-1)p} - M_n)^2\right] \tag{5.28}$$

where

$$M_{(n-1)p} = \left[\frac{G'_{BTBT}(L_1 + M_1 + M_2 \dots\dots\dots\dots + M_{n-2})M_n}{M'_{BTBT} - M_{BTBT}} \right] \tag{5.29}$$

$$M_n = \left[\frac{G_{BTBT}(L_1 + M_1 + M_2 \dots\dots\dots\dots + M_{n-1})}{G'_{BTBT}(L_1 + M_1 + M_2 \dots\dots\dots\dots + M_{n-1})} \right] \tag{5.30}$$

$$M'_{BTBT} = G'_{BTBT}(L_1 + M_1 + M_2 \dots\dots\dots\dots + M_{n-2}) \tag{5.31}$$

$$M_{BTBT} = G'_{BTBT}(L_1 + M_1 + M_2 + \dots\dots\dots M_{n-1}) \tag{5.32}$$

The total BTBT generation rate in the strong accumulation/inversion regime can be expressed as the difference between the sum of areas under the tangent lines and sum of

overlap areas between the tangent lines in n numbers of steps as:

$$G_{\mathrm{BTBT}}(A/I)=\left[\left(G_1+G_2+\ldots\ldots\ldots\ldots+G_n\right)-\left(G_{1p}+G_{2p}+\ldots\ldots+G_{(n-1)\mathrm{p}}\right)\right] \tag{5.33}$$

5.2.2.2 BTBT Generation Rate in Subthreshold Regime

For sub-threshold regime (*i.e.,* low gate voltage), the variation of G_{BTBT} along the channel of DG HJTFET is shown in Fig.5.5. The area of G_{BTBT} curve in subthreshold regime can be obtained by the TLA method in the same manner as considered earlier for the strong accumulation/inversion regime and can be expressed as:

$$G_{\mathrm{BTBT}}(Sub)=G_{\mathrm{BTBT}}(A/I)\big|_{L_1\Rightarrow L_1+L_2} \tag{5.34}$$

Since, both $G_{BTBT}(\mathrm{A/I})$ and $G_{BTBT}(\mathrm{Sub})$ are symmetrical about the interface junction, the total band-to-band tunneling generation rate (G_{TBTBT}) can be expressed as:

$$G_{TBTBT}=2\left(G_{BTBT}(A/I)+G_{BTBT}(Sub)\right) \tag{5.35}$$

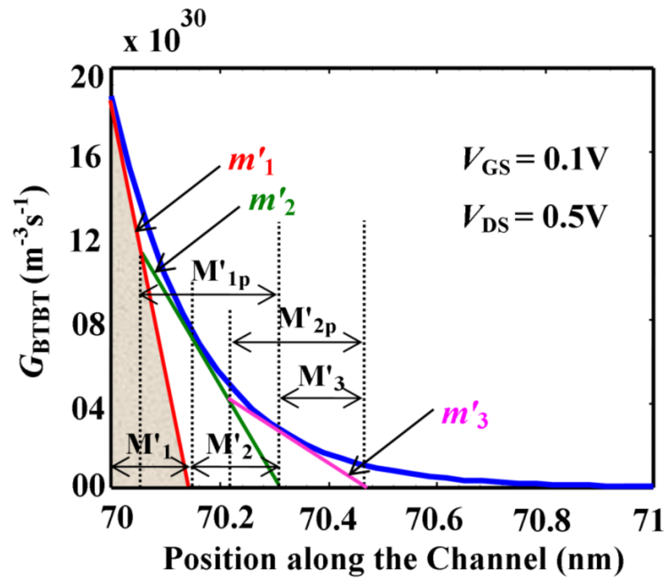

Fig. 5.5: G_{BTBT} along the channel for low V_{GS} (V_{GS} = 0.1V) of DG HJTFET with SiO_2/HfO_2 stacked gate oxide at constant V_{DS} = 0.5V

It is clear from Fig. 5.4 and Fig. 5.5 that the accuracy of TLA method can be improved (from 56% to 95%) by increasing the number of steps n (from 1 to 4). We have considered $n = 4$ in our model for better accuracy and efficiency [Vishnoi and Kumar (2014) , Guan *et al.* (2017)]. Assuming a fixed channel width $(w = 1\mu m)$ in Eq. (5.16), I_d can be expressed in $(Amp/\mu m)$ as:

$$I_d = qt_{si}G_{\text{TBTBT}}\, f_{\text{fermi}} \tag{5.36}$$

where $f_{fermi} = 1 - 2/(1 + \exp(V_{DS}/\xi V_T))$ is the correction factor, in which ξ is an empirical parameter, introduced to ensure zero drain current at $V_{DS} = 0\text{V}$ in the output characteristics [Zhang and Chan (2014)] of the device.

5.2.3 Modeling of Threshold Voltage

The threshold voltage (say V_{th}) is an important parameter of any TFET devices; and can be defined as the gate voltage (V_{GS}) at which the energy tunneling barrier tends to saturate [Boucart and Ionescu (2008)]. The concept of shortest tunneling path $(L_t^{\min})$ has been used to extract the threshold voltage (V_{th}) of the devices [Chander and Baishya (2015)]. When the surface potential at $x = L_t^{\min}$ reaches the potential $V_{DS} + V_T \ln(N_4/n_i)$, for $V_{DS} \le 0.5\text{V}$ [Chander and Baishya (2015)]; then exponential function of I_d becomes a linear function of applied V_{GS}; and the corresponding $V_{GS} = V_{th}$ which is obtained by solving the following equation:

$$\psi_{s,i}(x = L_t^{\min})\Big|_{V_{GS}=V_{th}} = V_{DS} + V_T \ln(N_4/n_i) \tag{5.37}$$

where, V_{DS}, N_4, and E_g are the drain-to-source voltage, drain doping concentration, and energy band gap of channel, respectively.

5.3 Result and Discussion

In this section, we will present our model results and their comparison with the ATLAS^{TM} TCAD simulation data for validation of our proposed models developed for the DG HJTFETs. The Shockley-Read-Hall recombination (SRH), Non-local BTBT, concentration and electric field dependent Lombardi (CVT), Auger recombination and bandgap-narrowing (BGN) models have been adopted for TCAD simulation of the device. We have neglected the effect of quantum confinement by assuming a channel thickness above 10nm for which the energy states of both the valance band of the source and conduction band of the channel region are continuum in nature [Omura (1993), Vandenberghe *et al.* (2011)]. In this chapter, "Hetero" and "Homo" acronyms are used for Si/Ge DG HJTFET and conventional DG TFET structures respectively. The doping concentration of source (homo), $N_{1h} = 1e20cm^{-3}$, source (hetero), $N_1 = 5e19cm^{-3}$, channel, $N_2 = 1e16cm^{-3}$ and drain, $N_3 = 5e18cm^{-3}$ with $L = 50nm$, $t_{ox} = 1nm$, $t_k = 2nm$, and gate work function is $\varphi_M = 4.2eV\,(Mo, IrO_2)$. Figure 5.6 shows the simulated electron concentration (EC) along the channel for different V_{GS} at constant $V_{DS} = 0.5V$. It is observed from the figure that device can be operated either in the depletion for $EC < 10^{16}cm^{-3}$ or accumulation/inversion for $EC >> 10^{16}cm^{-3}$ modes depending on the applied V_{GS} bias voltages. The variation of surface potential against V_{GS} for different V_{DS} is shown in Fig. 5.7. It also clearly shows that the device operation in the depletion or accumulation/inversion regime depends not only on V_{GS} but also on V_{DS}. Further, the surface potential is pinned due to accumulation/inversion formation in the channel for V_{GS} more a certain value. Thus, the inclusion of both the depletion and accumulation/inversion charges in our model of drain current is well justified.

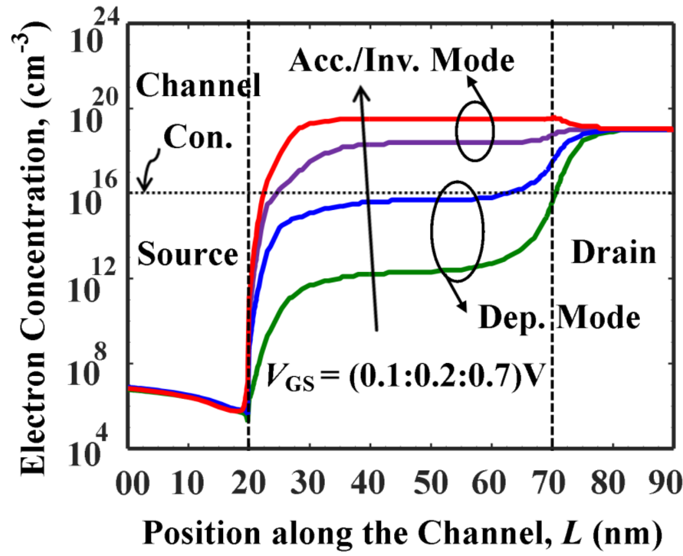

Fig. 5.6: Electron concentration along the channel for different V_{GS} of DG HJTFET with SiO_2/HfO_2 gate oxide at $V_{DS} = 0.5V$, $L = 50nm$, $t_{si} = 12nm$

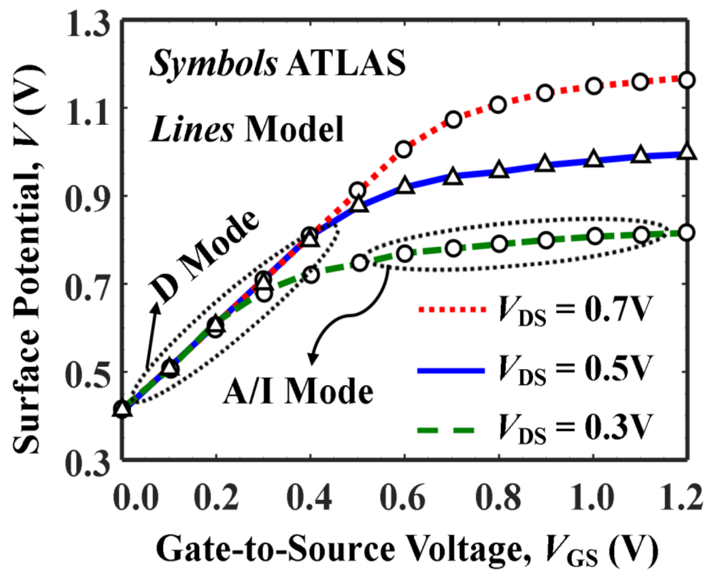

Fig. 5.7: Variation of surface potential against V_{GS} for different V_{DS} of DG HJTFET with SiO_2/HfO_2 gate oxide at $L = 50nm$, $t_{si} = 12nm$

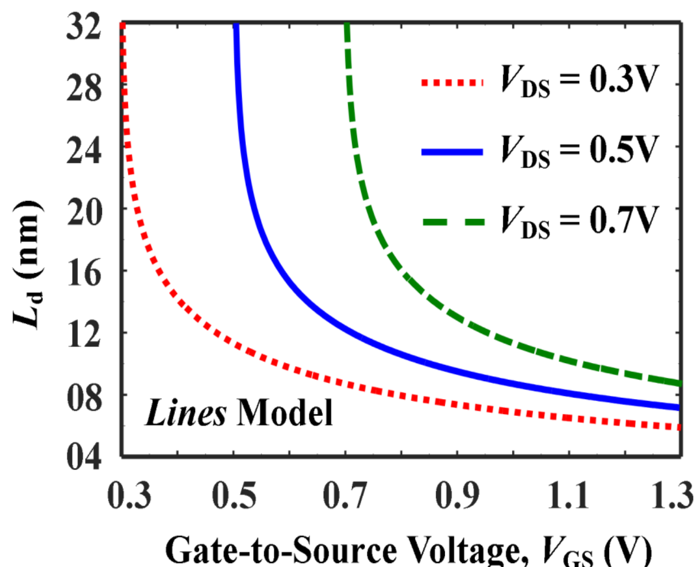

Fig. 5.8: Variation of L_d against V_{GS} for different V_{DS} of DG HJTFET with SiO_2/HfO_2 gate oxide at L = 50nm, t_{si} = 12nm

Figure 5.8 shows the variation of depletion length (L_d) against V_{GS} for different V_{DS}. When either V_{GS} or V_{DS} is increased, L_d is decreased due to accumulation/inversion charge in the channel. Note that the channel is fully depleted $(i.e. L_d = L)$ for $V_{GS} \le 0.3\text{V} = \text{V}_{DS}$, $V_{GS} \le 0.5\text{V} = \text{V}_{DS}$ and $V_{GS} \le 0.7\text{V} = \text{V}_{DS}$ since no accumulation/inversion layer is formed in this case. The simulated energy band diagram along the channel for different homo and hetero DG TFET structures is shown in Fig. 5.9 for ON state condition. It shows that both tunneling length (L_t) [Gholizadeh and Hosseini (2016)] and potential barrier (PB) are decreased in the heterojunction devices.

Fig. 5.10 compares the variation of I_d against V_{GS} between homo and heterojunction devices with and without considering the subthreshold regime. It is observed that model results of homojunction device with or without using subthreshold regime are better matched with the TCAD simulation data. However, mismatching between the model and simulation results of heterojunction device in subthreshold region is observed when

the charge under subthreshold regime is neglected. Thus, the effect of subthreshold regime is included in our model for improving the accuracy of drain current in heterojunction devices.

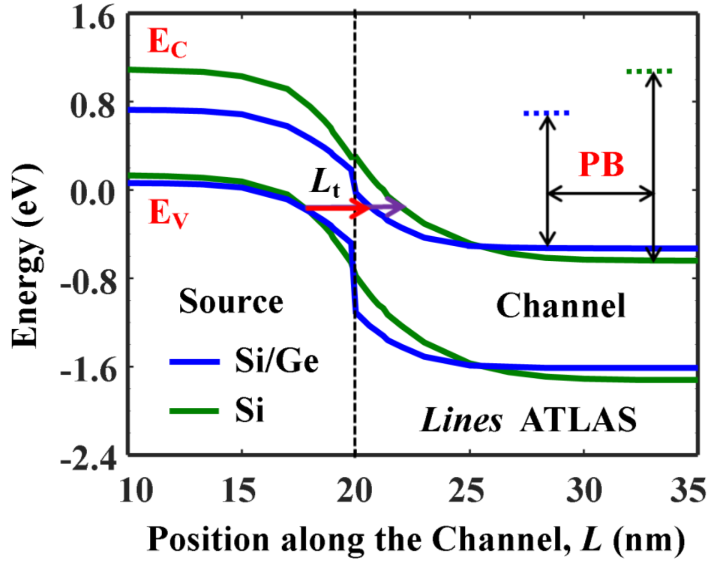

Fig. 5.9: Comparisons of energy band diagram of homo (Si) and hetero (Si/Ge) DG TFET in ON-state (V_{GS} = V_{DS} = 0.5V).

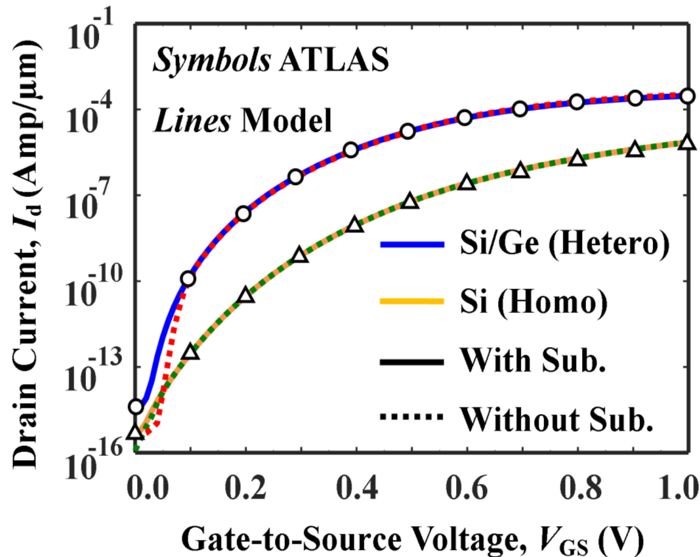

Fig. 5.10: Variation of I_d against V_{GS} for Si (Homo) and Si/Ge (Hetero) SiO_2/HfO_2 stacked gate DG TFET with & without subthreshold regime oxide at L = 50nm, t_{si} = 12nm, V_{DS} = 0.5V

The output characteristics of the heterojunction device for different V_{GS} stacked gate DG HJTFET is shown in Fig. 5.11. The increased V_{GS} lower the tunneling barrier, which in turn, increases the current by allowing large number of electron transfers from the source to channel regions.

The variation of I_d against V_{GS} for different homo and heterojunction TFET devices, shown in Fig. 5.12, demonstrates that both the ON and OFF currents are increased with low band gap materials in homojunction devices which results the decrease of I_{ON}/I_{OFF} current ratio. However, in case of heterojunction devices, an improvement in the ON current without degrading the OFF current improves the I_{ON}/I_{OFF} significantly.

The transfer characteristic of DG HJTFET device for different channel length (L) is shown in Fig. 5.13. Note that both the ON and OFF currents are increased for $L < 50\text{nm}$. For $L > 50\text{nm}$ (*e.g.*, $L = 300\text{nm}$), the ON current is decreased with the channel length. It is observed that $L = 50\text{nm}$ is the best suitable for higher ON/OFF current ratio.

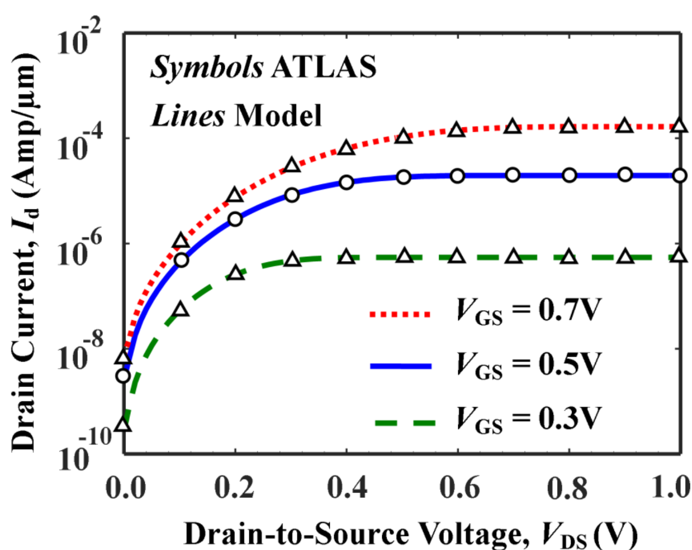

Fig. 5.11: Variation of I_d against against V_{DS} for different V_{GS} of DG HJTFET with SiO_2/HfO_2 stacked gate oxide at L = 50nm, t_{si} = 12nm

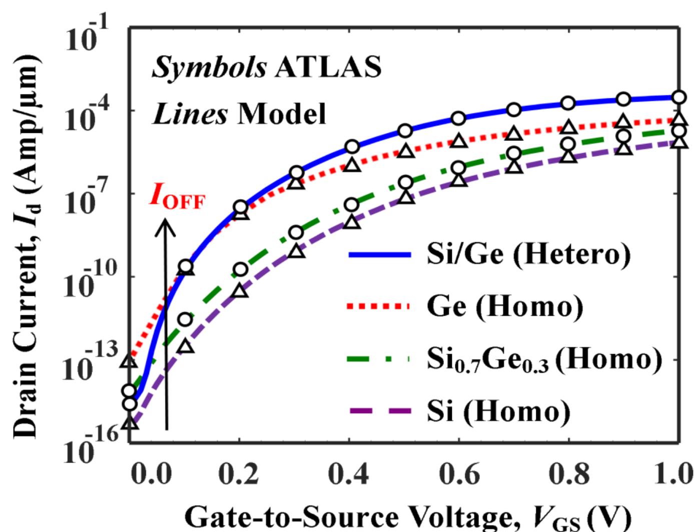

Fig. 5.12: Variation of I_d against V_{GS} for different homo and heterojunction DG TFET device at $V_{DS} = 0.5$V, $L = 50$nm, $t_{si} = 12$nm

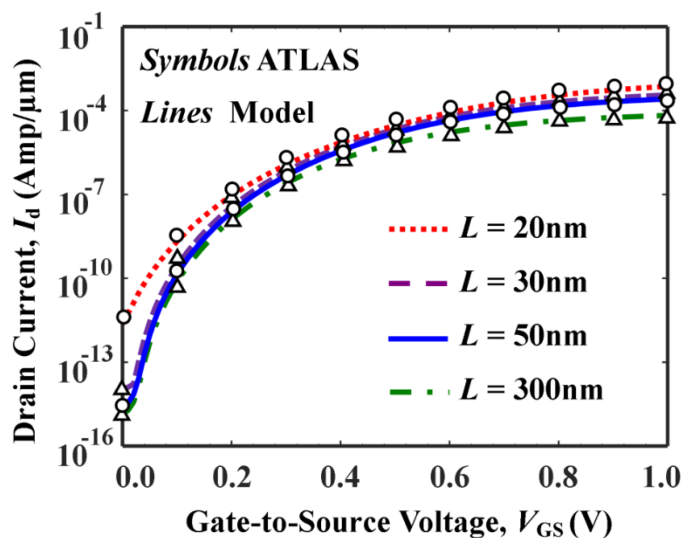

Fig. 5.13: Variation of I_d against V_{GS} for different channel length of DG HJTFET with SiO_2/HfO_2 stacked gate oxide at $V_{DS} = 0.5$V, $L = 50$nm, $t_{si} = 12$nm

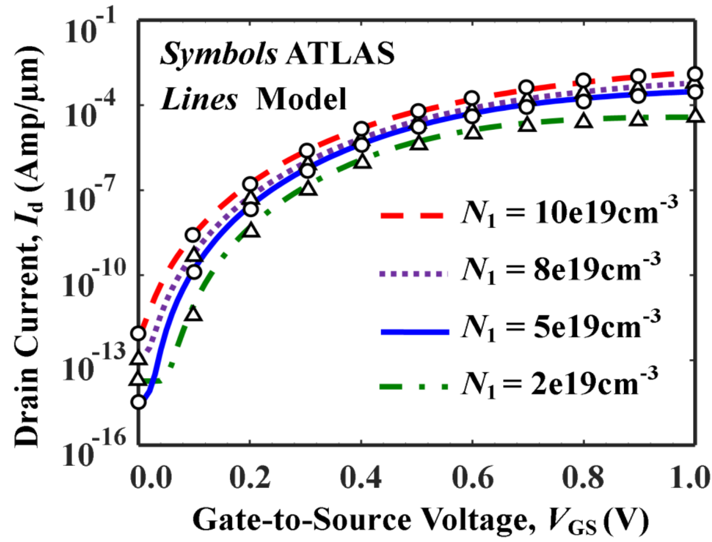

Fig. 5.14: Variation of I_d against V_{GS} for different source doping concentration (N_1) of DG HJTFET device with SiO_2/HfO_2 stacked gate oxide at V_{DS} = 0.5V, L = 50nm, t_{si} = 12nm

Since the source doping concentration (N_1) is very sensitive parameter to drain current for any TFET device, we have shown the variation of I_d against V_{GS} for different N_1 of DG HJTFET with SiO_2/HfO_2 stacked gate oxide in Fig. 5.14. For $N_1 > 5\times10^{19}\text{cm}^{-3}$, both the ON and OFF currents are increased resulting in no significant improvement in ON/OFF current ratio. On the other hand, the ON current decreases with $N_1 < 5\times10^{19}\text{cm}^{-3}$. However, the improvement in the ON current without degrading the OFF current is observed for $N_1 = 5\times10^{19}\text{cm}^{-3}$ which gives the optimum value of N_1.

Our proposed model is not only valid for the Si/Ge DG HJTFET device, but also for other devices like SOI HJTFETs [Chander and Baishya (2016)] and InAS/GaSb (GaSb as a Source) DG HJTFETs [Mehta *et al.* (2016)]. The variation of I_d against V_{GS} for different combinations of the dielectric constants of both SOI HJTFET and InAS/GaSb DG HJTFET structures are shown in Fig. 5.15 and Fig. 5.16.

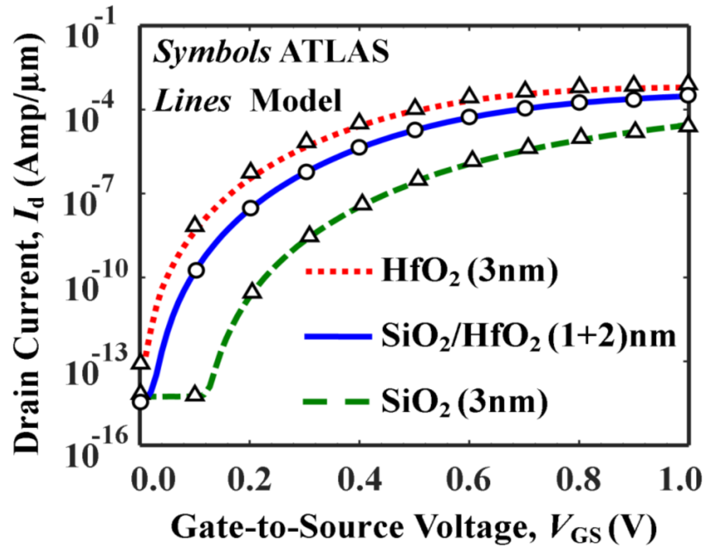

Fig. 5.15: Variation of I_d against V_{GS} for different combinations of dielectric constant of SOI HJTFET with SiO_2/HfO_2 stacked gate oxide at V_{DS} = 0.5V, L = 50nm, t_{si} = 12nm

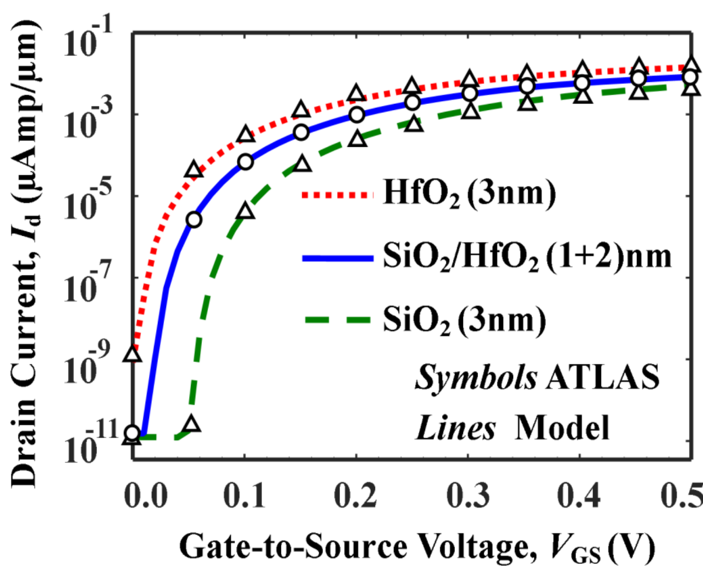

Fig. 5.16: Variation of I_d against V_{GS} for different combinations of dielectric constant of InAS/GaSb DG HJTFET with SiO_2/HfO_2 stacked gate oxide at V_{DS} = 0.3V and φ_M = 4.7eV.

The primary difference between SOI and DG HJTFET is the characteristics length (λ_i) and its value for SOI HJTFET is $\lambda_i = \sqrt{(2/r_i + 3/4)\, t_{si}^2}$. The vertical electric field in the channel/buried oxide interface has been assumed to be negligible due to high buried oxide thickness $(t_{box} = 300\text{nm})$[Chander and Baishya (2015)].

It is observed from Fig. 5.15 and Fig. 5.16 that I_d of both SOI HJTFET and InAs/GaSb DG HJTFET devices is increased with the increased value of dielectric constant due to increased electric field at the source/channel junction (See Fig. 2.5 of Chapter 2). Since the drain current is directly proportional to the electric field in Eq. (5.36), the higher electric field results in higher drain current. Note that there are two types of heterojunction devices: 1) staggered-gap (*e.g.,* Si/Ge), in which the effective energy band gap $(E_{g,eff})$ is positive, and 2) broken gap (*e.g.,* InAs/GaSb) type, in which $E_{g,eff}$ is negative. Both the ON current and subthreshold swing of broken gap heterojunction device are much superior to the staggered gap heterojunction devices [Vandenberghe *et al.* (2011)]. However, our proposed model is suitable for both the homo and heterojunction TFETs devices.

Comparisons of both SS (point and average) for different homo and heterojunction TFET devices, shown in Fig. 5.17, demonstrates that both SS (point and average) are increased with high band gap materials in homojunction devices thereby resulting in no significant improvement in switching characteristics. However, in case of heterojunction devices, an improvement in SS (both point and average) significantly.

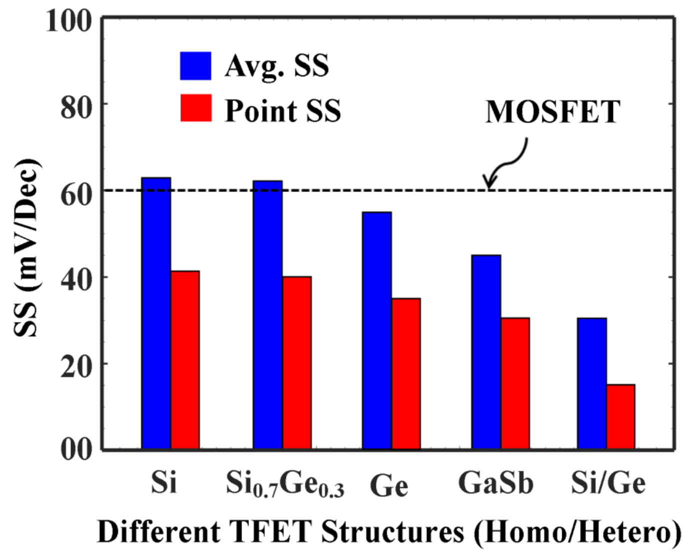

Fig. 5.17: Comparisions of SS for different homo and heterojunction DG TFET device with SiO_2/HfO_2 stacked gate oxide at V_{DS} = 0.5V, V_{GS} = 1.0V, L = 50nm, t_{si} = 12nm

The variation of V_{th} with L for different homo and heterojunction DG TFET device is plotted in Fig. 5.18 shows that V_{th} is nearly independent of L (*i.e.,* threshold voltage roll-off is almost zero) due to the dependency of tunneling on the source-channel junction characteristics only, not on the entire channel region. It is further observed from the figure 5.18 that, for a hetrojunction based DG TFET structure, V_{th} is lowered than homojunction based DG TFET structure due to the lowering of the tunneling width than homojunction DG TFET device.

Fig. 5.19 illustrates the variation of V_{th} against t_{Si} for different combinations of dielectric constant of HJ DG TFET device. From the figure, it is observed that V_{th} increases with t_{si} due to reduction in the tunneling volume owing to the increase in $L_t^{\min}$. Thus, our proposed model is useful for understanding the device physics of homo/heterojunction based any TFETs devices.

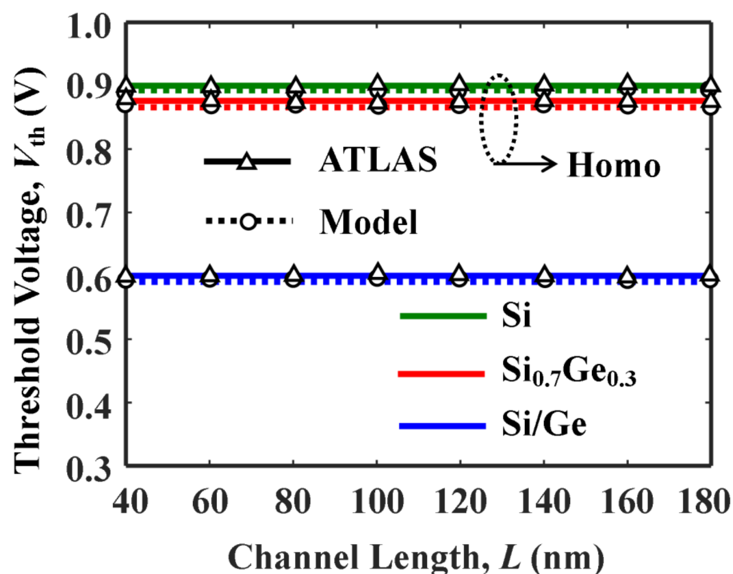

Fig. 5.18: Variation of V_{th} against L for different homo and heterojunction DG TFET with SiO_2/HfO_2 stacked gate oxide at $V_{DS} = 0.5V$, $L = 50nm$, $t_{si} = 12nm$

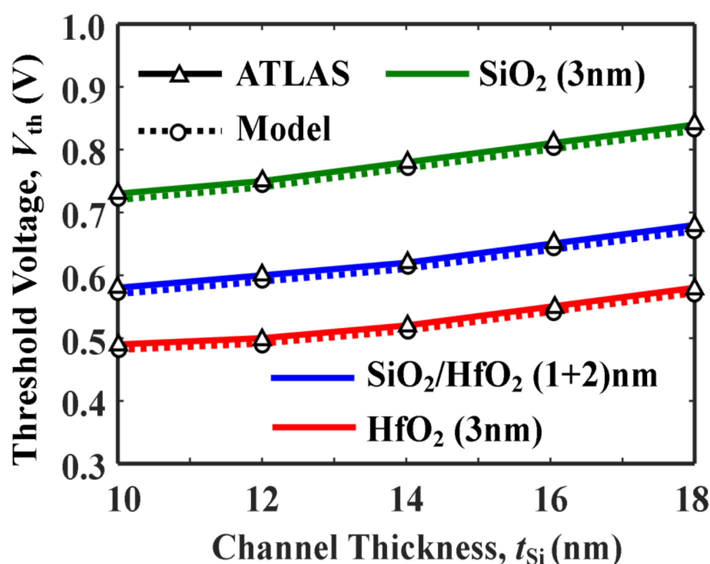

Fig. 5.19: Variation of V_{th} against t_{si} for different combinations of dielectric constant of DG HJTFET stracture at $V_{DS} = 0.5V$, $L = 50nm$, $t_{si} = 12nm$

5.4 Conclusion

A 2-D analytical model for the surface potential of DG HJTFETs with a SiO_2/HfO_2 stacked gate-oxide structures has been developed by taking both the effects of junctions depletion and accumulation/inversion charges into consideration. The concept of TLA method has been used to calculate the drain current by numerically integrating the BTBT generation rate over the entire channel volume of the device. For accurate modeling of the drain current in the subthreshold region, we have included the effects of electric field formation at the drain/channel interface at low gate and high drain bias voltage. The model has been developed for Si/Ge hetero and Si homojunction based TFET devices. The proposed model is also valid for III-V materials like InAs/GaSb DG HJTFET and SOI-based HJTFET structures. There is good agreement between our model results and numerical simulation results obtained by the commercial available ATLAS^{TM} device simulation software.