Chapter 4

4.1 Introduction

Over the previous decade, metal-oxide thin film transistors (TFT) have been extensively studied for various applications including active-matrix organic light-emitting diodes (AMOLEDs)[184], biosensors arrays[185], light emitting transistors[186], photodetectors[10] etc, due to their outstanding transport properties (good dielectric/semiconductor interface). These metal oxides TFT show reasonably high mobility, excellent chemical and thermal stability, which are the essential requirements for practical application. In addition, the possibility of their easy solution processed fabrication and optical transparency makes them superior, low-cost optoelectronic application[187, 188], which include flexible devices[189] and paper-like displays.[151] However, most of these TFTs require high operating voltages (≥25V) because of the low dielectric constant (k) SiO_2 gate dielectric which is commonly used for metal oxide TFT, limiting its application to portable low power electronics.[161] Previously, a number of efforts have been made for developing low voltage low power TFT which can be classified in to the following four types: (1) ion gel,[162, 164, 190] (2) self-assembled layer,[154, 191] (3) ion conducting metal oxide (ICMO)[55, 57, 153, 192, 193] and (4) metal oxide insulator[194, 195]. In general, for metal oxide TFT fabrication, ICMO and metal oxide dielectrics are considered superior materials because of its compatibility with metal oxide semiconductor and its excellent morphological stability at higher processing temperature. Among other different oxide insulators, Ta_2O_5[194], Y_2O_3[195], TiO_2[196, 197], ZrO_2[198, 199], HfO_x[65], $HfLaO_x$[200], $LaAlO_3$[201] and silicates[202, 203] etc. have been reported for the fabrication of high performance TFT. But, for low voltage operation, ICMO is

considered much better material than those metal oxide insulators. In addition to its low voltage operation, its coherent interface formation with oxide semiconductor also leads to achieving superior TFT performance, including its carrier mobility and subthreshold voltage.[55, 193] Additionally, these ICMO dielectrics are fabricated with non-toxic, eco-friendly solution processed technique that can be an appropriate choice for large area fabrication. However, the key difficulty of these ICMO is a high-temperature fabrication process to form a crystalline solid thin film restricting the substrate selectivity.[55]

From this point of view, the fabrication of high-quality ionic dielectrics at a lower temperature is a critical issue in this emerging field. Particularly, the crystallization temperature lower than 400 ^{o}C is expected to take into account the traditional processing temperature for flat panel displays.[199] In this search, we have identified $LiAlO_2$, a popular ion conducting electrolyte for Li^+ ion battery, that can be grown in a crystalline form by sol-gel technique at 350 ^{o}C.[149] This $LiAlO_2$ has three allotropic forms alpha (α), beta (β) and gamma (γ). Among these β phase are unstable under ambient atmosphere. However, α and γ phases are thermodynamically stable.[204]

In this chapter describes the synthesis of crystalline ionic α-phase $LiAlO_2$ (α-$LiAlO_2$) by a sol-gel technique which requires only 350 ^{o}C processing temperature that has been successfully utilized as a gate dielectric of metal oxide TFT. This α-$LiAlO_2$ remained stable up to 500 ^{o}C, while γ-phase (γ-$LiAlO_2$) was developed by direct annealing of precursor film at 700 ^{o}C. Therefore, for detail study, sol-gel derived precursor thin films were annealed at 350 ^{o}C, 500 ^{o}C and 700 ^{o}C which formed α-, α- and γ-phases of $LiAlO_2$ respectively. To realize the effect of these two crystalline phases on TFT performance, three different types of the device were fabricated with the $LiAlO_2$ dielectrics annealed at

three different temperatures. It is observed that all these TFTs show excellent device performance at a low operating voltage (≤ 2.00 V). Although the highest carrier mobility was obtained from the TFT fabricated with the dielectric annealed at 700 ^{o}C, but the variation in carrier mobility is not significant for the TFT fabricated with the dielectric annealed at 350 ^{o}C. Most interesting achievement of this work is to develop 1.0-volt operation voltage TFT by using 350 ^{o}C annealed α-$LiAlO_2$ dielectric, which is possible due to existing high concentration Li^+ with higher ion mobility inside the gate insulator. The other novelty of this work is to lower the processing temperature of the ICMO dielectric. The first reported ICMO dielectric, sodium beta-alumina (SBA), requires ≥800 ^{o}C to obtain a crystalline phase.[55] However, in this study, the dielectric requires only ~ 350 ^{o}C to form the crystalline phase that achieves comparable device performance. Therefore, this ICMO dielectric makes it more acceptable material for low operating, high-performance TFT fabrication that can be utilized in display technology.

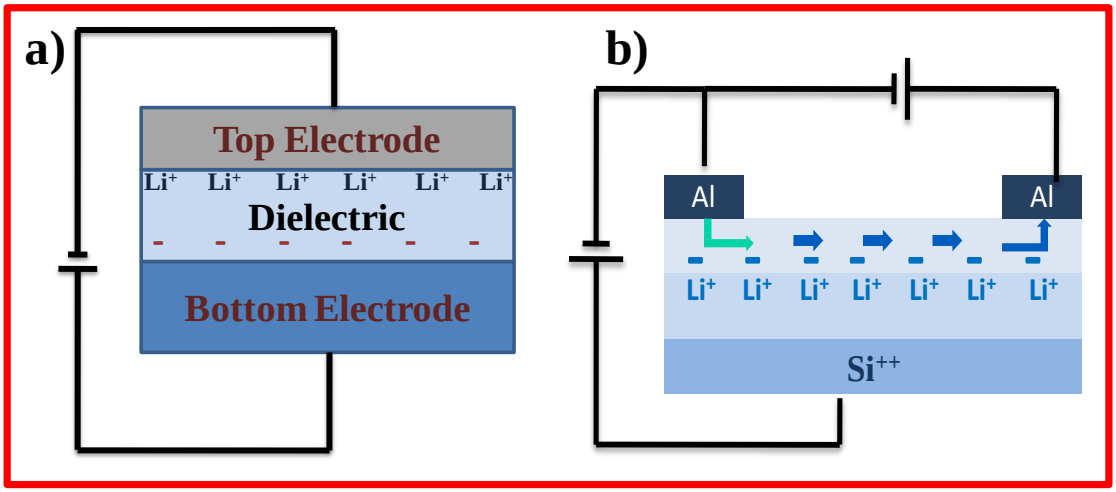

Figure 4.1: *Schematic diagram of* ***a)*** *charge polarization of the* $LiAlO_2$ *ionic dielectric thin films due to* Li^+ *ion shift under the external bias and* ***b)*** *influence of that dielectric on the flow of electrons in the active channel at low voltage.*

As mentioned earlier, $LiAlO_2$ has two thermodynamically stable polymorphs that are recognized by XRD and referred to as α and γ-$LiAlO_2$ crystallized phases with hexagonal ($P4_12_12$) and tetrahedral (R3m) space group.[204] In these $LiAlO_2$ crystals structures, Al and oxygen atoms are in tetrahedral position and connected to the lithium ion. This $LiAlO_2$ forming interstitial Li^+ ion shows high ionic conductivity arising from the partially occupied site in $LiAlO_2$.[205] Because of this Li^+ ion conductivity, it is possible to fabricate a high capacitive thin film with $LiAlO_2$, which is an important factor for the development of low voltage TFT. In TFT, carrier accumulation in semiconductor/dielectric interface is directly proportional to the capacitance and higher capacitive gate dielectric film requires low voltage to accumulate the desired amount of carrier in the channel. As shown in **figure 4.1**, Li^+ ion is free to move through the crystal lattice plane that gets accumulated in either surface according to the external bias and contributes additional ionic polarization to introduce a high capacitive effect. Apart from this high capacitive effect, leakage current density and dielectric interfaces are also important issues for a high-quality gate dielectric. The $LiAlO_2$ is a unique solid-state electrolyte that has very good ion conductivity and very poor electron conductivity serving as a good electronic insulator. Further, by sol-gel method, it can be fabricated in a very compact thin film facilitating in reducing the leakage current. Moreover, because of very low surface roughness, it is also possible to fabricate high-quality semiconductor/dielectric interface with very low trap state, which is an essential factor for high-performance TFT fabrication.

4.2 Results and discussion

4.2.1 Thermal analysis

The thermal behavior of the sol-gel synthesized $LiAlO_2$ powder was investigated through thermo-gravimetric analysis (TGA) and differential thermal analysis (DTA) study. Powder sample for DTA-TGA experiment was prepared by removing the solvent of the sol-gel precursor solution. These studies were carried out in N_2 atmosphere with a 20 ^oC/minute heating rate. **Figure 4.2 a)** shows the thermal behavior of the sample, which indicates weight loss occurred in two steps. From room temperature to 120 ^oC, the weight loss is ~12 % arising from the loss of moisture, physically absorbed water and trapped solvent which is well supported by an exothermic peak in DTA. On the other hand, the second significant weight loss and its corresponding peak in DTA at 300 ^oC is due to the dehydroxylation and removal of other organic impurities. A sharp intense DTA peak observed at 350 ^oC is associated with the crystallization of sol-gel $LiAlO_2$ powder. In the temperature range between 350 ^oC to 800 ^oC, a negligible weight loss was observed, it is suggesting that $LiAlO_2$ has a broad crystallization window. XRD data confirms that $LiAlO_2$ has three crystallization temperatures. The endothermic peak at 600 ^oC is associated with the phase transformation of $LiAlO_2$ crystal.[206]

4.2.2 Fourier-transform infrared spectroscopy (FTIR)

The presence of organic residue and hydroxyl group in the dielectric thin film act as trap states for the carriers. Those can introduce additional gate leakage current leading to the degradation in the device performance. To ensure the removal of organic residual, Fourier-transform infrared spectroscopy (FTIR) measurements were carried out with $LiAlO_2$ thin films, which is shown in **figure 4.2 b)**. For this study, all thin films have been deposited

under the same condition as a gate dielectric for TFT fabrication. This FTIR study clearly indicates that there is no absorption peak at 3000-3500 cm^{-1}, 2700-2960 cm^{-1} and 1300-1700 cm^{-1} which are associated with the absorption of OH, CH_3 and NO_3 stretching vibration. Therefore, it's obvious that organic precursor doesn't exist in the thin film sample annealed even at 350 ^oC implying its applicability for the development of TFT with stable and high performance.

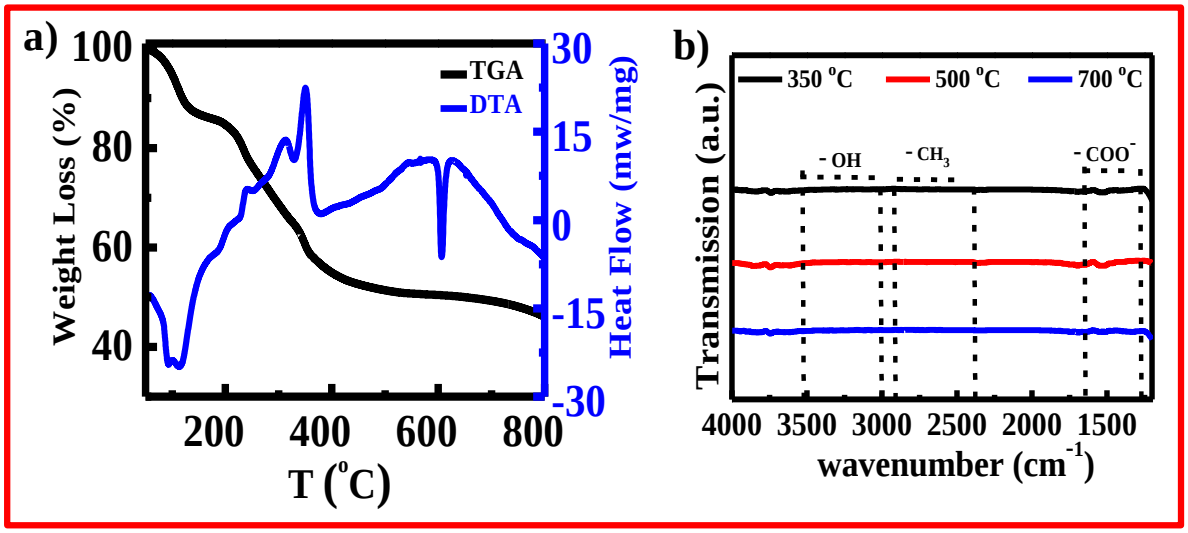

Figure 4.2: a) *TGA and DTA of the precursor powder of $LiAlO_2$* ***b)*** *FTIR analysis of the thin films of $LiAlO_2$ dielectric annealed at 350 ^oC, 500 ^oC and 700 ^oC.*

4.2.3 Structural properties of the thin film and powder of ionic dielectric $LiAlO_2$

For the structural study of $LiAlO_2$, X-ray diffraction (XRD) and Grazing Incidence X-ray Diffraction (GIXRD) measurements were carried out with powder and thin film samples, respectively. XRD data for powder samples are shown in **figure 4.3 a)**.

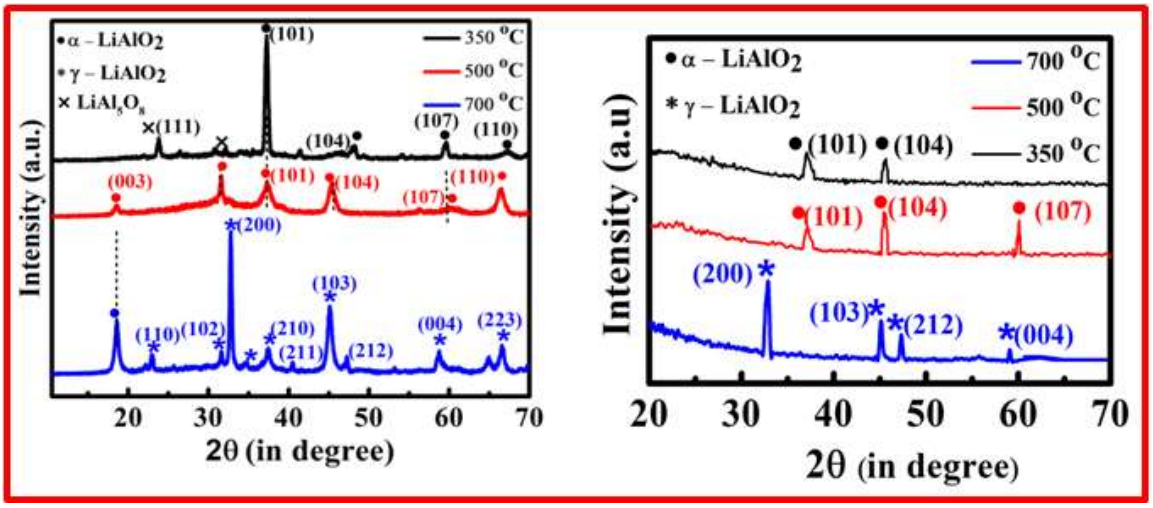

Figure 4.3: a) *Powder XRD of $LiAlO_2$ dielectric* ***b)*** *GIXRD plot of $LiAlO_2$ thin films, with different annealing temperatures 350 °C, 500 °C and 700 °C.*

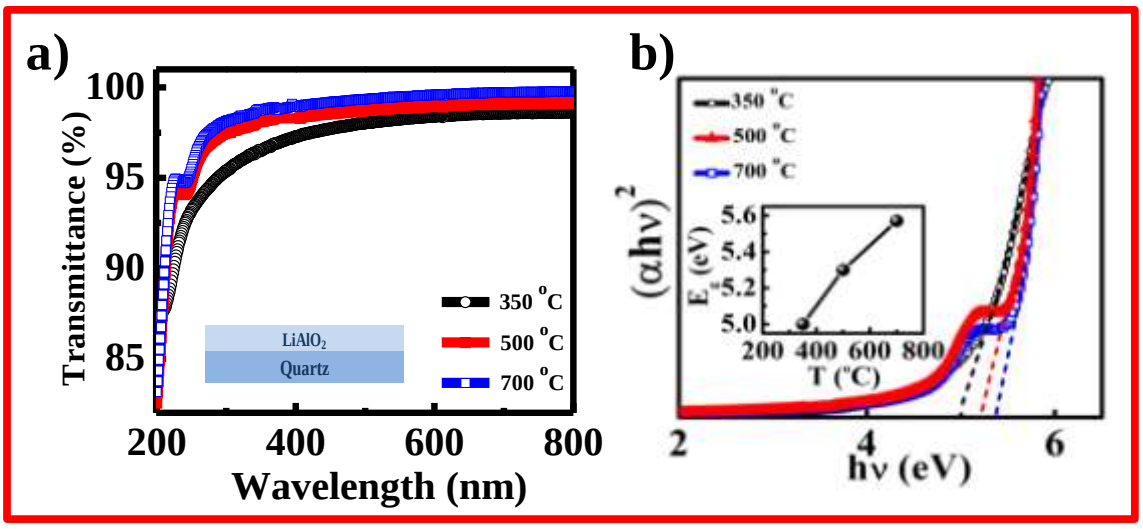

Figure 4.4: a) *Optical transmittance plot of the sol-gel derived $LiAlO_2$ dielectric thin films of ~80 nm thickness annealed at different temperatures for $LiAlO_2$/quartz (inset)* ***b)*** *The Tauc's plot of thin films annealed at various temperatures and the inset shows the band gaps of the $LiAlO_2$ thin films.*

The GIXRD of solution processed $LiAlO_2$ thin films annealed at 350 °C, 500 °C and 700 °C for four hours, half hour, and a half hour respectively are shown in **figure 4.3 b**). These XRD study show that both the $LiAlO_2$ thin films annealed at 350 °C and 500 °C have a

clear crystalline phase with diffracted peak originated from the planes of the reflections of (101), (104), and (107) at 2θ angles of about 37^o, 45.5^o and 60.06^o which indicates the α phase of $LiAlO_2$ crystal. The distinct phase formation of γ-$LiAlO_2$ was observed in both the thin film and powder sample annealed at 700 ^oC. XRD data shows an intense peak at 2θ angles near about 32.88^o, 45.04^o, 47.36^o and 59.08^o associated to the reflection planes of (200), (103), (212) and (004) of the γ phase of $LiAlO_2$ crystal. Both the α and γ phase formation of $LiAlO_2$ are supported by our earlier DTA study. According to that study, first crystallization is observed at 350 ^oC associated with α- phase formation of $LiAlO_2$. Similarly, endothermic peak at 600 ^oC was observed due to the phase transformation from α to γ phase of $LiAlO_2$ crystal. The crystallized phase of $LiAlO_2$ is always preferred in the fabrication of a TFT, because of the higher Li^+ ion conductivity resulting in the higher dielectric constant compared to that of the amorphous phase. Moreover, high capacitance provides low operating voltage, low subthreshold swing, and high mobility, which are crucial parameters for the high performance of a TFT.[55]

4.2.4 Optical properties of ionic dielectric $LiAlO_2$ thin films

For transmittance study, a thin film of $LiAlO_2$ was fabricated on a quartz substrate under the same condition that has been followed in TFT dielectric fabrication. **Figure 4.4 a)** shows the transmittance data of the samples annealed at three different temperatures. The data shows that all these films are optically very transparent (>97%) in the visible region. The sample annealed at 350 ^oC exhibits relatively lower transparency most likely due to the higher surface roughness of the film facilitating in the surface scattering from grains/grain boundaries. The optical bandgap was extracted by extrapolating the linear region of the square of absorption coefficient (αhν) to the X-axis, as shown in **figure 4.4 b)**. It is

observed that the bandgap of the $LiAlO_2$ thin films increases from 5.0 eV to 5.6 eV with the annealing temperatures. This large bandgap (E_g>4.7) value helps in preventing the electronic conduction between the active channel layer and the dielectric layer, which results in low gate leakage current.

4.2.5 Surface morphologies of ionic dielectric $LiAlO_2$ thin films at different temperatures

The surface morphologies of p^{++}-Si/$LiAlO_2$ films is measured by atomic force microscopy (AFM) as shown in **figure 4.5**. The extracted root mean square roughness values of the samples annealed at 350 ^oC, 500 ^oC and 700 ^oC are 5.49 nm, 1.66 nm, and 0.96 nm, respectively. This data implies that the surface roughness of $LiAlO_2$ thin films is reduced slightly and forms a denser and smoother film as the annealing temperature is raised from 500 ^oC to 700 ^oC. However, the sample annealed at 350 ^oC offers higher roughness compared to that annealed at 500 ^oC and 700 ^oC, since higher temperature facilitates in forming denser metal-oxygen-metal bonds.[198] As discussed earlier, this difference in roughness may create a significant difference in carrier mobility of devices contributed from the surface trap states and dielectric/semiconductor interfaces. From 3-D AFM analysis (**figure 4.5 d-f**), it is observed that the grain size increases with increasing temperature, which makes film denser and smoother. Therefore, the carrier mobility is expected to be higher for the sample annealed at 700 ^oC.

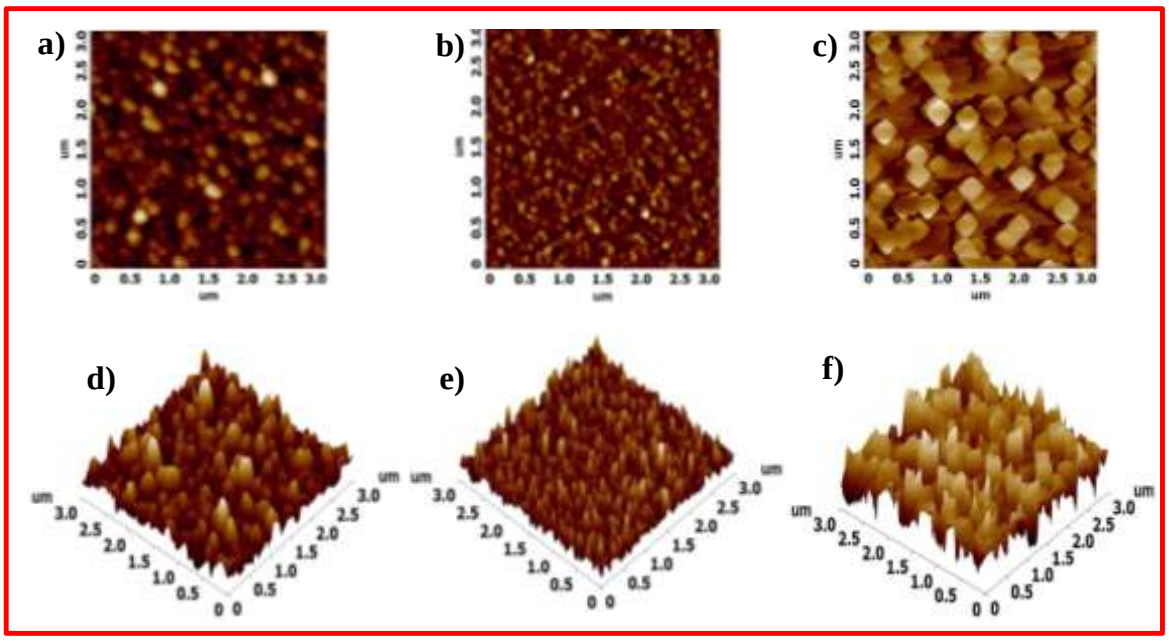

Figure 4.5: *2-D Surface morphologies of the solution processed $LiAlO_2$ dielectric thin films for p^{++}-Si / $LiAlO_2$ at different annealing temperatures* ***a)*** *350 ^oC* ***b)*** *500 ^oC* ***c)*** *700 ^oC and for 3-D* ***d)*** *350 ^oC* ***e)*** *500 ^oC* ***f)*** *700 ^oC (scan surface area 3 x 3 µm).*

4.2.6 Leakage current and capacitance measurements of ionic dielectric thin film

Figure 4.6 a) represents the leakage current density versus applied voltage data which shows that the leakage current density of 1.9 x 10^{-9} amp/cm^2, 1.8 x 10^{-8} amp/cm^2 and 8.1 x 10^{-9} amp/cm^2 at 5V for the dielectric sample annealed at 350 ^oC, 500 ^oC and 700 ^oC respectively. These data clearly point out that the leakage current density for all of these samples is extremely low, which is the signature for the successful fabrication of highly dense and low defect density dielectric thin films. In the case of ion conducting dielectric, amorphous materials provide lower capacitance with respect to the crystalline materials, which play a negative role in the development of low voltage TFTs.[195, 200] Crystalline dielectric $LiAlO_2$ has the high capacitance because of Li^+ ion free to move in crystal plane and least leakage current density than previously reported research article on thin film transistor.[151, 195, 207, 208] Structural defects like pinholes in a thin film and non-

uniformity are the probable reasons for the leakage current rather than crystalline grain boundary or ionic leakage current (Li^+). This indicates that solution processed $LiAlO_2$ thin film has the least pinhole with very high uniformity which can be used as a good ion conducting dielectric in thin film transistors.

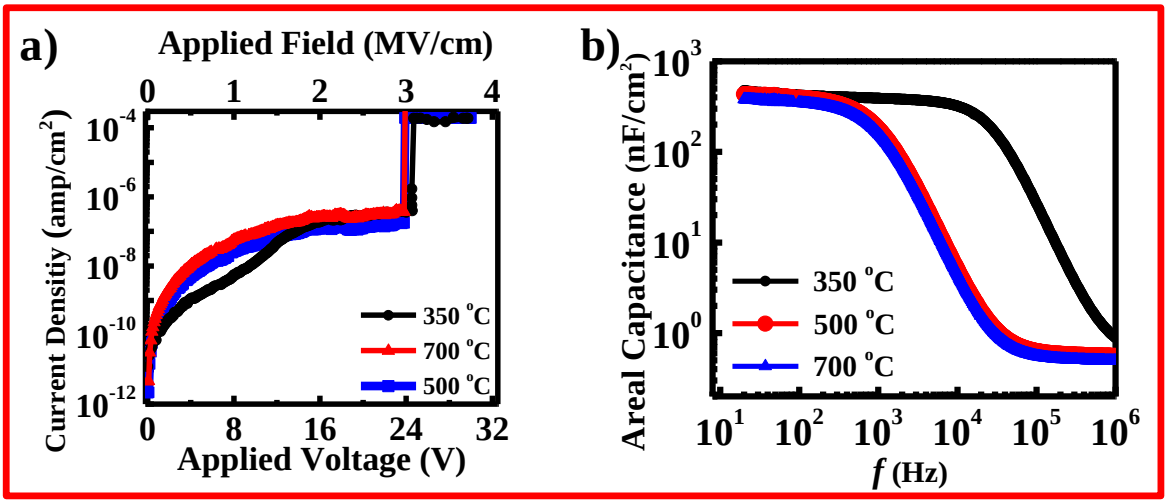

Figure 4.6: a) *Leakage current density vs applied voltage of $LiAlO_2$ thin films annealed at 350 ^oC, 500 ^oC and 700 ^oC.* ***b)*** *capacitance versus frequency curves of the solution processed ionic dielectric $LiAlO_2$ thin films annealed at 350 ^oC, 500 ^oC and 700 ^oC with p^{++}-Si /$LiAlO_2$/ Al device structure.*

Variation of capacitance (C) per unit area of the $LiAlO_2$ film under different frequency (f) of AC bias is shown in **figure 4.6 b)**. The capacitance values (around 500 nF/cm^2 at low-frequency range) are more or less same for all the samples annealed at three different temperatures and it decreases rapidly after some certain values of frequency. It is very clear that the variation of capacitance per unit area for the sample annealed at 350 ^{o}C is wider than that for two other samples. At 50 Hz, the capacitance value of $LiAlO_2$ thin film samples annealed at 350 ^{o}C, 500 ^{o}C and 700 ^{o}C are 445 nF/cm^2, 410 nF/cm^2 and 380 nF/cm^2 respectively. These values are significantly higher than that of some insulators

which have been used as gate dielectrics in previously reported thin film transistors.[151, 207, 208] These capacitance values indicate that spin-coated thin films of $LiAlO_2$ are good alternate as a gate dielectric in thin film transistors. From **figure 4.6 b)** it is clear that the capacitance per unit area for the film annealed at 350 ^oC is the highest in value indicating the removal of all hydroxyl groups at this temperature (also confirmed from FTIR data).

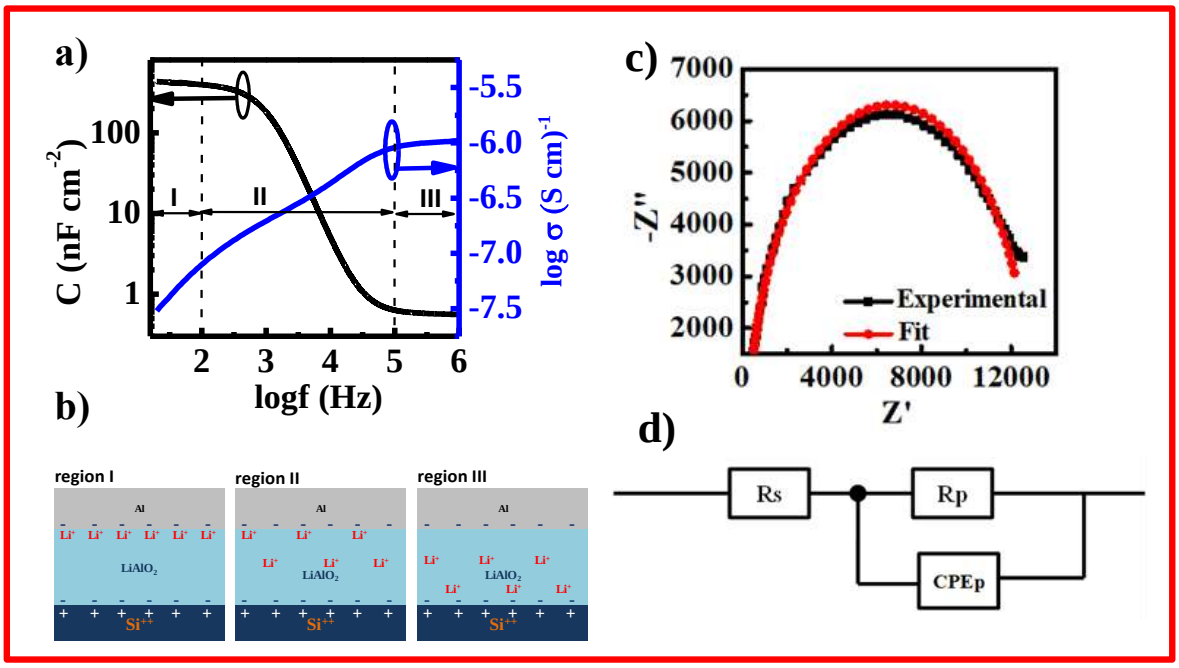

Figure 4.7: a) *The specific capacitance and ionic conductivity vs. frequency for a 500 ^oC annealed dielectric thin film with a device structure of p^{++}-Si/ α-$LiAlO_2$/Al* ***b)*** *illustrations Li^+ ion position in α-$LiAlO_2$ thin film in these three frequency regions* ***c)*** *Nyquist plot experimental (black) data and fitted data (red)* ***d)*** *the corresponding equivalent circuits.*

The hydroxyl group does not contribute to the capacitance value since metal oxide shows more capacitance than their metal hydroxide.[161, 195] One of the possible reasons for lower capacitance density of $LiAlO_2$ film annealed at higher temperature arises from the SiO_2 formation at p^{++}-Si/ $LiAlO_2$ interface usually formed at the annealing temperature >450 ^oC. Due to the interfacial SiO_2 formation, overall capacitance (C) value needs to be

calculated from the combination of the series of capacitors $1/C=1/C_{LiAlO_2} + 1/C_{SiO_2,}$ which reduces the effective capacitance value.

4.2.7 Dielectric polarization mechanism

To identify the dielectric polarization mechanism, the ion conductivity of dielectric film has been studied at various frequency range with a device structure of p^{++}-Si/ α-$LiAlO_2$/Al. **Figure 4.7 a) and b)** demonstrated the specific capacitance and ionic conductivity data at a different frequency for 500 ^oC annealed α-$LiAlO_2$ capacitor. This figure clearly indicates three different frequency regions of capacitance. At low frequencies (<2 kHz) most of the Li^+ accumulate near the α-$LiAlO_2$/Al interfaces that cancel the electric field in the bulk part of α-$LiAlO_2$ thin film (region I). This ion accumulation creates a drop in ionic conductivity of the film. The nature of this capacitive behavior is related to the formation of electronics double layer (EDL) at dielectric/electrode interfaces. At medium frequencies (2 kHz< f < 500 kHz), a limited number of Li^+ ions can accumulate at the α-$LiAlO_2$/Al interfaces (region II). The residual part of Li^+ ions remains in the bulk part of the α-$LiAlO_2$ thin film that moves up and down under electric field. As a result, the ionic conductivity increases with frequency and eventually approach to plateaus when all Li^+ transfer from the α-$LiAlO_2$/Al interface to the bulk part of the film (region III). This resistive nature created from the migration of separated Li^+ ion of an ionic dielectric. Thus, it behaves like an electronically insulating, ionically-conducting material. Such kind of behavior has been observed earlier for other ionic dielectrics thin film.[56, 177] A constant-phase-element (CPE) study has been done in α-$LiAlO_2$ thin film device which is shown in **figure 4.7 c)**.[209] The equivalent circuit of this AC impedance study is shown in **figure 4.7 d**).

4.3 Thin film transistor characterization

To confirm the feasibility of the dielectric application of the solution processed $LiAlO_2$ as a gate dielectric, TFT devices with bottom gate, top electrodes architecture was fabricated (**figure 4.8 and 4.9**) at different temperatures in an ambient atmosphere. Aluminum electrodes as a source and drain were deposited by thermal evaporator through a shadow mask to provide a width to channel length ratio of 118 (W = 23.6 mm; L = 0.2 mm). To neglect the overestimation of mobility calculation due to grain boundary effect, this width to channel ratio (W/L) was selected very cautiously.[157] [210] On the other hand, interdigitated source-drain electrodes with a large W/L ratio also demonstrates better information about the film quality compared to the small W/L ratio.

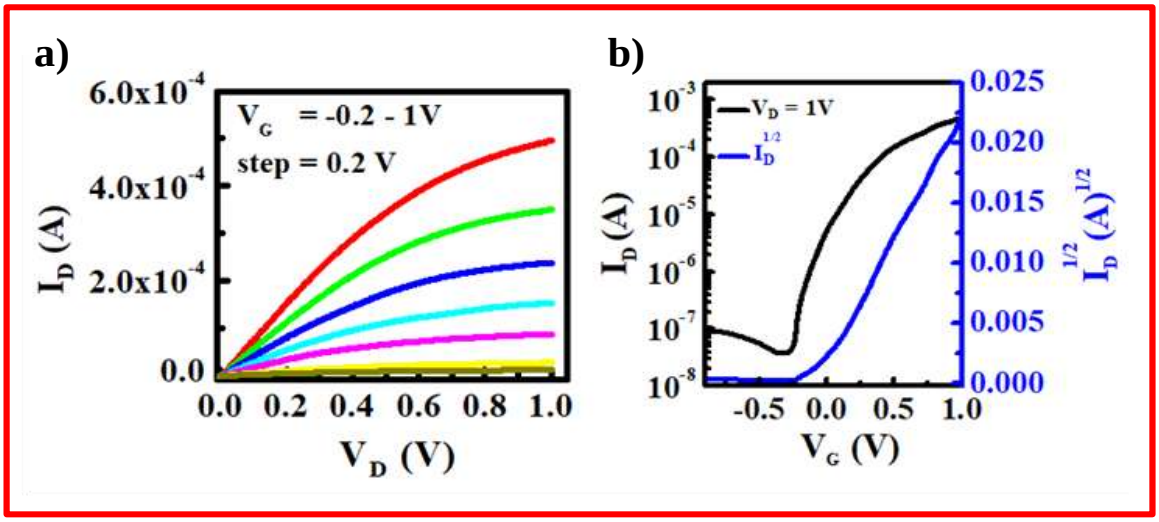

Figure 4.8: *Output characteristics of the device -1 under 1.0-volt operating voltage* ***a)*** *output characteristics,* ***b)*** *transfer characteristics with device architecture* p^{++}*-Si/α-*$LiAlO_2$*/IZO/Al.*

To achieve a higher carrier transport in a TFT with a larger W/L ratio, the dielectric film is required to be a smoother and void-free one. In this study, the TFTs with large W/L ratio

provides higher drain current (I_D) and mobility, which implies that the dielectric film is smooth, pinhole, defect-free and well matched with the semiconducting layer. The output and transfer characteristics of device-1 (TFT with 350 ^oC annealed α -$LiAlO_2$ dielectric) are shown in **figure 4.8 a) and b)**. **Figure 4.8 a)** shows that I_D needs only 1.0 V or less to saturate when we apply 1.0 V gate voltage. Similarly, lower gate voltage characteristic required lower drain voltage to saturate, indicating its capability to operate at 1.0 V only. For comparison of three different TFTs, the applied drain voltage was swept from 0 V to 2.0 V and the gate voltage -0.5 V to 2.0 V for all three TFTs which are shown in **figure 4.9**. From all these output characteristics **(figure 4.9 a), b) and c)),** it is clear that the devices with the dielectric annealed at different temperatures display typical n-channel transistor with clear linear region and current saturation at ≤2.0 V. Output characteristics indicates that the saturation current can be achieved at or above 1.5 V, i.e., the operating voltage of the TFT can be as low as 2 V, which is beneficial for low power electronics. Low drain voltage region of the output characteristics shows the linear behavior indicating good ohmic contact at the semiconductor and electrode interface.

Effective carrier mobility (μ) and sub-threshold swing (SS) of these TFTs are calculated from the following equations respectively,

$$\mathbf{I_D} = \mu \mathbf{C} \frac{\mathbf{W}}{\mathbf{2L}} (\mathbf{V_G} - \mathbf{V_T})^2 \quad \text{.....(4.1)}$$

$$SS = \left[\frac{d(log\, I_D)}{dV_G}\right]^{-1} \quad \text{.....(4.2)}$$

Where I_D, C, V_G, V_T are saturation drain current, capacitance per unit area, gate voltage, and threshold voltage, respectively. The extracted carrier mobility, on/off ratio and subthreshold swings are listed in **table 4.1**.

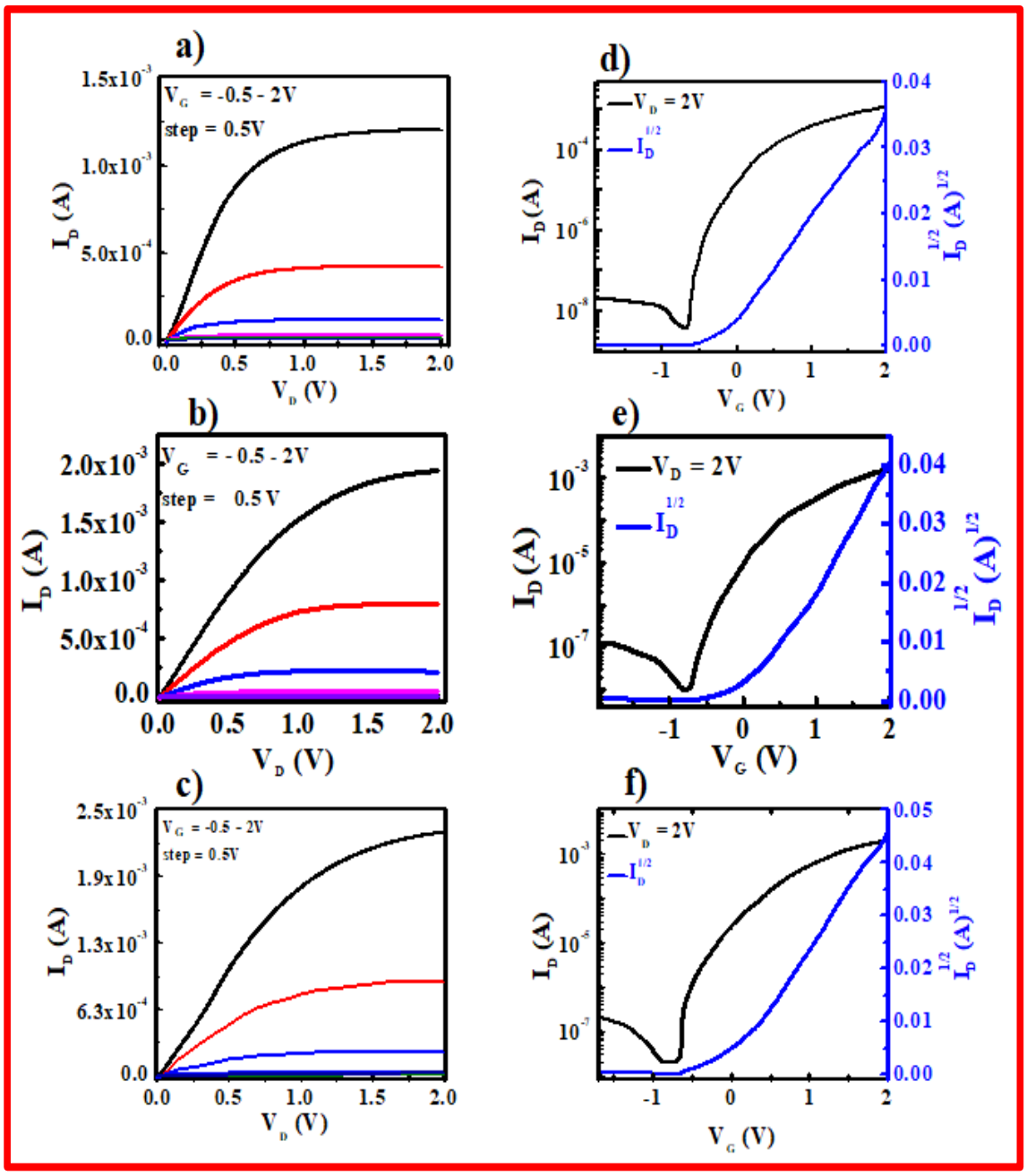

Figure 4.9: *Output characteristics of the IZO TFT with $LiAlO_2$ dielectric annealed at* ***a)*** *350 ^oC* ***b)*** *500 ^oC* ***c)*** *700 ^oC and transfer characteristics* ***d)*** *350 ^oC* ***e)*** *500 ^oC* ***f)*** *700 ^oC with V_G of 2V with device architecture p^{++}-Si/$LiAlO_2$/IZO/Al.*

Since the TFT operation was performed in direct voltage, the capacitance at low frequency (50 Hz) is considered for mobility calculation to avoid the overestimation. To calculate the threshold voltage of the device by fitting the straight line to the transfer characteristics of

the square root of I_{DS} versus V_G. Comparing three different TFTs, the highest electron mobility has been achieved with device-3 (700 ^oC annealed γ-$LiAlO_2$ dielectric TFT) with a value of 25 cm^2/V.s. Although this value is not much different from the device -2 that shows mobility 22 cm^2/V.s. Relatively, device-1 has relatively lower carrier mobility (14 cm^2/V.s) when it operates in 2.0 volt operating range which is mainly due to the lower temperature (350 ^oC) annealed IZO semiconductor which has more amorphous nature than device 2 and 3. Under 1.0-volt operation, device-1 doesn't show much different mobility (13.5 cm^2/V.s) with respect to its 2.0-volt operation. Beside this semiconductor crystallinity issue, the surface roughness of $LiAlO_2$ also affects the carrier mobility of TFT. From our AFM study, it is observed that with higher annealing temperature, the surface roughness of dielectric reduces. This surface roughness has two major negative roles in carrier transport; firstly, it increases the number of trap states that can lower mobile carrier density and secondly it introduces carrier scattering that reduces effective carrier mobility. From this discussion, it is clear that mobility decreases with increasing roughness. **Figure 4.10** shows the variation of field effect mobility of TFT with the roughness of the dielectric surface, which clearly indicates that effect.

Besides the carrier mobility, there are two other parameters which determine the quality of TFT. One of the on/off current ratio and the other one is the sub-threshold voltage of the device. From our detail studies, it is observed that all these three different TFTs have very high on/off ratio (>10^5) with a small subthreshold voltage swing (~150 mV/decade), indicates very high switching properties of these TFTs. Histogram of the sub-threshold swing for three different devices are shown in **figure 4.11**.

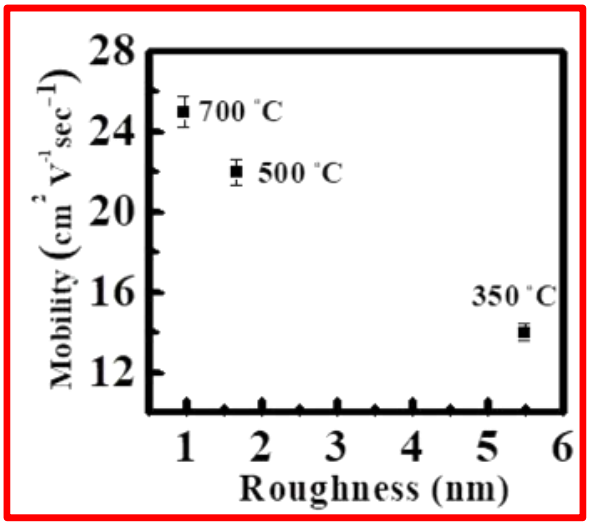

Figure 4.10: *Mobility versus roughness of dielectric at different annealed temperatures.*

It is noted that, although device-1 has lower electron mobility, but it has similarly high on/off ratio and low sub-threshold voltage swing like two other devices. This on/off ratio and sub-threshold voltage swing parameters are superior to earlier reported solution processed TFTs.[55, 114] Therefore, in summary, all these three TFTs with $LiAlO_2$ dielectric shows excellent field effect transistor behavior with high mobility and low operating voltage.

By utilizing the subthreshold swing (SS) data of output characteristics, the maximum density of the interface states (N_{ss}^{max}) was calculated by using the following equation,[161]

$$N_{SS}^{max} = \left[\frac{SS \times \log e}{kT/q} - 1\right]\frac{C}{q} \qquad \text{..... (4.3)}$$

where C, k and q are capacitance Boltzmann constant and electronic charge, respectively.

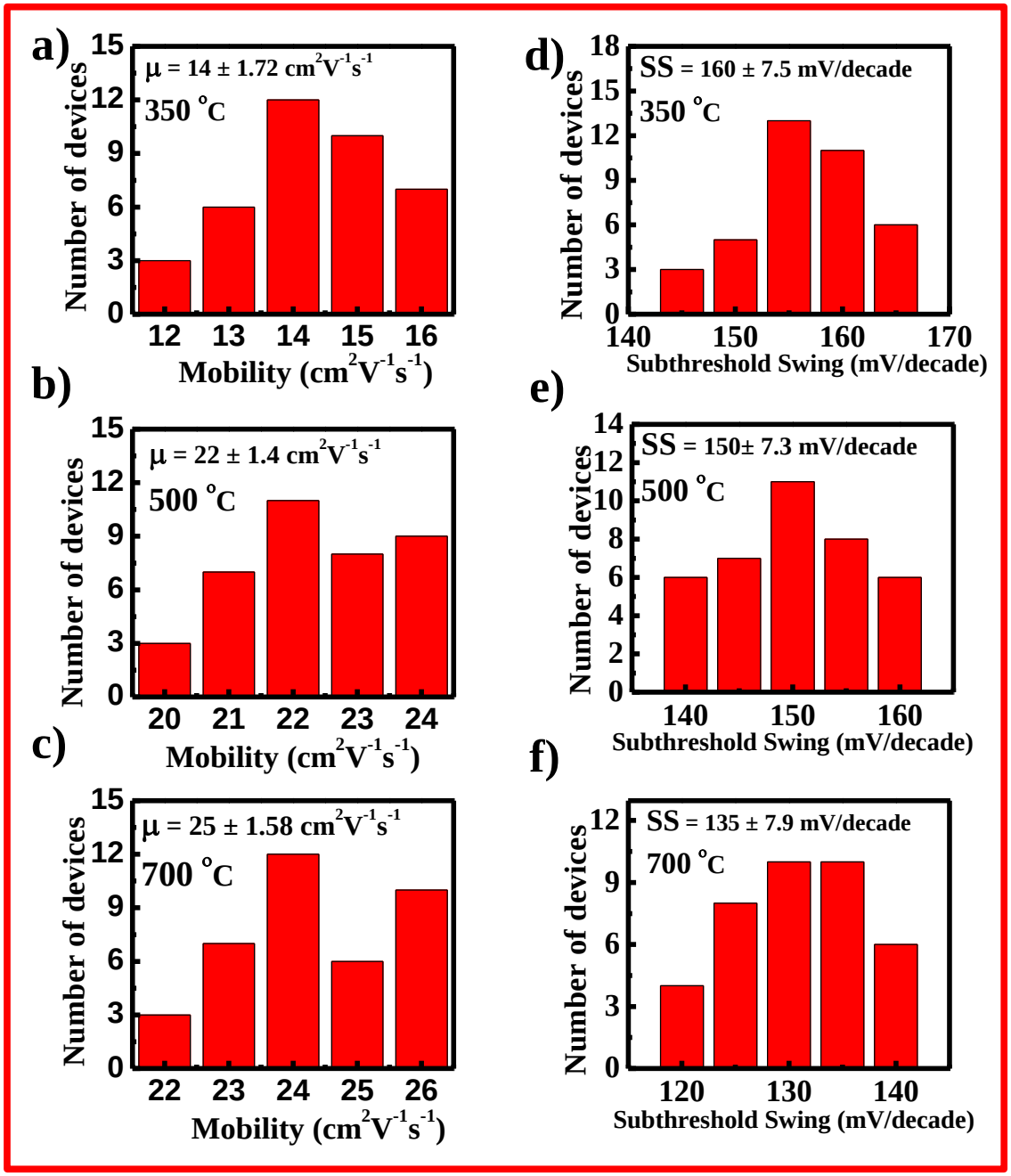

Figure 4.11: *Histogram of the field effect mobility* ***a)*** *350 °C,* ***b)*** *500 °C and* ***c)*** *700 °C and subthreshold swing for* ***d)*** *350 °C,* ***e)*** *500 °C and* ***f)*** *700 °C $LiAlO_2$/IZO TFT.*

The maximum density of the interface states N_{ss}^{max} was calculated 3.9 x 10^{12} cm^{-2}, 2.9 x 10^{12} cm^{-2} and 1.9 x 10^{12} cm^{-2} for device-1, 2 and 3 respectively which is significantly low for solution-processed metal oxide TFT.[152, 195] This small (N_{ss}^{max}) value implies that

the $LiAlO_2$ dielectric form an excellent dielectric/semiconductor interfaces which are required for reaching high carrier mobility of the device. It is very worth to mention that the device-1 has similarly low N_{ss}^{max} value like two other TFTs. This result implies that even with 350 ^oC annealing temperature $LiAlO_2$ can work as an excellent gate dielectric of a TFT. Overall in addition to the low operating voltage, all these $LiAlO_2$ ionic dielectrics create a coherent and compatible interface with IZO semiconducting layer with the less number of interfacial traps that result in reasonably high carrier mobility of these TFTs. This high performance of the optimized $LiAlO_2$ TFT annealed at different temperature should be assigned to the collective effect of the high quality of semiconductor layer, a smooth high capacitance solution processed $LiAlO_2$ dielectric layer and well optimized dielectric and semiconductor interface (low roughness, i.e. lower trap density at the interface).

To realize the combined low operating voltage and high mobility issue of $LiAlO_2$ dielectric based TFT, a specific carrier transport mechanism has been proposed which is schematically presented in **figure 4.12 a) and b).** It is known, in these IZO TFT the electron transport through amorphous/polycrystalline semiconductor through electron hopping between neighboring cation. For this transport, it is required to fill the localized states between the energy bands of semiconductor before involving in the conduction of carriers. For low voltage operating with high carrier mobility, it is required to induce the enormous amount of carrier in the dielectric/semiconductor interface that has been achieved by utilizing high-capacitive $LiAlO_2$ thin film in current devices. As soon as, gate voltage has been applied in TFT in accumulation mode, high concentration Li^+ of the $LiAlO_2$ dielectric attract huge number of electron carrier in the interface and a small

fraction of that carrier attract toward the 'lower lying' localized state of the oxide semiconductor and hurriedly filled those localized states as shown in **figure 4.12.** Then the remaining accumulated electron could occupy the upper lying localized states. As a consequence of electron filled neighboring localizes states, the carrier can jump to the neighboring ion, ultimately can improve the drain current, electron mobility and overall device performance.[211, 212]

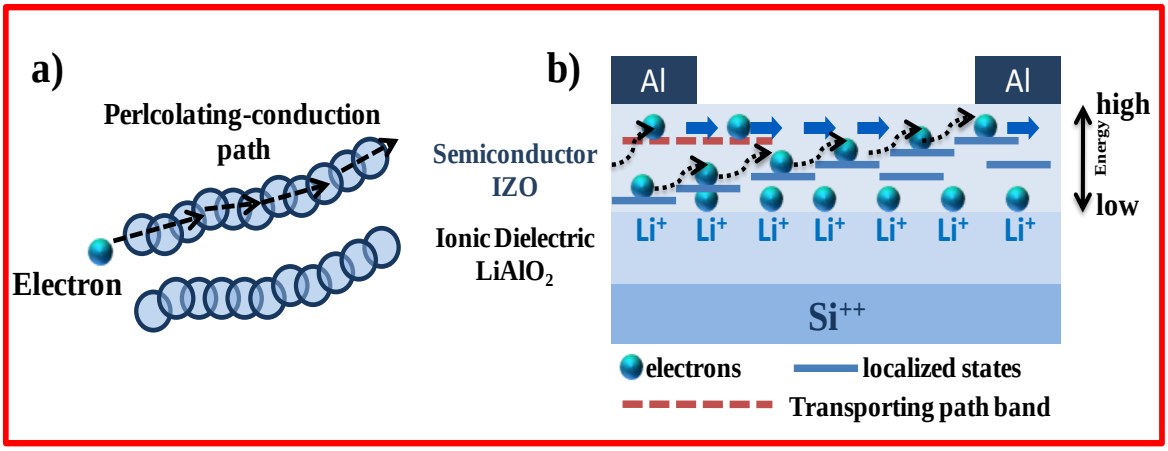

Figure 4.12: *Electron transporting principle of oxide semiconductor* ***a)*** *electron hopping through a percolation-conduction path in semiconductor channel,* ***b)*** *schematic device diagram with charge accumulation in different localized states and subsequent charge transportin accumulation mode operation by the effect of high capacitance ionic dielectric* $LiAlO_2$.

To analyze the effect of ion diffusion on device stability, repeated transfer characteristics have been done for 45 minutes with an interval of 1 minute. **Figure 4.13 and 4.14** show the I_D-V_G 'bias stress stability' data for device-1 and device-3. Both characteristics show that there is almost no variation in mobility, On/Off ratio and sub-threshold voltage swing of the device under repeated measurement in ambient conditions.

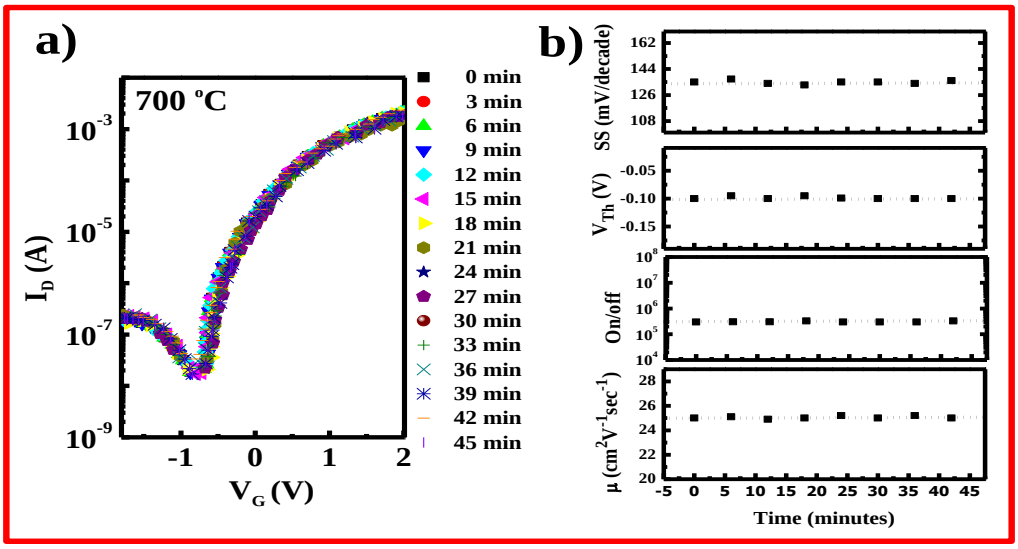

Figure 4.13: *Operational stability of the ionic dielectric $LiAlO_2$/IZO TFT* ***a)*** *evolution of the transfer curves of ionic dielectric annealed at 700 °C $LiAlO_2$/IZO TFT. The gate bias during stress was 2V* ***b)*** *change in field effect mobility, on/off, threshold voltage and subthreshold swing during continuous operation for 45 minutes.*

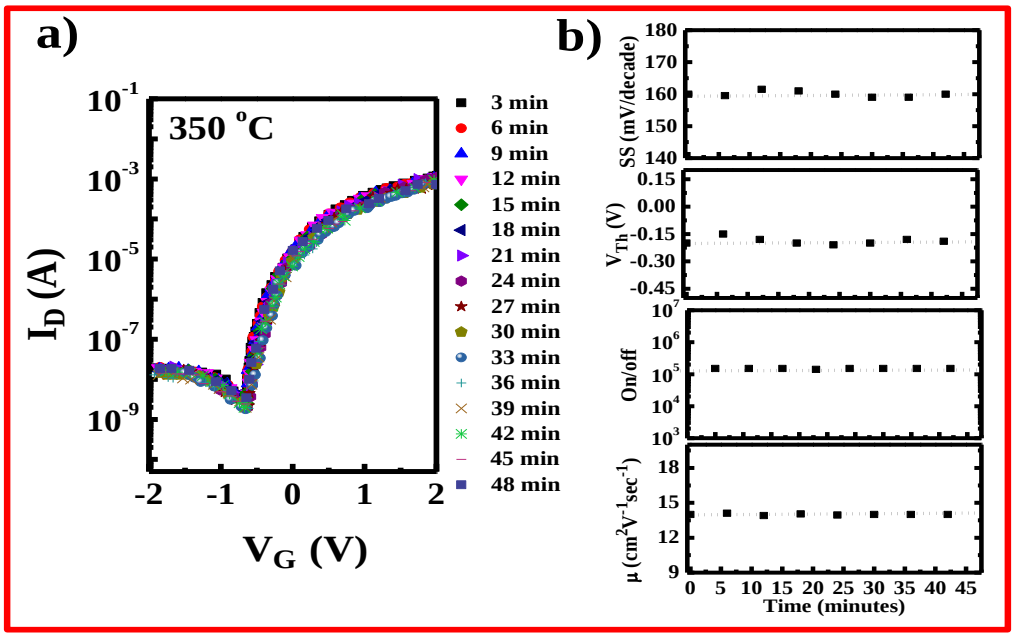

Figure 4.14: *Operational stability of the ionic dielectric $LiAlO_2$/IZO TFT* ***a)*** *evolution of the transfer curves of ionic dielectric annealed at 350 °C $LiAlO_2$/IZO TFT. The gate bias during stress was 2V* ***b)*** *change in field effect mobility, on/off, threshold voltage and subthreshold swing during continuous operation for 45 minutes.*

Table 4.1: *The summary of different device parameters of IZO TFTs fabricated with three different temperatures annealed $LiAlO_2$ dielectric.*

Device no.	**Dielectric**	**Dielectric Annealed temperature**	**C (nF/cm^2) at 50 Hz**	**V_{Th} (V)**	**ON/OFF**	**Density of interfaces sates (N_{ss}^{max})(cm^{-2})**	**Subthreshold swing (SS) (mV/decade)**	**Electron Mobility (μ) ($cm^2\ V^{-1}\ sec^{-1}$)**
1.	α-$LiAlO_2$	350 ^oC	445	-0.2	1.5 x 10^5	3.9x10^{12}	160	14
	α-$LiAlO_2$ (< 1V)	350 ^oC	445	-0.18	1 x 10^4	4.1x10^{12}	180	13.5
2.	α-$LiAlO_2$	500 ^oC	410	-0.05	2.5 x 10^5	2.6 x10^{12}	150	22
3.	γ-$LiAlO_2$	700 ^oC	380	-0.1	4 x 10^5	1.8 x10^{12}	135	25

4.4 Conclusions

In summary of this chapter, crystalline ionic α-phase $LiAlO_2$ (α-$LiAlO_2$) has been synthesized by the sol-gel technique which requires only 350 ^oC processing temperature and it has been successfully utilized as a gate dielectric of metal oxide TFT for the first time. It has been observed that α-$LiAlO_2$ remained stable up to 500 ^oC. The other thermodynamically stable γ-phase (γ-$LiAlO_2$) was developed by direct annealing of precursor film at 700 ^oC. To realize the effect of these two different crystalline phases on TFT performance, three devices were fabricated with three different temperatures (350 ^oC, 500 ^oC and 700 ^oC) annealed $LiAlO_2$ dielectrics. It is observed that all these TFTs show excellent device performance at a low operating voltage (≤ 2.00 V) and high carrier mobility. The highest carrier mobility 25 $cm^2V^{-1}s^{-1}$ was obtained with γ-$LiAlO_2$ dielectric TFT with very high on/off ratio (>10^5) with a very low subthreshold swing (~150 mV/decade). Such kind of low subthreshold swing is not commonly achieved in solution-

processed metal oxide TFT. However, the most interesting realization of this work is to develop 1.0-volt operation voltage TFT by using 350 ^{o}C annealing α-$LiAlO_2$ dielectric, which became possible due to existing high concentration Li^+ with higher ion mobility inside gate insulator. In addition to the 1.0-volt operating voltage, this device also shows higher carrier mobility (13.5 $cm^2V^{-1}s^{-1}$) and high on/off ratio (10^4) with low subthreshold voltage swing (~150 mV/decade) which is rarely found in the literature. The other novelty of this work is to achieve the least processing temperature (350 ^{o}C) of ICMO dielectric, which is now compatible for display application.