Chapter 4

Hardware Implementation

4.1 Outline

From literatures, it is found that the relays used for protection of power transformers can be categorized on the basis of hardware implementations involved. Micro-controller based relays, with a nonlinear transformer model to determine health conditions of the transformer is investigated in [67] [68] [69] [70]. Some relays use presence of harmonics to identify magnetizing inrush. To deal with fault under CT saturation an algorithm to estimate CT secondary current using flux/current curve is performed using Digital Signal Processor (DSP) TMS320C in ref. [86] [87]. An algorithm for estimating fundamental and second harmonic component using Kalman filter is implemented using TMS 320 DSP [18]. Implementation of Hidden-Markov Model based fault classifier on a floating-point DSP based hardware platform to detect fault transients is developed in [66]. The fault classification system was verified using waveforms from an actual fault data recorder [66].

This chapter discusses implementation of matched wavelet filters on hardware to prove the practical feasibility of the developed scheme. The input to this scheme are differential current waveforms of power transformers of ratings 315 MVA, 200 MVA, and 25 MVA(used in simulations). The actual differential waveforms on 1 KVA, 220/110V transformer are also generated in the laboratory to test the performance of proposed scheme in practical environment. The input waveforms are recorded on Field Programmable Gate Array (FPGA) board and replicated for testing the developed algorithm. This chapter describes Xilinx simulation block sets used for designing hardware simulation model. The developed filter units, based on matched wavelets, deploy series of operations, for process-

ing the differential input waveforms. The results obtained in simulation studies reported in the previous chapter are verified using hardware simulation model and hardware implementations.

4.2 Outline of the Hardware Implementation Studies

The summary of the outline of various stages of implementation in software as well as in hardware can be given in four stages. These four stages are as follows.

Stage 1 - Simulation Model: In this stage, the transformer waveforms are simulated in PSCAD and MATLAB software. The wavelet filters, mainly the inrush-filter and fault-filter are simulated in MATLAB environment. The tests are performed on a PC and the results are generated in simulation environment. Thus, the whole concept of wavelet based protection system was developed and conceptualized in a simulated environment. The results obtained from this model are already discussed in Chapter 3. The schematic diagram showing the implementation details of software implementation is shown in Fig. 4.1

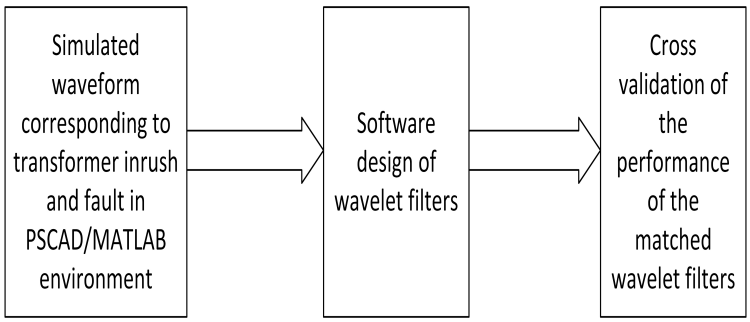

Figure 4.1: Details of software implementation (stage 1)

Stage 2 - Hardware Simulation Model: In this stage, the transformer waveforms are simulated in PSCAD and MATLAB as in stage 1. The wavelet filters (inrush- and fault-filters) are implemented in hardware simulation environment i.e. as a System-generator model. The timing analysis and performance of the System Generator models of the filters are evaluated. The results (waveforms and verification etc.) are generated in simulated environment for testing the System Generator model (hardware simulation model) of the filter design part. All the resulting waveforms are generated on PC as plots in MATLAB. The test and performance of the hardware simulation model is presented as a part of

this chapter. The details of hardware-simulation model are depicted as schematic block diagram in Fig. 4.2.

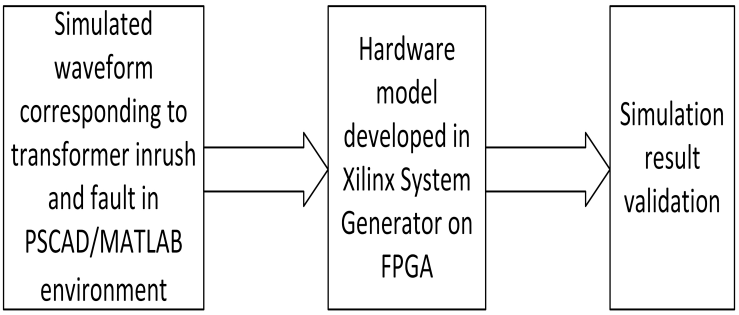

Figure 4.2: Details of hardware simulation model (stage 2)

Stage 3 - Hardware Implementation-I: In this stage, the waveforms are simulated in PSCAD and MATLAB environment as in stage 1 and 2. It is worthy to mention that the wavelet filters are implemented on FPGA board (filter-board). The FPGA board is equipped with ADCs. In order to initiate the hardware design of the filter, the set of analog signals which is indispensable is retrieved from PSCAD/MATLAB environment which is subsequently stored in FPGA board (waveform-board). The time synchronization of the waveform-board is adjusted to match the power frequency so that the stored signals become suitable for real-time analysis. The schematic diagram of Fig. 4.3 shows the details of the hardware implementation-I of stage 3.

Stage 4 - Hardware Implementation-II: In this stage, the waveforms are generated from physical single-phase transformer with physical CTs. The actual waveforms obtained through the CTs are then recorded on a FPGA board (waveform-board). The wavelet filters are implemented on a FPGA board (filter-board) as discussed in stage 3. In this stage the waveforms obtained from a physical transformer are provided in real-time to the filter-board. The filter-board output responses are recorded on a Digital Storage Oscilloscope (DSO) for verification and presentation in this chapter. Fig. 4.4 depicts the scheme of hardware implementation-II of stage 4.

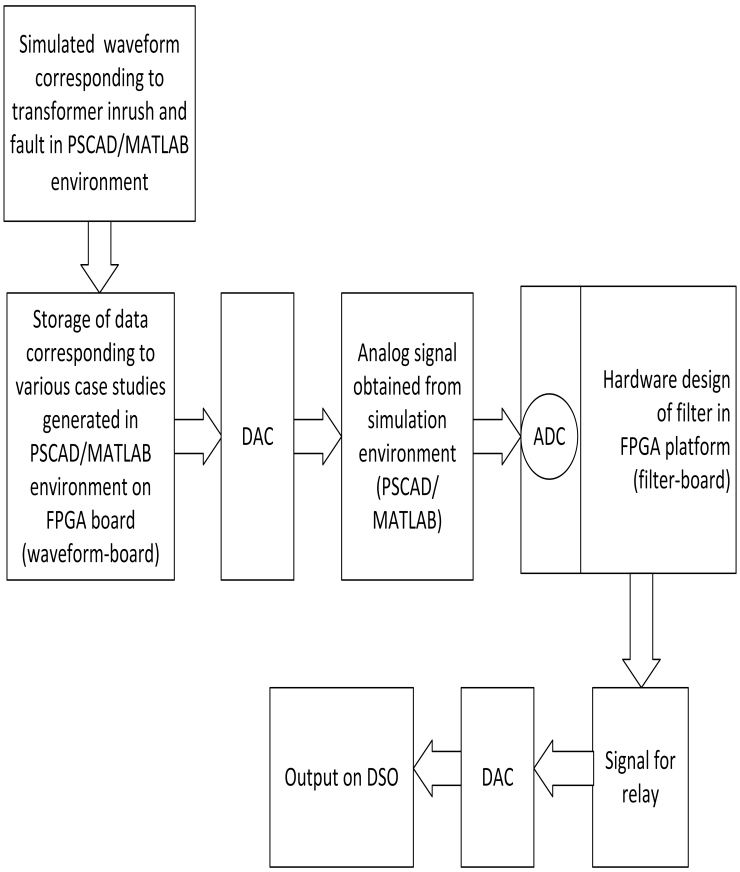

Figure 4.3: Hardware implementation-I (stage 3)

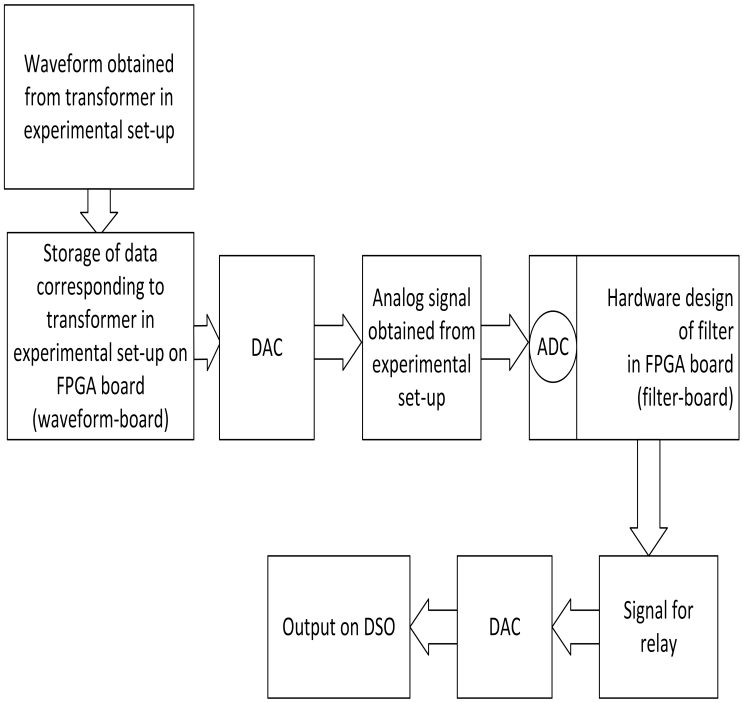

Figure 4.4: Hardware implementation-II (stage 4)

4.3 Hardware Simulation for Inrush- and Fault-Filter: (Stage-2)

In the previous chapters, designing and testing of matched wavelet filters were discussed. The waveforms corresponding to the inrush- and fault-filters are implemented as a MATLAB simulations. The matched inrush- and fault-filters are properly designed to distinguish between different inrush and fault conditions. The matched wavelet filter responses to inrush and fault waveforms are shown for selected threshold (as discussed in section 3.3.3). It was found that response of inrush-filter crosses threshold for inrush waveform and the response obtained is well-below the threshold limit for fault waveform. Whereas, response of matched fault-filter crosses threshold for fault waveforms and remains well-below the threshold limit for inrush waveforms which is desirable. The present section, discusses the implementation of inrush- and fault-filters on FPGA board. In order to verify the correctness of the performance of System Generator filter model the comparison is made with that of the simulation results (PSCAD/MATLAB) pertaining to the specific case studies. The computation time analysis is performed to ensure that the filter computations are made before arrival of the up-coming waveform sample. The parallelism and number of units are decided in this stage through several iterations and re-design process. After implementing the inrush- and fault-filters, the filter responses are again tested for their accuracy of implementations on a few waveforms. The objective (or aim) of the tests is to ascertain the accuracy of calculations, and, therefore, only selected (or limited) number of waveforms is tested.

This section describes implementation of the filter unit on hardware simulation platform (i.e. System Generator). The components of the hardware simulation comprises of ADC, delay, comparator, normalizing, Multiply-Add-Accumulate (MAA), absolute calculation and DAC units. The overall process of calculation of filter response is depicted in schematic diagram of Fig. 4.5.

The ADC unit is in-built on the FPGA board. The delay unit is essentially a memory unit which stores the delayed waveform samples. The normalizing unit normalizes the whole set of waveforms to have the maximum of the absolute values of the peaks or valleys to be unity. This unit divided all the samples by a number selected from the sample-set of the delay unit. It first scans the whole delay unit to find the values of the peaks and

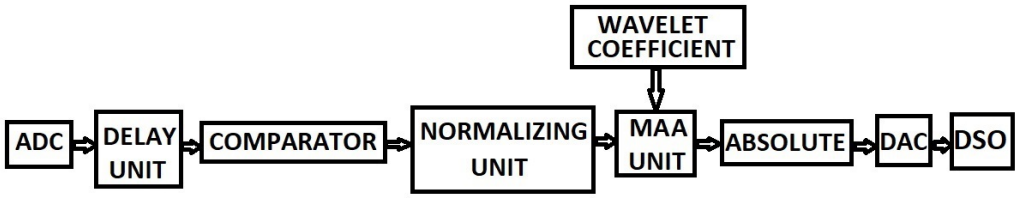

Figure 4.5: Schematic diagram for filter unit

valleys in the samples. Then all the samples are divided by maximum of $\{ |peak|, |valley| \}$ in the sample set. The MAA unit utilizes saved wavelet coefficients and the normalized waveforms to calculate wavelet transform of the waveforms. The final response is the absolute value of wavelet transform of waveform which is observed as an output. The envisaged DAC and DSO in the final hardware setup (stage 3) are also shown in Fig. 4.5. Hence, in actual practice all the calculations are performed in hardware simulation model. The implementation of hardware simulation model for inrush- and fault-filter is shown in Fig. 4.6. Fig. 4.6 shows example of calculation for two samples (sample and its delayed version) of a signal waveform. Fig. 4.6 shows implementation of all the mathematical calculations described in this section as per Fig. 4.5. The blocks of delay, comparator , normalizing and MAA units are implemented in parallel mode to allow fast calculations before arrival of next sample (in real-time). The Xilinx hardware filter unit designed in the System Generator is shown in Fig. 4.6 is implemented on Nexys video board, so that this can be used as inrush-filter and fault-filter. From Fig. 4.6 the calculations involved in the filter unit can be observed. Due to high computational burden, the Nexys video board is chosen because it provides greater number of DSP slices required for large number of computations involved.

4.4 Results of Hardware-Simulation Model (Stage 2): Testing Accuracy of Implementation

The test results of hardware simulation model are carried out for selective waveforms only. As described earlier the tests are carried out to ascertain the accuracy of implementation, i.e. to ascertain whether this model when implemented on actual board, will work almost in similar fashion or not. Some of the waveforms, pertaining to inrush (Fig. 4.7 and

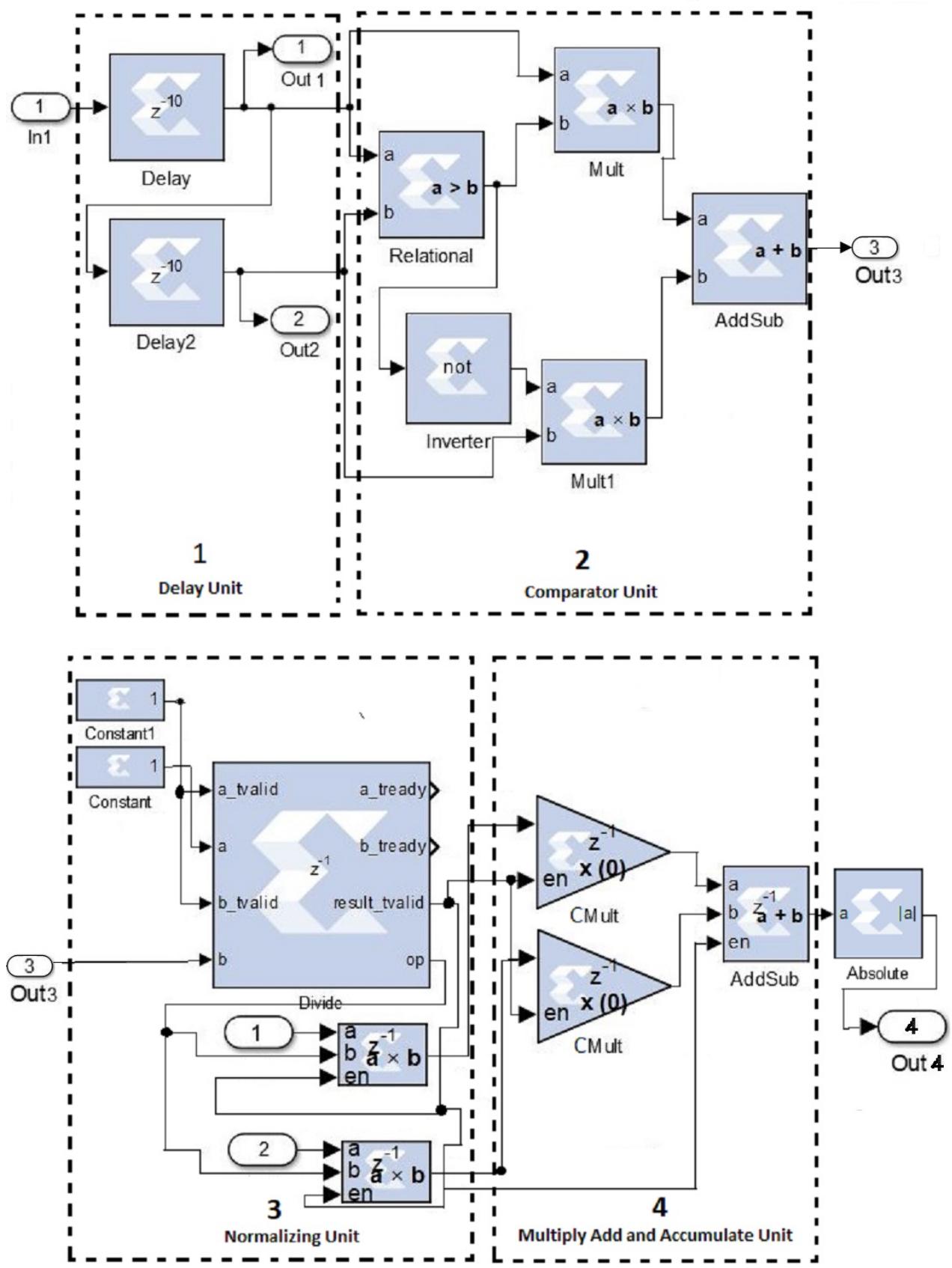

Figure 4.6: Inrush-filter/fault-filter hardware simulation model for two samples

Fig. 4.8), in-zone faults with different levels of CT saturation (Fig. 4.9 and Fig. 4.10), and external fault with CT saturation (Fig. 4.11) are tested. The results obtained from the hardware simulation models are compared with the results of the simulated models of Chapter 2 to make sure that the implemented inrush- and fault-filters are sufficiently close to their simulation counterparts.

It can be observed that inrush- and fault-filter responses for inrush waveforms shown in Fig. 4.7 and Fig. 4.8 show similar values to that of one observed in simulations. These two waveforms are selected to observe the response of the hardware simulation model for both types of inrush waveforms, i.e. waveform having positive peaks and negative peaks respectively. Similarly, some representative fault waveforms are taken for observation of calculations. The inrush- and fault-filter responses for waveforms of different in-zone faults are depicted in Figs. 4.9 and 4.10. The inrush- and fault-filter response for external fault under CT saturation is depicted in Fig. 4.11. The quantization errors in digital implementation are evident for very small values of responses shown in Fig. 4.9(b) and 4.10(b), however, these quantization errors do not affect the performance of the filter.

In all these figures the filter responses of inrush- and fault-filter are shown with proper selection of inrush and fault thresholds. If the response values of inrush-filter cross the inrush threshold, the waveform is detected as inrush and similarly, if the fault-filter response crosses the fault threshold, the waveform is detected as fault waveform. These crossings of a threshold gives the relaying signals for the relaying scheme proposed in Chapter 3 Section 3.3.2.

4.5 Hardware Implementation-I (Stage 3)

As indicated in Section 4.2, in this stage of hardware implementation, the simulated waveforms are recorded on a waveform-board and these waveforms are provided to the filter-board as inputs for detection of in-zone fault and inrush. For this purpose, the task is divided in two subparts. First part is to generate the differential waveforms on FPGA board i.e. the waveform-board which mimics real-time signal. The second part is to verify and test the filter implemented on the hardware i.e. filter-board. The output of the waveform-board is 12-bit digital output and hence, a DAC is used to get its analog equivalent for supplying it as analog input to filter-board. The waveforms obtained from

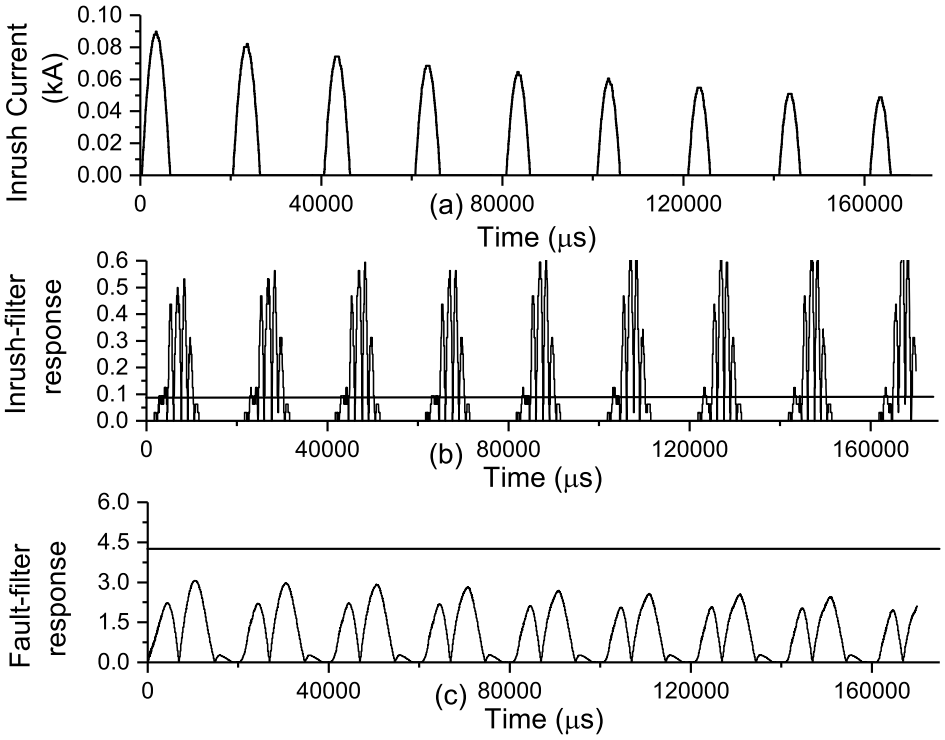

Figure 4.7: (a)Magnetizing inrush current waveform given as input to inrush- and fault-filters (b) Response of inrush-filter (c) Response of fault-filter

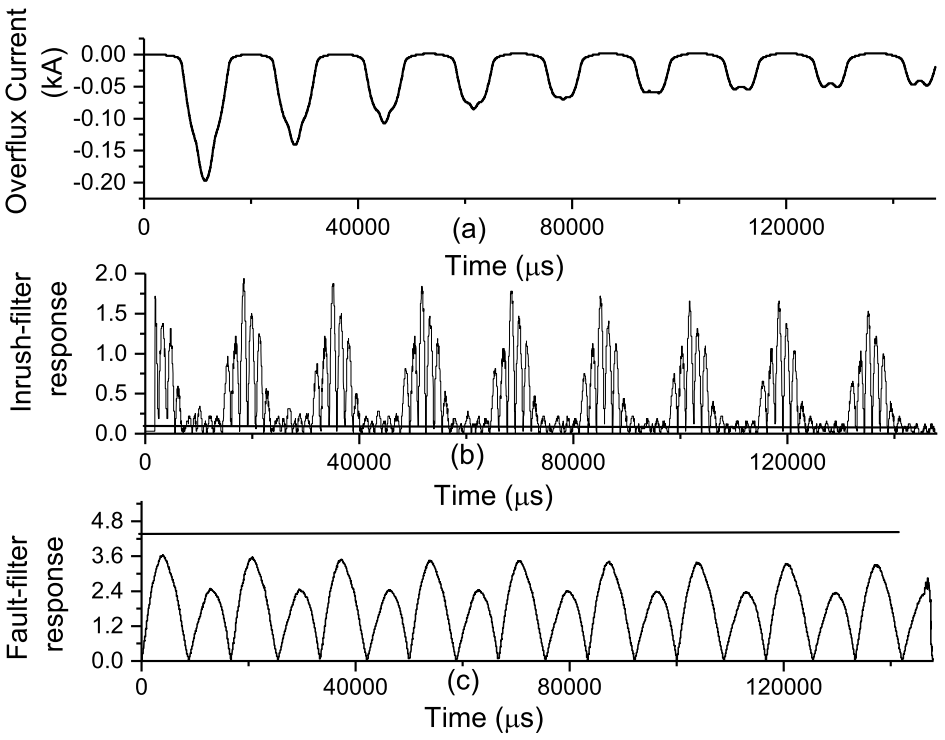

Figure 4.8: (a)Over fluxing current waveform given as input to inrush- and fault-filters (b) Response of inrush-filter (c) Response of fault-filter

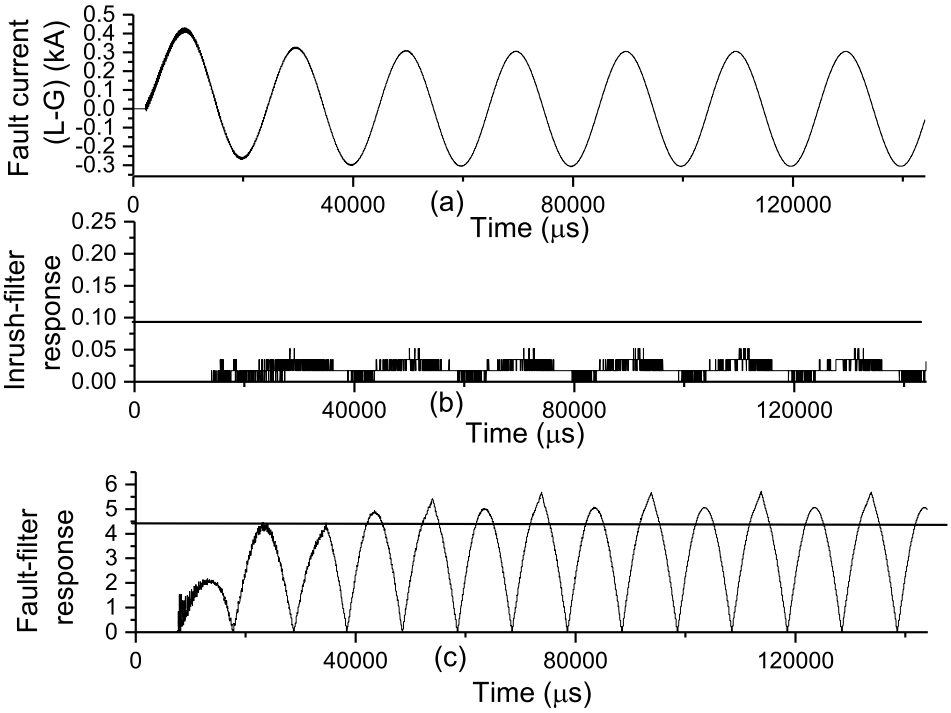

Figure 4.9: (a)In-zone fault without CT saturation given as input to inrush- and fault-filters (b) Response of inrush-filter; the quantization errors in digital implementation are evident for very small values of responses (c) Response of fault-filter

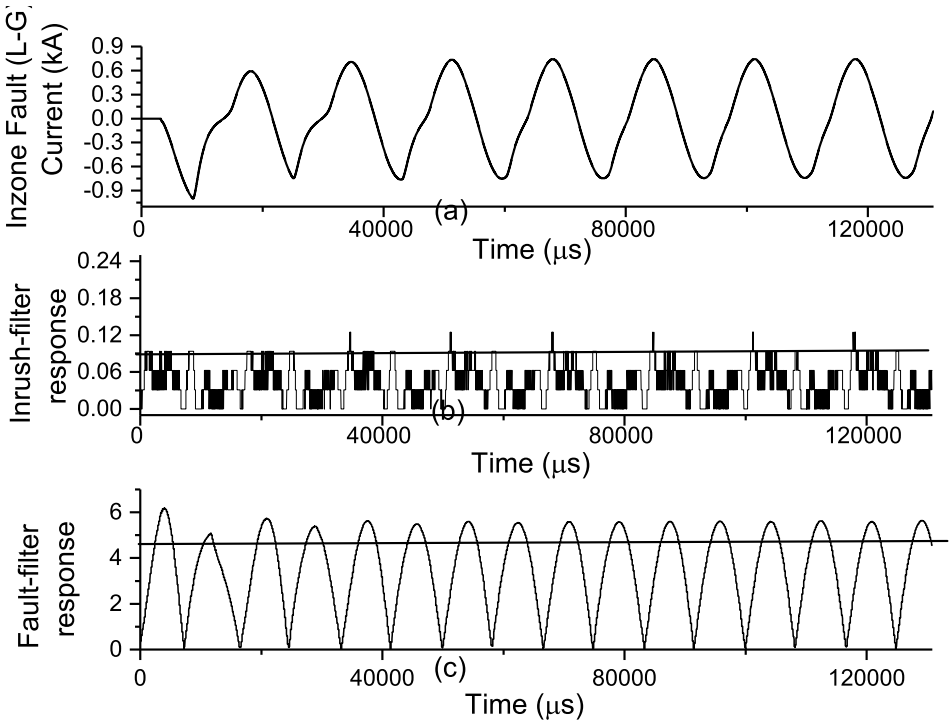

Figure 4.10: (a)In-zone fault (L-G fault) with CT saturation given as input to inrush- and fault-filters (b) Response of inrush-filter; the quantization errors in digital implementation are evident for very small values of responses (c) Response of fault-filter

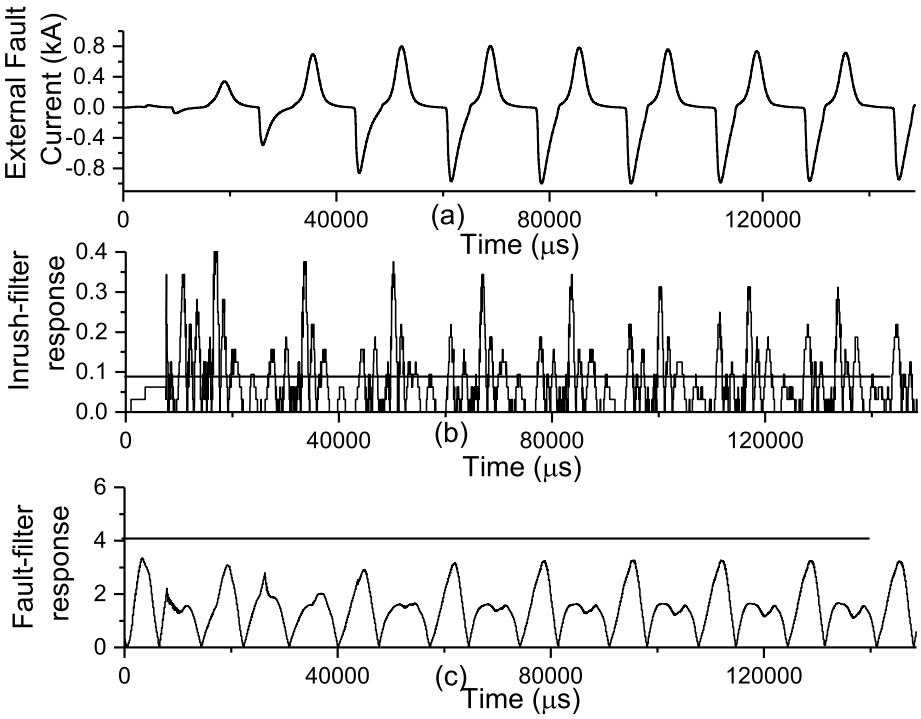

Figure 4.11: (a)External fault (L-G fault) with CT saturation given as input to inrush- and fault-filters (b) Response of inrush-filter (c) Response of fault-filter

the waveform-board is fed directly to the ADC channel of the filter-board which has the filter implemented on it. The matched inrush-filter is designed using matched inrush wavelet coefficients. Similarly, the matched fault-filter is designed with matched fault-wavelet coefficients. The complete flow of the steps involved in generating the differential waveforms on the waveform-board and the implementation of filter unit are shown in Fig. 4.12.

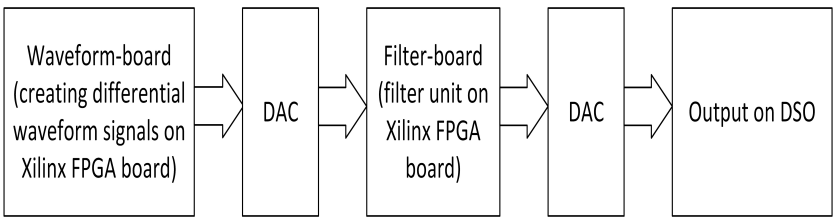

Figure 4.12: The complete flow of process

4.5.1 Waveform-Board Design

For implementing input waveforms, a hardware model is designed in System Generator. The main idea is to store the resulting waveform samples from the PSCAD/EMTDC sim-

ulation in the memory block (ROM) so that when this model is implemented on FPGA board, it will provide the same waveform at desired frequency (50 Hz) as output. Fig. 4.13 shows the System Generator Simulink model for creating input signal. The functional descriptions of various blocks are as follows.

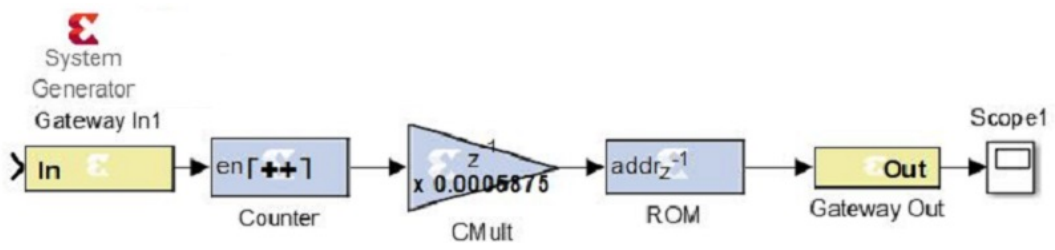

Figure 4.13: Hardware simulation model for creating Input

Gateway-In / Gateway-Out : Gateway-in blocks as the name implies are inputs and gateway-out blocks are outputs from the Xilinx environment of MATLAB - Simulink design. The blocks gateway-in and Gateway out act as top level input and output interface to HDL (Hardware Description Language) design generated by System Generator. Various operations performed between gateway-in and gateway-out block may be fixed-point or floating-point data types, which are then converted to Simulink integer data types as it comes out from gateway-out block. In the present work, fixed-point data type is used.

Counter : The Counter block is used for implementing free-running/count limited (i) up-counter (ii) down-counter (iii) up/down counter. In present context, this block is used as a count limited up-counter. This block is used for addressing the ROM block.

CMULT : CMULT is constant multiplier block. A constant gain is multiplied to the input data types. The purpose of using this block is to introduce delay between the samples or to decrease the frequency of output signal. The output of counter block is given to CMULT block which is multiplied by a gain so that there is certain delay between two samples and frequency of signal is adjusted to power frequency (50 Hz).

ROM : This block is used as single port read only memory (ROM). The data file containing required data information is loaded in the ROM. The file should contain data samples at least equal to depth of ROM block.

Counter block is enabled by the gateway in (GI) block. For this, boolean (1) input is provided internally at the GI block from FPGA itself. As the Counter block is enabled,

it starts counting from the preset initial value. We could have taken this counter output directly to address the memory location of ROM block, but instead, a CMULT block is used in between counter block and ROM. The reason for this is, that the output of the FPGA board will be at the clock speed of 10 MHz when this model is implemented on the board. But according to the present requirement, we want to create the input signal of 50 Hz. So a CMULT block is inserted to adjust the frequency of the waveform at the output.

The Counter count limit is set as $2^{25}-1$ in present case. We have taken 1024 samples to be addressed in ROM block. It is required that the multiplier constant of the CMULT block must be chosen such that it counts up to 1024 for addressing the ROM. After completing the count, the counter restarts from the initial value. Thus, the continuous stream of repeated samples are stored in ROM.
The constant for multiplier block is chosen based on following calculation, that is, if 1 cycle of waveform takes 20 ms then three cycles will take 60 ms. The 1024 samples stored in the ROM corresponds to the three power cycles, each of 20 ms. Thus, if 1024 samples are considered in 60 ms, then one sample takes 60/1024 ms i.e. 0.0586 ms. Hence the delay of 0.0586 ms is to be used as constant in CMULT block as shown in the Fig. 4.13. In this way, input similar to power signal at 50 Hz is created by using Xilinx FPGA board. The 12-bit digital output from the FPGA is then converted to its analog equivalent using 12-bit DAC. The voltage divider circuit is used to get analog signal between 0-1 V range as the voltage specification for ADC of the FPGA board is 0 - 1 V (unipolar). This analog input is to be given to the filter-board for further processing. The input created for magnetizing inrush resulting from hardware simulation model is shown in Fig. 4.14. It can be observed from Fig. 4.14 that repeated sequence of the three cycles of inrush current waveform is present. The data of first three cycles of the simulation waveform is stored in the ROM block of Fig. 4.13. The same data is repeated as the address counter of the ROM block is pointing again from its initial value, hence, repeated sequence is observed. Each cycle corresponds to time period of 20 ms. Similarly Fig. 4.15 shows three cycles of overflux inrush waveform where, three cycles appears repeatedly.

Fig. 4.16 shows created differential signal for in-zone fault without considering the CT saturation case. In this case, it can be observed that four cycles of the waveform from the occurrence of fault are stored in the ROM and are appearing repeatedly. These

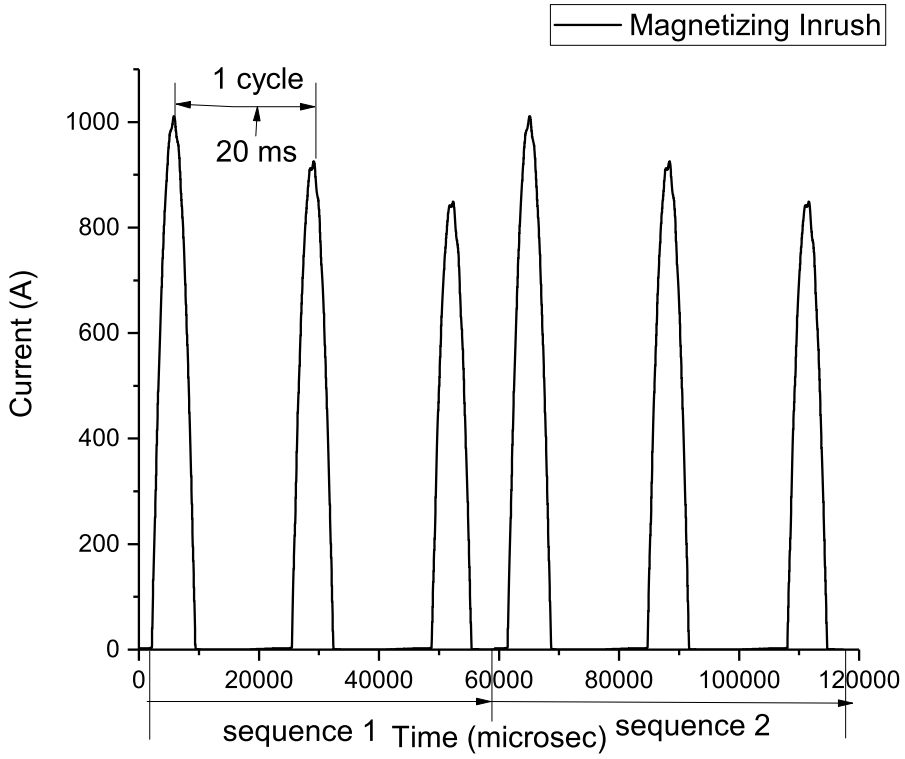

Figure 4.14: Recorded simulation waveform for magnetizing inrush using hardware simulation model

waveforms correspond to MATLAB simulation where the number of samples in 20 ms cycle are 250. The CMULT was adjusted accordingly to get each cycle of 20 ms time period. Fig. 4.17 shows input signal for in-zone fault with CT saturation case. Fig. 4.18 shows input signal created for external fault with CT saturation case.

The hardware simulation model implemented in the System Generator is implemented on a hardware system consisting of Nexys A7 FPGA board. The waveform generated by the waveform-board was tested for its accurate performance.

4.5.2 Filter-Board Design

The steps to perform matched wavelet analysis on the stored differential waveform as discussed in section 4.5.1, the steps are shown in schematic diagram of Fig. 4.5. The ADC inbuilt in the Xilinx board is used to feed the analog differential signal to the board. The input voltage range of the ADC is 0-1 volt and hence voltage divider circuit is used at the output of the first FPGA (waveform-board). After analog-to-digital conversion, the output of ADC is 12 bit wide. Each of these samples undergo series of operations as described in Section 4.3. Each of these operations is to be performed well within the occurrence of two consecutive samples. That is, the block timings are to be appropriately timed to get the multiple operations done between two subsequent samples. The required clock time/frequency is calculated in the following manner.
The matched wavelet corresponding to 12 coefficients operates on one cycle data window containing equally spaced 173 data samples. Hence, 173 samples are involved in 20 ms time duration. Therefore, 1 sample will take 20/173 ms i.e. 11560 ns. All the samples in the data window are then passed through the Comparator unit to get the maximum absolute value. These 173 samples are then divided with the maximum in order to normalize the data samples. Note, in simulations also the wavelet analysis is done on normalized signal in order to get unbiased result. After normalization, the data samples are given to MAA unit. The normalized delayed signals are multiplied with wavelet coefficients and aggregated in the MAA unit. The output of the MAA unit is 12-bit wide and DAC is employed to get the analog equivalent for observing the output on the DSO. The analog output was taken to ascertain the correctness and accuracy of the processing of the filter unit.

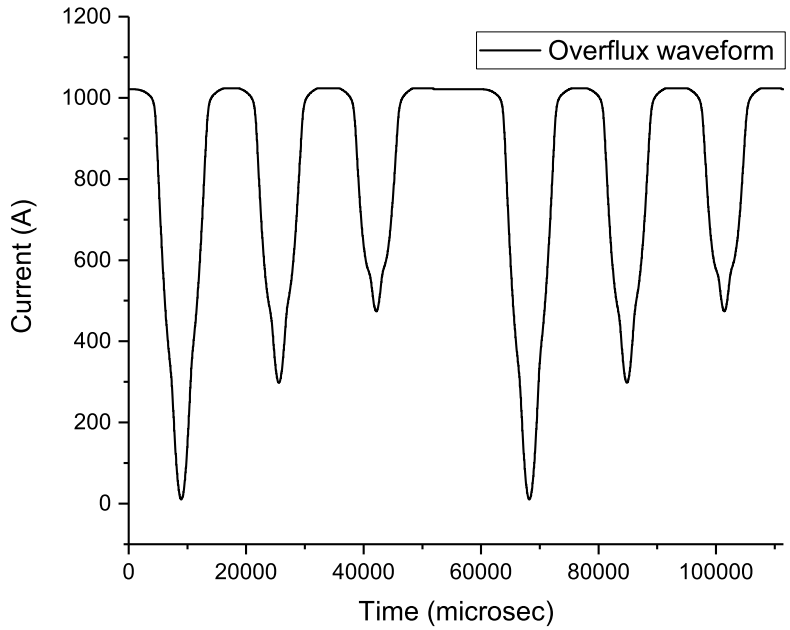

Figure 4.15: Recorded simulation waveform for over-flux inrush waveform using hardware simulation model

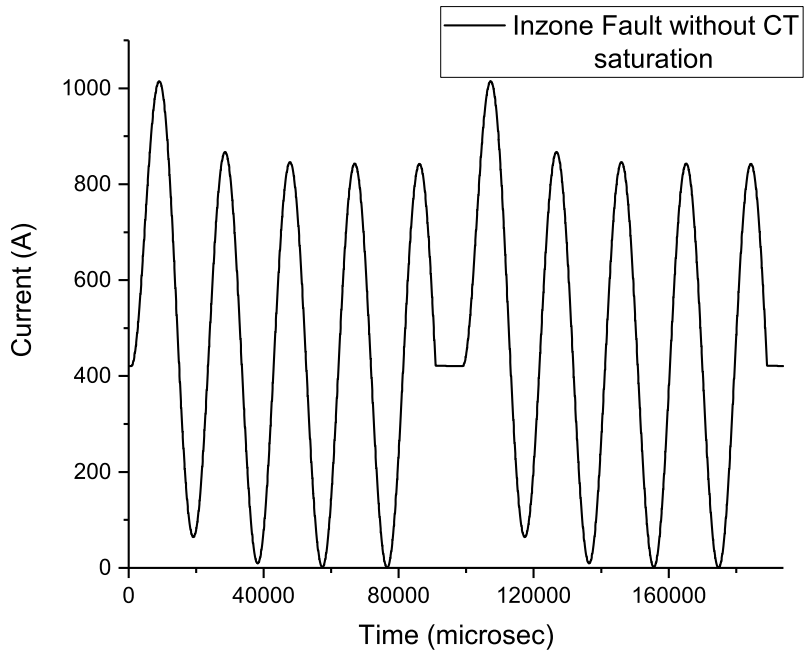

Figure 4.16: Recorded simulation waveform for in-zone fault without CT saturation using hardware simulation model

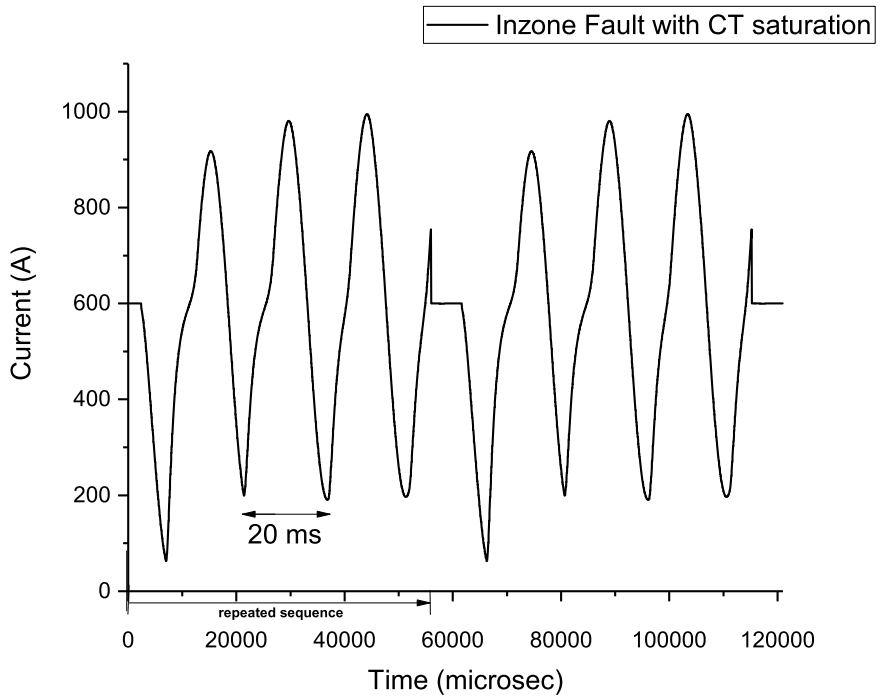

Figure 4.17: Recorded simulation waveform for in-zone fault (L-G fault) with CT saturation using hardware simulation model

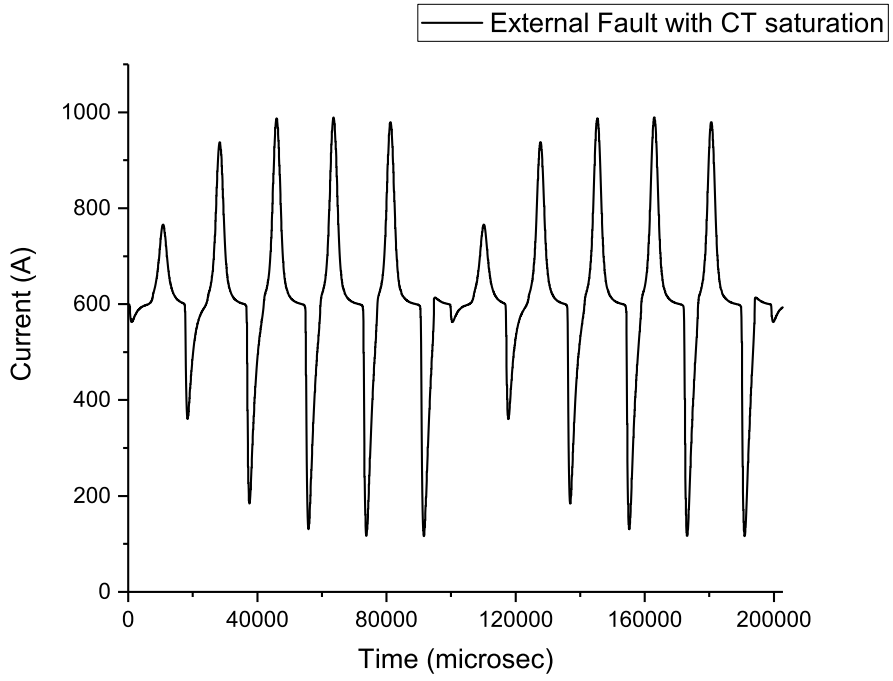

Figure 4.18: Recorded simulation waveform for external fault (L-G fault) without CT saturation using hardware simulation model

4.5.3 Hardware Set-up (Stage 3)

Fig. 4.19 shows the hardware set-up for the proposed scheme of differential protection of power transformer. As discussed previously, in this chapter two Xilinx FPGA boards are used for the purpose. From Fig. 4.19 it can be observed that Nexys A7 and Nexys Video are two FPGA boards used for the purpose. The hardware simulation model for creating input waveform, i.e waveform-board, shown in Fig. 4.13 is implemented on Nexys A7 FPGA board. Digital output from the waveform-board is given to the 12-bit R-2R ladder DAC1 implemented on breadboard. Thus, the analog output from 12-bit DAC1 is given to ADC channel of second FPGA board i.e. filter-board. As per the scheme, two separate Nexys video boards are used for each filter i.e. inrush-filter and fault-filter. However in the developed set-up, the processing of each filter was done one-by-one for each waveform using single Nexys video board (as per the availability). During planning stages it was assumed that a single board would suffice to implement both the filters in parallel. Also, the output of this DAC1 is connected to the DSO on one of the channels. The Nexys video Xilinx FPGA board, implementing the filter-board, has an inbuilt ADC which takes analog input in the range of 0-1 V range. Hence output of the DAC1 is to be first scaled to 0-1 V range before giving the same to the ADC channel of the filter-board in Fig. 4.19.

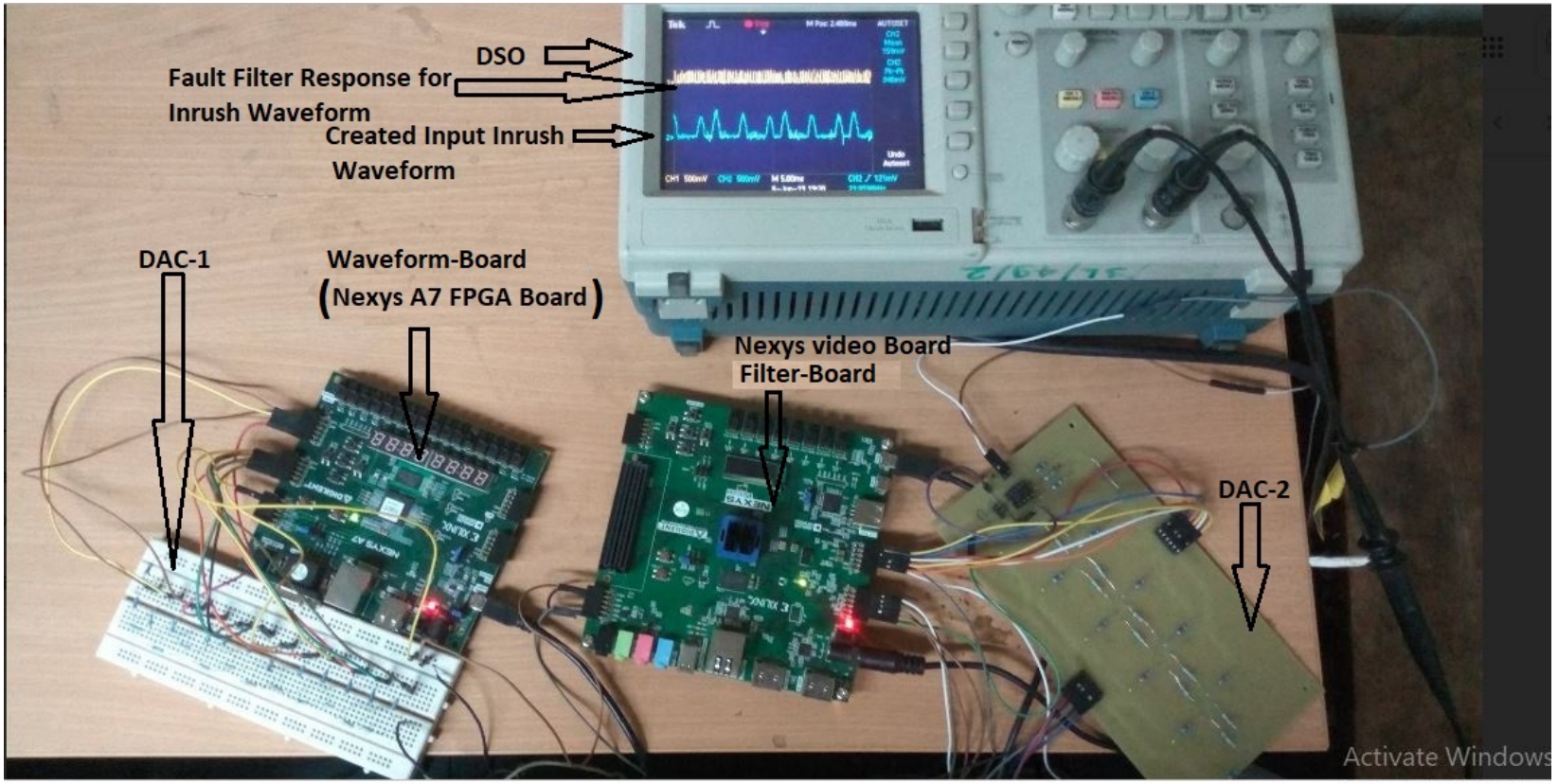

Figure 4.19: Hardware set-up

4.5.4 Results and Discussion (Stage 3)

The results obtained from the hardware set-up for magnetizing inrush current are shown in Fig. 4.20 and Fig. 4.21. Fig. 4.20 is the closer view of Fig. 4.21. Fig. 4.21 gives complete view of the response for three cycles. It is observed that for the inrush waveform as shown in Fig. 4.21(CH-2), the response of the inrush-filter (Fig. 4.21(CH-1)) is higher than the threshold. Thus, the inrush-filter on hardware gives correct response and successfully detects the presence of inrush signal. Response of fault-filter to the inrush waveform is shown in Fig. 4.22(CH-1). Similarly Fig. 4.23(CH-1) shows the response of fault-filter for in-zone fault with low CT saturation along with the in-zone fault current in Fig. 4.23(CH-2). It can be observed from Fig. 4.23 that fault-filter response is crossing the threshold and hence correctly detecting the presence of fault signal. Fig. 4.24(CH-1) shows the response of inrush-filter to in-zone fault with low CT saturation. Fig. 4.24(CH-1) depicts that the response of inrush-filter for fault signal is well below the threshold as desired. Fig. 4.25 and Fig. 4.26, respectively show responses of inrush- and fault-filters to over-flux inrush current. It can be observed from Fig. 4.25(CH-1), that inrush-filter is successfully detecting the over-flux inrush current, as its response is higher than the threshold, whereas, in Fig. 4.26(CH-1) fault-filter response is well below threshold for this case. Fig. 4.27 and Fig. 4.28, respectively show responses of inrush- and fault-filters for external fault with CT saturation. The fault-filter response is well below the threshold as desired for external fault signal as shown in Fig. 4.28(CH-1). In order to augment the correctness of the obtained response, the fault-filter response (indicating no in-zone fault) is considered, to ensure that it does not cross the threshold. It is apparent that the decision is finally made (indicating no in-zone fault), even though for inrush it crosses the threshold (as discussed in section 3.3.2). Fig. 4.29 and Fig. 4.30, respectively show responses of inrush- and fault-filters for in-zone fault with moderate CT saturation. Fig. 4.30(CH-1) depicts that fault-filter response crossing threshold and Fig. 4.29(CH-1) depicts that inrush-filter response also crosses the threshold but trip decision is taken accordingly as per the *independent* detection of fault. All the waveforms discussed in Chapter 3 are applied to the filters implemented in FPGA hardware for testing the efficacy of the matched wavelets in hardware. It was found that the hardware implementation accurately performed the detection thereby confirming the efficacy of matched wavelet implementation in hardware.

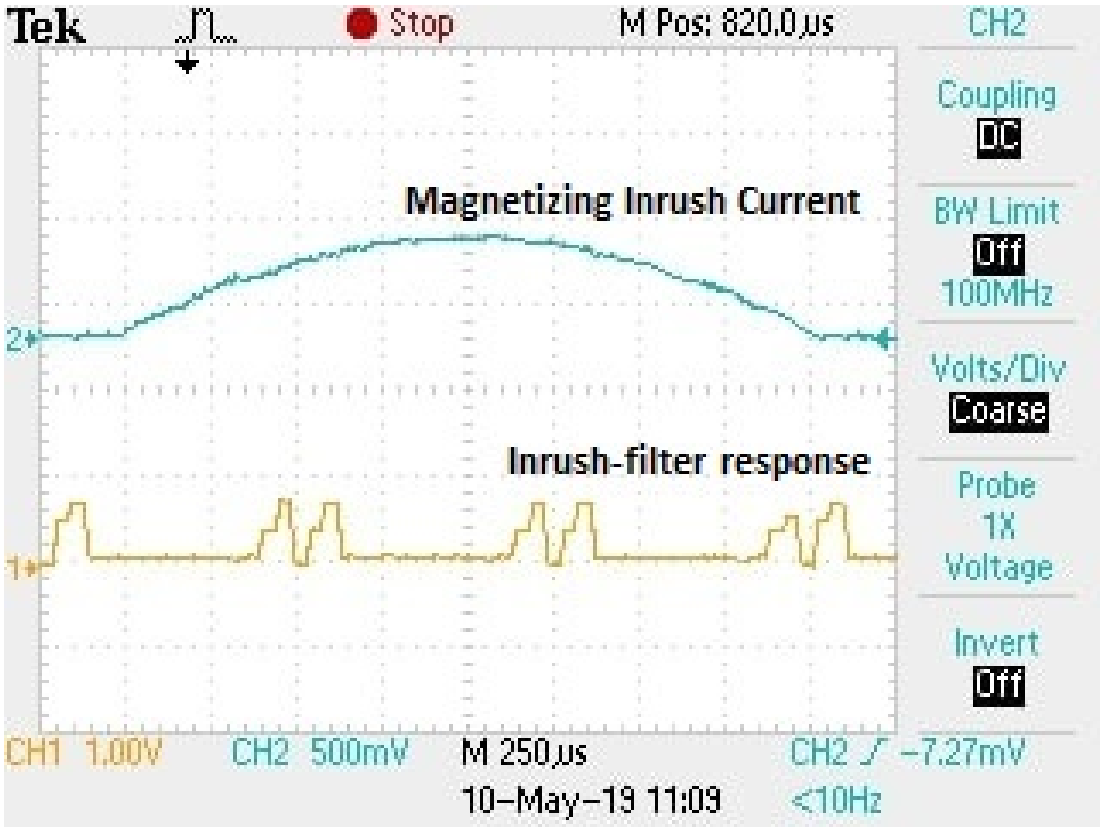

Figure 4.20: (CH2) Magnetizing inrush current. (CH1) Response of inrush-filter indicating inrush.

4.6 Hardware Implementation-II (Stage 4)

As discussed in section 4.2, in stage-4 of implementation, the transformer differential waveforms are generated for an actual transformer. For this purpose, an isolation transformer of 1 kVA, 220/110V is used to generate differential current waveforms under different conditions. The hardware set-up to obtain and test proposed matched wavelet algorithm is depicted in Fig. 4.31. The important component of the hardware set-up are labeled in Fig. 4.31. The detail of the components shown in the diagram are as follows.

1. Transformer1: For generating inrush and fault current waveforms.

2. Transformer2: For generating sympathetic inrush conditions.

3. Auto-Transformer: For controlling the primary side voltage for controlling fault currents.

4. Current Transformers (CTs): Two CTs are used in differential mode. To balance

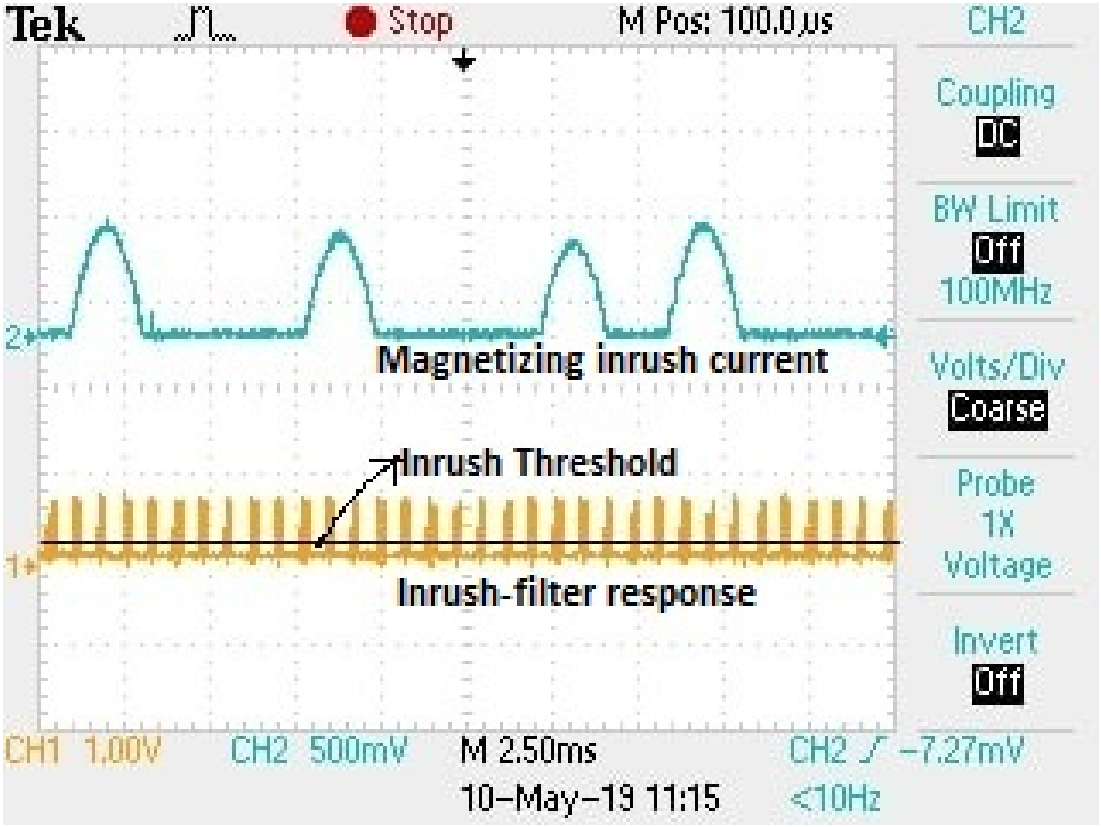

Figure 4.21: (CH2) Magnetizing inrush current. (CH1) Response of inrush-filter indicating inrush.

the primary and secondary current, the turn ratios are adjusted on the primary side of CTs.

5. Load: To generate inrush, in-zone fault, and external fault waveforms under loaded conditions.

6. MCB switch: MCB switch is used to generate fault condition for short circuiting the secondary windings of the transformer.

7. Mangnine Resistance Box: The resistance box is connected in series with MCB switch for connecting different fault resistances.

8. NI PXIe-1078: The NI PXIe system is used to acquire the differential waveform signals obtained from the CTs.

9. Filter-board: This FPGA board is used to implement the matched wavelet inrush- and fault-filter proposed in these studies.

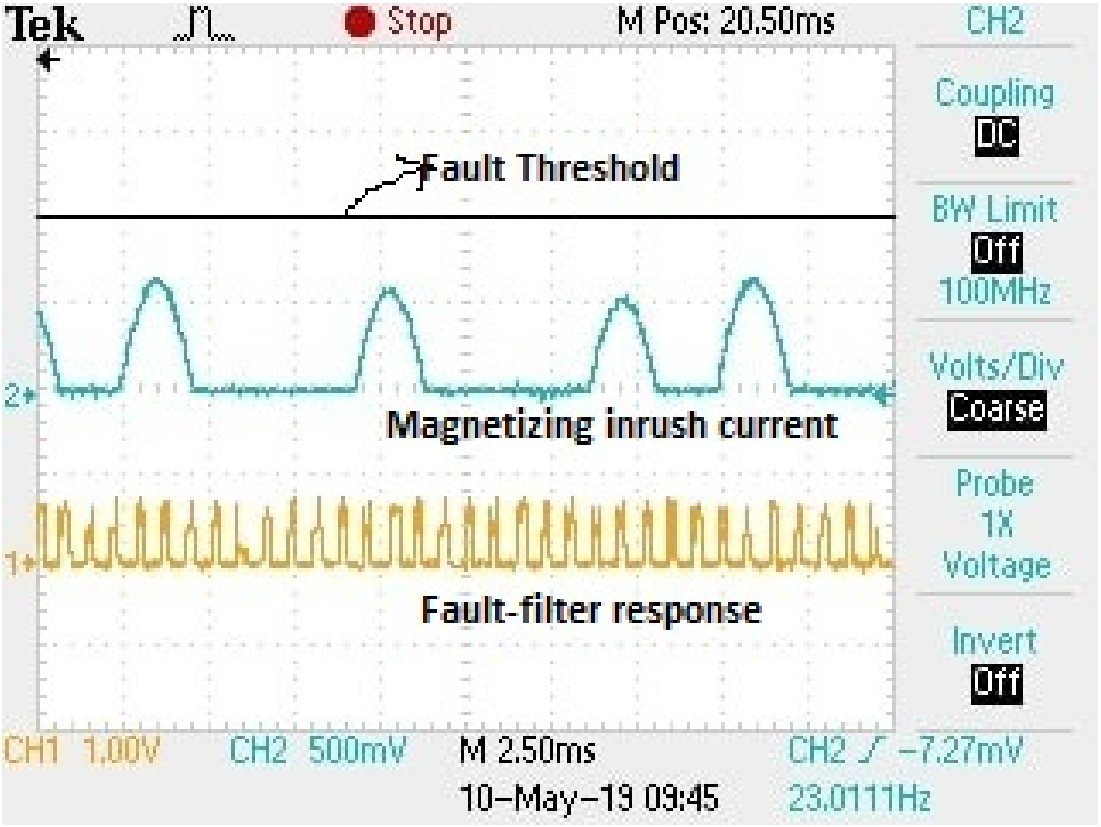

Figure 4.22: (CH2) Magnetizing Inrush current. (CH1) Response of fault-filter indicating no fault.

10. Waveform-board: This FPGA board is used to record the transformer waveform acquired through NI PXIe-1078 system.

11. DSO: to record and display the differential waveforms and filter responses as outputs.

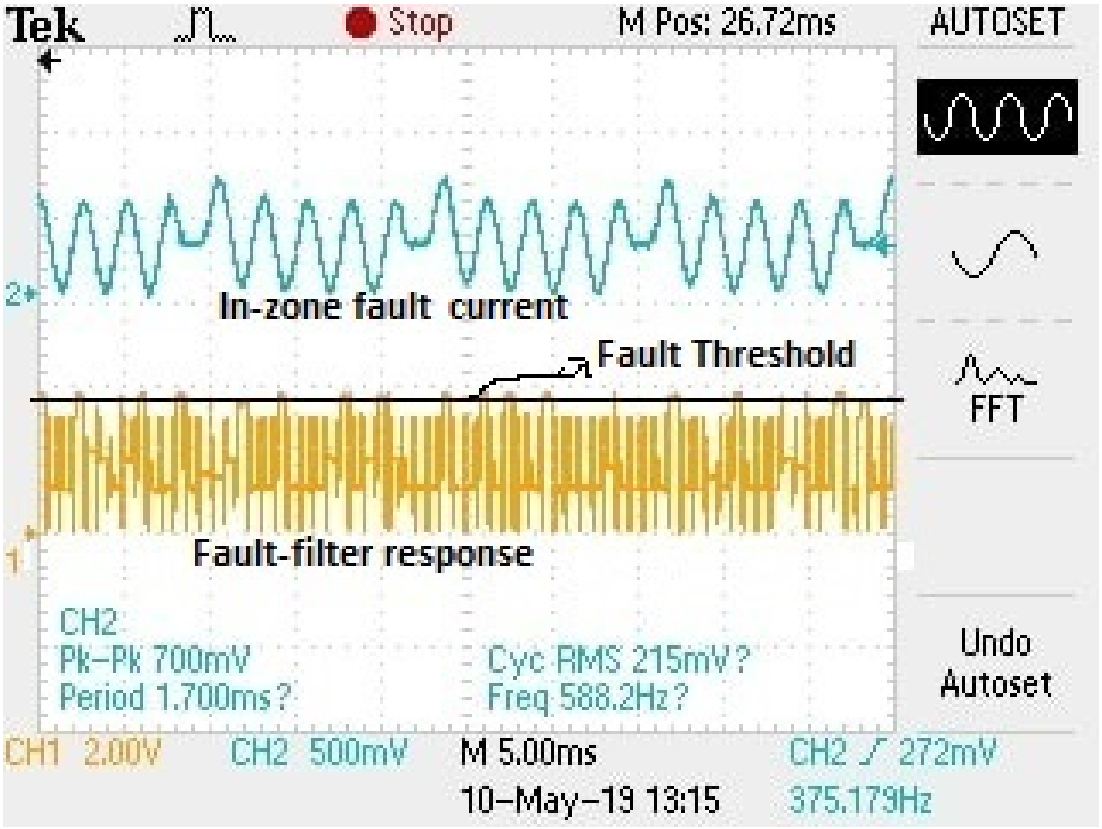

Figure 4.23: (CH2) In-zone fault (L-G fault) current with low CT saturation. (CH1) Response of fault-filter indicating fault.

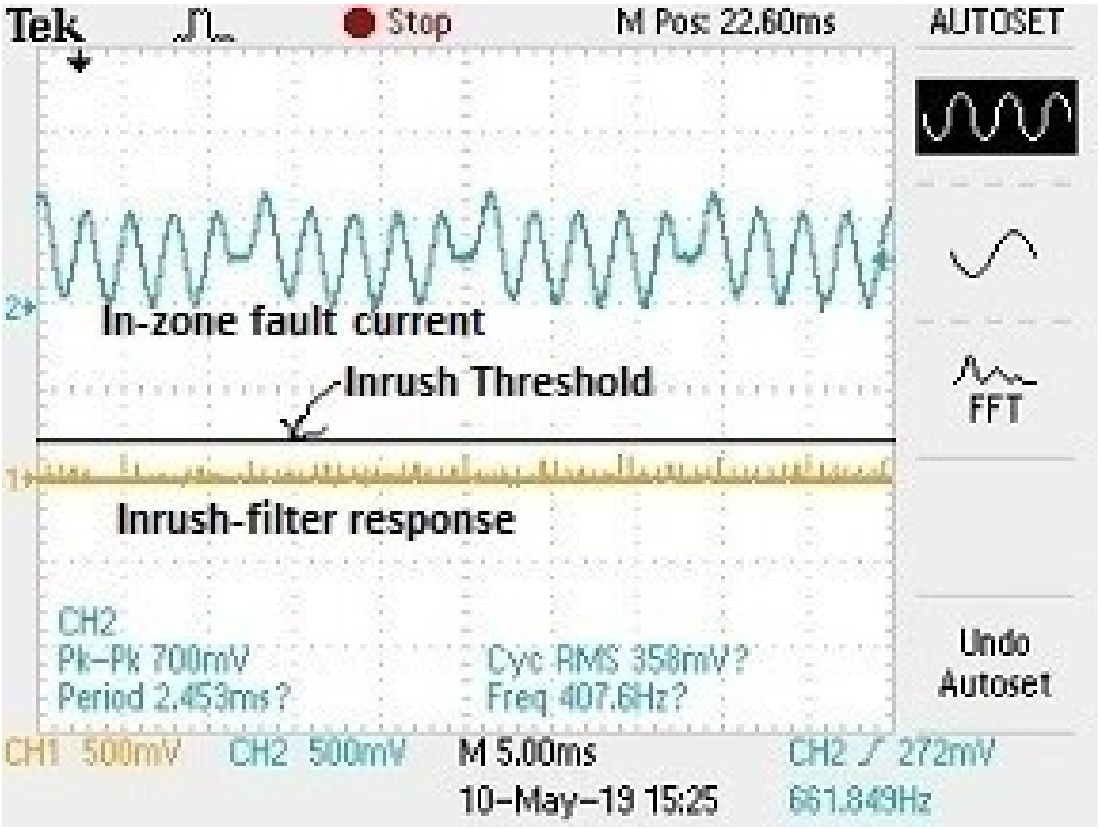

Figure 4.24: (CH2) In-zone fault (L-G fault) current with low CT saturation. (CH1) Response of inrush-filter indicating no inrush.

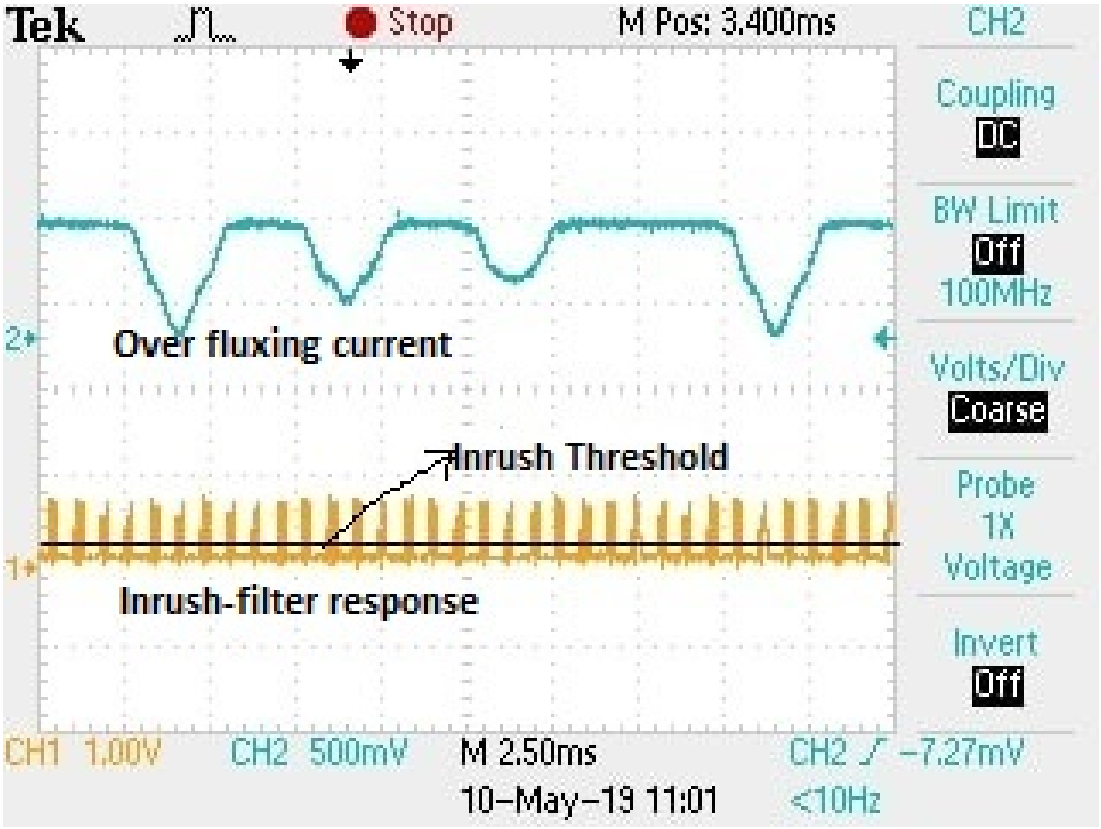

Figure 4.25: (CH2) Over fluxing current. (CH1) Response of inrush-filter indicating inrush.

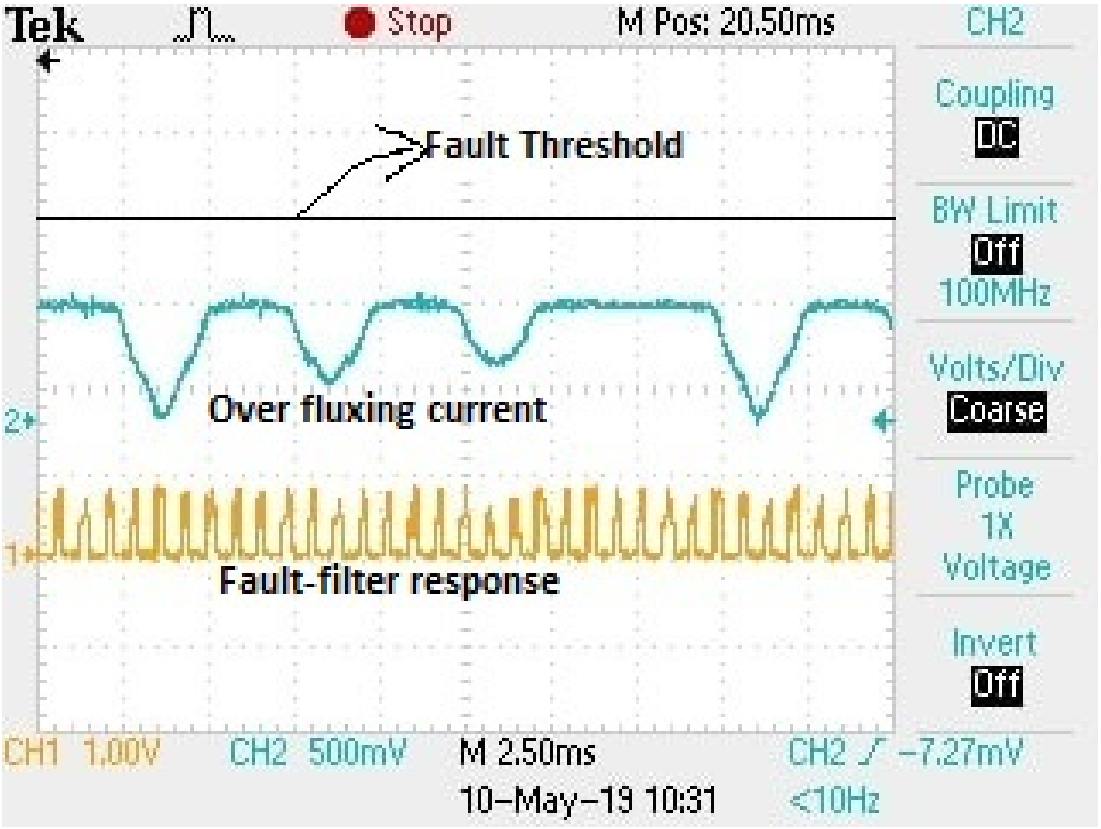

Figure 4.26: (CH2) Over fluxing current. (CH1) Response of fault-filter indicating no fault.

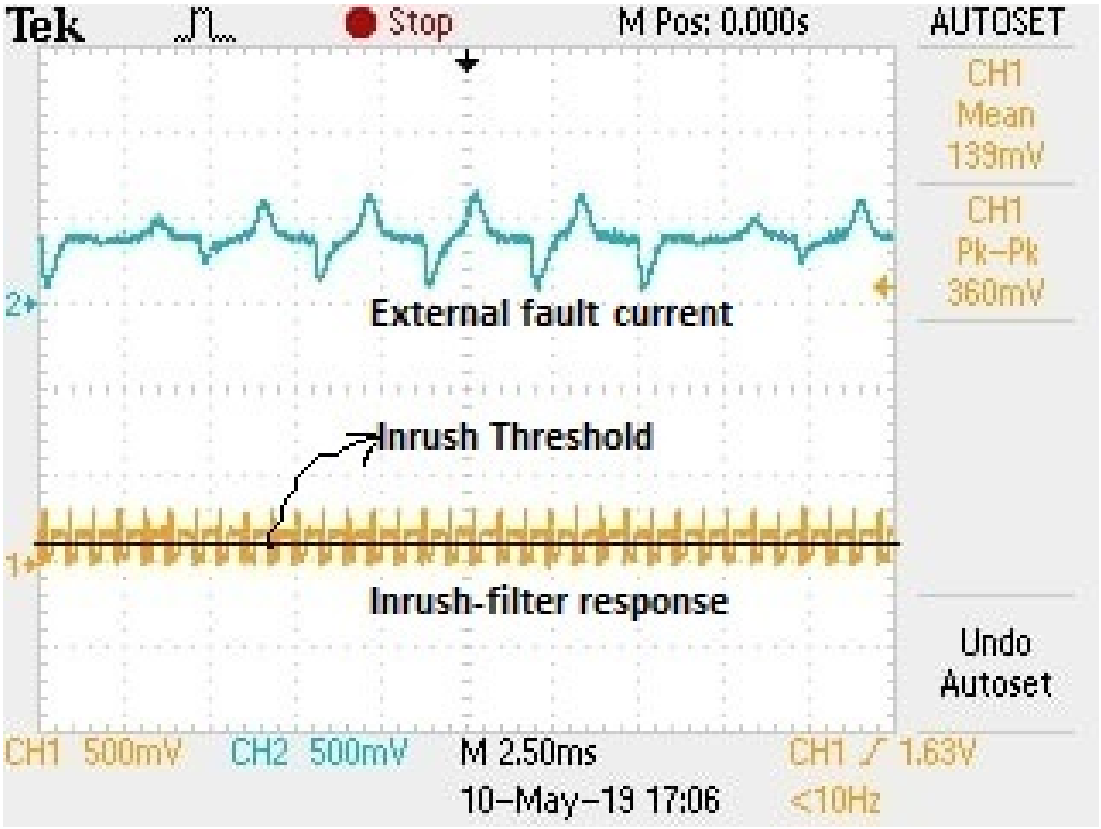

Figure 4.27: (CH2) External fault (L-G fault) current with CT saturation. (CH1) Response of inrush-filter indicating inrush.

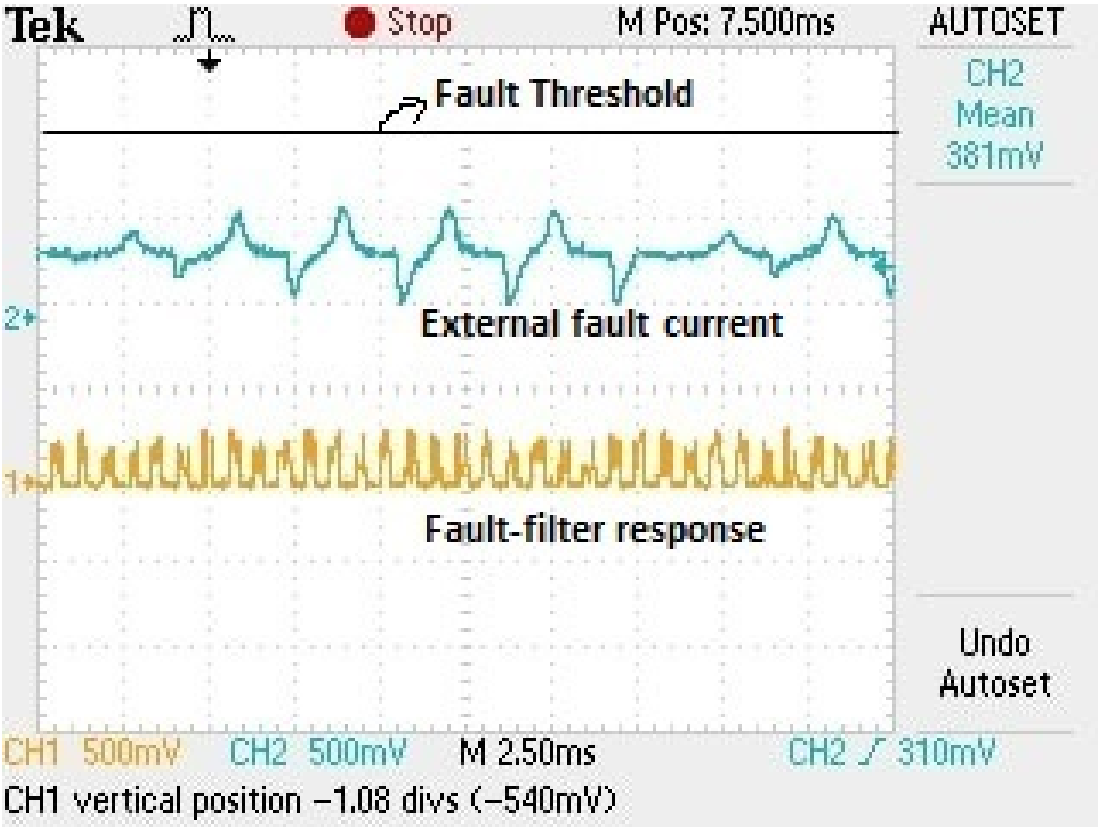

Figure 4.28: (CH2) External fault (L-G fault) current with CT saturation. (CH1) Response of fault-filter indicating no fault.

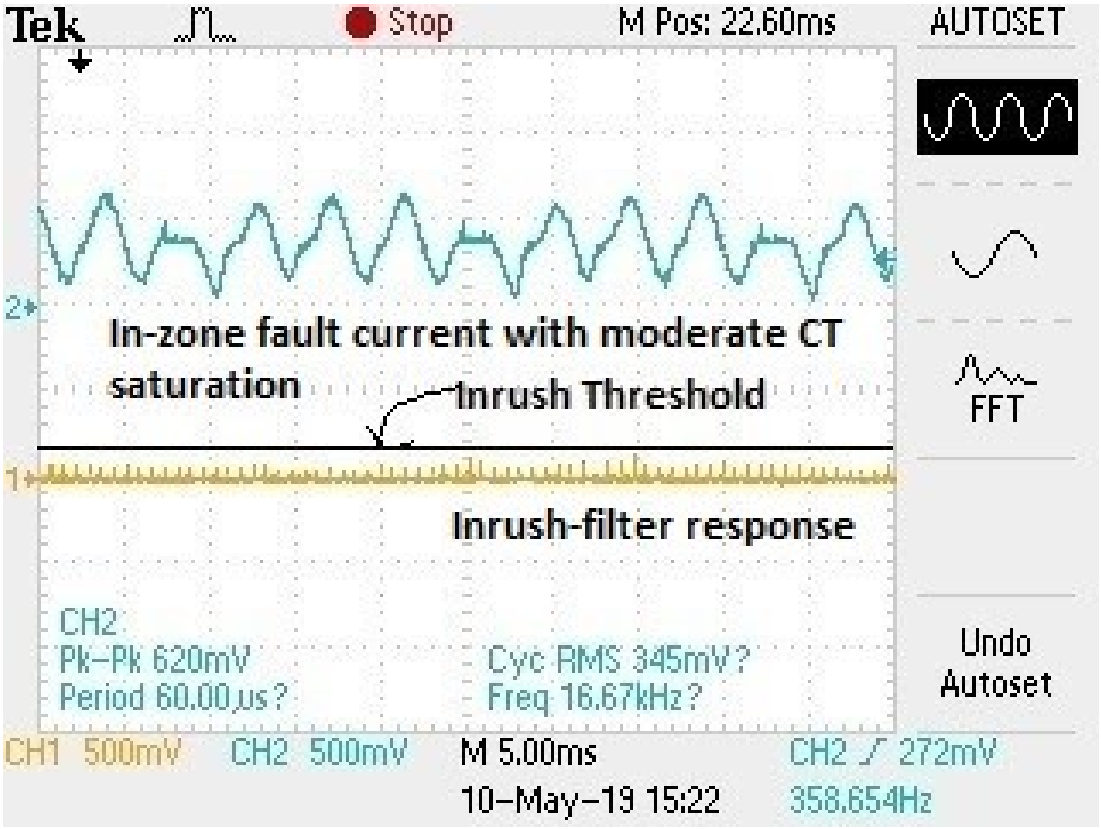

Figure 4.29: (CH2) In-zone fault (L-G fault) current with moderate CT saturation. (CH1) Response of inrush-filter indicating no inrush.

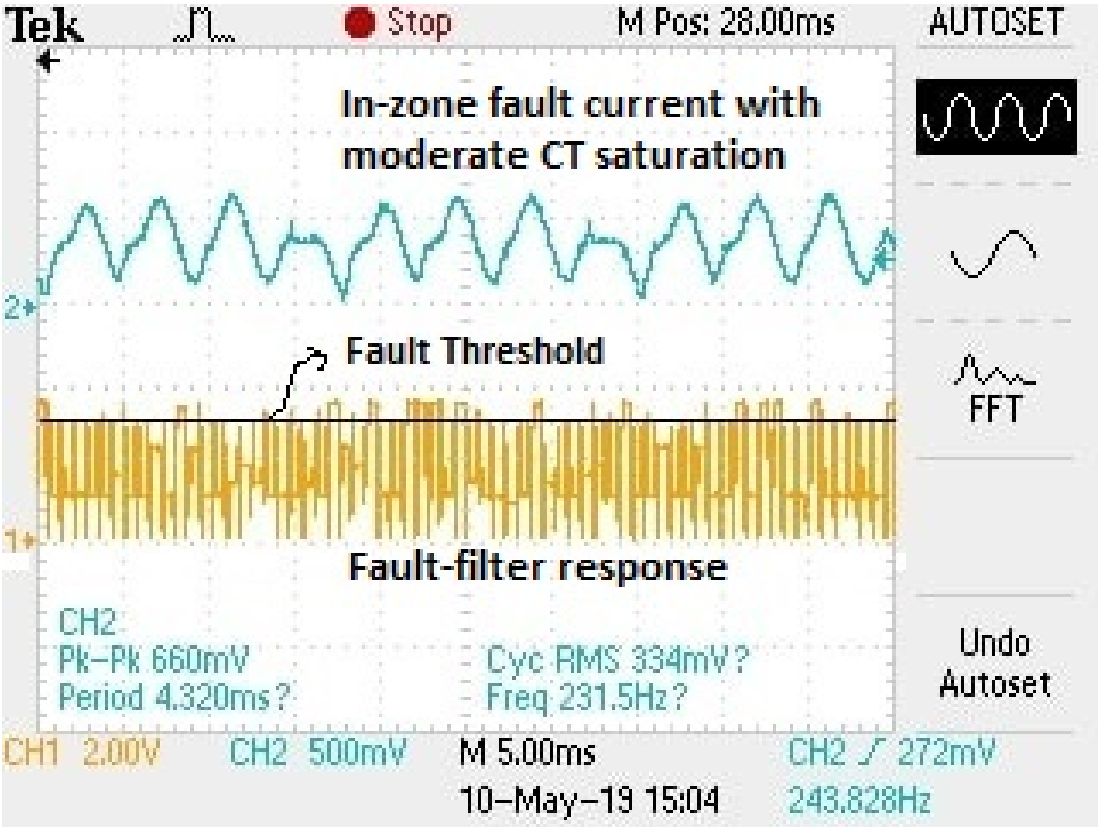

Figure 4.30: (CH2) In-zone fault (L-G fault) current with moderate CT saturation. (CH1) Response of fault-filter indicating fault.

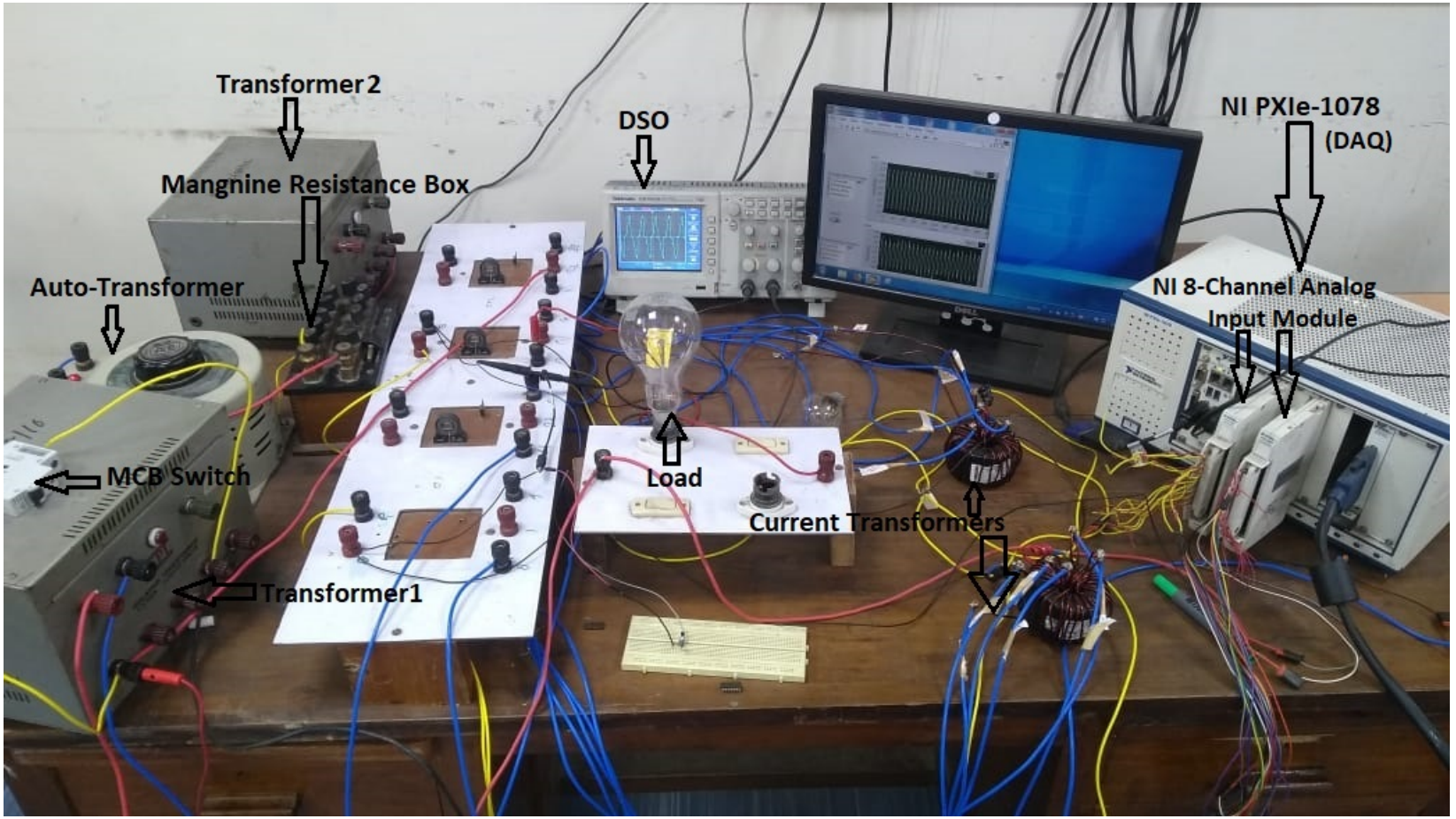

Figure 4.31: Hardware set-up

4.7 Hardware Results on a Physical Transformer

As discussed in the previous section, an isolation transformer of rating 1 kVA, 220/110V, 50 Hz (details provided in Appendix-II) is used to obtain actual waveforms for testing the performance of the proposed matched wavelet system in a practical environment. The threshold value decided for the inrush-filter is 0.08, i.e. the response value crossing a value of 0.08 indicates presence of inrush. Similarly, the threshold value decided for the fault-filter is 3.6, i.e. the response crossing a value of 3.6 indicates presence of fault. The results obtained for different conditions are discussed in the following sections.

4.7.1 Inrush Conditions

The tests are carried out for testing the performance of the matched wavelet filters under different inrush conditions. Fig. 4.32 channel 2 (CH-2) shows inrush waveform obtained for the unloaded transformer. The response of the inrush-filter is depicted in Fig. 4.32(CH-3). From Fig. 4.32(CH-3) it is observed that the response of inrush-filter crosses the threshold value indicating presence of inrush in the waveform of Fig. 4.32(CH-2). The inrush waveform of Fig. 4.32(CH-2) is also depicted in Fig. 4.33(CH-2) with response of the fault-filter in Fig. 4.33(CH-3). The response of the fault-filter in Fig. 4.33(CH-3) shows that the threshold for the fault-filter is not crossed, thereby indicating absence of fault phenomenon in the waveform of Fig. 4.33(CH-2).

An inrush waveform under loaded condition is depicted in Fig. 4.34(CH-2). The waveform was generated by loading the transformer with a resistive load of 200W bulb. The response of inrush-filter was captured on Channel 3 of the DSO and depicted in Fig. 4.34(CH-3). From the response of inrush-filter, it was observed that response crosses the threshold thereby indicating inrush condition. Fig. 4.35(CH-2) depicts the same waveform of Fig. 4.34(CH-2) with response of fault-filter in Fig. 4.35(CH-3). It is observed that the response indicates the presence of no-fault condition.

The waveform indicating sympathetic inrush under no-load condition is depicted in Fig.4.36(CH-2). The response of the inrush-filter shown in Fig.4.36(CH-3) clearly indicates an inrush condition in the waveform. The response of the fault-filter to the sympathetic inrush condition of Fig.4.36(CH-2) is depicted in Fig.4.37(CH-3) along with the waveform in Fig.4.37(CH-2). The response of the fault-filter correctly indicates no-

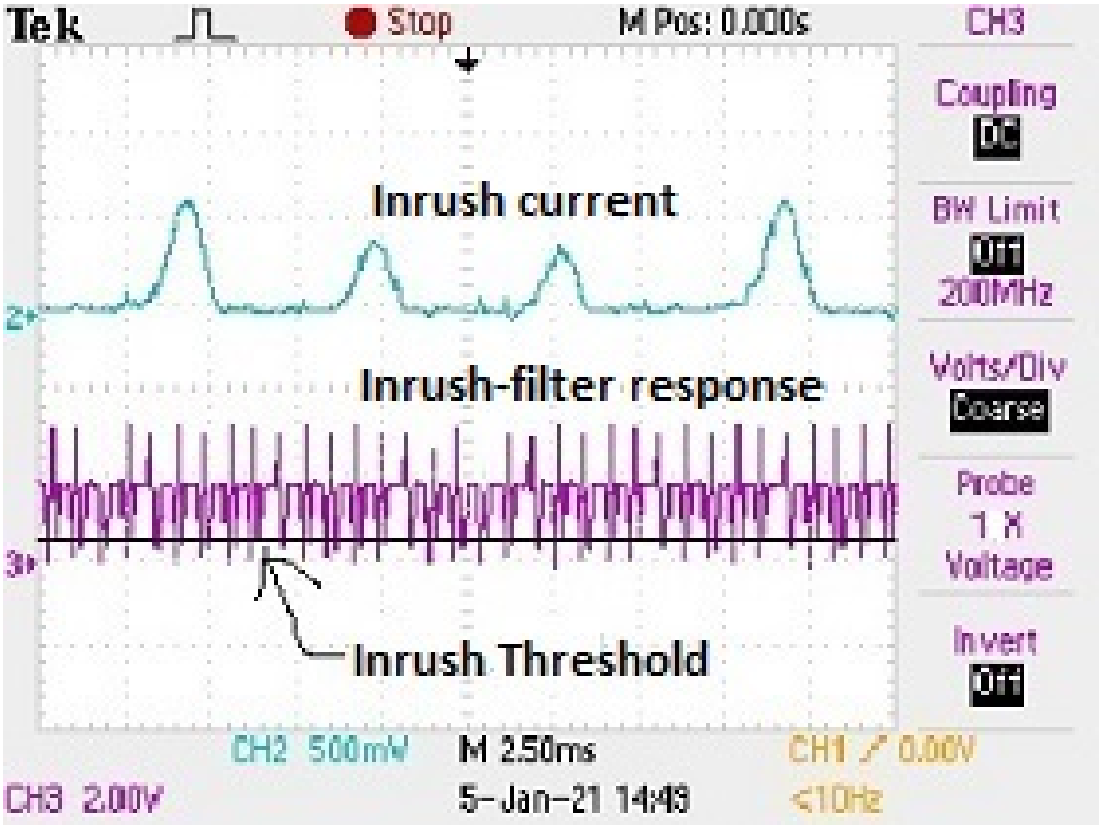

Figure 4.32: (CH2) Inrush current. (CH3) Response of inrush-filter indicating inrush.

fault condition for the waveform.

Fig. 4.38 (CH-2) and (CH-3) depict sympathetic inrush waveform and the inrush-filter response respectively, for transformer under loaded conditions. It was observed that the response of the inrush-filter crosses the threshold value detecting the presence of inrush phenomena in the presented waveform. The response of the fault-filter for same waveform is depicted in Fig. 4.39(CH-3). The response of the fault-filter is consistently below the threshold level indicating absence of fault phenomena in the presented waveform.

The detailed analysis of the developed inrush-filter and fault-filter for different inrush conditions shows that the inrush- and the fault-filter are able to perform quite accurately for the practical environment. The performance was similar to the case obtained earlier during simulation studies. The detection was successfully made within half cycle for all the inrush cases for the physical transformer.

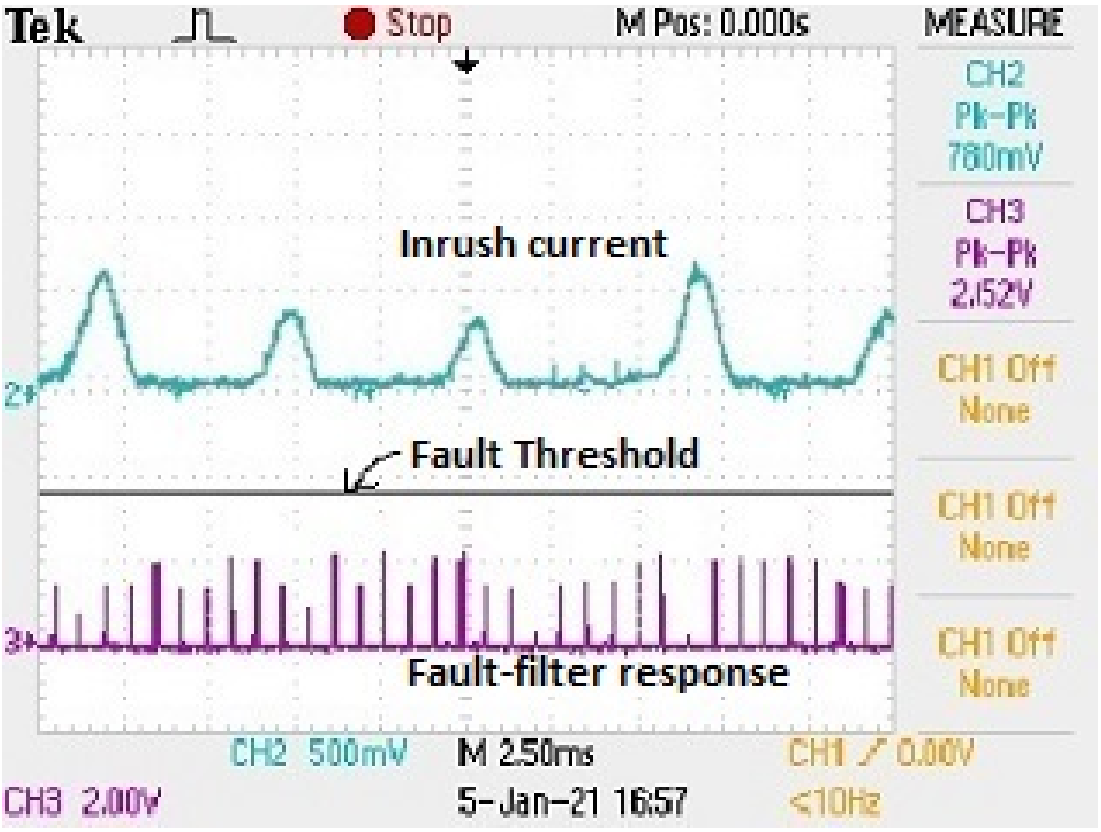

Figure 4.33: (CH2) Inrush current. (CH3) Response of fault-filter indicating no-fault.

4.7.2 In-zone Fault Conditions

Similar to the inrush waveforms, different in-zone fault conditions are also generated for testing the performance of the proposed inrush- and fault-filter. The fault waveforms are generated for different levels of CT saturation and different fault resistance conditions. As we have used a single-phase transformer for studies only L-G fault waveforms could be generated for studying the performance in the practical environment.

Fig. 4.40(CH-2) depicts an in-zone fault signal with very low or no CT saturation. It is observed that the waveform is almost sinusoidal with less distortion and disturbances. Fig. 4.40(CH-3) shows the response of inrush-filter to the fault waveform of Fig. 4.40(CH-2). The response of the inrush-filter is below the threshold level indicating absence of inrush phenomena in the presented waveform. The response of the fault-filter to the fault waveform of Fig. 4.40(CH-2) is depicted in Fig. 4.41(CH-3) along with the waveform in Fig. 4.41(CH-2). The response of the fault-filter clearly depicts the presence of fault phenomena in the presented waveform.

Fig. 4.42(CH-2) depicted waveform for an in-zone fault with moderate level of CT

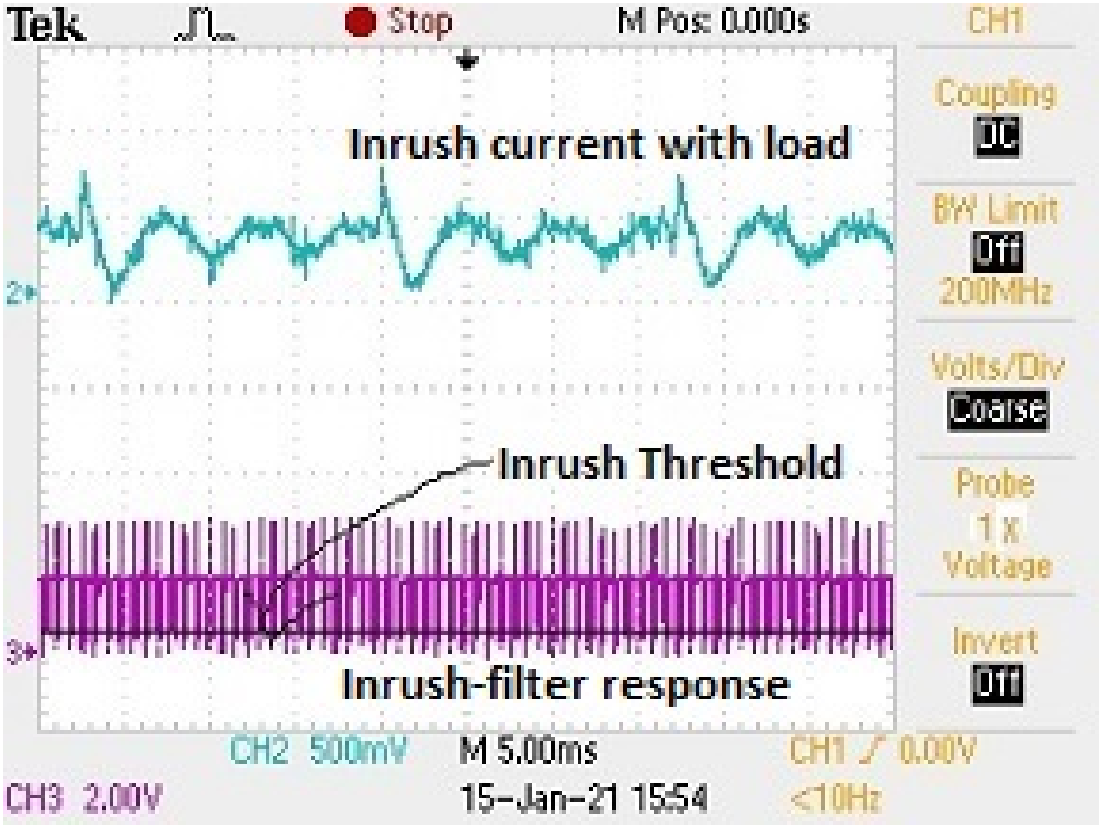

Figure 4.34: (CH2) Inrush current with load. (CH3) Response of inrush-filter indicating inrush.

saturation. The response of the inrush-filter is given in Fig. 4.42(CH-3) for the waveform of Fig. 4.42(CH-2). It is observed that the response of inrush-filter stays below the threshold level thereby indicating absence of inrush phenomena in the presented waveform. The response of the fault-filter for fault waveform of Fig. 4.42(CH-2) (also given in Fig. 4.43(CH-2)) is given in Fig. 4.43(CH-3). It is observed from the response of fault-filter that the presence of in-zone fault is detected successfully as the response crosses the threshold mark.

The fault current waveform obtained under high CT saturation condition is depicted in Fig. 4.44(CH-2). The associated response of the inrush-filter is depicted in Fig. 4.44(CH-3). The response of the inrush-filter clearly indicates the absence of fault phenomenon in the presented waveform. Thus, the inrush-filter is quite effective in detecting the absence of inrush condition even under high CT saturation condition. The fault-filter response to the fault waveform of Fig. 4.44(CH-2)(same as Fig. 4.45(CH-2)) is depicted in Fig. 4.45(CH-3). The response of the fault-filter detects the waveform as a

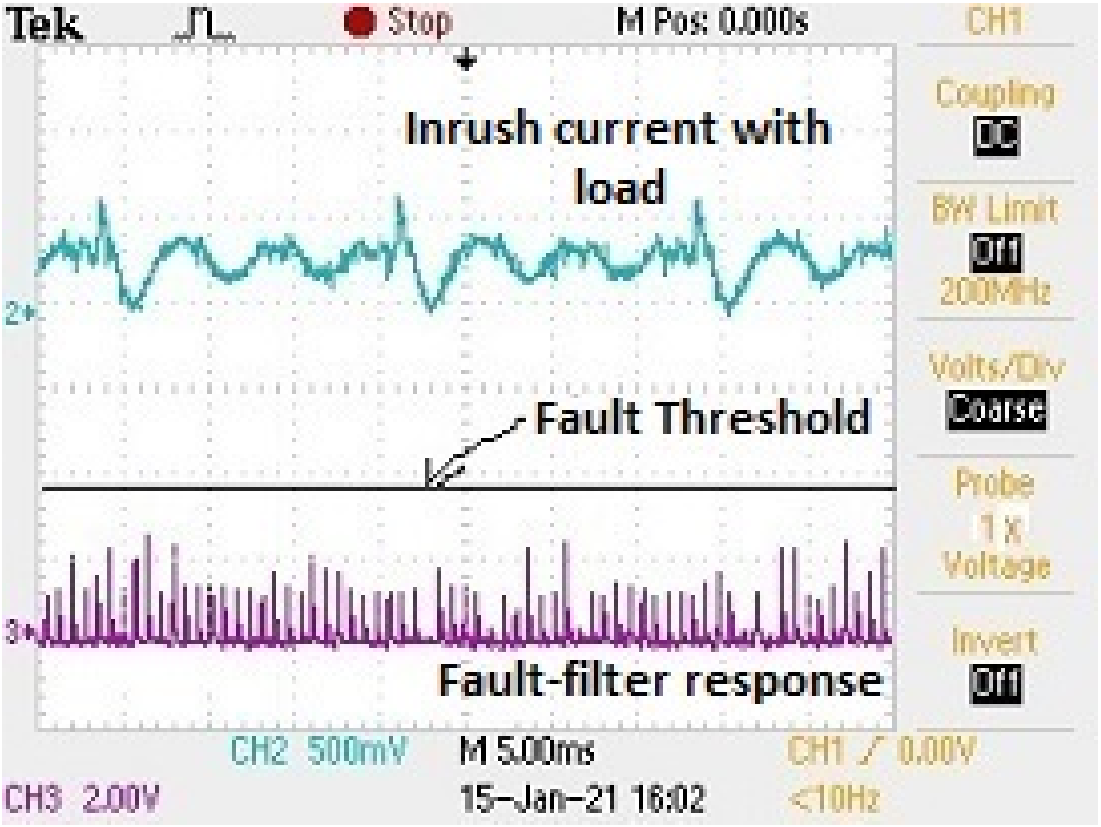

Figure 4.35: (CH2) Inrush current with load. (CH3) Response of fault-filter indicating no-fault.

fault waveform effectively.

The efficacy of the proposed algorithm is also tested for detection of fault under different fault resistances. A case of in-zone fault with fault resistance of $0.1 ohm$ is obtained from a practical transformer and the same is depicted in Fig. 4.46(CH-2). The response of the inrush-filter to the presented waveform is shown in Fig. 4.46(CH-3). It is observed from the response that the inrush-filter successfully detects the absence of inrush phenomena in the presented practical waveform. The waveform of Fig. 4.46(CH-2) is again plotted in Fig. 4.47(CH-2) with the associated response of the fault-filter plotted in Fig. 4.47(CH-3). The fault-filter, clearly detects the waveform as a fault waveform. Fig. 4.48(CH-2) shows the fault waveform with fault resistance of $0.5 ohm$ and the response associated with waveform is shown in Fig. 4.48(CH-3). The response of the inrush-filter clearly indicates the absence of inrush in the presented waveform. The response of the fault-filter for the waveform of Fig. 4.48(CH-2), (also shown in Fig. 4.49(CH-2)) is depicted in 4.49(CH-3). The response of the fault-filter indicates the detection of fault as

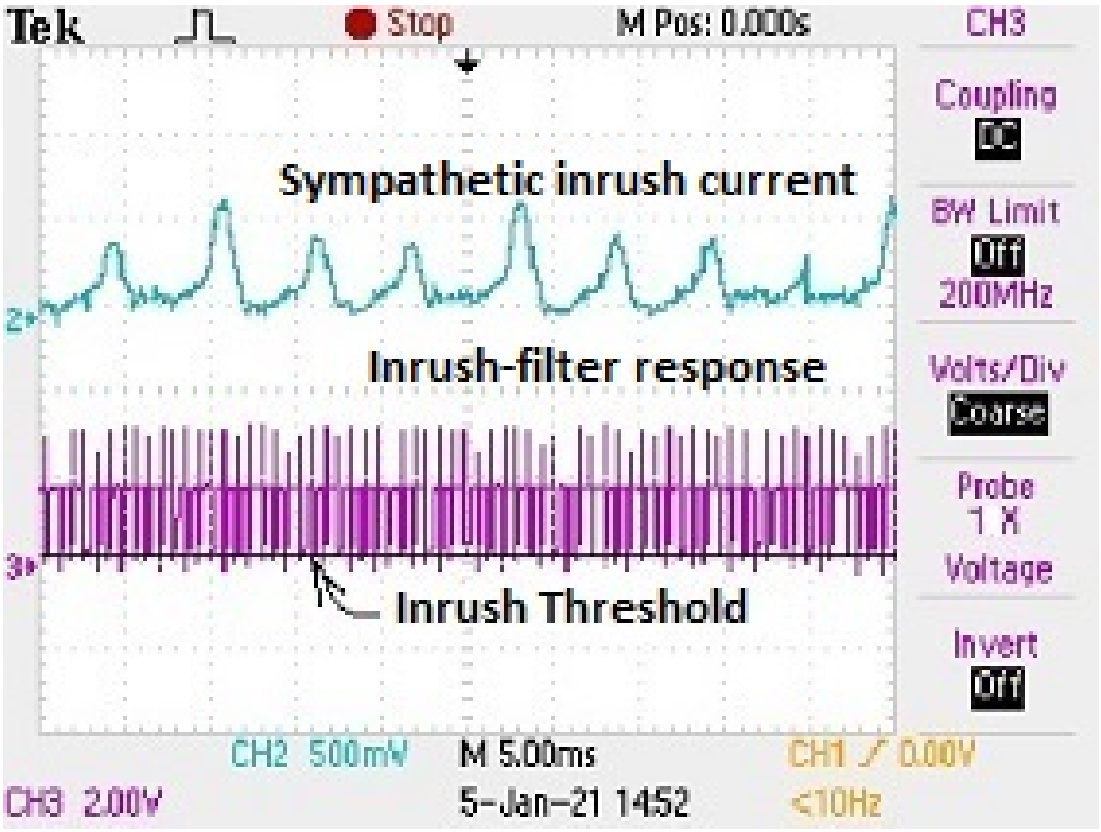

Figure 4.36: (CH2) Sympathetic inrush current. (CH3) Response of inrush-filter indicating inrush.

the response crosses the fault-filter threshold level. The set of Fig. 4.50 and Fig. 4.51 demonstrates the response of inrush- and fault-filter for in-zone fault current in presence of high fault resistance of $1 ohm$. The responses of inrush- and fault-filter clearly indicates the absence of inrush and presence of fault respectively.

The performance of the proposed inrush- and fault-filter on fault waveforms under varied conditions show that the proposed algorithms performed satisfactorily.

4.7.3 External Fault under CT Saturation

The external faults theoretically do not give rise to any differential current as the primary and secondary currents balance. However, the saturation of CTs give rise to a peaky differential current which may have substantial value leading to mal-operation of differential protection for out-of-zone or external fault in practical situations. Fig. 4.52(CH-2) shows the differential current waveform for a external fault for high amount of CT saturation. The response of inrush-filter depicted in Fig. 4.52(CH-3) indicates that the inrush-filter

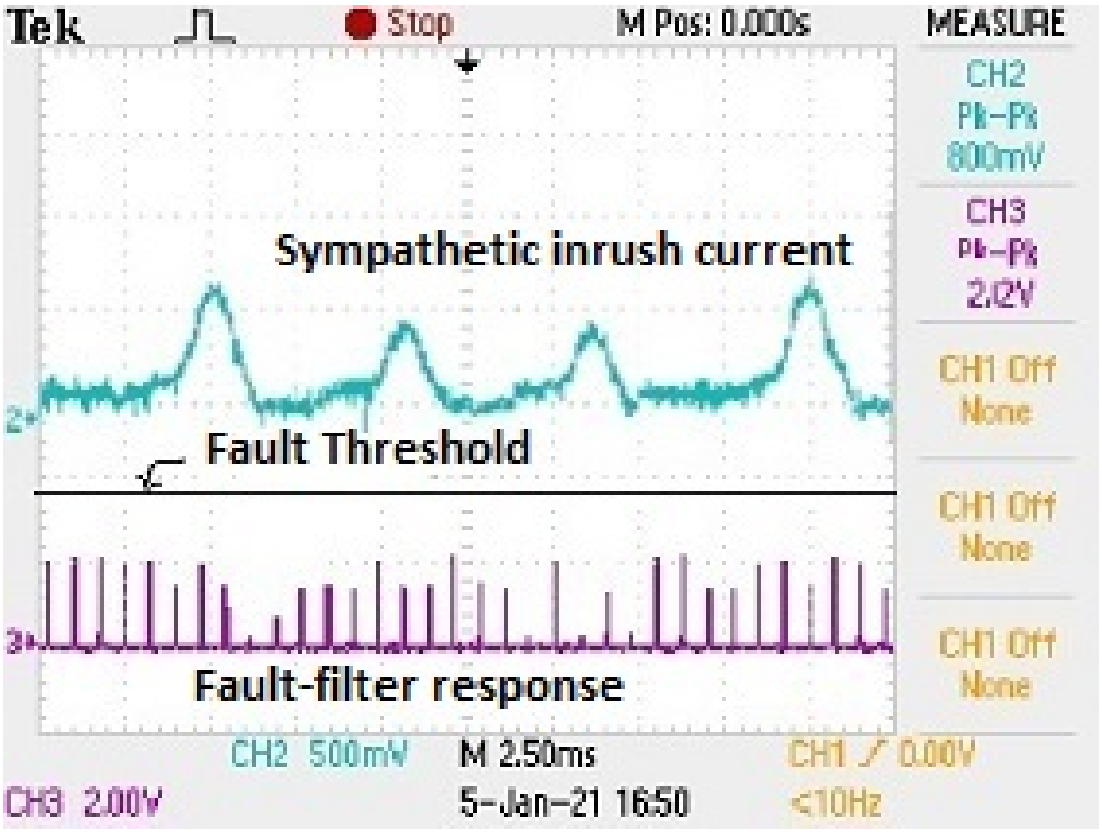

Figure 4.37: (CH2) Sympathetic inrush current. (CH3) Response of fault-filter indicating no-fault.

detects the waveform as an inrush waveform. As per the simulation results, this is expected as the external fault signals are close to inrush waveform. The waveform depicted in Fig. 4.52(CH-2) is also shown in Fig. 4.53(CH-2) along with the response of fault-filter depicted in Fig. 4.53(CH-3). The response of the fault-filter clearly detects the absence of in-zone fault phenomena in the waveform given to the fault-filter.

It is observed that the proposed inrush- and fault-filter act satisfactorily for the external faults in presence of CT saturation.

4.7.4 Energizing Transformer under Faulted Condition

One of the typical cases which are difficult to detect in case when a transformer under faulted condition is energized. Conventionally, during energisation it is believed that the high current is due to inrush, and the correct condition is detected only when several cycles of fault current passes through the transformer. The modified relaying scheme, relying on independent detection of fault and inrush currents handles this problem quite effectively

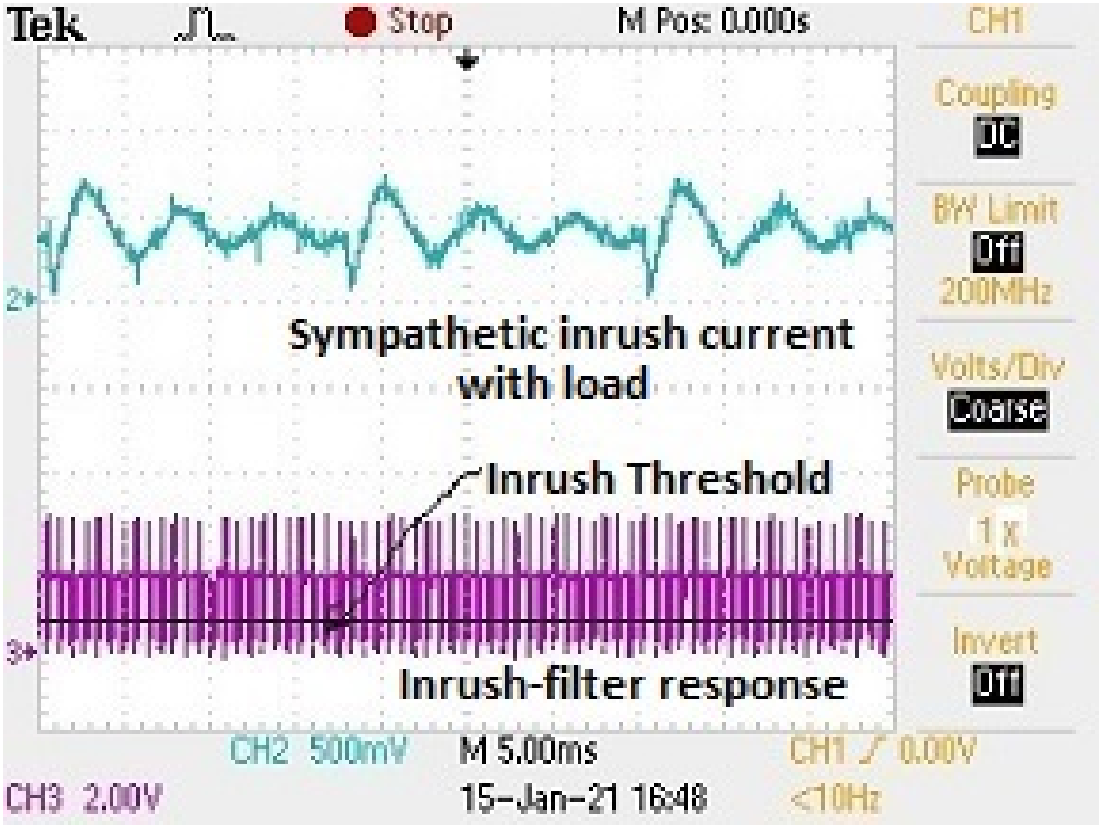

Figure 4.38: (CH2) Sympathetic inrush current with load. (CH3) Response of inrush-filter indicating inrush.

(refer to section 3.3.2). Fig. 4.54(CH-2) shows the waveform pertaining to energisation of transformer under fault. The response of inrush-filter clearly detects presence of no-inrush, as the response remain below the threshold. The response of the fault-filter for the energisation of transformer under fault is depicted in Fig. 4.55(CH-3). The response of the fault-filter correctly crosses the threshold indicating the fault.

4.7.5 Inter-turn Faults

Detection of inter-turn faults is considered as one of the good qualities of a differential relaying scheme. The detection of fault involving large number of turns (say higher than 80%) is considered similar to normal fault. However, when the number of turns involved is less than 20% the detection becomes quite difficult. The proposed wavelet based filters are tested for inter-turn fault involving up to 60% of the winding in simulation studies. In the present hardware studies, the transformer had tapping at 50% and 80% of the winding, therefore, the inter-turn fault involving up to 80% and 50% of the winding are

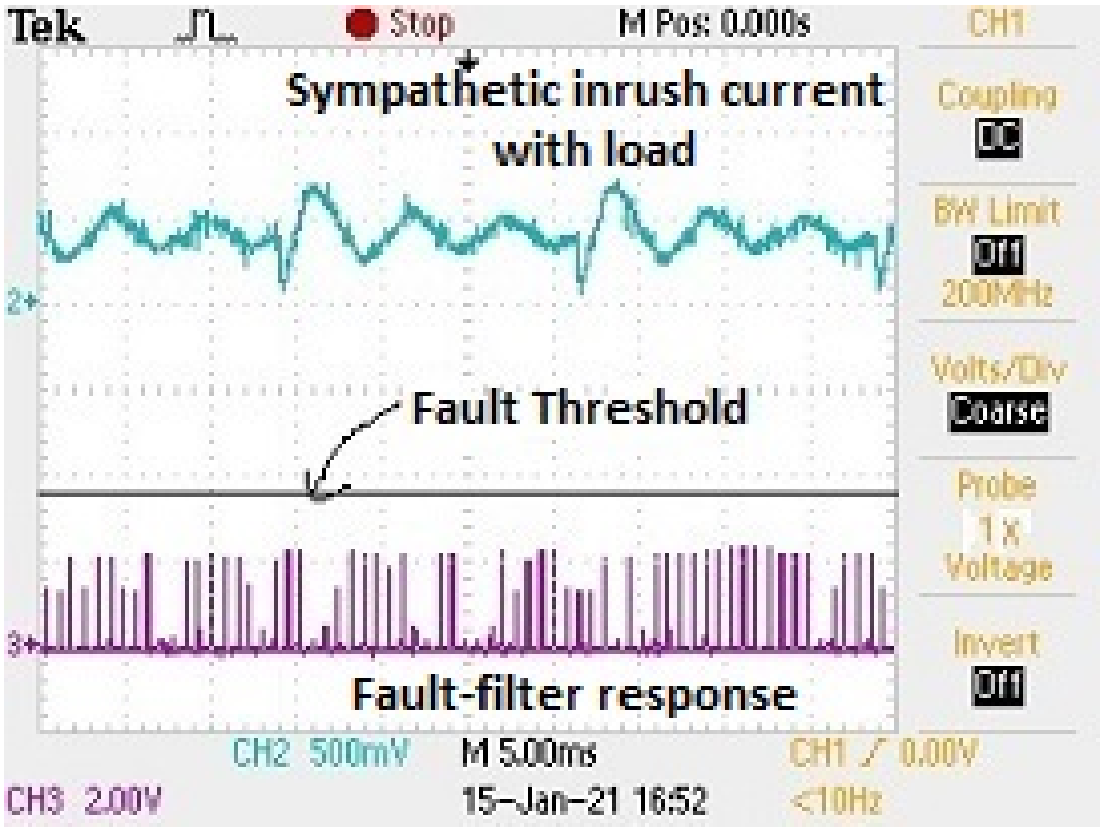

Figure 4.39: (CH2) Sympathetic inrush current with load. (CH3) Response of fault-filter indicating no-fault.

studied.

Fig. 4.56(CH-3) shows the response of inrush-filter for inter-turn fault (80% of the winding) waveform of Fig. 4.56(CH-2).It is observed that the inrush-filter do not detect any inrush in the waveform. However, the fault-filter in its response, shown in Fig. 4.57, correctly detects the presence of fault for the waveform in Fig. 4.57(CH-2).

The response of the inrush-filter and fault-filter for inter-turn fault involving 50% of the secondary turns, are depicted in Fig. 4.58(CH-3) and Fig. 4.59(CH-3) respectively. It is evident from Fig. 4.58(CH-3) that the response of inrush-filter shows no-inrush whereas the response of fault-filter depicted in Fig. 4.59(CH-3), correctly detects the presence of fault-condition.

4.8 Summary

The main contribution of this chapter is development of hardware set-up of the proposed method for differential protection scheme. The process of developing inrush- and fault-

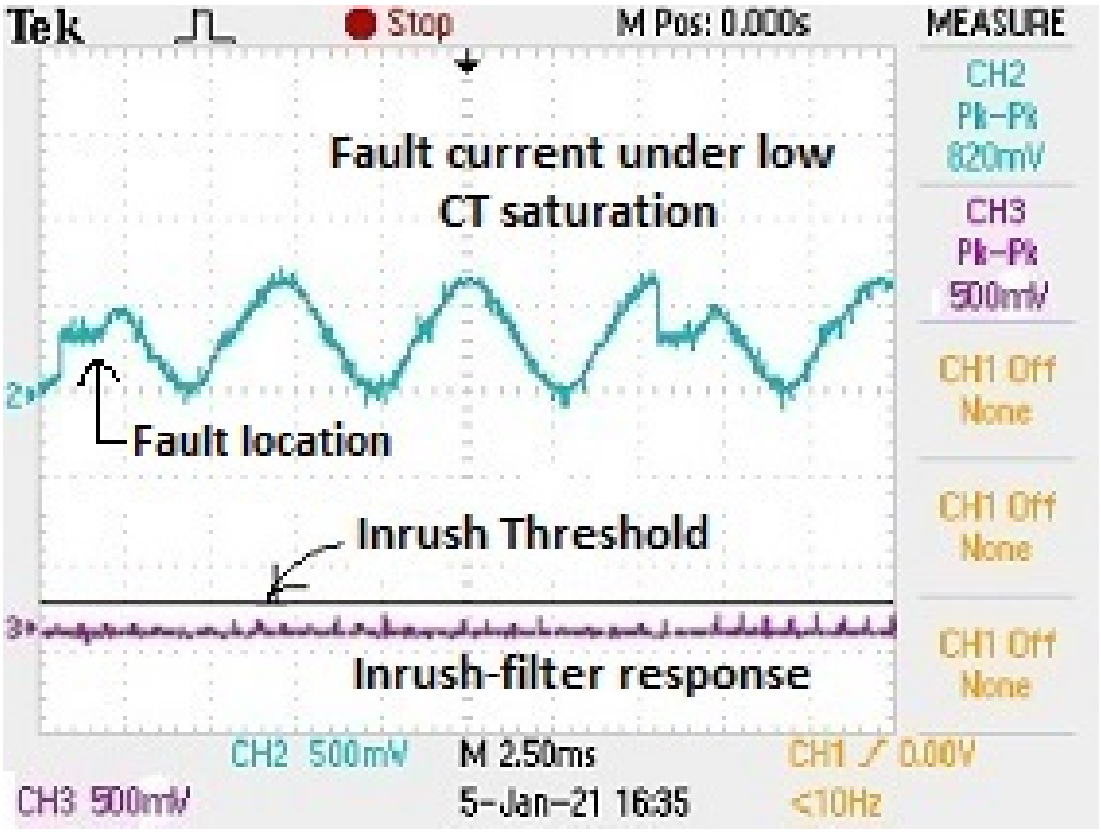

Figure 4.40: (CH2) Fault (L-G fault) current under low CT saturation. (CH3) Response of inrush-filter indicating no-inrush.

filter in hardware simulation mode on System Generator Software is discussed. The tested hardware simulation is then implemented on a FPGA board. The inrush- and fault-filter implemented in the FPGA board is tested for real-time performance on recorded waveforms obtained from PSCAD simulations. Later, the performance of the inrush- and fault-filter are tested on waveform from a physical transformer testing the performance of the hardware filters in real-time mode.

This chapter establishes that the proposed matched wavelet filters can be implemented successfully using existing technologies.

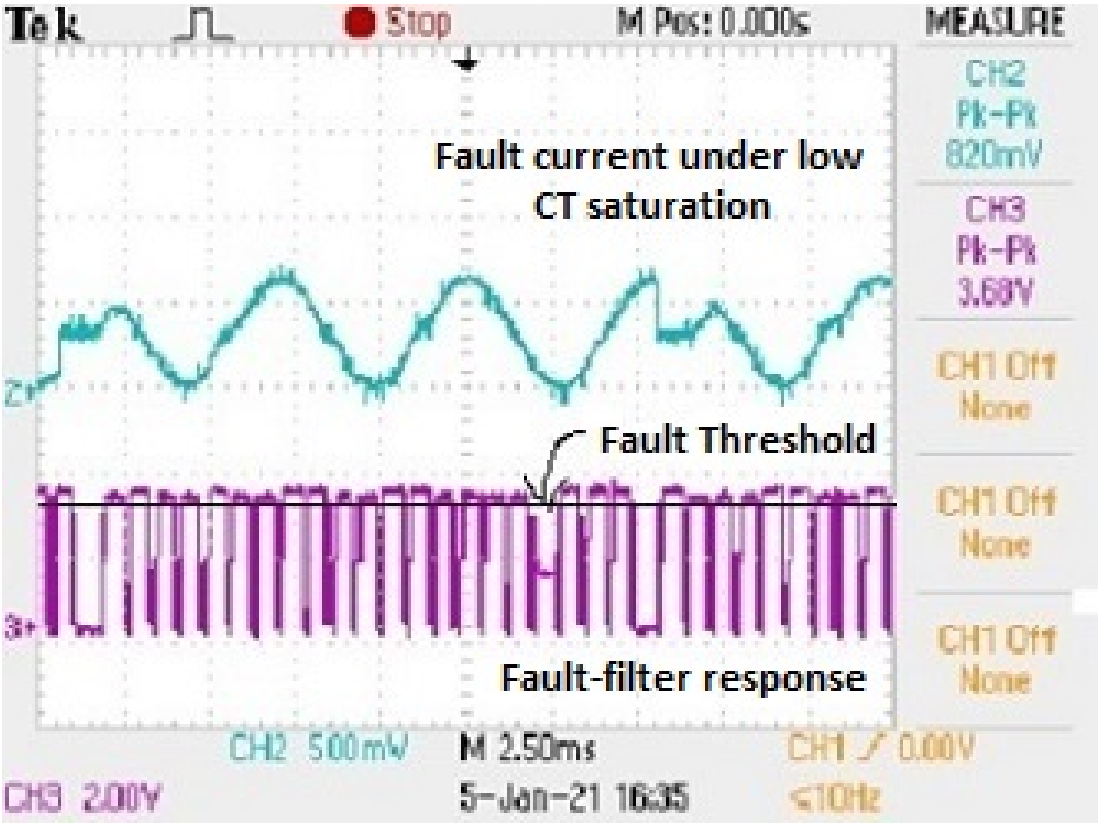

Figure 4.41: (CH2) Fault (L-G fault) current under low CT saturation. (CH3) Response of fault-filter indicating fault.

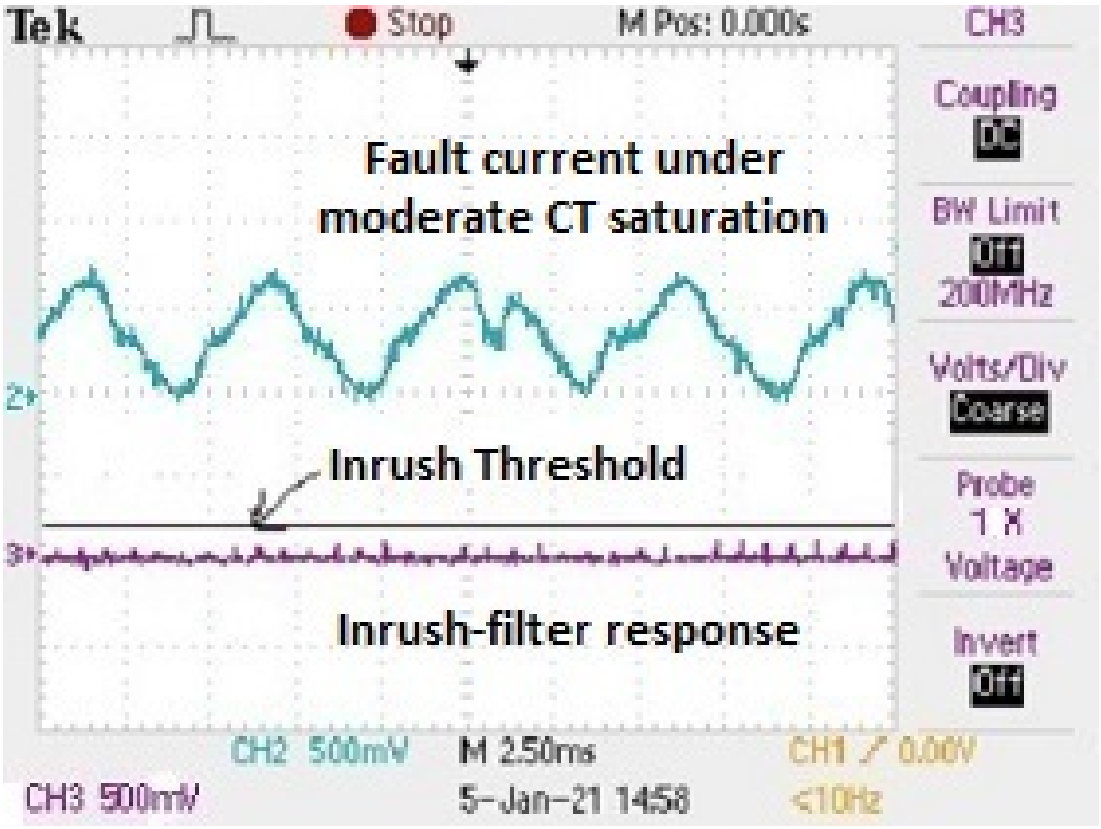

Figure 4.42: (CH2) Fault (L-G fault) current under moderate CT saturation. (CH3) Response of inrush-filter indicating no-inrush.

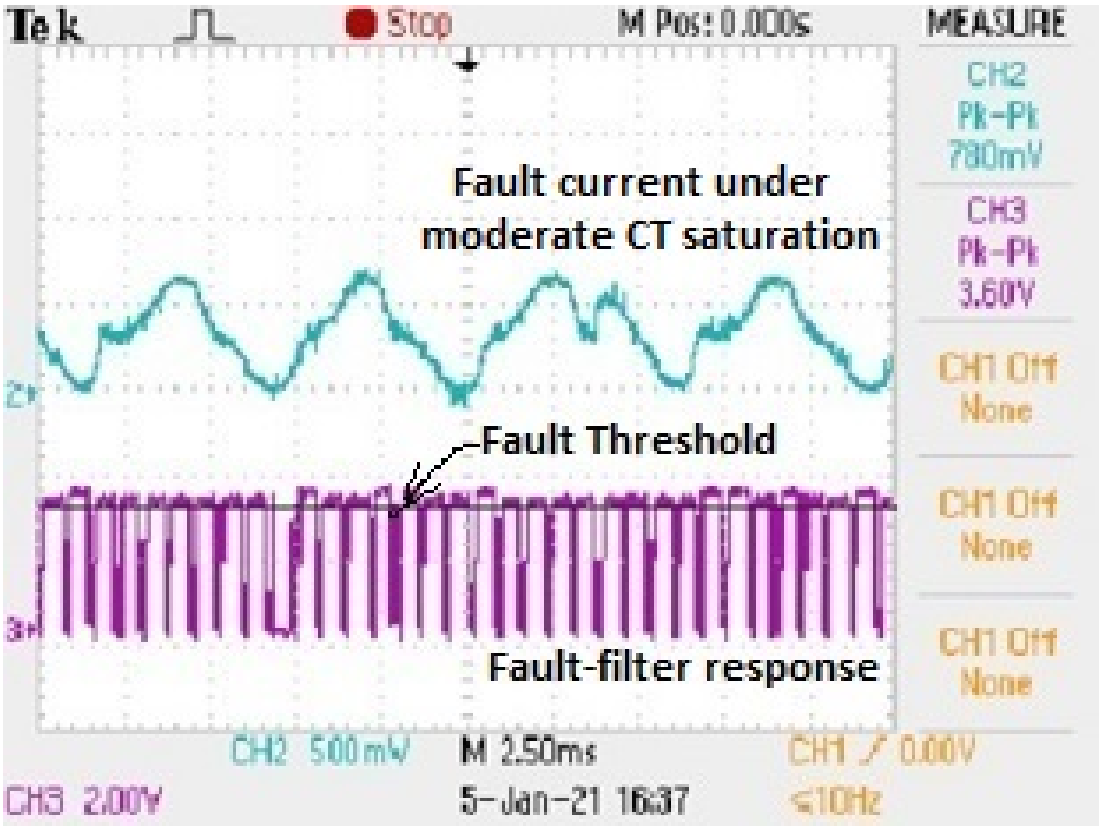

Figure 4.43: (CH2) Fault (L-G fault) current under moderate CT saturation. (CH3) Response of fault-filter indicating fault.

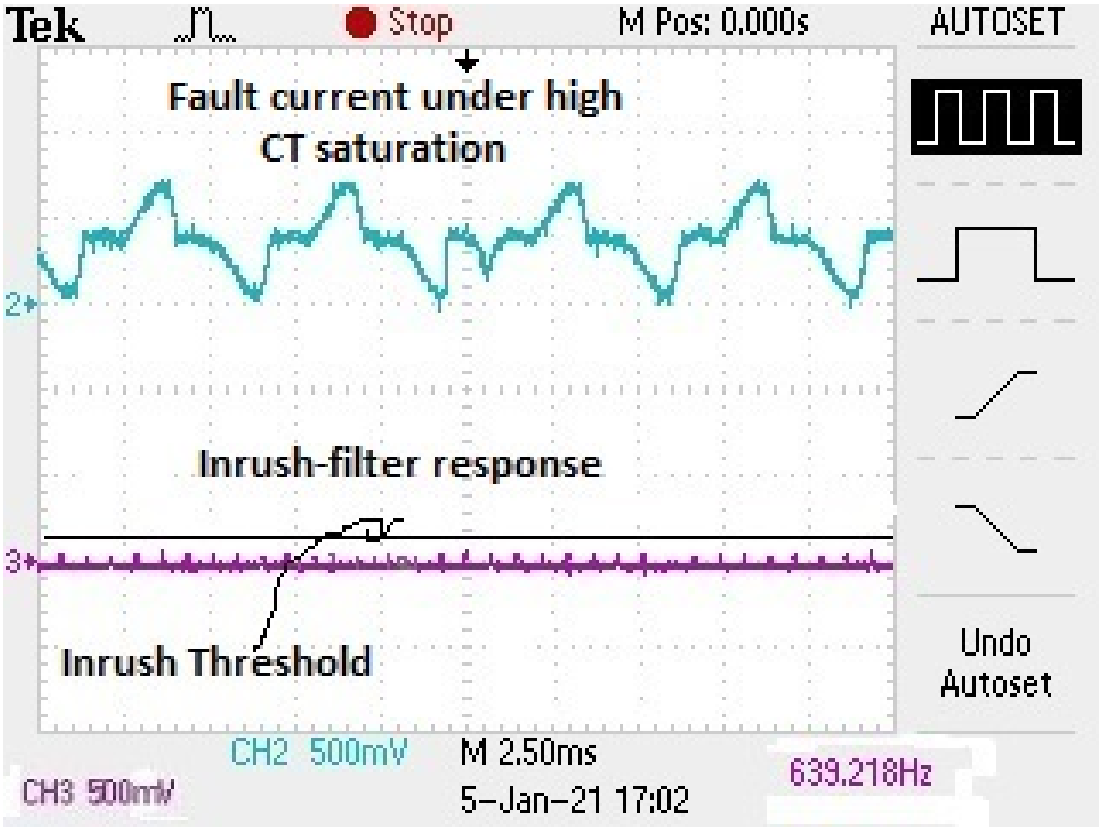

Figure 4.44: (CH2) Fault (L-G fault) current under high CT saturation. (CH3) Response of inrush-filter indicating no-inrush.

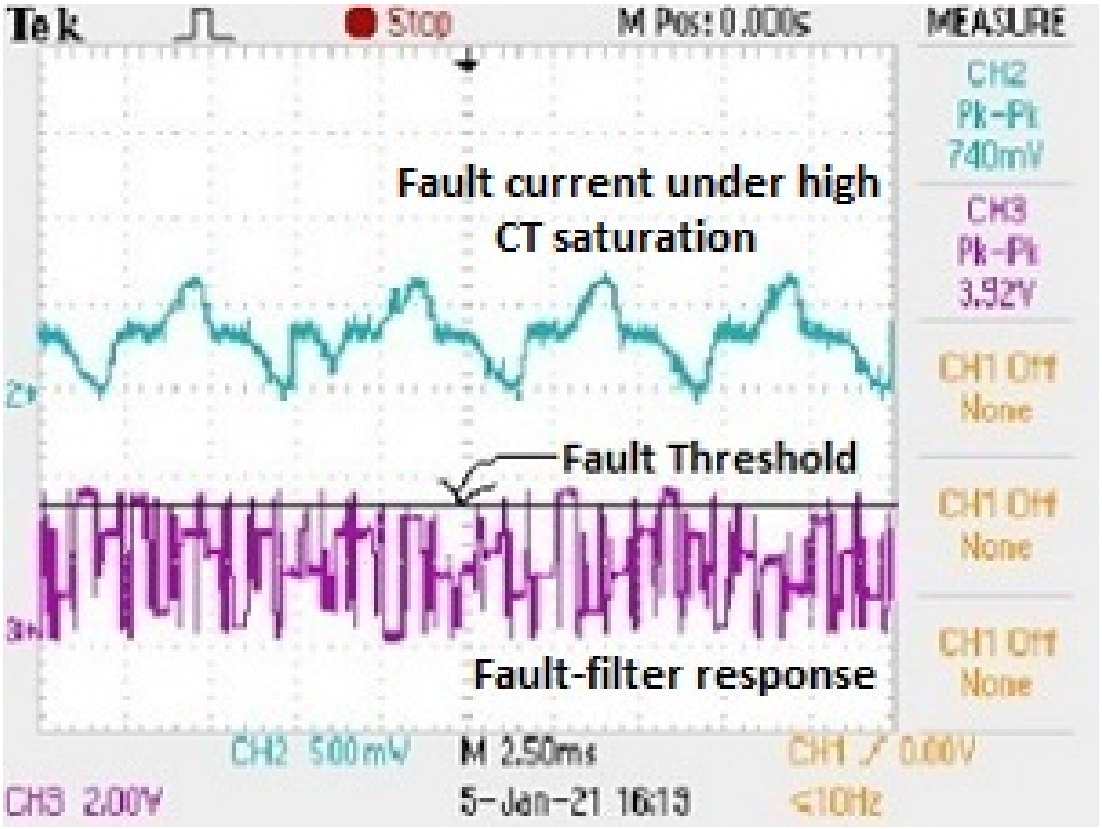

Figure 4.45: (CH2) Fault (L-G fault) current under high CT saturation. (CH3) Response of fault-filter indicating fault.

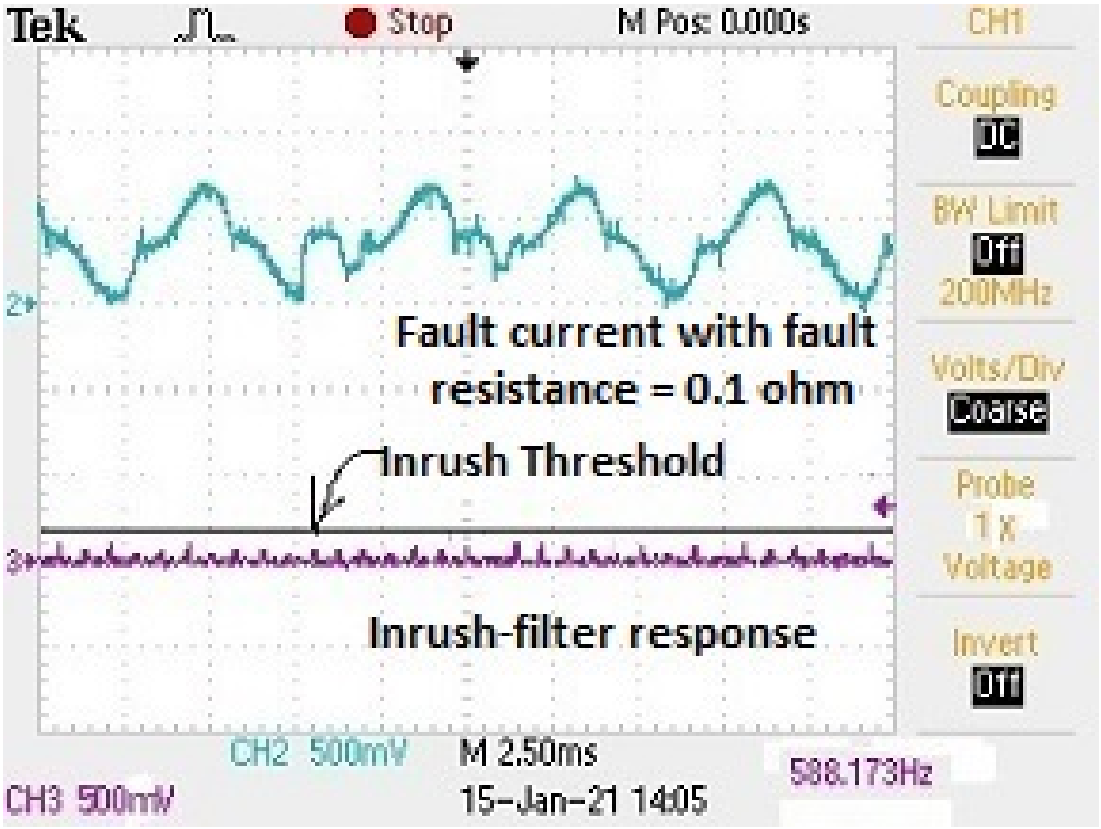

Figure 4.46: (CH2) Fault (L-G fault) current with fault resistance = $0.1 ohm$. (CH3) Response of inrush-filter indicating no-inrush.

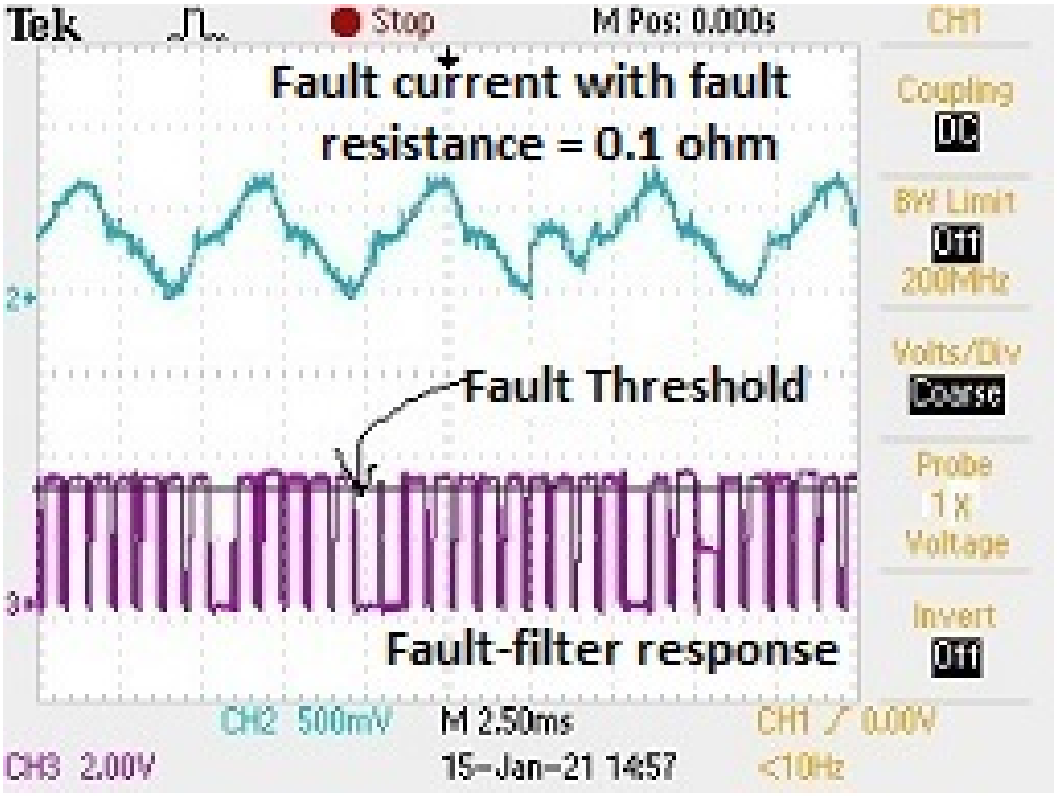

Figure 4.47: (CH2) Fault (L-G fault) current with fault resistance = $0.1 ohm$. (CH3) Response of fault-filter indicating fault.

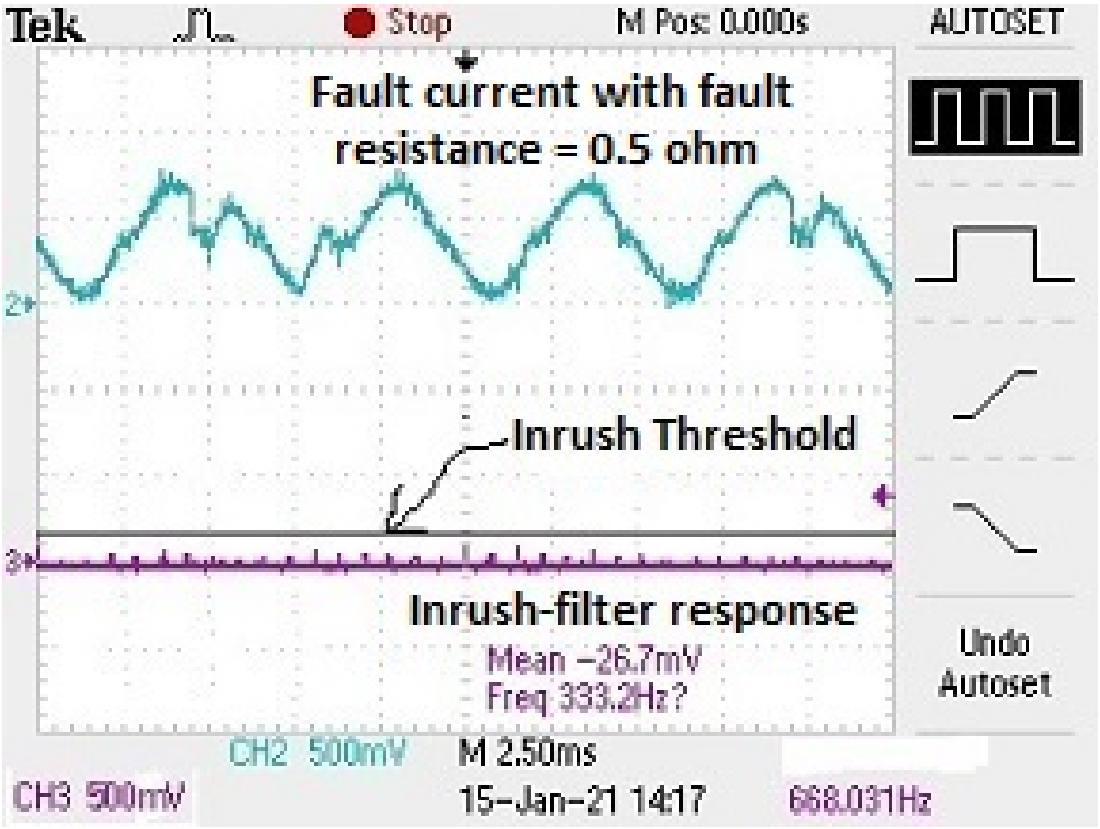

Figure 4.48: (CH2) Fault (L-G fault) current with fault resistance = $0.5 ohm$. (CH3) Response of inrush-filter indicating no-inrush.

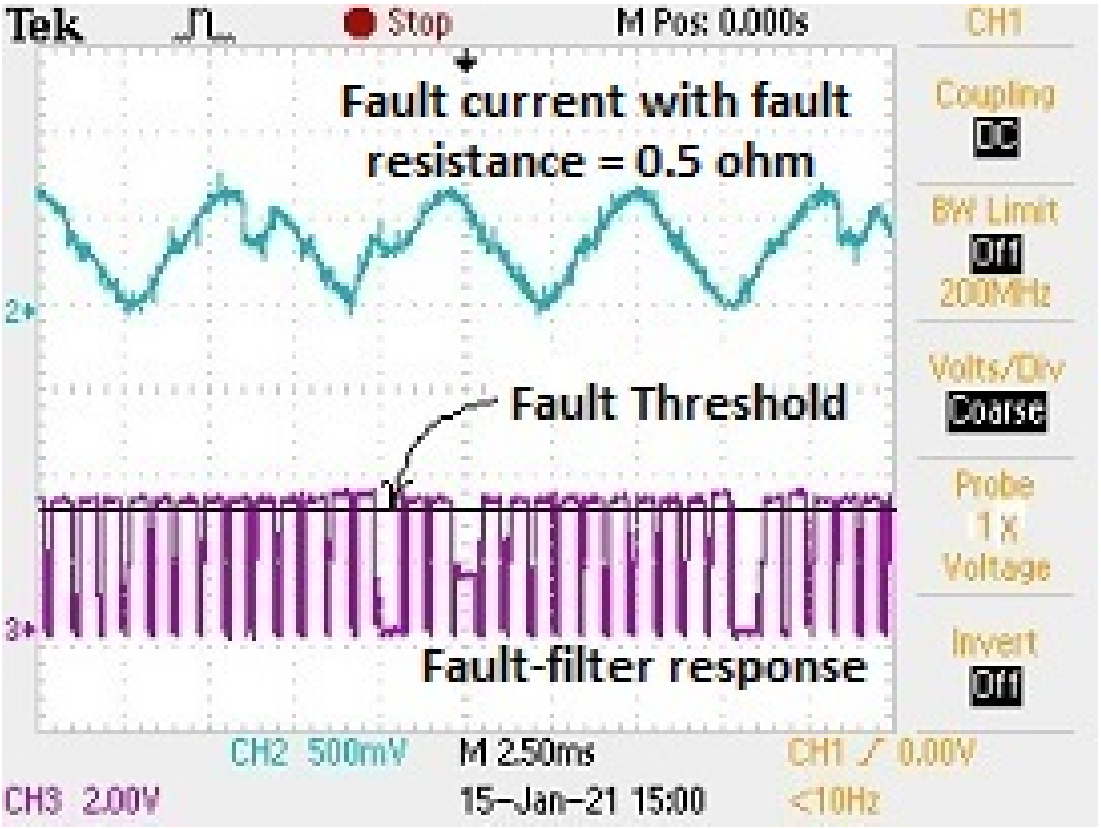

Figure 4.49: (CH2) Fault (L-G fault) current with fault resistance = $0.5 ohm$. (CH3) Response of fault-filter indicating fault.

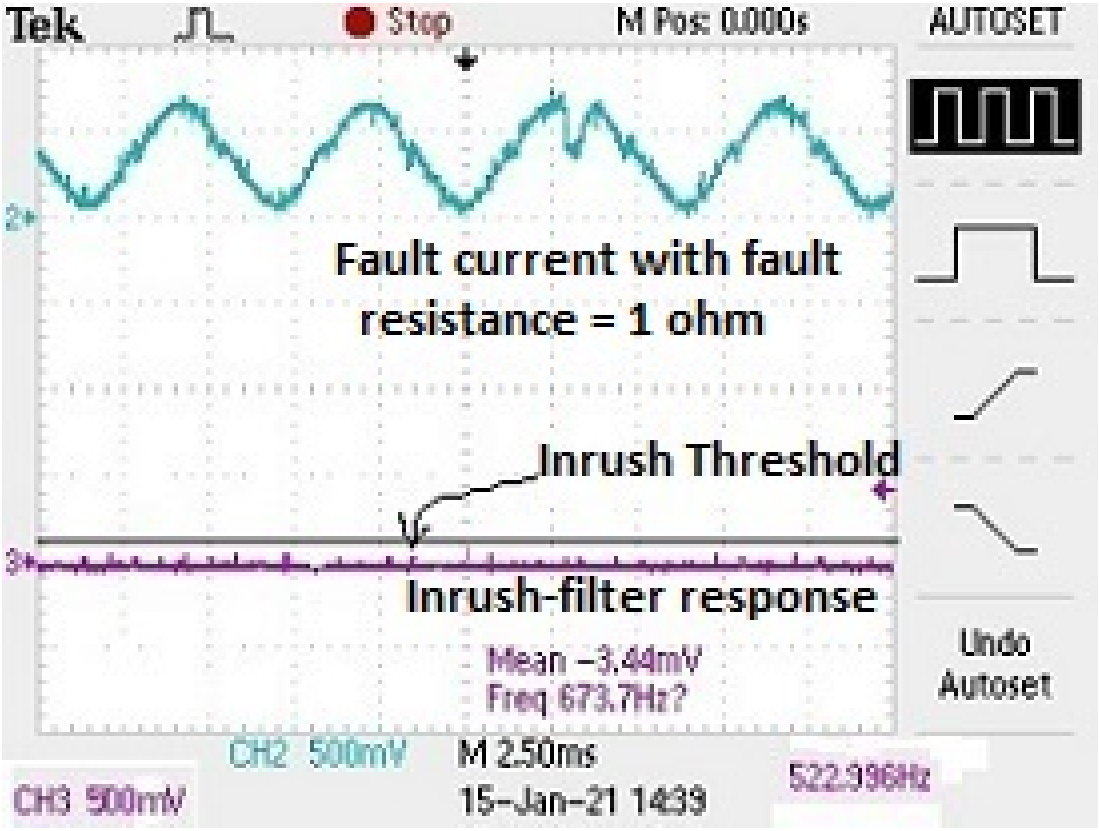

Figure 4.50: (CH2) Fault (L-G fault) current with fault resistance = $1 ohm$. (CH3) Response of inrush-filter indicating no-inrush.

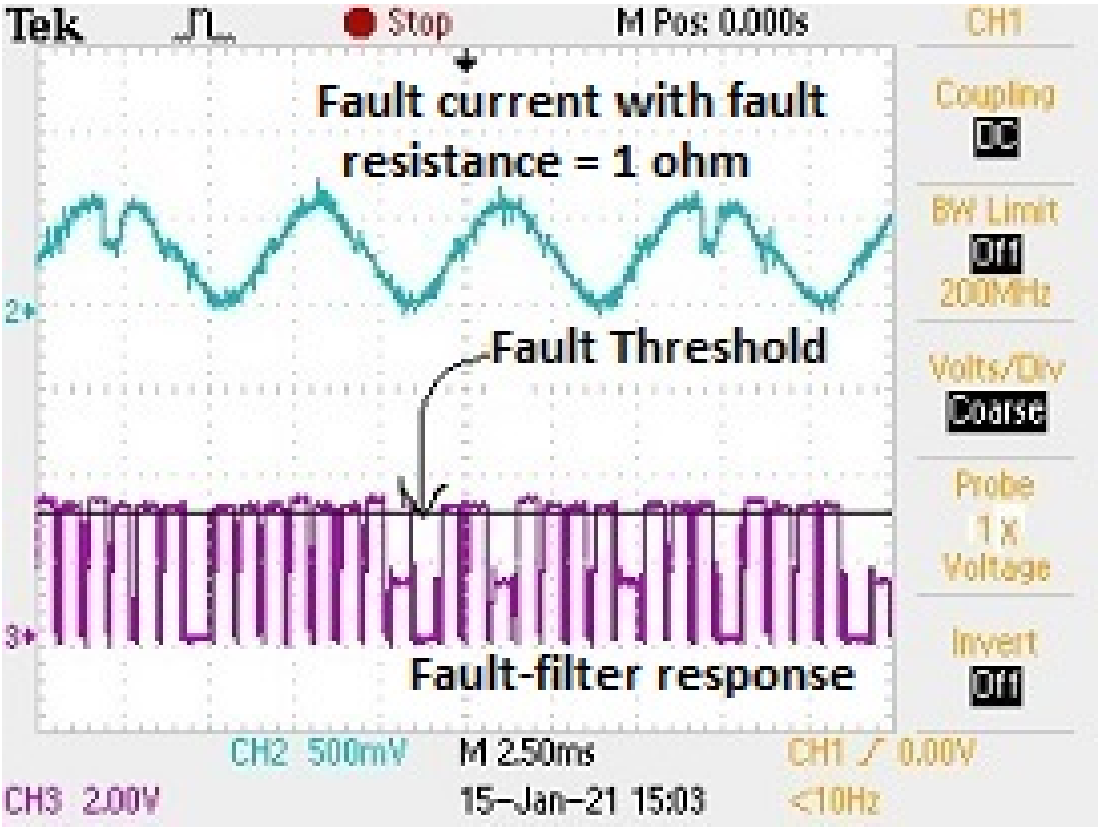

Figure 4.51: (CH2) Fault (L-G fault) current with fault resistance = $1 ohm$. (CH3) Response of fault-filter indicating fault.

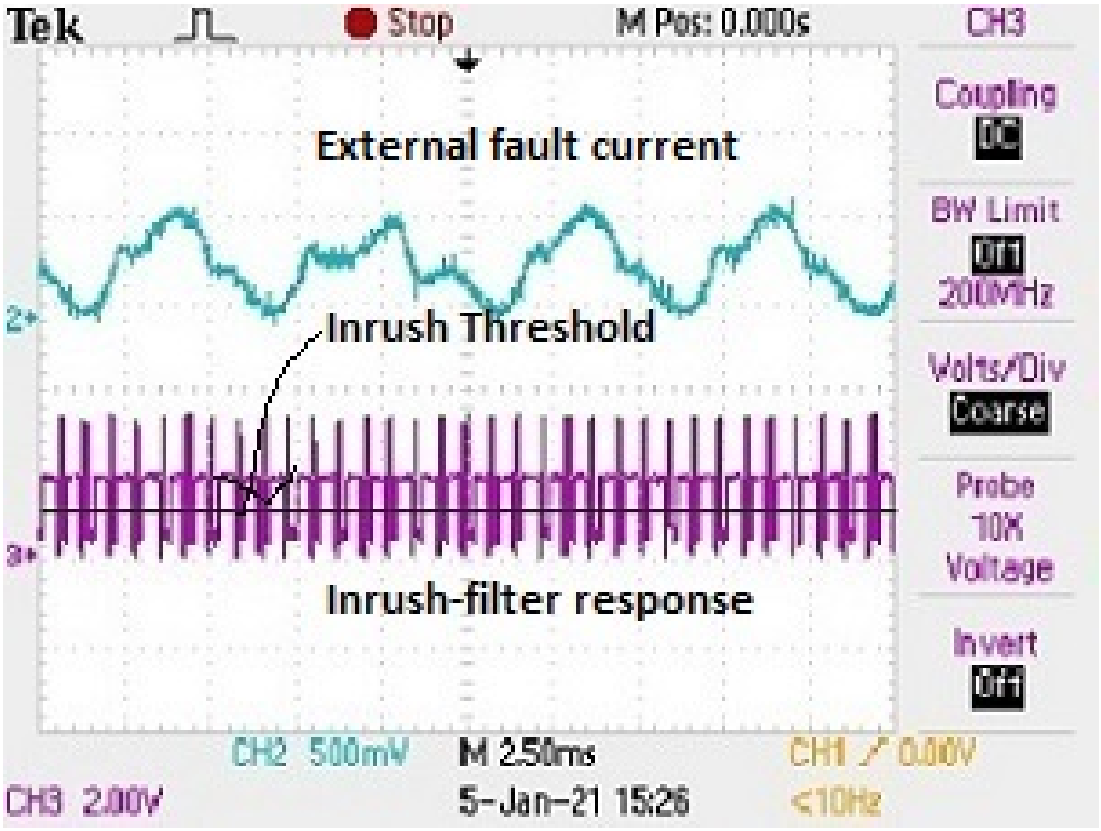

Figure 4.52: (CH2) External fault (L-G fault) current. (CH3) Response of inrush-filter indicating inrush.

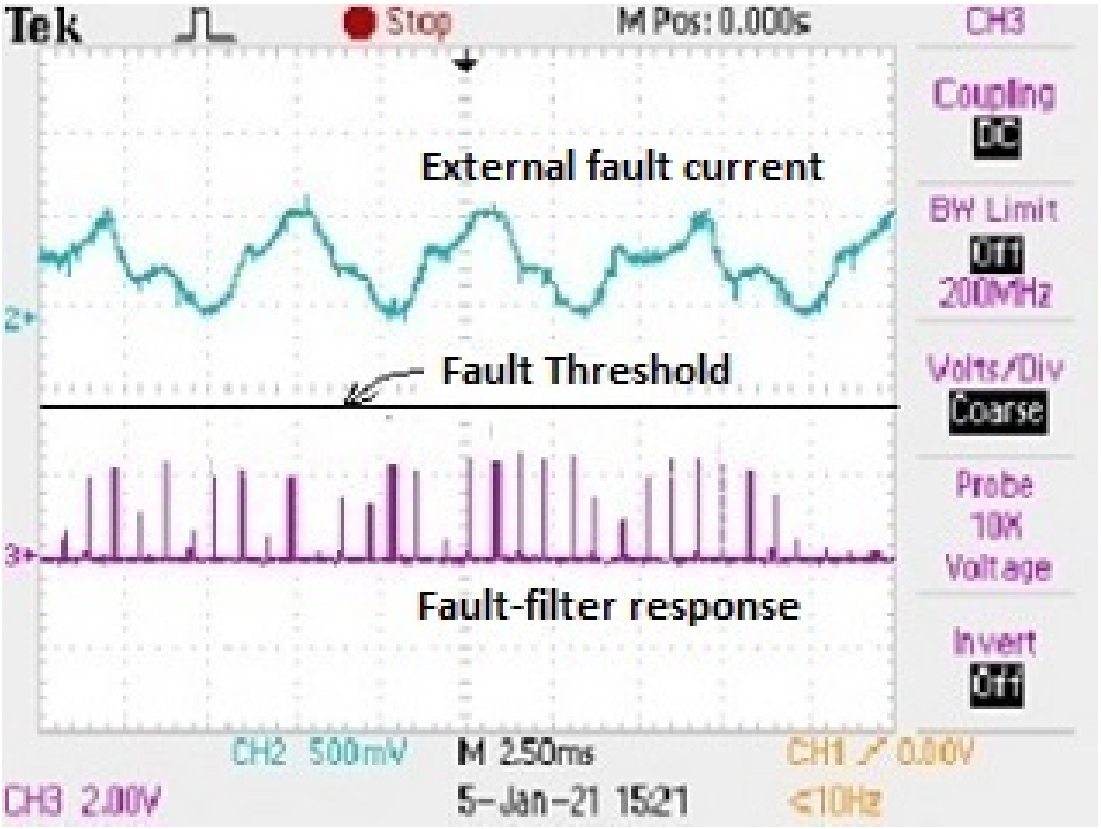

Figure 4.53: (CH2) External fault (L-G fault) current. (CH3) Response of fault-filter indicating no-fault.

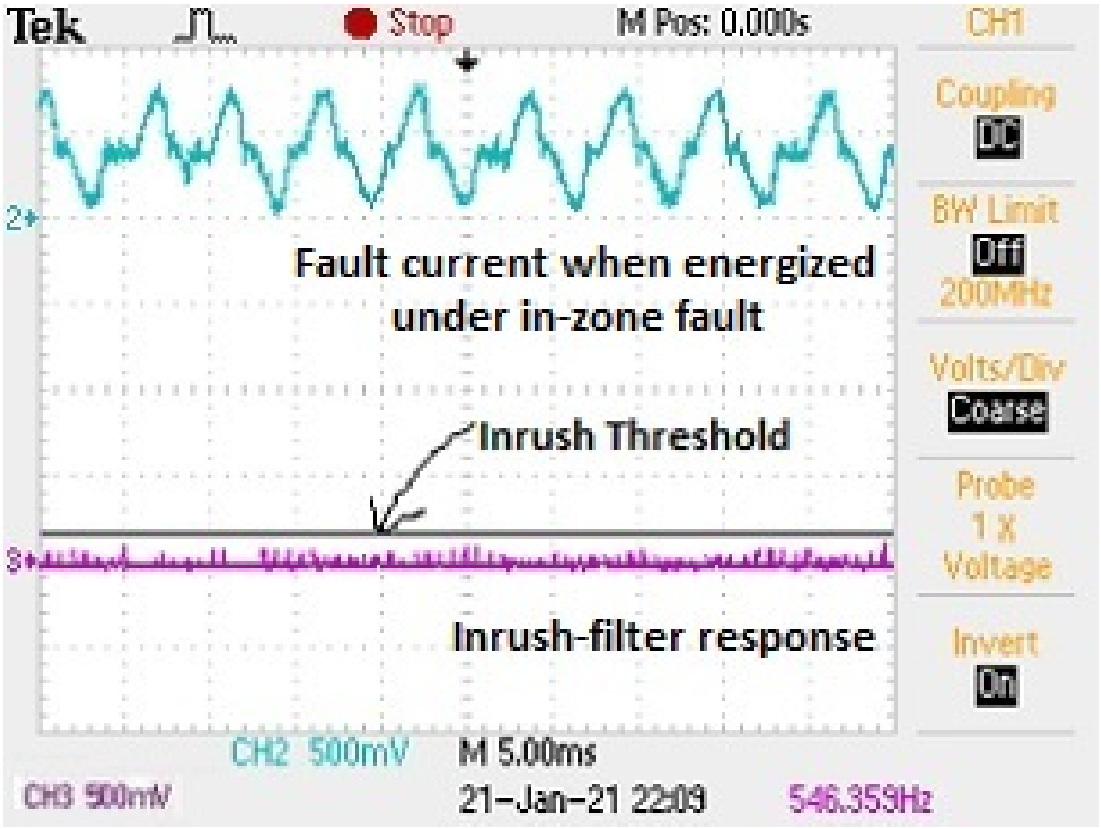

Figure 4.54: (CH2) Transformer fault current when energized under in-zone fault (L-G fault). (CH3) Response of inrush-filter indicating no-inrush.

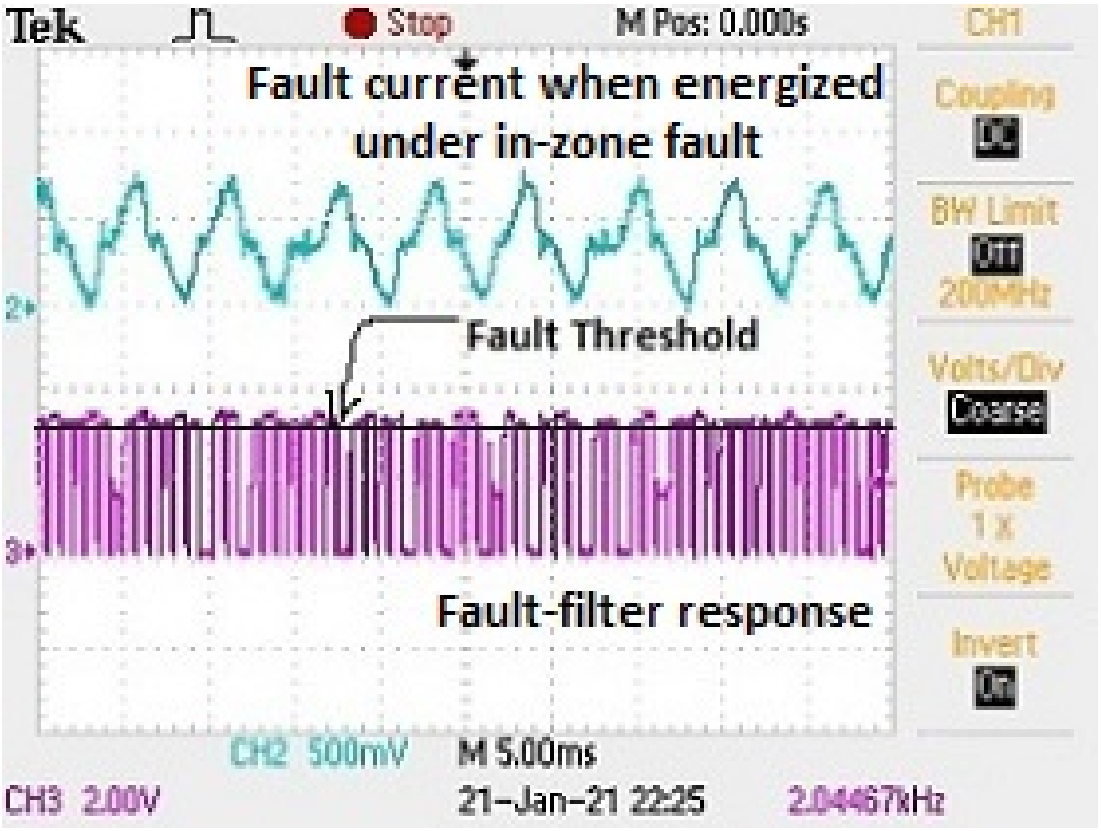

Figure 4.55: (CH2) Transformer fault current when energized under in-zone fault (L-G fault). (CH3) Response of fault-filter indicating fault.

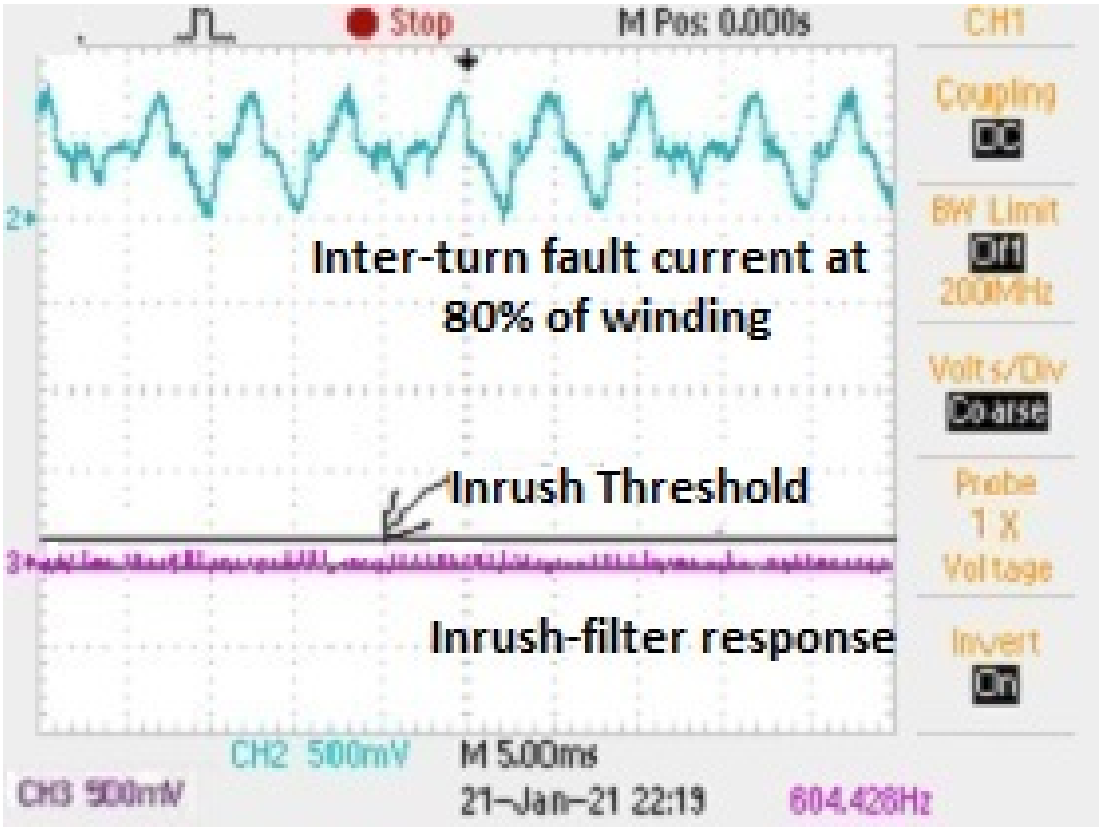

Figure 4.56: (CH2) Inter-turn fault current at 80% of winding. (CH3) Response of inrush-filter indicating no-inrush.

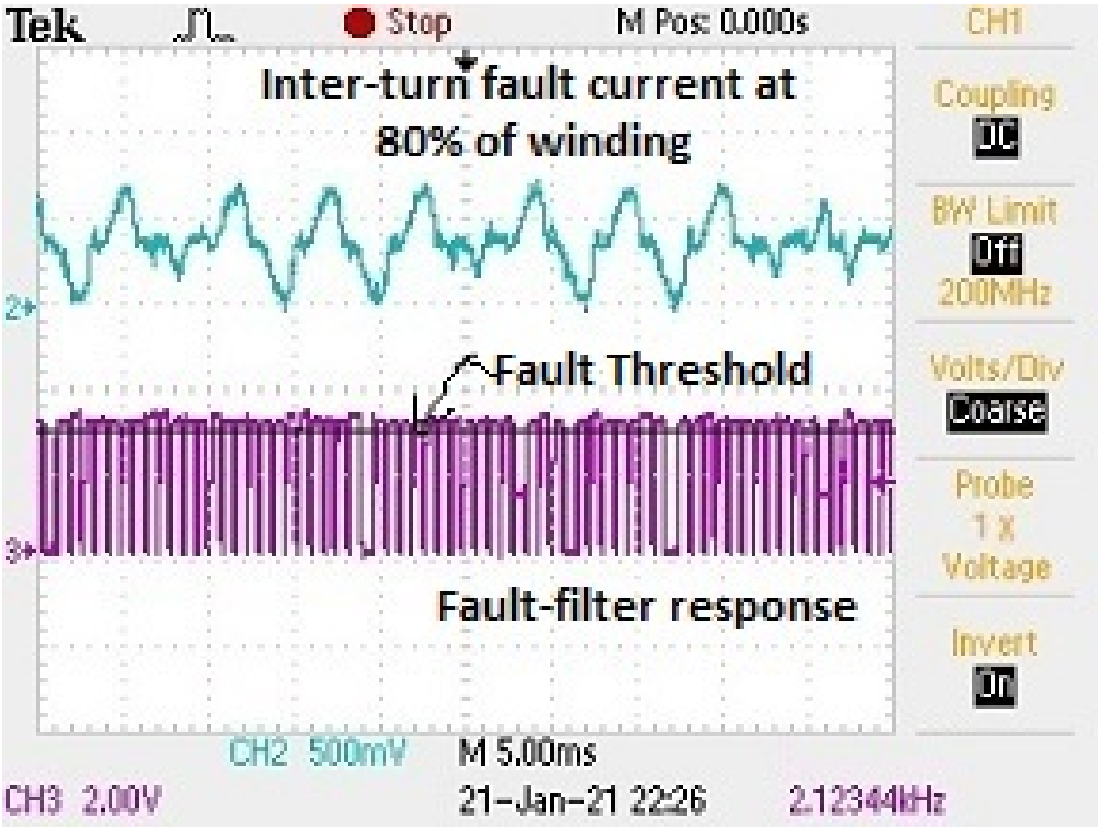

Figure 4.57: (CH2) Inter-turn fault current at 80% of winding. (CH3) Response of fault-filter indicating fault.

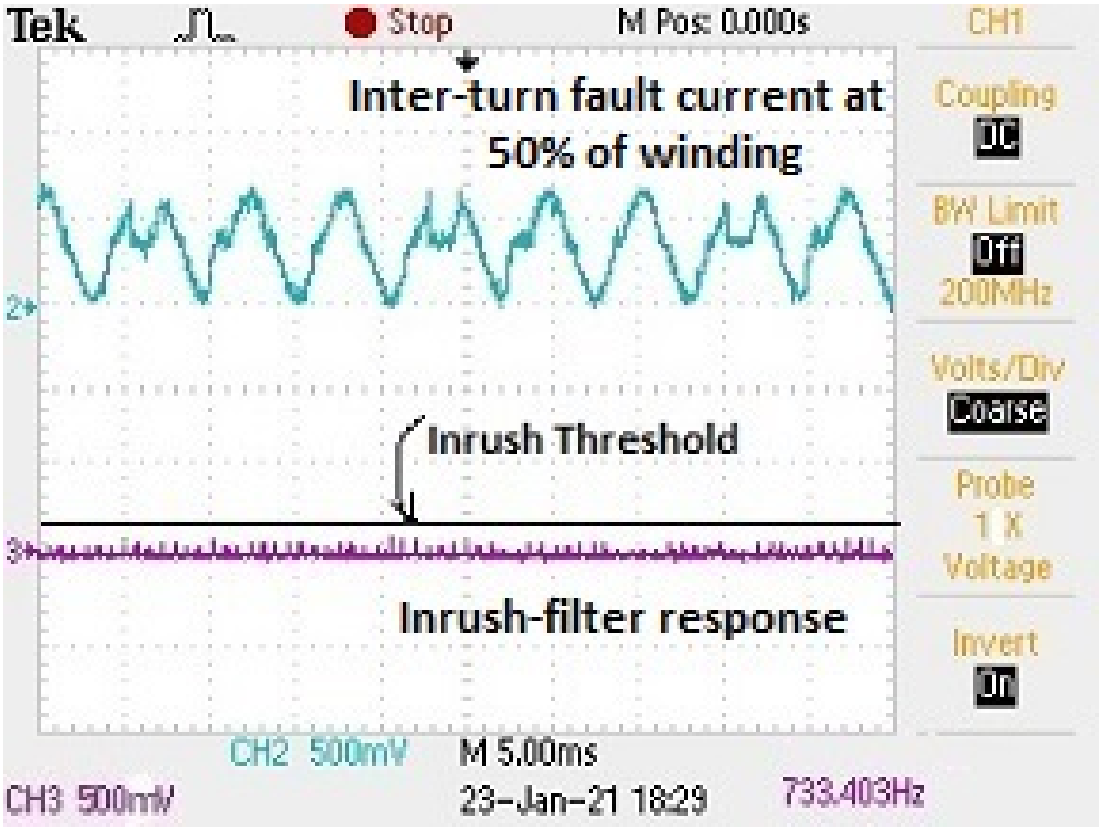

Figure 4.58: (CH2) Inter-turn fault current at 50% of winding. (CH3) Response of inrush-filter indicating no-inrush.

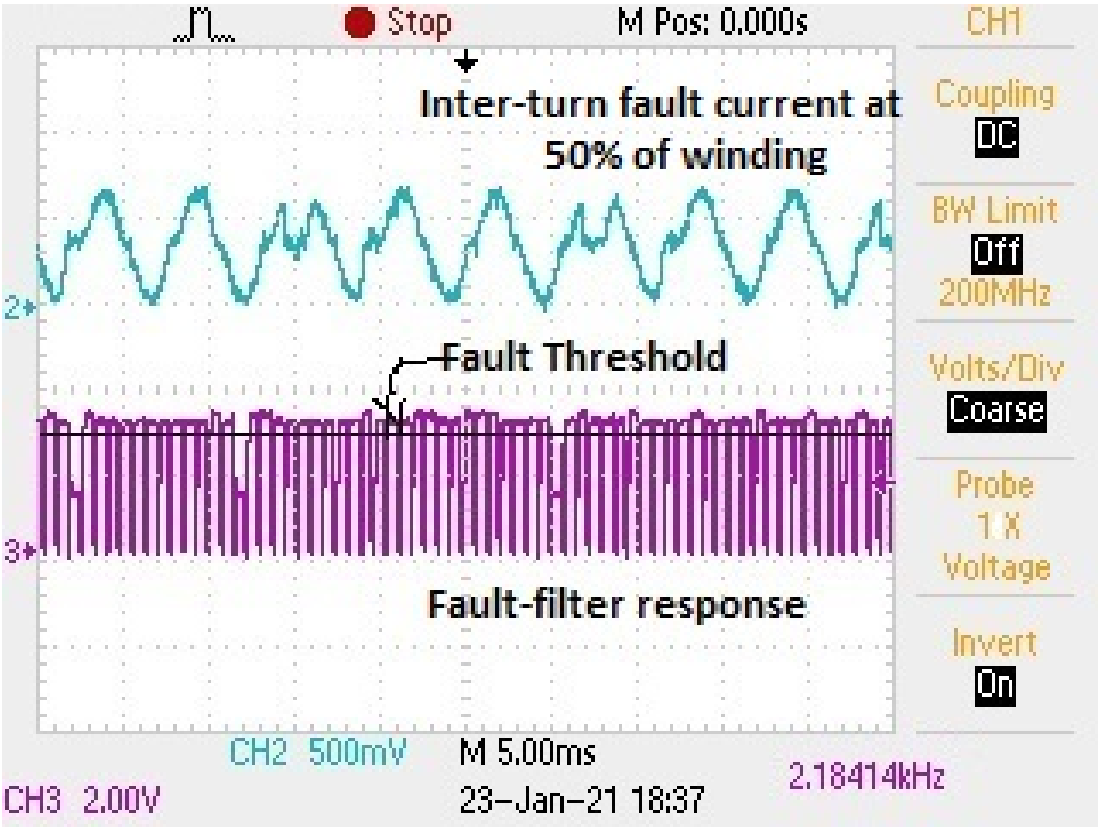

Figure 4.59: (CH2) Inter-turn fault current at 50% of winding. (CH3) Response of fault-filter indicating fault.