CHAPTER 4

Single-Phase Switched LC Z-Source Inverters

4.1 Introduction

Chapters 2 and 3 present high gain DC-DC converters (TSHGC and HGIBC) to operate as front-end DC-DC converters for two-stage power conversion. The two DC-DC converters have high voltage gain with reduced elements and continuous input current. However, the two-stage power conversion occupies more space and is less reliable due to the use of conventional DC-AC converters as discussed in chapter 1. To take care of these issues, this chapter presents two single-phase switched LC Z-source inverters (SLC-ZSIs), Type 1 SLC-ZSI and Type 2 SLC-ZSI [114]. The Type 2 SLC-ZSI is an improved version of Type 1 SLC-ZSI. The two SLC-ZSIs can be used as single-stage power conversion (DC-AC) for AC loads/grid operated by low voltage DC sources. Two control variables D_{st} and M operate the two SLC-ZSIs similar to the conventional single-phase ZSI. The operation of two SLC-ZSIs is explained based on a modified unipolar sinusoidal pulse width modulation (SPWM) technique. As the two SLC-ZSIs are non-isolated and based on SL cells, some reported non-isolated high gain SL based ZSIs are considered for comparison. The performance of two SLC-ZSIs is verified through simulation and experimental studies. The salient features of two SLC-ZSIs are as follows.

- They have high voltage gain at low values of D_{st} with reduced elements.
- As they operate at low values of D_{st}, M can be increased which leads to inversion at reduced harmonic distortion.
- As they have a lesser number of elements, the overall volume of system is reduced which results in better power density as compared to reported SL based ZSIs.
- Moreover, they can be modified to operate as a DC-DC converter as per the requirement of a particular application.

4.2 Proposed Single-Phase Type 1 SLC-ZSI

Fig. 4.1 shows a single-phase Type 1 SLC-ZSI. As shown in Fig. 4.1, it has one SL cell, two switches (S_a and S_b), one diode (D_{in}) and one capacitor (C) along with an HB circuit ($S_1 - S_4$). The Type 1 SLC-ZSI has continuous input current with slightly more ripple due to the presence of SL cell at the input side. Further, it can limit start-up inrush current. It has a common ground between the input DC source and HB circuit. For easy analysis of Type 1 SLC-ZSI, the HB circuit is replaced by a parallel combination of a single switch (S_{inv}) and equivalent resistance (R_{eq}) as shown in Fig. 4.2. The operation of Type 1 SLC-ZSI is explained based on switching state of S_{inv}; when S_{inv} is ON, it is in shoot-through operation and when S_{inv} is OFF, it is in non-shoot-through operation. The shoot-through operation gives the shoot-through state (STS) for boosting the input DC voltage and the non-shoot-through operation gives power state (PS) and zero state (ZS) for AC output.

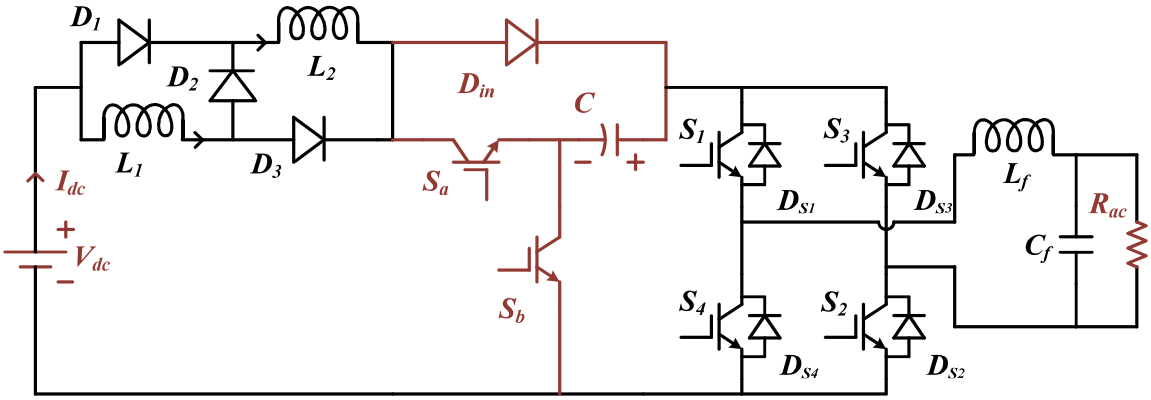


Fig. 4.1. A single-phase Type 1 SLC-ZSI.

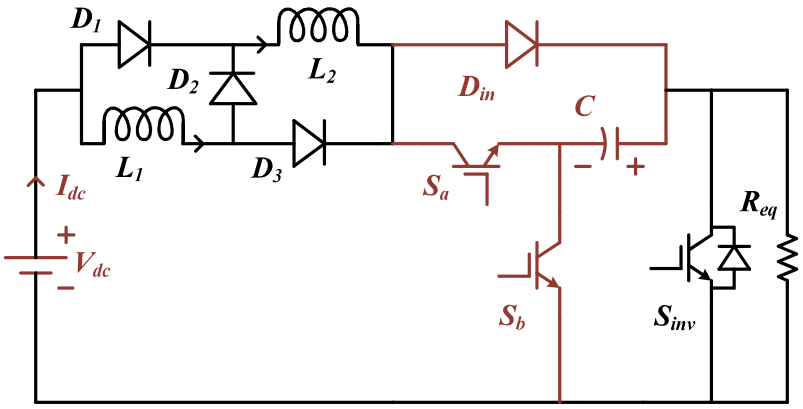


Fig. 4.2. Simplified circuit of Type 1 SLC-ZSI for analysing its operation.

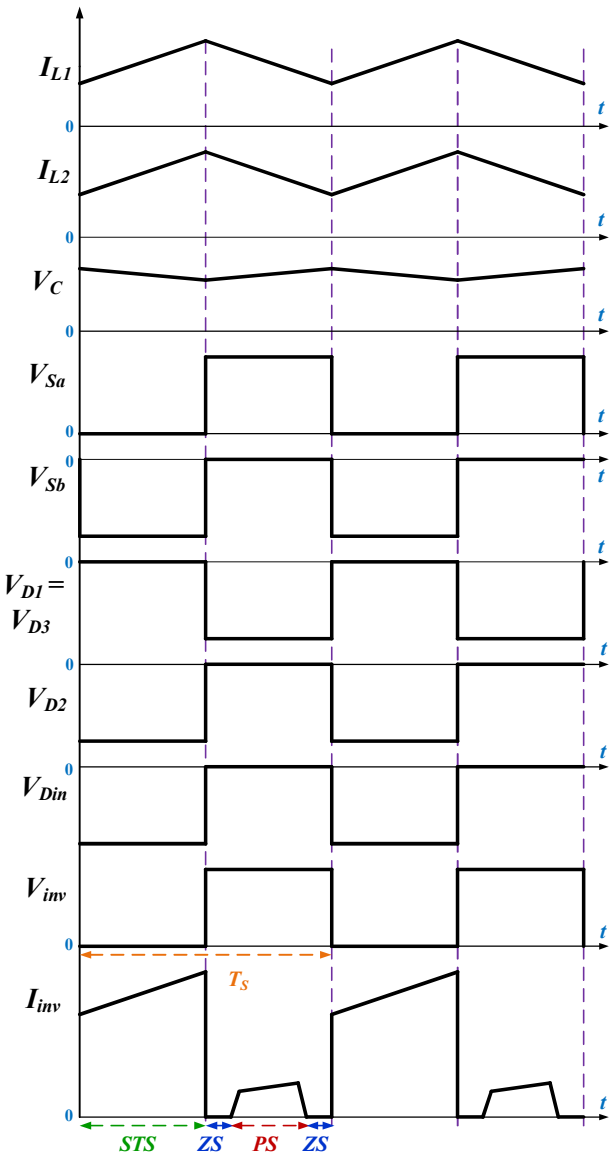


Fig. 4.3. Operating waveforms of Type 1 SLC-ZSI.

4.2.1 Operation of Type 1 SLC-ZSI

The operating waveforms of Type 1 SLC-ZSI are shown in Fig. 4.3. As shown in Fig. 4.3, the Type 1 SLC-ZSI has three operating states; shoot-through, zero and power states. The STS exists due to turn-on of switches (either S_1 and S_4 or S_2 and S_3) at the same instant. Due to STS, the input voltage (V_{dc}) is boosted to higher voltages and appear as equivalent input voltage (V_{inv}) across the HB circuit of Type 1 SLC-ZSI during PS and ZS.

(a) Shoot-Through Operation of Type 1 SLC-ZSI

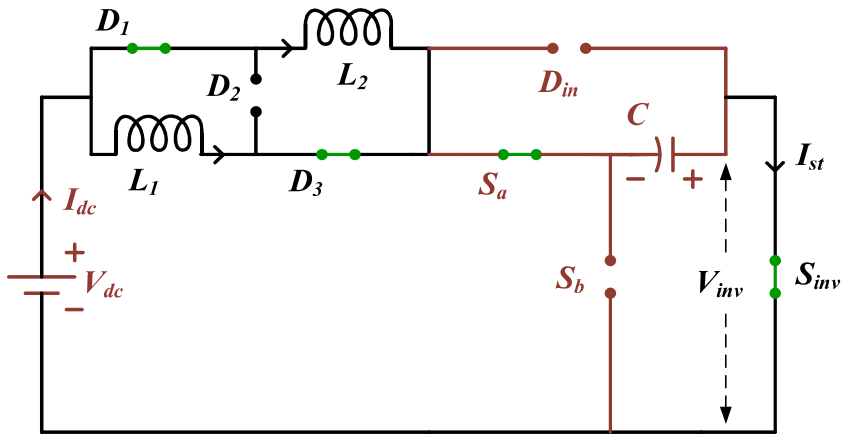
The equivalent circuit of Type 1 SLC-ZSI during shoot-through operation is shown in Fig. 4.4(a). In this shoot-through operation, switches (S_{inv} and S_a) are turned-on and S_b is turned-off. Meanwhile diodes (D_1 and D_3) are forward biased and diodes (D_2 and D_{in}) are reverse biased. The stored energy in C starts discharging. The inductors (L_1 and L_2) parallelly store energy from V_{DC} and C through S and S_a. From Fig. 4.4(a) corresponding KCL and KVL expressions are given in (4.1).

$$\left.\begin{array}{c} v_{L1} = L_1 \frac{di_{L1}}{dt} = v_{dc} + v_C \\ v_{L2} = L_2 \frac{di_{L2}}{dt} = v_{dc} + v_C \\ C\frac{dv_C}{dt} = i_C = -(i_{L1} + i_{L2}) \\ v_{inv} = 0 \\ i_{st} = i_{L1} + i_{L2} \end{array}\right\} \tag{4.1}$$

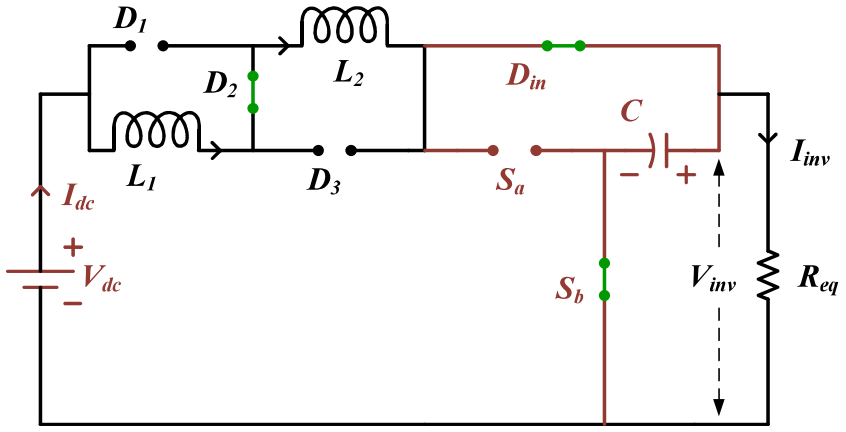
(b) Non-Shoot-Through Operation of Type 1 SLC-ZSI

The equivalent circuit of Type 1 SLC-ZSI during non-shoot-through operation is shown in Fig. 4.4(b). In this non-shoot-through operation, S_{inv} and S_a are turned-off and S_b is turned-on. Meanwhile D_1 and D_3 are reverse biased, and D_2 and D_{in} are forward biased. During this operation, L_1 and L_2 are connected in series and start discharging their stored energy, whereas C is still in charging state. Also, the combined energy of DC source and stored magnetic energy appears across the HB circuit. From Fig. 4.4(b) corresponding KCL and KVL expressions are given in (4.2).

$$\left.\begin{array}{c} v_{L1} + v_{L2} = L_1 \frac{di_{L1}}{dt} + L_2 \frac{di_{L2}}{dt} = v_{dc} - v_C \\ i_C = i_{L1} - i_{inv} \\ v_{inv} = v_C \end{array}\right\} \tag{4.2}$$



(a)



(b)

Fig. 4.4. Equivalent circuits of Type 1 SLC-ZSI **(a)** during shoot-through operation **(b)** during non-shoot-through operation.

4.2.2 Steady-State Analysis of Type 1 SLC-ZSI

After applying volt-second balance principle to L_1 and L_2 over T_s, the obtained steady-state voltage across C, V_C is given in (4.3).

$$V_C = \frac{1+D_{st}}{1-3D_{st}} V_{dc} \tag{4.3}$$

Similarly, after applying charge-second balance principle to C and assuming $v_{L1} = v_{L2} = v_L$, $i_{L1} = i_{L2} = i_L$, $L_1 = L_2 = L$, the obtained steady-state average inductor currents expression (I_{L1} and I_{L2}) is given in (4.4).

$$I_{L1} = I_{L2} = \frac{1-D_{st}}{1-3D_{st}} I_{inv} \tag{4.4}$$

The boosted equivalent DC voltage, V_{inv} appearing across the HB of Type 1 SLC-ZSI is same as that of V_C and the expression of V_{inv} is given in (4.5).

$$V_{inv} = \frac{1+D_{st}}{1-3D_{st}} V_{dc} = BV_{dc} \tag{4.5}$$

where B is boosting ability of Type 1 SLC-ZSI and defined as a ratio of V_{inv} and V_{dc}. The mathematical expression of B is given in (4.6).

$$B = \frac{V_{inv}}{V_{dc}} = \frac{1+D_{st}}{1-3D_{st}} \tag{4.6}$$

Further, the Type 1 SLC-ZSI is operated at the following condition.

$$D_{st} + M \leq 1 \tag{4.7}$$

The fundamental peak AC output voltage of single-phase Type 1 SLC-ZSI is given in (4.8).

$$V_{ac(pk)} = MV_{inv} = MBV_{dc} = GV_{dc} \tag{4.8}$$

where G is voltage gain of Type 1 SLC-ZSI and is defined as the ratio of $V_{ac(pk)}$ and V_{dc}. The mathematical expression of G is given in (4.9).

$$G = \frac{V_{ac(pk)}}{V_{dc}} = MB = \frac{M(1+D_{st})}{1-3D_{st}} \tag{4.9}$$

It can be determined from (4.6) and (4.7) that the Type 1 SLC-ZSI has maximum values of $D_{st} = 0.333$ and $M = 0.667$. The correlation among G, M and D_{st} of Type 1 SLC-ZSI is plotted and is shown in Fig. 4.5 based on the operating condition $D_{st} + M \leq 1$. Fig. 4.5(a) shows D_{st} versus M. It can be observed from Fig. 4.5(a) that D_{st} decreases, when M increases. Fig. 4.5(b) shows a 3-D surface plot representing the relationships among D_{st}, M and G. Figs. 4.5(c) and 4.5(d) show G versus D_{st} and G versus M respectively. It can be observed from Figs. 4.5(c) and 4.5(d) that G increases when D_{st} increases, and G decreases when M increases. Further, the derived topologies of Type 1 SLC-ZSI are discussed in section 4.3, appendix A and B of this thesis.

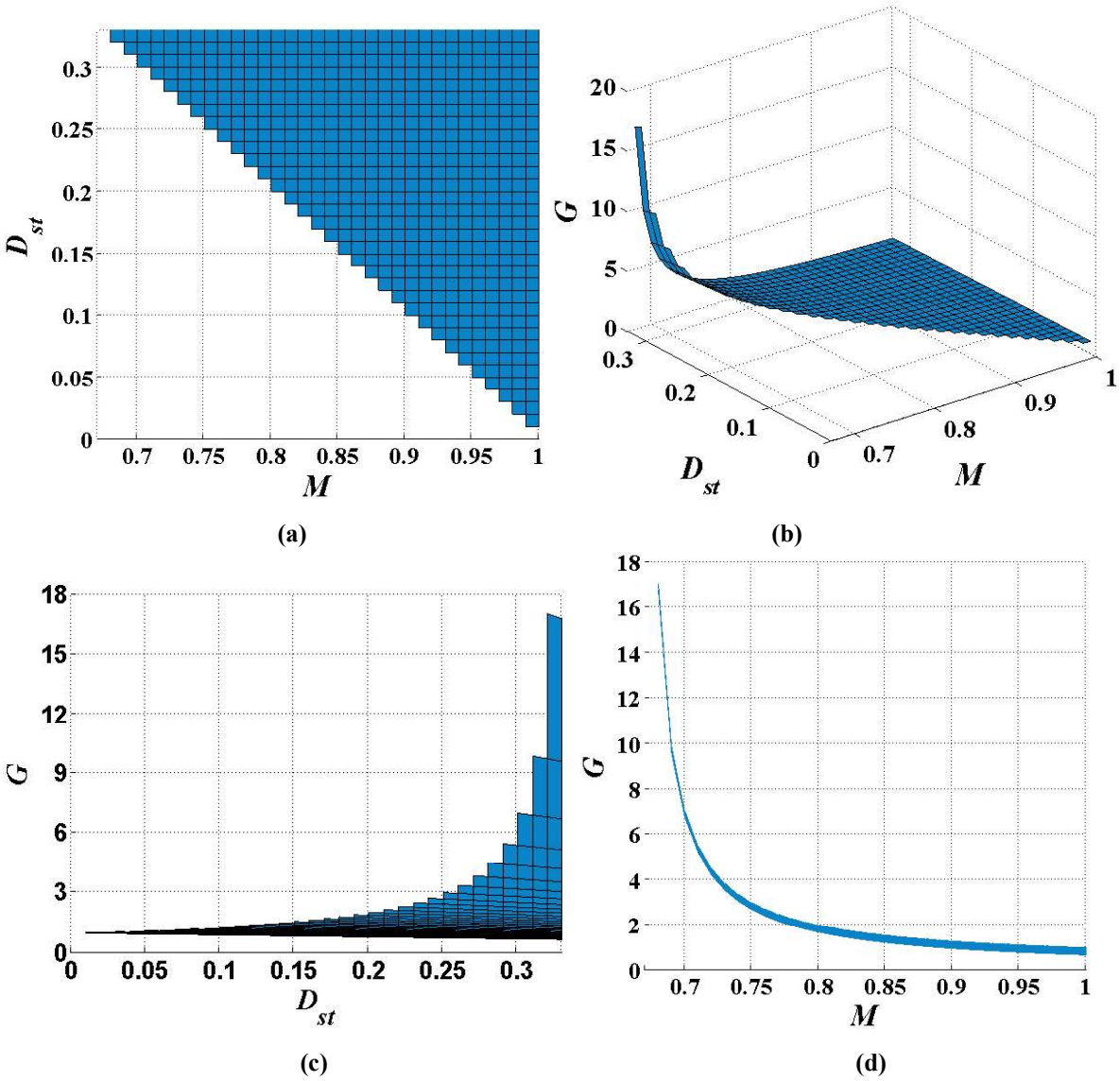
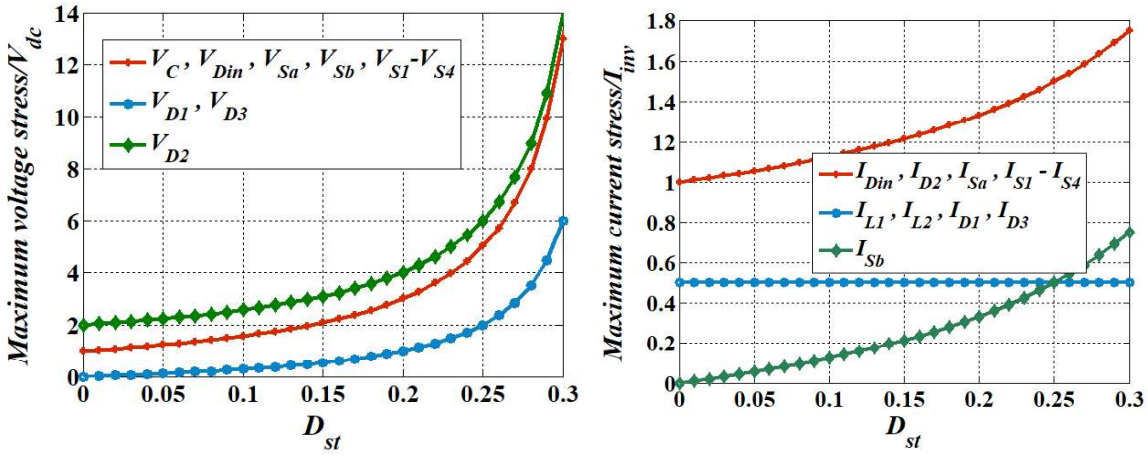


Fig. 4.5. Graphical representation of the correlation among G, D_{st} and M of Type 1 SLC-ZSI **(a)** D_{st} versus M **(b)** 3-D surface plot **(c)** G versus D_{st} **(d)** G versus M.

The maximum current and voltage stresses on the elements of Type 1 SLC-ZSI are determined and given in Table 4.1. The normalized stresses are plotted with respect to D_{st} and is shown in Fig. 4.6. It can be observed from Fig. 4.6(a) that D_2 has higher voltage stress, diodes (D_1 and D_3) have lesser voltage stress and the remaining elements have voltage stress which is equal to B of Type 1 SLC-ZSI. It can be observed from Fig. 4.6(b) that S_b has lesser current stress, switches of HB circuit have higher current stress and elements (D_1, D_3, L_1 and L_2) have constant current stress irrespective of D_{st}.

Table 4.1. Maximum current and voltage stresses on the elements of Type 1 SLC-ZSI.

	Maximum voltage stress	**Maximum current stress**
C	$\frac{(1+D_{st})V_{dc}}{(1-3D_{st})}$	$I_{dc}-I_{inv}$
D_1	$\frac{(2D_{st})V_{dc}}{(1-3D_{st})}$	$\frac{(1-D_{st})I_{inv}}{(2-2D_{st})}$
D_2	$\frac{(2-2D_{st})V_{dc}}{(1-3D_{st})}$	$\frac{(1-D_{st})I_{inv}}{(1-2D_{st})}$
D_3	$\frac{(2D_{st})V_{dc}}{(1-3D_{st})}$	$\frac{(1-D_{st})I_{inv}}{(2-2D_{st})}$
D_{in}	$\frac{(1+D_{st})V_{dc}}{(1-3D_{st})}$	$\frac{(1-D_{st})I_{inv}}{(1-2D_{st})}$
L_1	$\frac{2(1-D_{st})V_{dc}}{1-3D_{st}}$	$\frac{(1-D_{st})I_{inv}}{(2-2D_{st})}$
L_2	$\frac{2(1-D_{st})V_{dc}}{1-3D_{st}}$	$\frac{(1-D_{st})I_{inv}}{(2-2D_{st})}$
S_a	$\frac{(1+D_{st})V_{dc}}{(1-3D_{st})}$	$\frac{(1-D_{st})I_{inv}}{(1-2D_{st})}$
S_b	$\frac{(1+D_{st})V_{dc}}{(1-3D_{st})}$	$\frac{(D_{st})I_{inv}}{(1-2D_{st})}$
S_1-S_4	$\frac{(1+D_{st})V_{dc}}{(1-3D_{st})}$	$\frac{(1-D_{st})I_{inv}}{(1-2D_{st})}$



(a) **(b)**

Fig. 4.6. Normalized maximum current and voltage stresses on the elements of Type 1 SLC-ZSI **(a)** normalized device voltage stress versus D_{st} **(b)** normalized device current stress versus D_{st}.

4.2.3 Design of Passive Elements of Type 1 SLC-ZSI

For CCM operation of Type 1 SLC-ZSI, minimum values of passive elements can be calculated from the inequalities given in (4.10).

$$\left.\begin{aligned} L_1 &\geq \frac{2{V_{dc}}^2 T_s D_{st}(1+D_{st})}{x_{L1}\%P_{ac}(1-3D_{st})} \\ L_2 &\geq \frac{2{V_{dc}}^2 T_s D_{st}(1+D_{st})}{x_{L2}\%P_{ac}(1-3D_{st})} \\ C &\geq \frac{2(1-D_{st})(1-3D_{st})P_{ac}T_{st}D_{st}}{x_C\%{V_{dc}}^2(1+D_{st})^2} \end{aligned}\right\} \quad (4.10)$$

where $x_{L1}\%$ and $x_{L2}\%$ are percentage ripple in inductor currents (I_{L1} and I_{L2}), $x_C\%$ is percentage ripple in capacitor voltage (V_c), T_s is the switching period, V_{dc} is the input voltage and P_{ac} is the output power.

Moreover, ripple in inductor currents (ΔI_L) of Type 1 SLC-ZSI can be calculated from the expression given in (4.11).

$$\Delta I_L = \int_0^{D_{st}T_s} \frac{di_L}{dt}\,dt \quad (4.11)$$

Using (4.11), the obtained ripples in inductor currents are given in (4.12).

$$\left.\begin{aligned} \Delta I_{L1} &= \frac{V_{L1}}{L_1} D_{st} T_s \\ \Delta I_{L2} &= \frac{V_{L2}}{L_2} D_{st} T_s \end{aligned}\right\} \quad (4.12)$$

where $V_{L1}$and V_{L2} are voltages across L_1 and L_2 during shoot-through operation.

The ripple in capacitor voltage (ΔV_C) of Type 1 SLC-ZSI can be calculated from the expression given in (4.13).

$$\Delta V_C = \int_0^{DT_s} \frac{dV_C}{dt}\,dt \quad (4.13)$$

Using (4.13), the obtained ripple in capacitor voltage is given in (4.14)

$$\Delta V_C = \frac{I_C}{C} D_{st} T_s \quad (4.14)$$

where I_C is the current flowing through C during shoot-through operation.

Further, the design criteria of second-order low-pass filter (C_f and L_f) which gives fundamental sinusoidal wave across AC load is discussed here. The cutoff frequency (f_c) of low-pass filter should be chosen one decade below the switching frequency of Type 1 SLC-ZSI, to obtain a 40-dB attenuation for voltage components at switching frequency and unity gain at frequency of AC output. As per the said statements and assuming value of C_f, value of L_f can be determined from the equation given in (4.15).

$$L_f = \frac{1}{(2\pi f_c)^2 C_f} \tag{4.15}$$

4.3 Proposed Single-Phase Type 2 SLC-ZSI

Fig. 4.7 shows a single-phase Type 2 SLC-ZSI. It is an improved version of Type 1 SLC-ZSI. Also, it has a similar circuit arrangement of Type 1 SLC-ZSI by replacing D_1 of SL cell with a capacitor C_1 as shown in Fig. 4.7. Although it has an equal number of elements as that of Type 1 SLC-ZSI, it has a higher voltage gain because of small modification in SL cell. As it is an improved version of Type 1 SLC-ZSI, its operation is similar to Type 1 SLC-ZSI. For simplifying the operation, the HB circuit of Type 2 SLC-ZSI is also replaced by a parallel combination of a switch S_{inv} and an equivalent resistance R_{eq} as shown in Fig. 4.8.

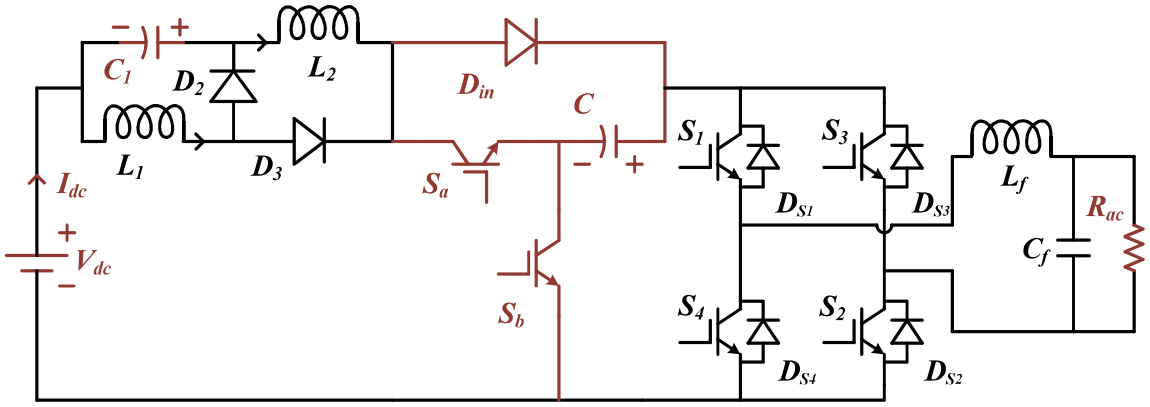


Fig. 4.7. A single-phase Type 2 SLC-ZSI.

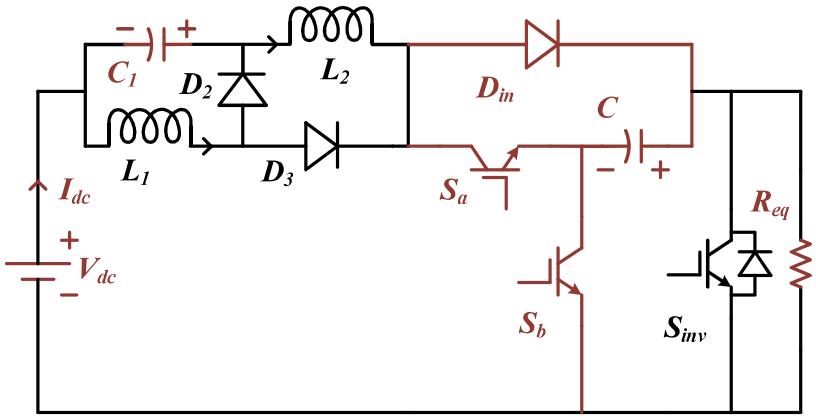


Fig. 4.8. Simplified circuit of Type 2 SLC-ZSI for analysing its operation.

4.3.1 Operation of Type 2 SLC-ZSI

The operating waveforms of Type 2 SLC-ZSI are explained in two operating intervals as shown in Fig. 4.9. As shown in Fig. 4.9, the Type 2 SLC-ZSI has also three switching states; shoot-through, zero and power states. The significance of these three states of Type 2 SLC-ZSI is the same as that of Type 1 SLC-ZSI.

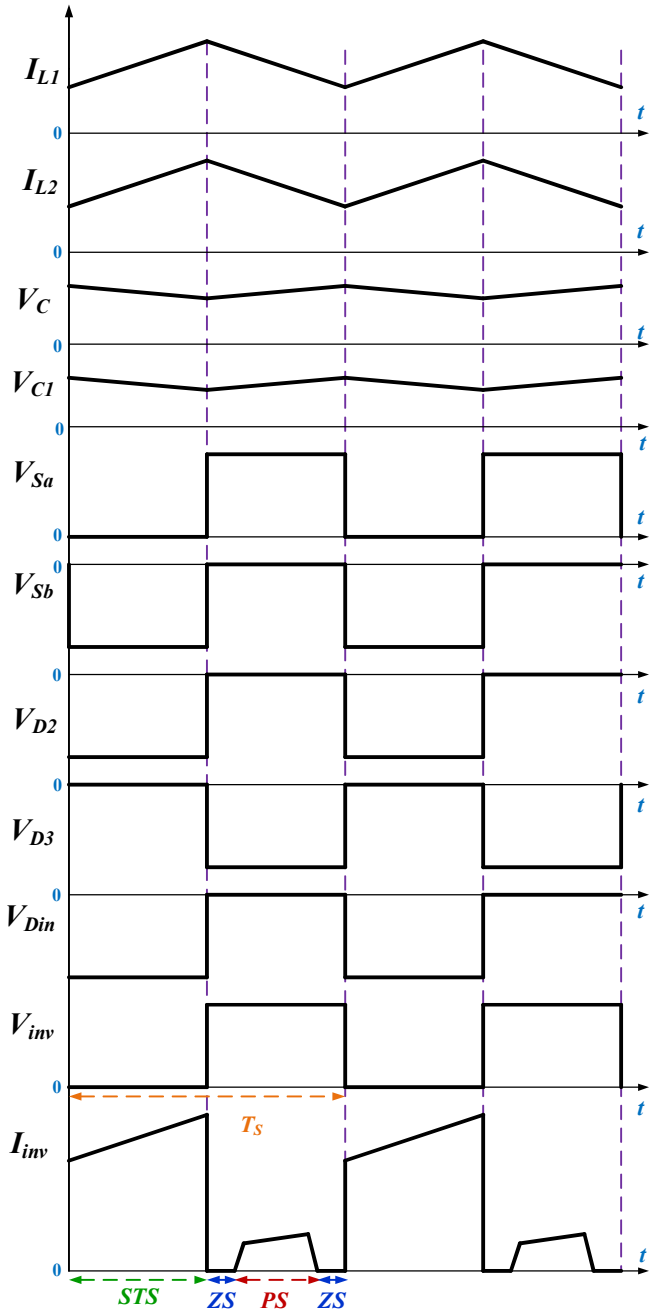


Fig. 4.9. Operating waveforms of Type 2 SLC-ZSI.

(a) Shoot-Through Operation of Type 2 SLC-ZSI

The equivalent circuit of Type 2 SLC-ZSI during shoot-through operation is shown in Fig. 4.10(a). During this operation, switches (S_{inv} and S_a) are turned-on and S_b is turned-off. Meanwhile, diodes (D_2 and D_{in}) are reverse biased and D_3 is forward biased. The capacitors (C and C_1) are start discharging and inductors (L_1 and L_2) start charging. From Fig. 4.10(a), the obtained KCL and KVL equations are given in (4.16).

$$\left.\begin{array}{c} v_{L1} = v_{dc} + v_{C2} \\ v_{L2} = v_{in} + v_{C2} + v_{C1} \\ i_{C1} = -i_{L2} \\ i_{C2} = -i_{L1} - i_{L2} \\ v_{inv} = 0 \\ i_{st} = i_{L1} + i_{L2} \end{array}\right\} \tag{4.16}$$

(b) Non-Shoot-Through Operation of Type 2 SLC-ZSI

The equivalent circuit of Type 2 SLC-ZSI during non-shoot-through operation is shown in Fig. 4.10(b). During this operation, switches (S and S_a) are turned-off and S_b is turned-on. Meanwhile, diodes (D_2 and D_{in}) are forward biased and D_3 is reverse biased. The combined energy of DC source and magnetic energy of inductors appears across the HB circuit of Type 2 SLC-ZSI and capacitors (C and C_1) are charged. From Fig. 4.10(b), the obtained KCL and KVL equations are given in (4.17).

$$\left.\begin{array}{c} v_{L1} = -v_{C1} \\ v_{L2} = v_{in} + v_{C1} - v_{C2} \\ i_{C1} = i_{L1} - i_{L2} \\ i_{C2} = i_{L2} - i_{inv} \\ v_{inv} = v_{C2} \end{array}\right\} \tag{4.17}$$

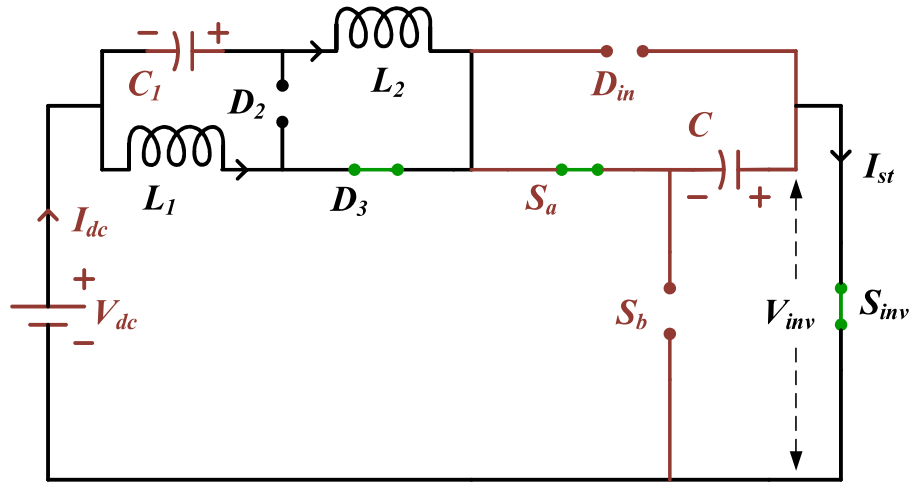
4.3.2 Steady-State Analysis of Type 2 SLC-ZSI

After applying volt-second balance principle to L_1 over T_s, the obtained steady-state expression is given in (4.18).

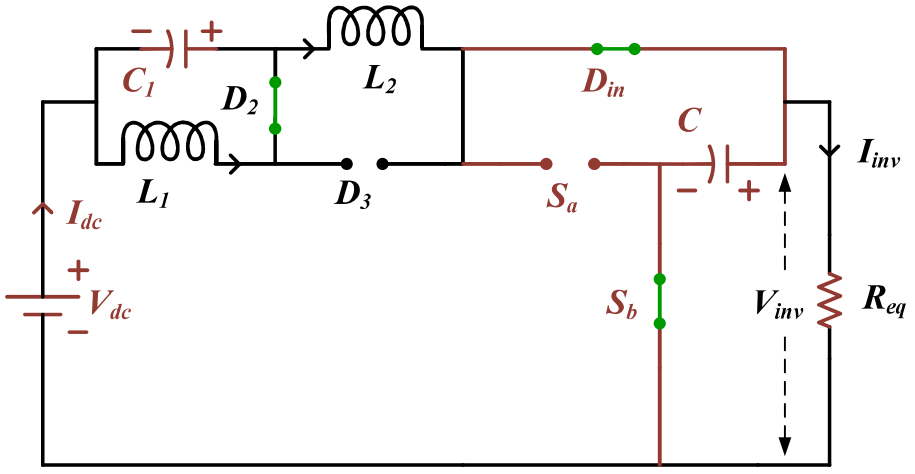
$$V_{C1} = \frac{D_{st}}{1-D_{st}}(V_{dc} + V_{C2}) \tag{4.18}$$

Similarly, by applying volt-second balance principle to L_2, the obtained steady-state expression is given in (4.19).

$$V_{dc} + V_{C1} = (1 - 2D_{st})V_{C2} \tag{4.19}$$



(a)



(b)

Fig. 4.10. Equivalent circuits of Type 2 SLC-ZSI **(a)** during shoot-through operation **(b)** during non-shoot-through operation.

By solving (4.18) and (4.19), the obtained steady-state voltage of C_2, V_{C2} is given in (4.20).

$$V_{C2} = \frac{V_{dc}}{1-4D_{st}+2{D_{st}}^2} \tag{4.20}$$

From (4.19) and (4.20), the obtained steady-state voltage of C_1, V_{C1} is given in (4.21).

$$V_{C1} = \frac{2D_{st}(1-D_{st})V_{dc}}{1-4D_{st}+2{D_{st}}^2} \tag{4.21}$$

Further, applying charge-second balance principle to C_1 over T_s, the obtained steady-state relation is given in (4.22).

$$I_{L2} = (1 - D_{st})I_{L1} \tag{4.22}$$

Similarly, applying charge-second balance principle to C_2, the obtained steady-state relation is given in (4.23).

$$(1 - 2D_{st}) = I_{L1}D_{st} + I_{inv}(1 - D_{st}) \tag{4.23}$$

Solving (4.22) and (4.23), the obtained steady-state average current through L_1 is given in (4.24).

$$I_{L1} = \frac{(1-D_{st})}{1-4D_{st}+2D_{st}^2} I_{inv} \tag{4.24}$$

From (4.22) and (4.24), the obtained steady-state average current through L_2 is given in (4.25).

$$I_{L2} = \frac{(1-D_{st})^2}{1-4D_{st}+2D_{st}^2} I_{inv} \tag{4.25}$$

The boosted voltage appearing across the HB circuit of Type 2 SLC-ZSI, V_{inv} is same as that of V_{C2} and is rewritten as given in (4.26).

$$V_{inv} = \frac{V_{dc}}{1-4D_{st}+2D_{st}^2} = BV_{dc} \tag{4.26}$$

where B is boosting ability of Type 2 SLC-ZSI and defined as the ratio of V_{inv} and V_{dc}. The mathematical expression of B of Type 2 SLC-ZSI is given in (4.27).

$$B = \frac{V_{inv}}{V_{dc}} = \frac{1}{1-4D_{st}+2D_{st}^2} \tag{4.27}$$

The fundamental peak AC output voltage $V_{ac(pk)}$ of single-phase Type 2 SLC-ZSI is given in (4.28).

$$V_{ac(pk)} = MV_{inv} = MBV_{in} = GV_{in} \tag{4.28}$$

where G is a voltage gain of Type 2 SLC-ZSI and defined as the ratio of $V_{ac(pk)}$ and V_{dc}. The mathematical expression of G of Type 2 SLC-ZSI is given in (4.29).

$$G = MB = \frac{V_{ac(pk)}}{V_{dc}} = \frac{M}{1-4D_{st}+2D_{st}^2} \tag{4.29}$$

It can be determined from (4.29) that the Type 2 SLC-ZSI has maximum values of $D_{st} = 0.292$ and $M = 0.708$ based on operating condition $D_{st} + M \leq 1$. The correlation among G, M and D_{st} of Type 2 SLC-ZSI is plotted and is shown in Fig. 4.11. The interdependence of D_{st} and M is shown in Fig. 4.11(a). It can be observed from Fig. 4.11(a) that M increases when D_{st} decreases, since $D_{st} + M \leq 1$. Fig. 4.11(b) shows a 3-D surface plot representing the relationship among D_{st}, M and G of Type 2 SLC-ZSI. Figs. 4.11(c) and 4.11(d) show G versus D_{st} and G versus M, respectively. It can be observed from Figs. 4.11(c) and 4.11(d) that G increases when D_{st} increases, and G decreases when M increases.

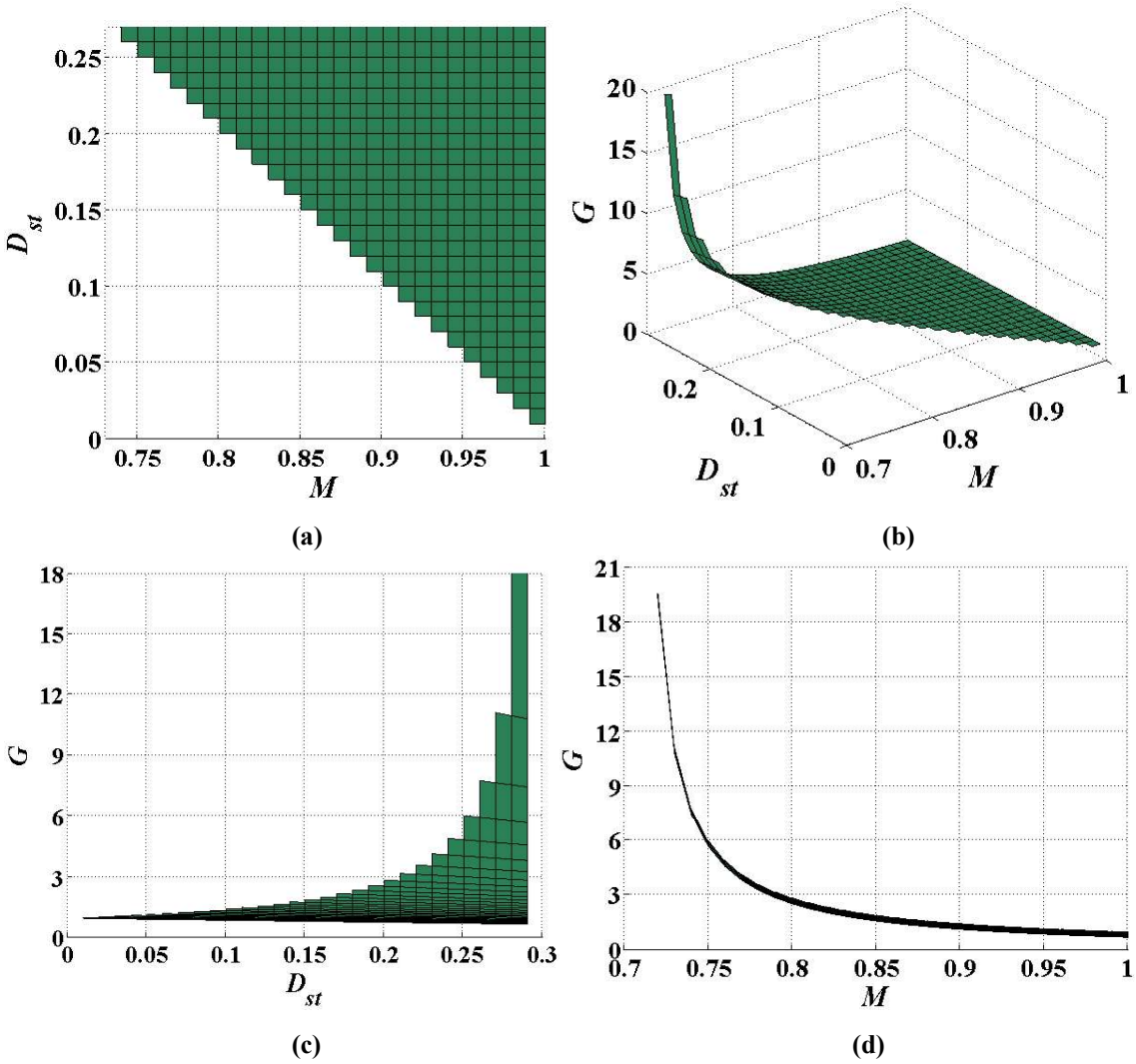


Fig. 4.11. Graphical representation of the correlation among G, D_{st} and M of Type 2 SLC-ZSI **(a)** D_{st} versus M **(b)** 3-D surface plot of G, D_{st} and M **(c)** G versus D_{st} **(d)** G versus M.

Table 4.2 shows maximum current and voltage stresses on the elements of Type 2 SLC-ZSI. Further, the stresses are normalized and plotted with respect to D_{st} as shown in Fig. 4.12. It can be observed from Fig. 4.12(a) that C_1 has lesser voltage stress and D_2 has higher voltage stress as compared to remaining elements of Type 2 SLC-ZSI. It can be observed from Fig. 4.12(b) that S_b has lesser current stress and other active switches (S_a and $S_1 - S_4$) have higher current stress as compared to remaining elements of Type 2 SLC-ZSI.

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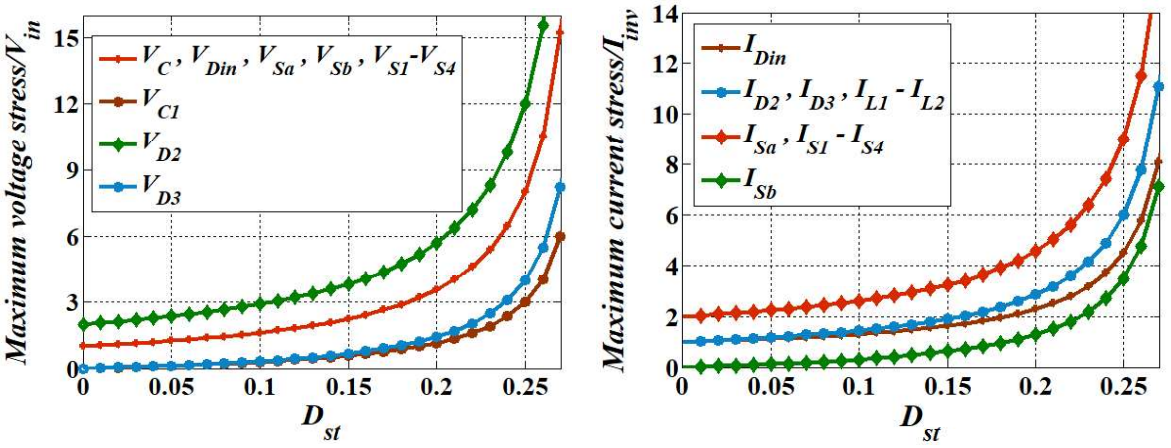
Table 4.2. Maximum current and voltage stresses on the elements of Type 2 SLC-ZSI.

	Maximum voltage stress	**Maximum current stress**
C	$\frac{V_{dc}}{(1-4D_{st}+2{D_{st}}^2)}$	$\frac{(2-D_{st})(1-D_{st})I_{inv}}{(1-4D_{st}+2{D_{st}}^2)}$
C_1	$\frac{(2D_{st}-2{D_{st}}^2)V_{dc}}{(1-4D_{st}+2{D_{st}}^2)}$	$\frac{(1-D_{st})^2 I_{inv}}{(1-4D_{st}+2{D_{st}}^2)}$
D_2	$\frac{(2-2D_{st})V_{dc}}{(1-4D_{st}+2{D_{st}}^2)}$	$\frac{(1-D_{st})I_{inv}}{(1-4D_{st}+2{D_{st}}^2)}$
D_3	$\frac{(2D_{st})V_{dc}}{(1-4D_{st}+2{D_{st}}^2)}$	$\frac{(1-D_{st})I_{inv}}{(1-4D_{st}+2{D_{st}}^2)}$
D_{in}	$\frac{V_{dc}}{(1-4D_{st}+2{D_{st}}^2)}$	$\frac{(1-2D_{st}+{D_{st}}^2)I_{inv}}{(1-4D_{st}+2{D_{st}}^2)}$
L_1	$\frac{(2-4D_{st}+2{D_{st}}^2)V_{in}}{(1-4D_{st}+2{D_{st}}^2)}$	$\frac{(1-D_{st})I_{inv}}{(1-4D_{st}+2{D_{st}}^2)}$
L_2	$\frac{2(1-D_{st})V_{dc}}{(1-4D_{st}+2{D_{st}}^2)}$	$\frac{(1-D_{st})^2 I_{inv}}{(1-4D_{st}+2{D_{st}}^2)}$
S_a	$\frac{V_{dc}}{(1-4D_{st}+2{D_{st}}^2)}$	$\frac{(2-4D_{st}+2{D_{st}}^2)I_{inv}}{(1-4D_{st}+2{D_{st}}^2)}$
S_b	$\frac{V_{dc}}{(1-4D_{st}+2{D_{st}}^2)}$	$\frac{(2D_{st}-{D_{st}}^2)I_{inv}}{(1-4D_{st}+2{D_{st}}^2)}$
$S_1 - S_4$	$\frac{V_{dc}}{(1-4D_{st}+2{D_{st}}^2)}$	$\frac{(2-4D_{st}+2{D_{st}}^2)I_{inv}}{(1-4D_{st}+2{D_{st}}^2)}$



(a) **(b)**

Fig. 4.12. Normalized maximum current and voltage stresses on the elements of Type 2 SLC-ZSI **(a)** normalized device voltage stress versus D_{st} **(b)** normalized device current stress versus D_{st}.

4.3.3 Design of Passive Elements of Type 2 SLC-ZSI

For CCM operation of Type 2 SLC-ZSI, minimum values of passive elements can be determined from the inequalities given in (4.30).

$$\left.\begin{aligned} L_1 &\geq \frac{{V_{dc}}^2(2-4D_{st}+2{D_{st}}^2)D_{st}T_s}{x_{L1}\%\,(1-D_{st})(1-4D_{st}+2D^2)P_{ac}} \\ L_2 &\geq \frac{{V_{dc}}^2 2(1-D_{st})D_{st}T_s}{x_{L2}\%\,(1-D_{st})^2(1-4D_{st}+2{D_{st}}^2)P_{ac}} \\ C &\geq \frac{(1-D_{st})(2-D_{st})(1-4D_{st}+2{D_{st}}^2)D_{st}T_sP_{ac}}{x_C\%\,{V_{dc}}^2} \\ C_1 &\geq \frac{(1-D_{st})^2(1-4D_{st}+2{D_{st}}^2)D_{st}T_sP_{ac}}{x_{C1}\%\,2D_{st}(1-D_{st}){V_{dc}}^2} \end{aligned}\right\} \tag{4.30}$$

where $x_{L1}\%$ and $x_{L2}\%$ are percentage ripple in inductor currents (I_{L1} and I_{L2}), $x_C\%$ and $x_{C1}\%$ are percentage ripple in capacitor voltages (V_C and V_{C1}), T_s is the switching period, V_{dc} is the input voltage and P_{ac} is the output power.

The ripple in inductor currents (ΔI_L) of Type 2 SLC-ZSI can be calculated using (4.31).

$$\Delta I_L = \int_0^{D_sT_s} \frac{di_L}{dt}\,dt \tag{4.31}$$

By using (4.30), the obtained ripples in inductor currents of Type 2 SLC-ZSI are given in (4.32).

$$\left.\begin{aligned} \Delta I_{L1} &= \frac{V_{L1}}{L_1}DT_s \\ \Delta I_{L2} &= \frac{V_{L2}}{L_2}DT_s \end{aligned}\right\} \tag{4.32}$$

where V_{L1} and V_{L2} are voltages across L_1 and L_2 during shoot-through operation.

The ripple in capacitor voltages (ΔV_C) of Type 2 SLC-ZSI can be calculated from the following expression.

$$\Delta V_C = \int_0^{D_{st}T_s} \frac{dV_C}{dt}\,dt \tag{4.33}$$

By using (4.33), the obtained ripples in capacitor voltages of Type 2 SLC-ZSI are given in (4.34).

$$\left.\begin{aligned} \Delta V_C &= \frac{I_C}{C}D_{st}T_s \\ \Delta V_{C1} &= \frac{I_{C1}}{C_1}D_{st}T_s \end{aligned}\right\} \tag{4.34}$$

where I_C and I_{C1} are currents through C and C_1 during shoot-through operation.

Further, the design criteria of second-order low-pass filter (C_f and L_f) of Type 2 SLC-ZSI is discussed here. The cutoff frequency (f_c) of low-pass filter should be chosen one decade below the switching frequency of Type 2 SLC-ZSI, to obtain a 40-dB attenuation for voltage

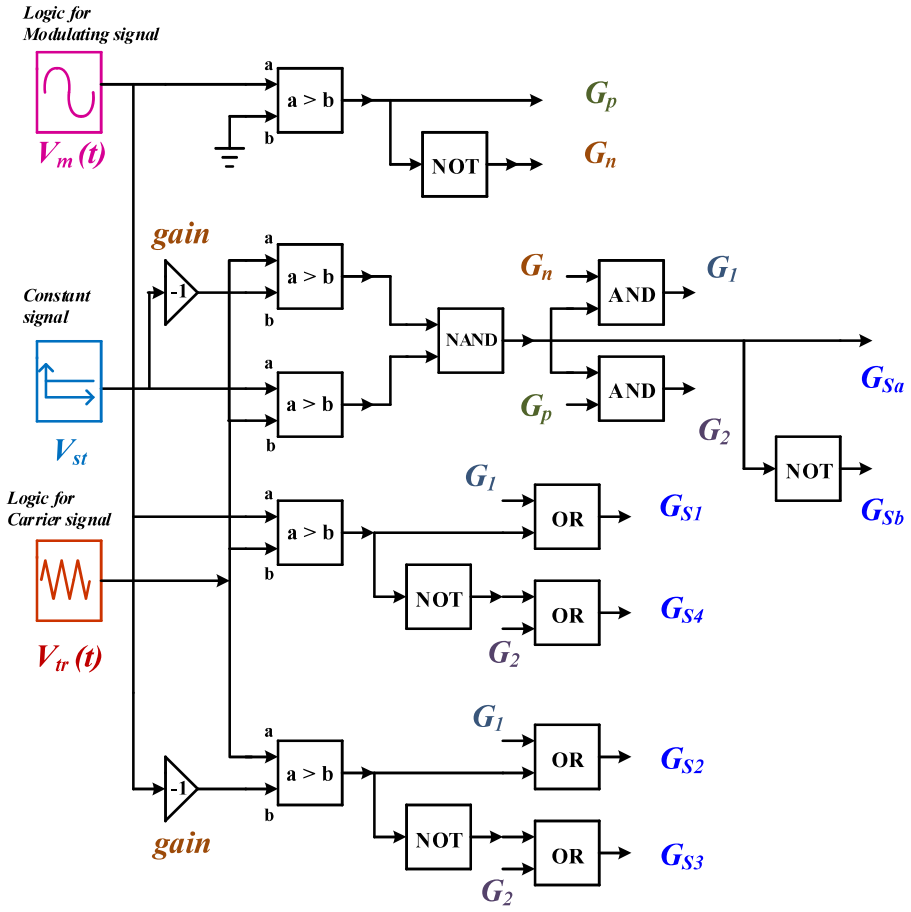
components at switching frequency and unity gain at frequency of the AC output. As per the said statements and assuming the value of C_f, value of L_f can be determined from the equation given in (4.35).

$$L_f = \frac{1}{(2\pi f_c)^2 C_f} \tag{4.35}$$

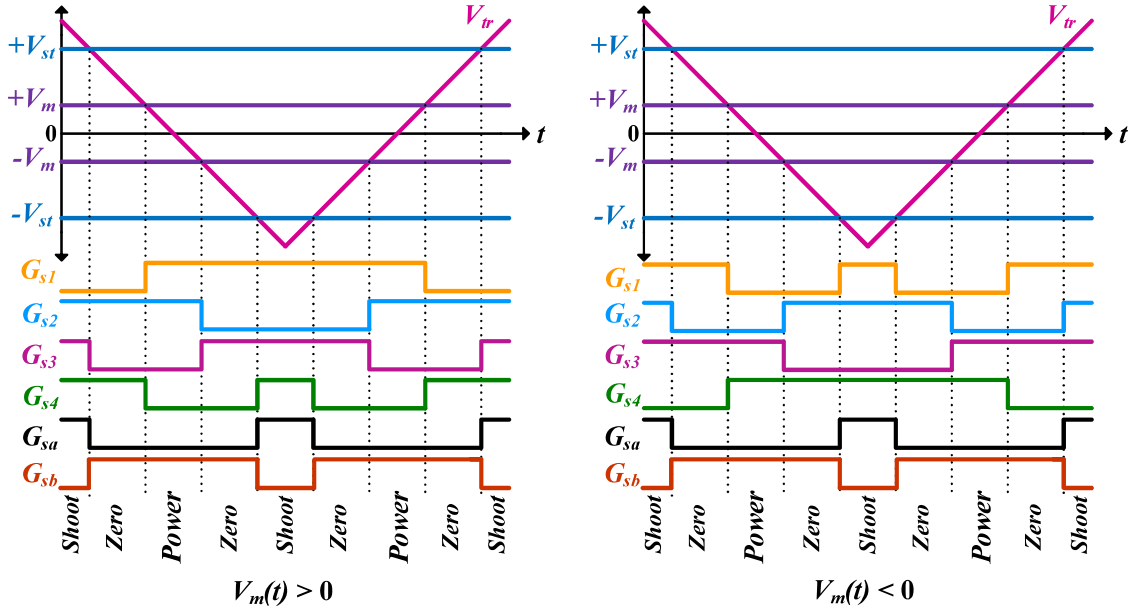
4.4 Modified Unipolar SPWM Technique of Proposed Single-Phase SLC-ZSIs

A modified unipolar SPWM technique has been derived from the conventional unipolar SPWM technique to operate the two SLC-ZSIs [115]-[117]. As the Type 2 SLC-ZSI is an improved version of Type 1 SLC-ZSI, the two SLC-ZSIs are operated by the same SPWM technique. The SPWM switching logic of SLC-ZSIs is implemented in the field-programmable gate array (FPGA) digital platform and its schematic is given in its analog version as shown in Fig. 4.13(a). It can be observed from Fig. 4.13(a) that the switching logic consists of three source signals; constant signal (V_{st}), modulation signal ($V_m(t)$) and carrier signal ($V_{tr}(t)$) to produce required gating signals of two SLC-ZSIs. The magnitude and frequency of $V_m(t)$ decide M and frequency of AC output. The frequency of $V_{tr}(t)$ is as same as the switching frequency of SLC-ZSIs. As stated earlier, the SLC-ZSIs are operated in three states. The STS is generated by comparing V_{st} with $V_{tr}(t)$. For ensuring the STS not to disturb PS, it is placed within ZS of each switching cycle. As per the switching logic, the expected gating signals of SLC-ZSIs are shown in Fig. 4.13(b) for $V_m(t) > 0$ and $V_m(t) < 0$, respectively. As discussed earlier that G of SLC-ZSIs is a function of D_{st} and M, the relations among D_{st}, V_{st}, $V_{tr}(t)$ and M, $V_m(t)$, $V_{tr}(t)$ are given in (4.36). Moreover, D_{st} and M are interdependent and their mathematical relations are given in (4.36).

$$\left.\begin{aligned} D_{st} &= 1 - \frac{V_{st}}{V_{tr}} \\ M &= \frac{V_m}{V_{tr}} \end{aligned}\right\} V_{st} \geq V_m \; and \; D_{st} + M \leq 1 \tag{4.36}$$



(a)



(b)

Fig. 4.13. Modified unipolar SPWM technique of proposed single-phase SLC-ZSIs **(a)** Switching logic for generating the required gating pulses **(b)** gate pulses of SLC-ZSIs for $V_m(t) > 0$ and $V_m(t) < 0$.

4.5 Comparison Among Proposed SLC-ZSIs and Some Reported SL based ZSIs

As the proposed SLC-ZSIs are non-isolated and based on SL concept, some reported non-isolated SL based ZSIs [72]-[74] are considered for comparison. Table 4.3 shows a comparison among proposed SLC-ZSIs and reported ZSIs in terms of number of elements, boosting capability (B) and voltage gain (G). It can be observed from Table 4.3 that the proposed SLC-ZSIs have lesser number of elements as compared to reported ZSIs. Further, B and G of two SLC-ZSIs are plotted with respect to D_{st} and M respectively and compared with reported ZSIs. Fig. 4.14(a) shows variation in B with respect to D_{st}. It can be noticed from Fig. 4.14(a) that the Type 2 SLC-ZSI has high boosting ability at low values of D_{st} in comparison to Type 1 SLC ZSI and reported ZSIs. Although the SL-ZSI and rsL-qZSI have same boosting ability as that of Type 1 SLC-ZSI, they have higher number of elements. Fig. 4.14(b) shows variation in G with respect to M. It can be noticed from Fig. 4.14(b) that the Type 2 SLC-ZSI has higher voltage gain in comparison to reported ZSIs and Type 1 SLC-ZSI.

Table 4.3. Comparison among the proposed SLC-ZSIs and some reported SL based ZSIs.

	L-ZSI	**SL-ZSI**	**SL-qZSI**	**rSL-qZSI**	**cSL-qZSI**	**Type 1 SLC-ZSI**	**Type 2 SLC-ZSI**
Inductors	2	4	3	4	4	2	2
Capacitors	0	2	2	2	2	1	2
Diodes	3	7	4	7	7	4	3
Switches	4	4	4	4	4	6	6
Total elements	9	17	13	17	17	13	13
B	$\frac{1+D_{st}}{1-D_{st}}$	$\frac{1+D_{st}}{1-3D_{st}}$	$\frac{1+D_{st}}{1-2D_{st}-D_{st}^2}$	$\frac{1+D_{st}}{1-3D_{st}}$	$\frac{1}{1-3D_{st}}$	$\frac{1+D_{st}}{1-3D_{st}}$	$\frac{1}{1-4D_{st}+2D_{st}}$
G	$2-M$	$\frac{2M-M^2}{3M-2}$	$\frac{M^2-2M}{M^2-4M+2}$	$\frac{2M-M^2}{3M-2}$	$\frac{M}{3M-2}$	$\frac{2M-M^2}{3M-2}$	$\frac{M}{2M^2-1}$

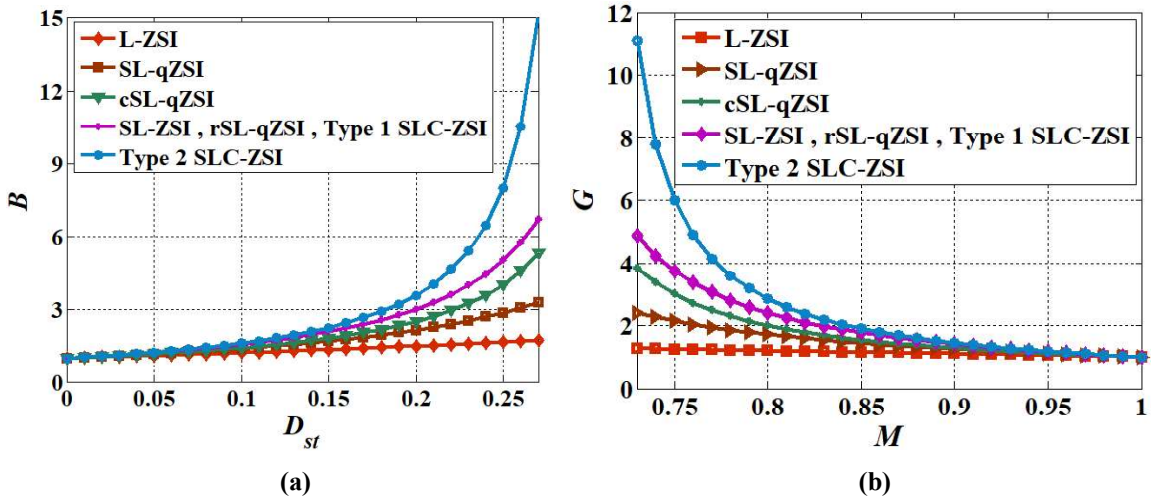


Fig. 4.14. Boosting ability and voltage gain of proposed SLC-ZSIs as compared to reported ZSIs **(a)** B versus D_{st} **(b)** G versus M.

Further, maximum total voltage and current stresses on the elements of all ZSIs (SLC-ZSIs and reported ZSIs) are derived and given in Tables 4.4 and 4.5, respectively. Also, the stresses are plotted with respect to G under same operating conditions and are shown in Fig. 4.15. It can be observed from Fig. 4.15(a) that the Type 1 SLC-ZSI has lesser total capacitor voltage stress as compared to reported ZSIs and Type 2 SLC-ZSI. Also, the rSL-qZSI has capacitor voltage stress is same as that of Type 1 SLC-ZSI. Fig. 4.15(b) shows maximum total diode voltage stress of all ZSIs. It can be observed from Fig. 4.15(b) that SL-qZSI has lesser diode voltage stress as compared to reported ZSIs. It can be noticed from Fig. 4.15(c) that the proposed SLC-ZSIs have higher total switch voltage stress in comparison to reported SL-ZSIs because they have higher number of switches. Fig. 4.15(d) shows maximum total inductor current stress of all ZSIs. It can be found from Fig. 4.15(d) that the proposed SLC-ZSIs have lesser total inductor current stress as compared to reported ZSIs. It can be observed from Fig. 4.15(e) that the proposed SLC-ZSIs have lesser total diode current stress as compared to reported ZSIs. Moreover, the Type 1 SLC-ZSI has lesser inductor and diode current stresses in comparison to Type 2 SLC-ZSI. Fig. 4.15(f) shows the total switch current stress of all ZSIs. It can be found from Fig. 4.15(f) that the Type 1 SLC-ZSI has lesser total switch current stress as compared to Type 2 SLC-ZSI and reported ZSIs.

Table 4.4. Maximum total voltage stress on the elements of proposed SLC-ZSIs and some reported SL based ZSIs.

	SL-ZSI	**SL-qZSI**	**rSL-qZSI**	**cSL-qZSI**	**Type 1 SLC-ZSI**	**Type 2 SLC-ZSI**
C_1	$\frac{(1-D_{st})V_{dc}}{1-3D_{st}}$	$\frac{(1-D_{st})V_{dc}}{1-2D_{st}-{D_{st}}^2}$	$\frac{1-D_{st}V_{dc}}{1-3D_{st}}$	$\frac{(1-D_{st})V_{dc}}{(1+D_{st})(1-3D_{st})}$	---	$\frac{2D_{st}(1-D_{st})V_{dc}}{1-4D_{st}+2{D_{st}}^2}$
C , C_2	$\frac{(1-D_{st})V_{dc}}{1-3D_{st}}$	$\frac{2D_{st}V_{dc}}{1-2D_{st}-{D_{st}}^2}$	$\frac{2D_{st}V_{dc}}{1-3D_{st}}$	$\frac{2D_{st}V_{dc}}{(1+D_{st})(1-3D_{st})}$	$\frac{(1+D_{st})V_{dc}}{1-3D}$	$\frac{V_{dc}}{1-4D_{st}+2{D_{st}}^2}$
D_{in}	$\frac{(1+D_{st})V_{dc}}{1-3D_{st}}$	$\frac{(1+D_{st})V_{dc}}{1-2D_{st}-{D_{st}}^2}$	$\frac{(1+D_{st})V_{dc}}{1-3D_{st}}$	$\frac{2V_{dc}}{1-3D_{st}}$	$\frac{(1+D_{st})V_{dc}}{1-3D_{st}}$	$\frac{V_{dc}}{1-4D_{st}+2{D_{st}}^2}$
D_1, D_3	$\frac{D_{st}V_{dc}}{1-3D_{st}}$	$\frac{D_{st}V_{dc}}{1-2D_{st}-{D_{st}}^2}$	$\frac{D_{st}V_{dc}}{1-3D_{st}}$	$\frac{(1-D_{st})V_{dc}}{(1+D_{st})(1-3D_{st})}$ $\frac{D_{st}(1+2{D_{st}}^2)V_{dc}}{(1+D_{st})(1-3D_{st})}$	$\frac{2D_{st}V_{dc}}{1-3D_{st}}$	$\frac{2D_{st}V_{dc}}{1-4D_{st}+2{D_{st}}^2}$
D_2, D_5	$\frac{(1-D_{st})V_{dc}}{(1-3D_{st})}$	$\frac{(1-D_{st})V_{dc}}{1-2D_{st}-{D_{st}}^2}$	$\frac{(1-D_{st})V_{dc}}{1-3D_{st}}$	$\frac{(1-D_{st})V_{dc}}{1-3D_{st}}$	$\frac{2(1-D_{st})V_{dc}}{1-3D_{st}}$	$\frac{2(1-D_{st})V_{dc}}{1-4D_{st}+2{D_{st}}^2}$
D_4, D_6	$\frac{D_{st}V_{dc}}{1-3D_{st}}$	---	$\frac{D_{st}V_{dc}}{1-3D_{st}}$	$\frac{2D_{st}V_{dc}}{(1+D_{st})(1-3D_{st})}$	---	---
$S_{1\to4}$	$\frac{(1+D_{st})V_{dc}}{1-3D_{st}}$	$\frac{(1+D_{st})V_{dc}}{1-2D_{st}-{D_{st}}^2}$	$\frac{(1+D_{st})V_{dc}}{1-3D_{st}}$	$\frac{V_{dc}}{(1-3D_{st})}$	$\frac{(1+D_{st})V_{dc}}{1-3D_{st}}$	$\frac{V_{dc}}{1-4D_{st}+2{D_{st}}^2}$
S_a	---	---	---	---	$\frac{(1+D_{st})V_{dc}}{1-3D_{st}}$	$\frac{V_{dc}}{1-4D_{st}+2{D_{st}}^2}$
S_b	---	---	---	---	$\frac{(1+D_{st})V_{dc}}{1-3D_{st}}$	$\frac{V_{dc}}{1-4D_{st}+2{D_{st}}^2}$

Table 4.5. Maximum total current stress on the elements of proposed SLC-ZSIs and some reported ZSIs.

	SL-ZSI	**SL-qZSI**	**rSL-qZSI**	**cSL-qZSI**	**Type 1 SLC-ZSI**	**Type 2 SLC-ZSI**
$\boldsymbol{L_{1\to4}}$	$\frac{(1-D_{st})I_{dc}}{1-3D_{st}}$	$\frac{(1-{D_{st}}^2)I_{inv}}{1-2D_{st}-{D_{st}}^2}$	$\frac{(1-D_{st})I_{dc}}{1-3D_{st}}$	$\frac{(1-D_{st})I_{dc}}{1-3D_{st}}$	$\frac{(1-D_{st})I_{inv}}{2(1-2D_{st})}$	$\frac{(1-D_{st})I_{inv}}{1-4D_{st}+2{D_{st}}^2}$
$\boldsymbol{D_{in}}$	$\frac{3(1-D_{st})I_{dc}}{1-3D_{st}}$	$\frac{(1+D_{st})I_{inv}}{1-2D_{st}-{D_{st}}^2}$	$\frac{(1-D_{st})I_{inv}}{1-3D_{st}}$	$\frac{(1+D_{st})I_{inv}}{1-3D_{st}}$	$\frac{(1-D_{st})I_{inv}}{1-2D_{st}}$	$\frac{(1-D_{st})^2I_{inv}}{1-4D_{st}+2{D_{st}}^2}$
$\boldsymbol{D_1, D_3}$	$\frac{(1-D_{st})I_{dc}}{1-3D_{st}}$	$\frac{(1-D_{st})I_{inv}}{1-2D_{st}-{D_{st}}^2}$	$\frac{(1-D_{st})I_{inv}}{1-3D_{st}}$	$\frac{(1-D_{st})I_{inv}}{1-3D_{st}}$	$\frac{(1-D_{st})I_{inv}}{2(1-2D)}$	$\frac{(1-D_{st})I_{inv}}{1-4D_{st}+2{D_{st}}^2}$
$\boldsymbol{D_2, D_5}$	$\frac{(1-D_{st})I_{dc}}{1-3D_{st}}$	$\frac{(1-D_{st})I_{inv}}{1-2D_{st}-{D_{st}}^2}$	$\frac{(1-D_{st})I_{inv}}{1-3D_{st}}$	$\frac{(1-D_{st})I_{inv}}{1-3D_{st}}$	$\frac{(1-D_{st})I_{inv}}{1-2D_{st}}$	$\frac{(1-D_{st})I_{inv}}{1-4D_{st}+2{D_{st}}^2}$
$\boldsymbol{D_4, D_6}$	$\frac{(1-D_{st})I_{dc}}{1-3D_{st}}$	---	$\frac{(1-D_{st})I_{inv}}{1-3D_{st}}$	$\frac{(1-D_{st})I_{inv}}{1-3D_{st}}$	---	---
$\boldsymbol{S_{1\to4}}$	$\frac{2(1-D_{st})I_{dc}}{1-3D_{st}}$	$\frac{(3-2D_{st}-{D_{st}}^2)I_{inv}}{1-2D_{st}-{D_{st}}^2}$	$\frac{2(1-D_{st})I_{inv}}{1-3D_{st}}$	$\frac{4(1-D_{st})I_{inv}}{1-3D_{st}}$	$\frac{(1-D_{st})I_{inv}}{1-2D_{st}}$	$\frac{(2-4D_{st}+2{D_{st}}^2)I_{inv}}{1-4D_{st}+2{D_{st}}^2}$
$\boldsymbol{S_a}$	---	---	---	---	$\frac{(1-D_{st})I_{inv}}{1-2D_{st}}$	$\frac{(2-4D_{st}+2{D_{st}}^2)I_{inv}}{1-4D_{st}+2{D_{st}}^2}$
$\boldsymbol{S_b}$	---	---	---	---	$\frac{D_{st}I_{inv}}{1-2D_{st}}$	$\frac{(2D_{st}-{D_{st}}^2)I_{inv}}{1-4D_{st}+2{D_{st}}^2}$

Table 4.6. Operating conditions and list of parameters for the validation of proposed SLC-ZSIs.

Parameter		**Value**
Input voltage (V_{dc})		48 V
Output power (P_{ac})		100 W
Switching frequency (f_s)		10 kHz
Line frequency (f_{line})		50 Hz
AC filter Inductor (L_f)		2000 uH
AC filter capacitor (C_f)		10 uF
Shoot-through duty ratio (D_{st})		0.2
Modulation index (M)		0.8
Type 1 SLC-ZSI	Inductor (L_1)	4.24 mH
	Inductor (L_2)	4.28 mH
	Capacitor (C)	220 uF
Type 2 SLC-ZSI	Inductor (L_1)	4.24 mH
	Inductor (L_2)	4.76 mH
	Capacitor (C)	180 uF
	Capacitor (C_1)	220 uF

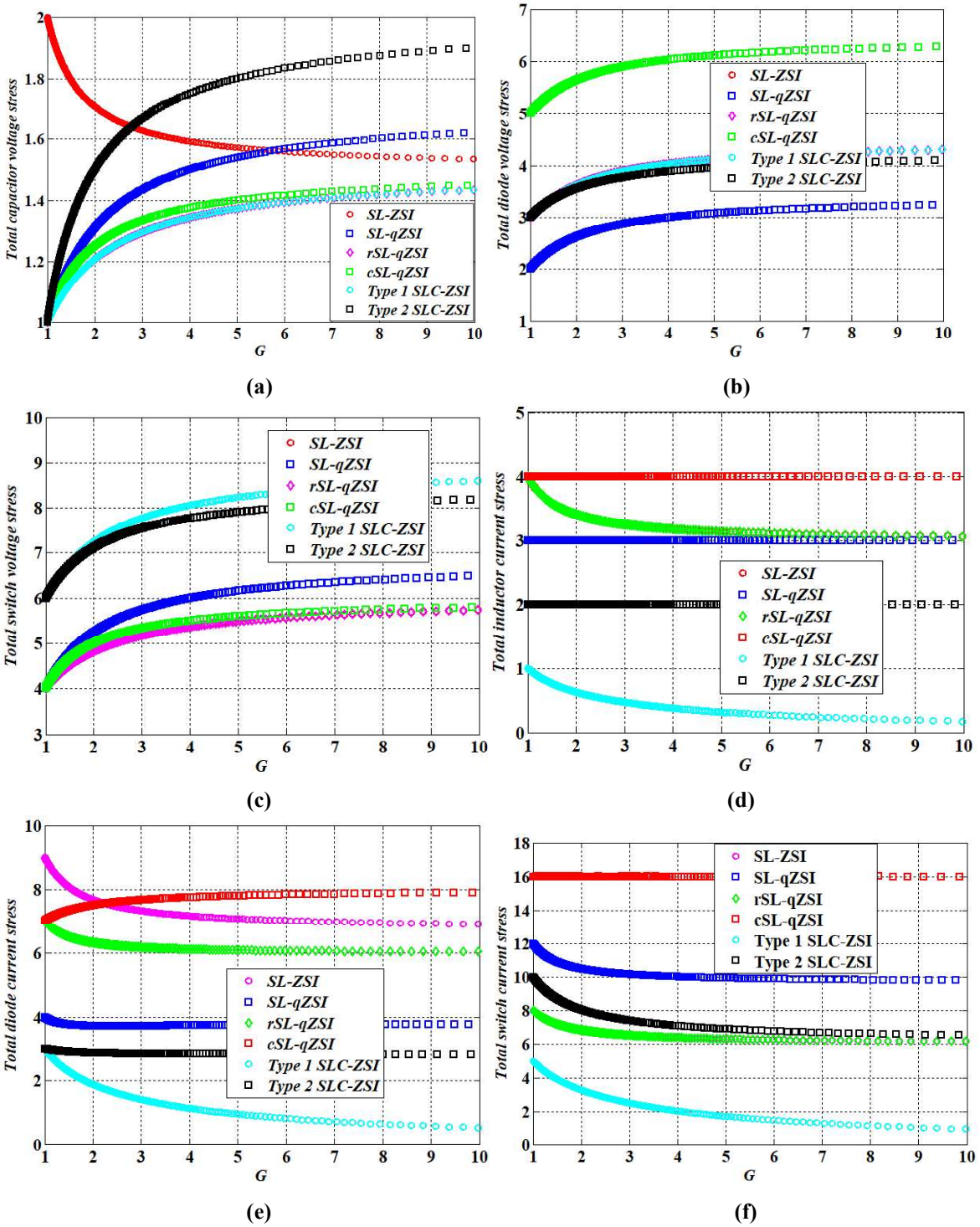


Fig. 4.15. Maximum total voltage and current stresses on the elements of proposed SLC-ZSIs and some reported SL based ZSIs **(a)** total capacitor voltage stress **(b)** total diode voltage stress **(c)** total switch voltage stress **(d)** total inductor current stress **(e)** total diode current stress **(f)** total switch current stress.

4.6 Verification of Proposed SLC-ZSIs

The performance of proposed SLC-ZSIs is verified through simulation and experimental results for the operating conditions given in Table 4.6. Moreover, different values of passive elements for verification of two SLC-ZSIs are considered at the same operating conditions.

4.6.1 Simulation Results of Proposed SLC-ZSIs

The simulation studies of proposed SLC-ZSIs are carried at ideal conditions of elements. Further, Y-axis in the simulation results consist of voltage/current scale having units "V" or "A" and X-axis has a time scale having a unit "s".

4.6.1.1 Simulation Results of Type 1 SLC-ZSI

Fig. 4.16 shows simulation results of Type 1 SLC-ZSI at $D_{st} = 0.2$ and $M = 0.8$ for R and RL loads. Figs. 4.16(a)-(e) show results at R load and Fig. 4.16(f) shows results at RL load. It can be observed from Fig. 4.16(a) that voltage appearing across capacitor (C) $V_C = 144$ V, fundamental RMS AC quantities $V_{ac(rms)} = 81.47$ V and $I_{ac(rms)} = 1.23$ A for input voltage $V_{dc} = 48$ V. Moreover, V_C has a double line frequency ripple due to single-phase inversion system. Fig. 4.16(b) shows voltage appearing across HB circuit $(S_1 - S_4)$, $V_{inv} = 144$ V and current drawn by HB circuit, $I_{inv} = 4.37$ A along with V_C and V_{dc}. It can be observed from Fig. 4.16(b) that I_{inv} has three current magnitudes because of power, shoot-through and zero states. Also, the low input voltage $(= V_{dc})$ is boosted $(= V_c)$ and appeared as equivalent input voltage $(= V_{inv})$ across the HB circuit $(S_1 - S_4)$ for AC output voltage (V_{ac}) as per the previous discussion. Figs. 4.16(c) and 4.16(d) show voltage stress experienced by power semiconductor devices. It can be noticed from Fig. 416(c) that $V_{Sa} = 144$ V and $V_{Sb} = 144$ V along with V_{inv} and V_{dc}. It is also clear that switches (S_a and S_b) have voltage stress which is equal to boosting ability of Type 1 SLC-ZSI. Fig. 4.16(d) shows $V_{D1} = -50$ V, $V_{D2} = -196$ V, $V_{D3} = -50$ V and $V_{Din} = -144$ V. The diode D_2 has higher voltage stress which is greater than boosting ability of Type 1 SLC-ZSI and diodes (D_1 and D_3) have lesser voltage stress as compared to other power semiconductor devices. Fig. 4.16(e) shows average current flowing through inductors (L_1 and L_2) as $I_{L1} = 1.34$ A and $I_{L2} = 1.34$ A along with gating pulse V_{GS5} of S_a and V_{dc}. The ON-time of S_a is the deciding factor of D_{st} of Type 1 SLC-ZSI. Also, L_1 and L_2 are charging and discharging at the same instant. Fig. 4.16(f) shows

V_{dc} = 48 V, V_C = 144 V, $V_{ac(rms)}$ = 81.33 V and $I_{ac(rms)}$ = 1.12 A for an *RL* load (R = 65.8 Ω and L = 100 mH). It can be noticed from Fig. 4.16(f) that I_{ac} has phase lag with respect to V_{ac} due to high load inductance.

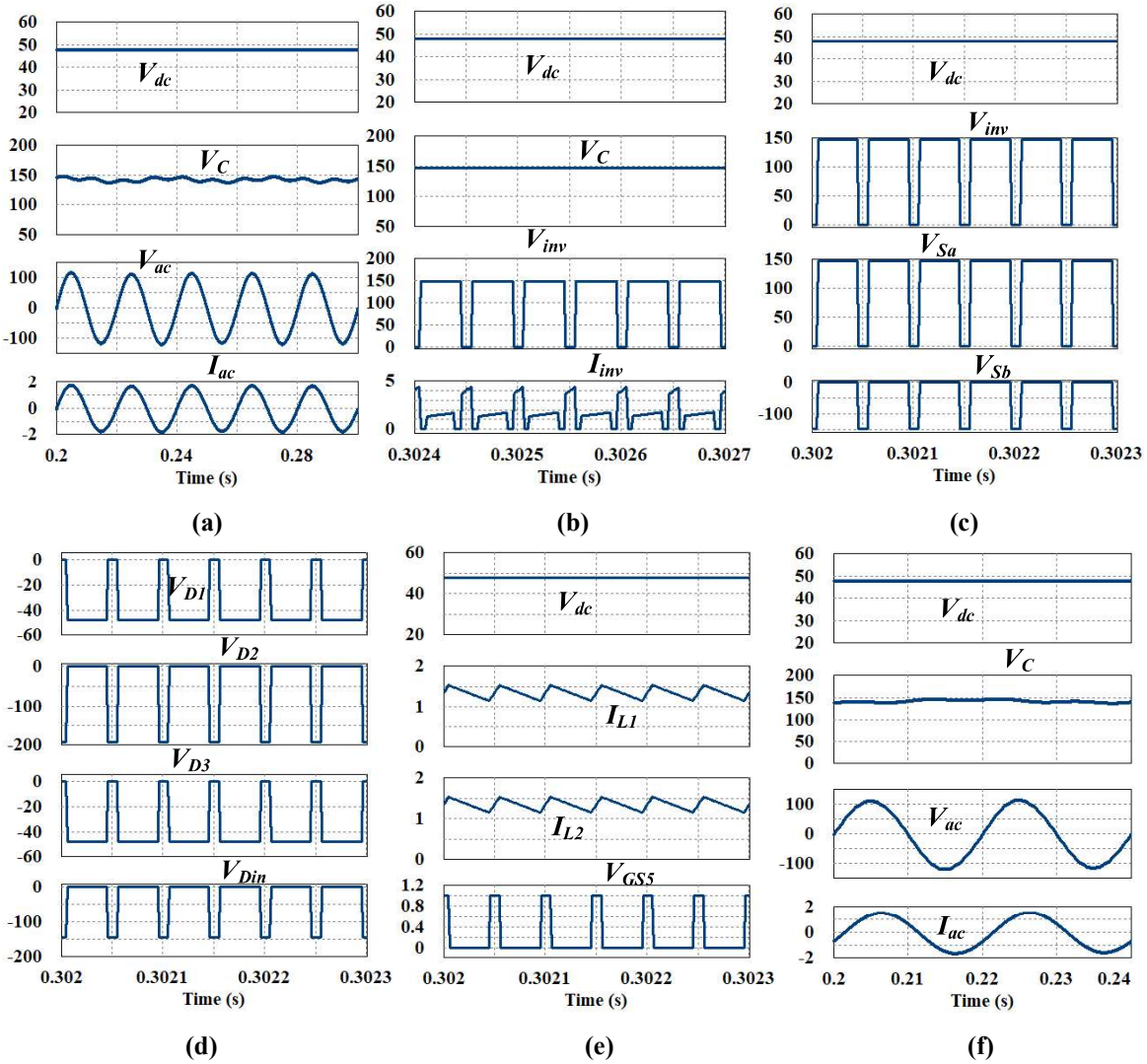


Fig. 4.16. Simulation results of Type 1 SLC-ZSI at D_{st} = 0.2 and M = 0.8 for R and RL loads **(a)** V_{dc}, V_C, V_{ac} and I_{ac} **(b)** V_{dc}, V_C, V_{inv} and I_{inv} **(c)** V_{dc}, V_{inv}, V_{Sa} and V_{Sb} **(d)** V_{D1}, V_{D2}, V_{D3} and V_{Din} **(e)** V_{dc}, I_{L1}, I_{L2} and V_{GS5} **(f)** V_{dc}, V_C, V_{ac} and I_{ac} at RL load (R = 65.8 Ω and L = 100 mH). **[Y-axis has voltage/current values, having units "V" or "A"]**

4.6.1.2 Simulation Results of Type 2 SLC-ZSI

Fig. 4.17 shows simulation results of Type 2 SLC-ZSI at $D_{st} = 0.2$ and $M = 0.8$. The performance of Type 2 SLC-ZSI is verified for R and RL loads. Figs. 4.17(a)-(e) show simulation results at R load and Fig. 4.17(f) shows simulation results at RL load. It can be found from Fig. 4.17(a) that voltage appearing across capacitor (C) $V_C = 171.41$ V, fundamental RMS AC quantities $V_{ac(rms)} = 96.97$ V and $I_{ac(rms)} = 1.03$ A for input voltage $V_{dc} = 48$ V. Although V_C of Type 2 SLC-ZSI also has double line frequency ripple, it has lesser in magnitude as compared to V_C of Type 1 SLC-ZSI. Fig. 4.17(b) shows voltage across the HB circuit ($S_1 - S_4$) of Type 2 SLC-ZSI as $V_{inv} = 171.41$ V and current drawn by HB circuit as $I_{inv} = 5.65$ A along with voltage across C_1, $V_{C1} = 59.6$ V and V_{dc}. It can be noticed from Fig. 4.17(b) that I_{inv} also has three different current profiles because of power, shoot-through and zero states as same as that of I_{inv} of Type 1 SLC-ZSI. Moreover, V_C is boosted voltage of Type 2 SLC-ZSI and appeared as V_{inv} for power and zero states of the HB circuit. Figs. 4.17(c) and 4.17(d) show voltage stress across power semiconductor devices. It can be observed from Fig. 4.17(c) that $V_{D2} = -279.1$ V, $V_{D3} = -64.1$ V and V_{Din} along with V_{dc}. The diode D_{in} has voltage stress which is equal to boosting ability and D_2 higher voltage stress among the diodes of Type 2 SLC-ZSI. Fig. 4.17(d) shows voltage stress across switches are $V_{Sa} = 171.4$ V, $V_{Sb} = 171.4$ V along with V_{inv} and V_{dc}. It is also evident that switches (S_a and S_b) have equal and opposite voltage values. It can be observed from Fig. 4.17(e) that average current flowing through inductors (L_1 and L_2) as $I_{L1} = 1.75$ A and $I_{L2} = 1.66$ A along with gating pulse V_{GS5} of S_a and V_{dc}. The ON duration of V_{GS5} is deciding factor of D_{st} of Type 2 SLC-ZSI. Moreover, L_1 and L_2 are charging during ON-state of S_a and discharging during OFF-state of S_a. It can be observed from Fig. 4.17(f) that $V_{dc} = 48$ V, $V_C = 171.4$ V, $V_{ac(rms)} = 97.42$ V and $I_{ac(rms)} = 1.34$ A for an RL load ($R = 65.8$ Ω and $L = 100$ mH). Also, the phase difference between I_{ac} and V_{ac} can be noticed from Fig. 4.17(f) due to high load inductance.

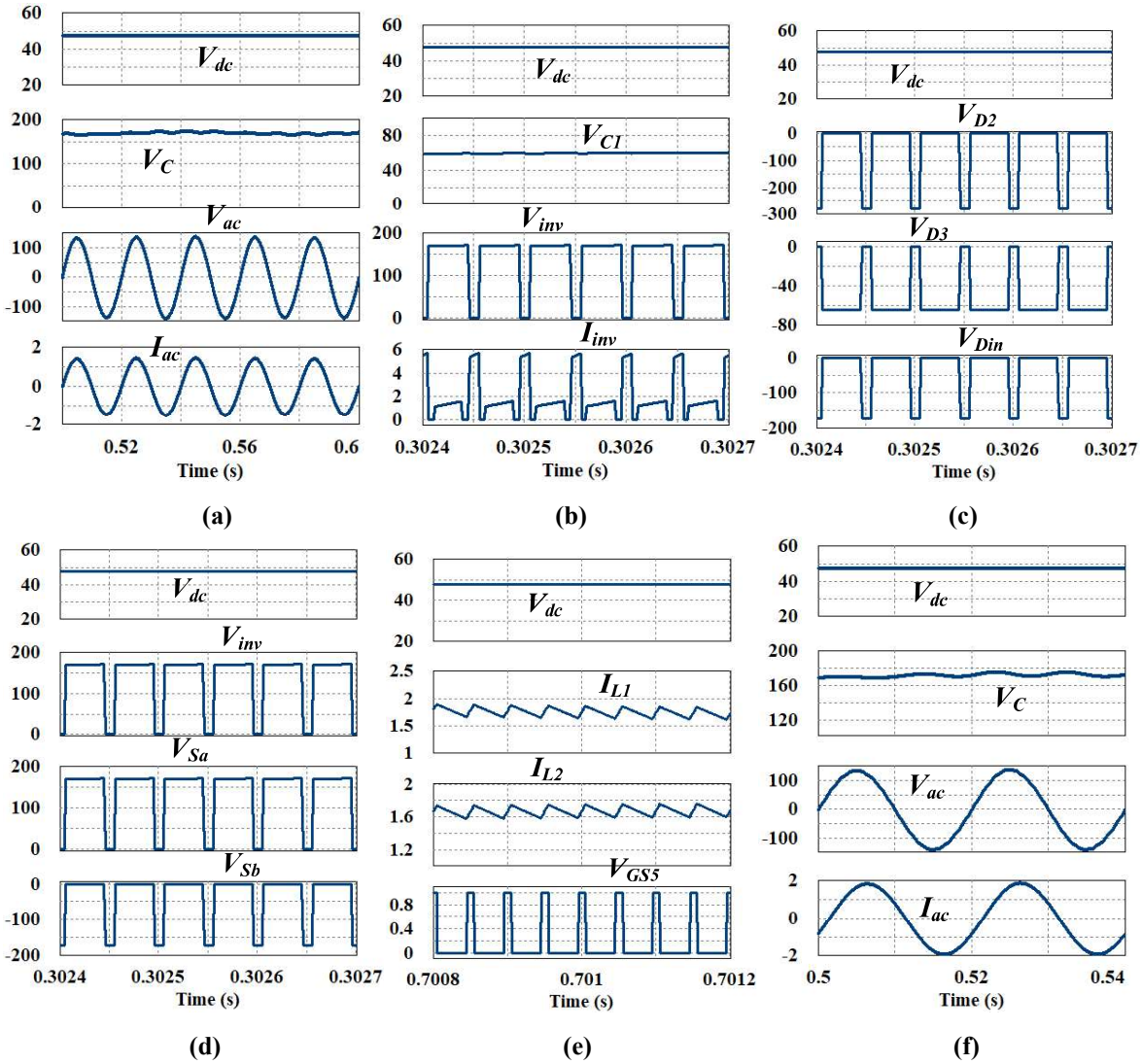


Fig. 4.17. Simulation results of Type 2 SLC-ZSI at $D_{st} = 0.2$ and $M = 0.8$ for R and RL loads **(a)** V_{dc}, V_C, V_{ac} and I_{ac} **(b)** V_{dc}, V_C, V_{inv} and I_{inv} **(c)** V_{dc}, V_{D2}, V_{D3} and V_{Din} **(d)** V_{dc}, V_{inv}, V_{Sa} and V_{Sb} **(e)** V_{dc}, I_{L1}, I_{L2} and V_{GS5} **(f)** V_{dc}, V_C, V_{ac} and I_{ac} at RL load ($R = 65.8\ \Omega$ and $L = 100$ mH). **[Y-axis has voltage/current values, having units "V" or "A"]**

4.6.2 Experimental Results of Proposed SLC-ZSIs

The performance of proposed SLC-ZSIs (Type 1 and Type 2) is verified through a laboratory prototype for the operating conditions given in Table 4.6. Fig. 4.18 shows a photograph of the experimental set-up of proposed SLC-ZSIs. The experimental gating signals of proposed SLC-ZSIs at $D_{st} = 0.2$ and $M = 0.8$ are shown in Fig. 4.19. It can be observed from Fig. 4.19(a) that shoot-through state (as same as that of ON period of G_{S5}) is inserted in G_{S3} and G_{S4} for modulation signal $V_m(t) > 0$. The ON period of G_{S5} is inserted in $G_{S1}$and G_{S2} for $V_m(t) < 0$. Further, G_{S6} of SLC-ZSIs is complementary of G_{S5}.

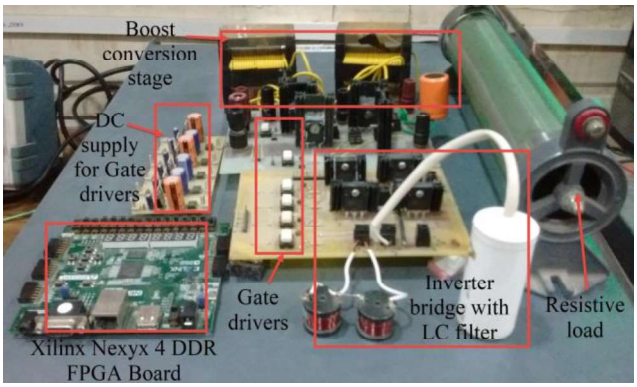
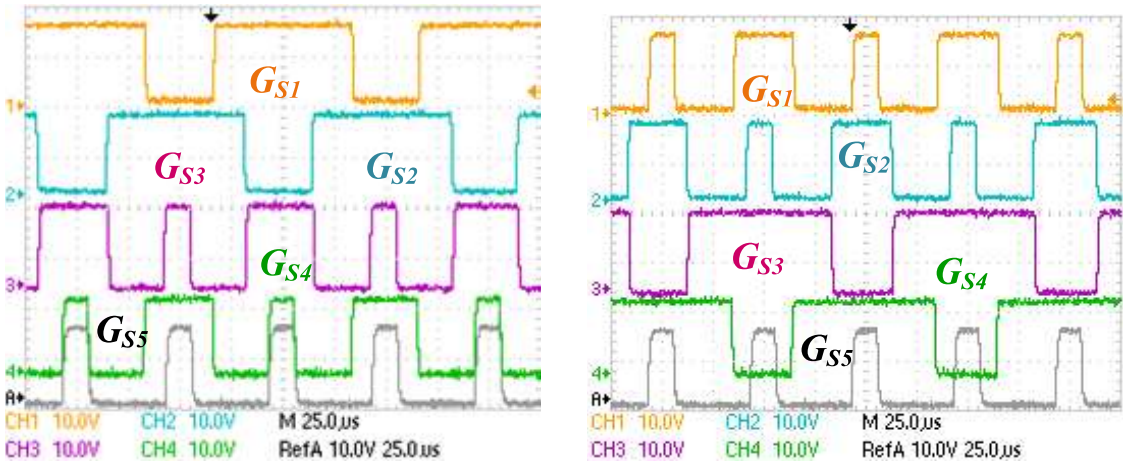


Fig. 4.18. A photograph of the experimental set-up of proposed SLC-ZSIs.



(a) **(b)**

Fig. 4.19. Experimental gating signals of proposed SLC-ZSIs at $D_{st} = 0.2$ and $M = 0.8$ **(a)** for modulation signal $V_m(t) > 0$ **(b)** for modulation signal $V_m(t) < 0$.

4.6.2.1 Experimental Results of Type 1 SLC-ZSI

Fig. 4.20 shows experimental results of Type 1 SLC-ZSI at $D_{st} = 0.2$ and $M = 0.8$. The performance of Type 1 SLC-ZSI is verified at R and RL loads and is shown in Fig. 4.20(a)-4.20(e) and Fig. 4.20(f) respectively. It can be observed from Fig. 4.20(a) that voltage across C, $V_C = 135.3$ V, fundamental AC output quantities $V_{ac(rms)} = 72.14$ V and $I_{ac(rms)} = 1.07$ A for $V_{dc} = 48$ V. The results obtained from Fig. 4.20(a) align with theoretical and simulation values at slightly reduced in magnitudes due to non-idealities of elements. Fig. 4.20(b) shows current and voltage experienced by the HB circuit of Type 1 SLC-ZSI are $I_{inv(pk)} = 4.42$ A and $V_{inv} = 135.8$ V along with V_C and V_{dc}. It can be observed from Fig.

4.20(b) that I_{inv} has three different current profiles because of power, shoot-through and zero states of Type 1 SLC-ZSI.

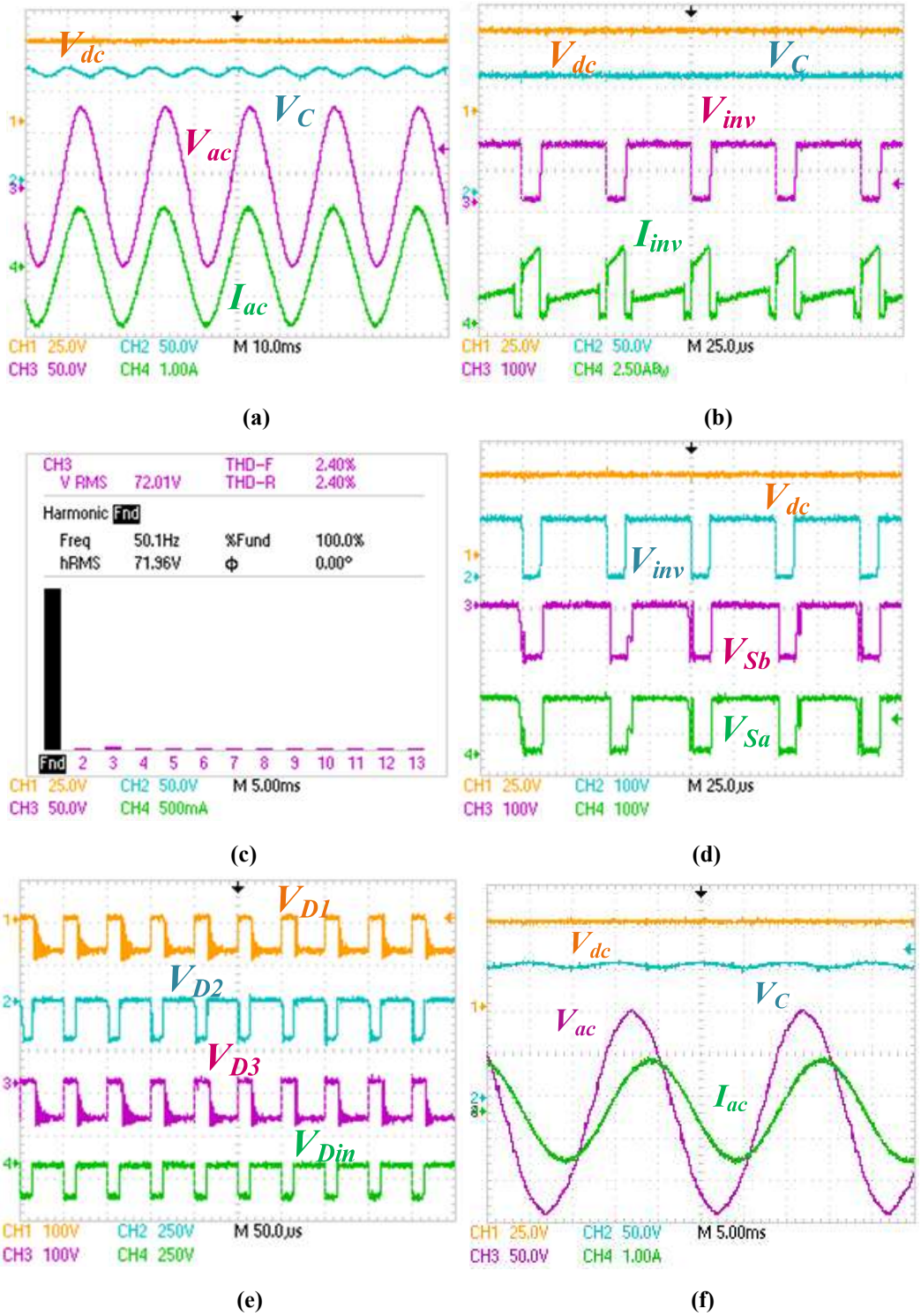


Fig. 4.20. Experimental results of Type 1 SLC-ZSI at $D_{st} = 0.2$ and $M = 0.8$ for R and RL loads (a) V_{dc}, V_C, V_{ac} and I_{ac} (b) V_{dc}, V_C, V_{inv} and I_{inv} (c) harmonic spectrum of V_{ac} (d) V_{dc}, V_{inv}, V_{Sa} and V_{Sb} (e) V_{D1}, V_{D2}, V_{D3} and V_{Din} (f) V_{dc}, V_C, V_{ac} and I_{ac} at RL load.

In the shoot-through state, HB switches ($S_1 - S_4$) experience high currents for a small period. Fig. 4.20(c) shows a harmonic spectrum of load voltage. It can be observed from Fig. 4.20(c) that total harmonic distortion (THD) of V_{ac} as 2.40%. Further, the THD can be reduced by fine-tuning of second-order low pass filter (L_f and C_f). It can be noticed from Fig. 4.20(d) that voltage stress experienced by switches are $V_{Sa} = 135.7$ V, $V_{Sb} = -135.6$ V and $V_{inv} = 135.8$ V. The equivalent DC voltage V_{inv} is appeared across switches ($S_1 - S_4$) based on their ON/OFF states. Fig. 4.20(e) shows voltages appeared across diodes as $V_{D1} = -53$ V, $V_{D2} = -191$ V, $V_{D3} = -53$ V and $V_{Din} = -141$ V. It can be observed from Fig. 4.20(e) that D_2 has higher voltage stress among all diodes. The diodes D_1 and D_3 have more ringing during transition from forward to reverse-biased state. However, it can be minimized by designing proper inductors (L_1 and L_2) and using snubber circuits. The performance of Type 1 SLC is also verified at RL load ($R = 65.8\ \Omega$ and $L = 100$ mH) and is shown in Fig. 4.20(f). It can be concluded from Fig. 4.20(f) that the Type 1 SLC-ZSI has reactive power capability. Further, there is no change in values of V_C and V_{ac} for RL load but a small change in the value of I_{ac} due to change in load impedance.

4.6.2.2 Experimental Results of Type 2 SLC-ZSI

The performance of Type 2 SLC-ZSI is verified through laboratory prototype at $D_{st} = 0.2$ and $M = 0.8$ and experimental results are shown in Figs. 4.21(a)-4.21(e) for R load and in Fig. 4.21(f) for RL load. It can be observed from Fig. 4.21(a) that voltage across C, $V_C = 164.3$ V, fundamental AC output voltage $V_{ac(rms)} = 86.4$ V and AC output current $I_{ac(rms)} = 0.94$ A for $V_{dc} = 48$ V. The capacitor voltage V_C has a double line frequency ripple because of a lossy power component of single-phase system. Fig. 4.21(b) shows voltage and currents experienced by HB are $V_{inv} = 164.3$ V and $I_{inv(pk)} = 5.48$ A along with V_C and V_{dc}. The current flowing through HB switches, I_{inv} has three current values because of power, shoot-through and zero states of Type 2 SLC-ZSI. Figs. 4.21(c) and 4.21(d) show voltages experienced by power semiconductor devices of Type 1 SLC-ZSI. It can be noticed from Fig. 4.21(c) that $V_{D2} = -264$ V, $V_{D3} = -72.3$ V and $V_{Din} = -171.6$ V for V_{dc}. The voltage across D_{in} is equal to boosting ability ($= V_{inv}$) of Type 2 SLC-ZSI and D_2 has higher voltage stress among other diodes. It can be found from Fig. 4.21(d) that voltage across switches are $V_{Sa} =$

164.4 V, $V_{Sb} = -164.6$ V and $V_{inv} = 164.3$ along with V_{dc}. Further, all switches of Type 2 SLC-ZSI have the same voltage stress.

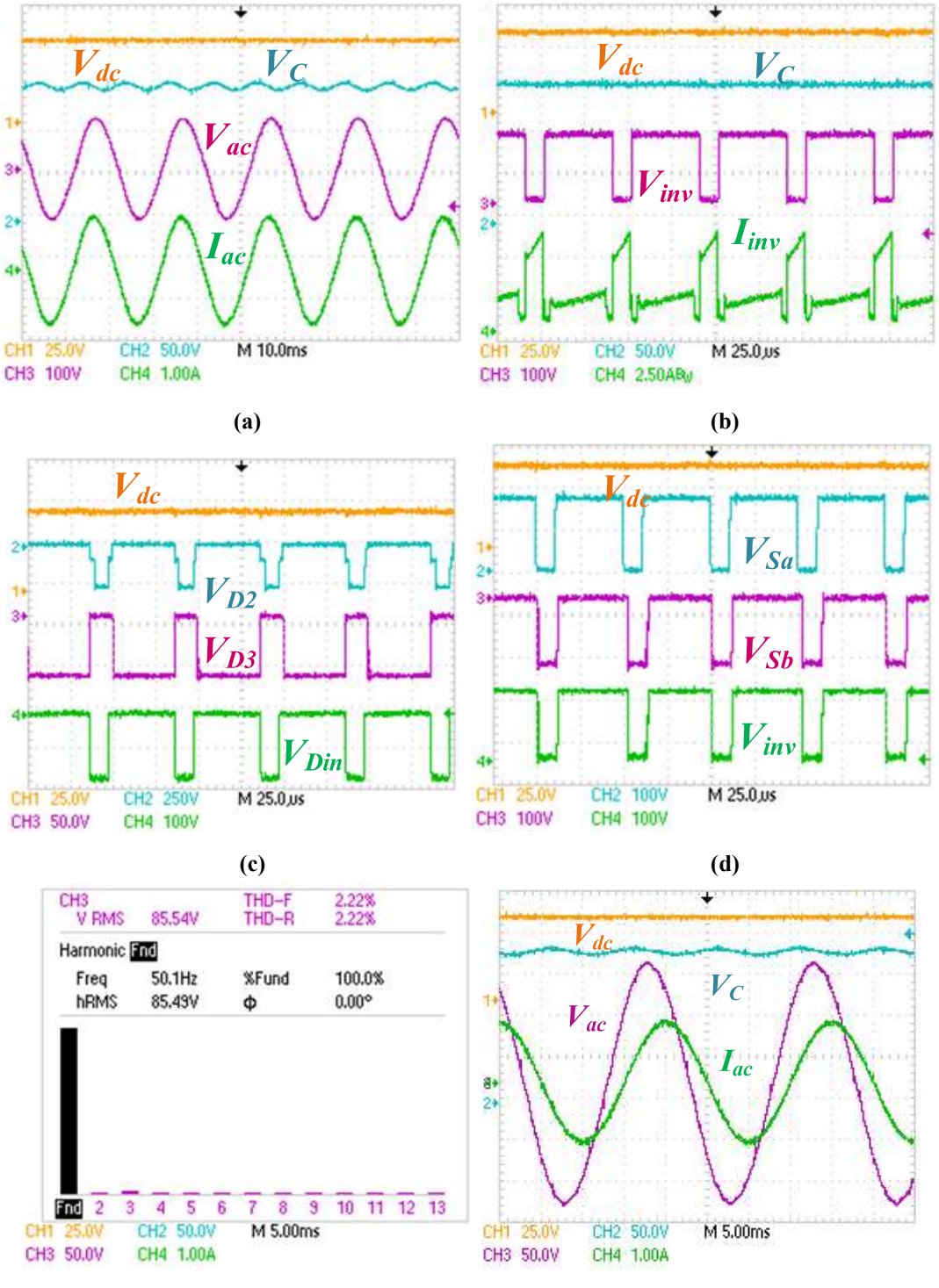


Fig. 4.21. Experimental results of Type 2 SLC-ZSI at $D_{st} = 0.2$ and $M = 0.8$ for R and RL loads **(a)** V_{dc}, V_C, V_{ac} and I_{ac} **(b)** V_{dc}, V_C, V_{inv} and I_{inv} **(c)** V_{dc}, V_{D2}, V_{D3} and V_{Din} **(d)** V_{dc}, V_{inv}, V_{Sa} and V_{Sb} **(e)** harmonic spectrum of V_{ac} **(f)** V_{dc}, V_C, V_{ac} and I_{ac} at RL load.

Fig. 4.21(e) shows harmonic spectrum of AC output voltage. It can be found from Fig. 4.21(e) that THD of V_{ac} as 2.22%. Further, the performance of Type 2 SLC-ZSI is verified for RL load (R = 65.8 Ω and L = 100 mH) at D_{st} = 0.2 and M = 0.8 and is shown in Fig. 4.21(f). Because of high load inductance, I_{ac} has phase lag with respect to V_{ac} and has variation in magnitude as compared to I_{ac} at R load.

4.6.3 Power Loss Calculations and Efficiency Variation of Proposed SLC-ZSIs

The power losses in elements of proposed SLC-ZSIs are determined which consist of switching and conduction losses of switches, reverse recovery (switching) and conduction losses of diodes, conduction losses in capacitors because of ESRs and conduction losses in inductors due to DCRs [106]-[112].

(a) Power Losses in Switches of Two SLC-ZSIs

Although the SLC-ZSIs are operated in three states (power, shoot-through, and zero states), the losses in zero states are neglected. The switching losses in the HB switches ($S_1 - S_4$) of SLC-ZSIs are calculated during PS and STS. The average switching power losses in the HB switches of SLC-ZSIs during PS, $P_{switc\_HB\_PS}$ are determined from the equation given in (4.37).

$$P_{switc\_HB\_PS} = \frac{4*f_{ef}*(E_{on}+E_{off})*V_{inv}*I_{PS}}{V_{ref}*I_{ref}} \tag{4.37}$$

where E_{on} and E_{off} are switching ON and OFF energies of switches at the reference voltage V_{ref} and current I_{ref} (can be known from manufacturer's datasheet of switches), I_{PS} is current flowing through HB switches during the PS, V_{inv} is the voltage appearing across HB switches and f_{ef} is the effective switching frequency of HB switches. The f_{ef} can be defined as $\frac{f_s}{f_{line}}$, where f_s is the switching frequency and f_{line} is the frequency of AC output of SLC-ZSIs.

The required current and voltage (I_{PS} and V_{inv}) expressions for calculating $P_{switc\_HB\_PS}$ of Type 1 SLC-ZSI are given in (4.38).

$$\left.\begin{aligned} V_{inv} &= \frac{1+D_{st}}{1-3D_{st}} V_{dc} \\ I_{PS} &= \frac{1-3D_{st}}{1+D_{st}} I_{dc} \end{aligned}\right\} \tag{4.38}$$

Similarly, the required expressions of I_{PS} and V_{inv} for determining $P_{switc\_HB\_PS}$ of Type 2 SLC-ZSI are given in (4.39).

$$\left.\begin{aligned} V_{inv} &= \frac{1}{1-4D_{st}+2{D_{st}}^2} V_{dc} \\ I_{PS} &= (1-4D_{st}+2{D_{st}}^2) I_{dc} \end{aligned}\right\} \tag{4.39}$$

During STS, each switch is forced ON either in positive half or negative half of AC output. Also, they are forced ON the same number of times as they are ON in PS in half of wave. As a result, the switching frequency becomes half of f_s. The current flowing through HB switches is I_{STS}. The average switching losses in HB switches of SLC-ZSIs during STS, $P_{switc\_HB\_STS}$ are determined from the equation given in (4.40).

$$P_{switc\_HB\_STS} = \frac{4*\frac{f_s}{2}*(E_{on}+E_{off})*V_{inv}*I_{STS}}{V_{ref}*I_{ref}} \tag{4.40}$$

where I_{STS} is the current flowing through HB switches during STS and remaining parameters of (4.40) are as same as discussed earlier. Further, V_{inv} can be considered from (4.38) and (4.39) for calculating $P_{switc\_HB\_STS}$ of SLC-ZSIs.

The required expression of I_{STS} for determining $P_{switc\_HB\_STS}$ of Type 1 SLC-ZSI is given in (4.41).

$$I_{STS} = I_{L1} + I_{L2} \tag{4.41}$$

Similarly, the required expression of I_{STS} for determining $P_{switc\_HB\_STS}$ of Type 2 SLC-ZSI is given in (4.42).

$$I_{STS} = I_{L1} + I_{L2} \tag{4.42}$$

Along with the HB switches, the SLC-ZSIs have two additional switches (S_a and S_b). The two switches are turned-on during shoot-through operation and turned-off during non-shoot-through operation. As discussed earlier that the non-shoot-through operation consists of PS and ZS. The switching losses in two switches (S_a and S_b) of SLC-ZSIs are determined from the equation given in (4.43).

$$\left.\begin{aligned} P_{switc\_Sa} &= \frac{2*f_s*(E_{on}+E_{off})*V_{Sa}*I_{Sa}}{V_{ref}*I_{ref}} \\ P_{switc\_Sb} &= \frac{2*f_s*(E_{on}+E_{off})*V_{Sb}*I_{Sb}}{V_{ref}*I_{ref}} \end{aligned}\right\} \tag{4.43}$$

where V_{Sa} and V_{Sb} are voltages across two switches, I_{Sa} and I_{Sb} are currents flowing through two switches and remaining parameters are as same as described earlier.

The required current and voltage expressions for calculating switching losses (P_{switc_Sa} and P_{switc_Sb}) of Type 1 SLC-ZSI are given in (4.44).

$$\left.\begin{aligned} V_{Sa} = V_{Sb} &= \frac{1+D_{st}}{1-3D_{st}} V_{dc} \\ I_{Sa} &= \frac{1-D_{st}}{1-2D_{st}} I_{inv} \\ I_{Sb} &= \frac{D_{st}}{1-2D_{st}} I_{inv} \end{aligned}\right\} \tag{4.44}$$

Similarly, the required current and voltage expressions for calculating switching losses (P_{switc_Sa} and P_{switc_Sb}) of Type 2 SLC-ZSI are given in (4.45).

$$\left.\begin{aligned} V_{Sa} = V_{Sb} &= \frac{V_{dc}}{(1-4D_{st}+2{D_{st}}^2)} \\ I_{Sa} &= \frac{(2-4D_{st}+2{D_{st}}^2) I_{inv}}{(1-4D_{st}+2{D_{st}}^2)} \\ I_{Sb} &= \frac{(2D_{st}-{D_{st}}^2) I_{inv}}{(1-4D_{st}+2{D_{st}}^2)} \end{aligned}\right\} \tag{4.45}$$

The conduction losses in switches (S_a, S_b and $S_1 - S_4$) of SLC-ZSIS during PS and STS are determined from the equation given in (4.46).

$$P_{cond\_S} = {I^2}_{S\_rms} r_{DS(on)} + I_{S\_avg} V_{DS(on)} \tag{4.46}$$

where $r_{DS(on)}$ is on-state resistance of switches and $V_{DS(on)}$ is on-state saturation voltage of switches. Also, $r_{DS(on)}$and $V_{DS(on)}$ are can be known from manufacturer's datasheet of switches.

The average and RMS currents for calculating P_{cond_S} of SLC-ZSIs during STS are determined from the equation given in (4.47).

$$\left.\begin{aligned} I_{S\_avg\_STS} &= \frac{1}{T_s}\int_0^{T_s} (i_S) * \frac{D_{st}}{2}\, dt \\ I_{S\_rms\_STS} &= \left(\frac{1}{T_s}\int_0^{T_s} (i_S)^2 * \frac{D_{st}}{2}\, dt\right)^{\frac{1}{2}} \end{aligned}\right\} \tag{4.47}$$

The average and RMS currents for calculating P_{cond_S} of SLC-ZSIs during PS are determined from the equation given in (4.48).

$$\left.\begin{aligned} I_{S\_avg\_PS} &= \frac{1}{T_s}\int_0^{T_s} i_S\, d(t) \\ I_{S\_rms\_PS} &= \left(\frac{1}{T_s}\int_0^{T_s} {i^2}_S\, d(t)\right)^{\frac{1}{2}} \end{aligned}\right\} \tag{4.48}$$

(b) Power Losses in Diodes of Two SLC-ZSIs

The power losses in diodes of SLC-ZSIs are occurred due to conduction and switching action of diodes and are calculated as discussed here. The conduction losses in diodes of two SLC-ZSIs, P_{cond_D} are determined from the expression given in (4.49).

$$P_{cond\_D} = V_{FD} * I_{D\_avg} + I^2{}_{D\_rms} r_D \tag{4.49}$$

where V_{FD} is forward voltage drop and r_D is forward resistance of diodes, I_{D_avg} and I_{D_rms} are average and RMS current of diodes. Further, the values of I_{D_avg} and I_{D_rms} are calculated from the equation given in (4.50).

$$\left.\begin{aligned} I_{D\_avg} &= \frac{1}{T_s}\int_0^{T_s}(i_D)dt \\ I_{D\_rms} &= \left(\frac{1}{T_s}\int_0^{T_s}(i_D)^2 dt\right)^{\frac{1}{2}} \end{aligned}\right\} \tag{4.50}$$

The required currents for calculating I_{D_avg} and I_{D_rms} of Type 1 SLC-ZSI are given in (4.51).

$$\left.\begin{aligned} i_{Din} &= \frac{(1-D_{st})I_{inv}}{(2-2D_{st})} \\ i_{D1} &= \frac{(1-D_{st})I_{inv}}{(2-2D_{st})} \\ i_{D2} &= \frac{(1-D_{st})I_{inv}}{(2-2D_{st})} \\ i_{D3} &= \frac{(1-D_{st})I_{inv}}{(2-2D_{st})} \end{aligned}\right\} \tag{4.51}$$

Similarly, the required currents for calculating I_{D_avg} and I_{D_rms} of Type 2 SLC-ZSI are given in (4.52).

$$\left.\begin{aligned} i_{Din} &= \frac{(1-2D_{st}+D_{st}{}^2)I_{inv}}{(1-4D_{st}+2D_{st}{}^2)} \\ i_{D2} &= \frac{(1-D_{st})I_{inv}}{(1-4D_{st}+2D_{st}{}^2)} \\ i_{D3} &= \frac{(1-D_{st})I_{inv}}{(1-4D_{st}+2D_{st}{}^2)} \end{aligned}\right\} \tag{4.52}$$

The switching losses in diodes of two SLC-ZSIs, P_{switc_D} are obtained from the expression given in (4.53)

$$P_{switc\_D} = 2 * f_s * Q_{rr} * V_D \tag{4.53}$$

where Q_{rr} is reverse recovery charge of diodes (can be known from manufacturer's datasheet of diodes) and V_D is voltage across diodes during their reverse biased condition.

The required voltages for calculating P_{switc_D} of Type 1 SLC-ZSI are given in (4.54).

$$\left.\begin{aligned} V_{Din} &= \frac{(1+D_{st})}{1-3D_{st}}V_{dc} \\ V_{D1} = V_{D3} &= \frac{2D_{st}}{1-3D_{st}}V_{dc} \\ V_{D2} &= \frac{2(1-D_{st})}{1-3D_{st}}V_{dc} \end{aligned}\right\} \tag{4.54}$$

Similarly, the required voltages for calculating P_{switc_D} of Type 2 SLC-ZSI are given in (4.55).

$$\left.\begin{aligned} V_{Din} &= \frac{V_{dc}}{(1-4D_{st}+2{D_{st}}^2)} \\ V_{D2} &= \frac{(2-2D_{st})V_{dc}}{(1-4D_{st}+2{D_{st}}^2)} \\ V_{D3} &= \frac{(2D_{st})V_{dc}}{(1-4D_{st}+2{D_{st}}^2)} \end{aligned}\right\} \tag{4.55}$$

(c) Power Losses in Inductors of Two SLC-ZSIs

The power losses in inductors of two SLC-ZSIs, P_L are occurred because of DCR of inductance and are determined from the equation given in (4.55=6).

$$P_L = I_{L\_rms}^2 r_{DCR} \tag{4.56}$$

where r_{DCR} is DCR of inductors which can be measured by LCR meter and I_{L_rms} is RMS inductor current. The value of I_{L_rms} is obtained from the equation given in (4.57).

$$I_{L\_rms} = \left(\frac{1}{T_s}\int_0^{T_s}(i_L)^2 dt\right)^{\frac{1}{2}} \tag{4.57}$$

The required inductor voltages for calculating P_L of Type 1 SLC-ZSI are given in (4.58) and (4.59).

$$v_{L1} = \left\{\begin{matrix} v_{dc}+v_C & 0 \le t \le D_{st}T_s & ;STS \\ \frac{1}{2}(v_{dc}-v_C) & (1-D_{st})T_s \le t \le T_s & ;nSTS \end{matrix}\right\} \tag{4.58}$$

$$v_{L2} = \left\{\begin{matrix} v_{dc}+v_C & 0 \le t \le D_{st}T_s & ;STS \\ \frac{1}{2}(v_{dc}-v_C) & (1-D_{st})T_s \le t \le T_s & ;nSTS \end{matrix}\right\} \tag{4.59}$$

Similarly, the required inductor voltages for calculating P_L of Type 2 SLC-ZSI are given in (4.60) and (4.61).

$$v_{L1} = \left\{\begin{matrix} v_{dc}+v_C & 0 \le t \le D_{st}T_s & ;STS \\ -v_{C1} & (1-D_{st})T_s \le t \le T_s & ;nSTS \end{matrix}\right\} \tag{4.60}$$

$$v_{L2} = \left\{\begin{matrix} v_{dc}+v_C+v_{C1} & 0 \le t \le D_{st}T_s & ;STS \\ v_{dc}+v_{C1}+v_C & (1-D_{st})T_s \le t \le T_s & ;nSTS \end{matrix}\right\} \tag{4.61}$$

(d) Power Losses in Capacitors of Two SLC-ZSIs

The power losses in capacitors of two SLC-ZSIs, P_C are occurred due to ESR of capacitance and are determined from the equation given in (4.62).

$$P_C = \frac{1}{T_s}\int_0^{T_s} i_C^2 r_{ESR} dt \tag{4.62}$$

The required currents for calculating P_C of Type 1 SLC-ZSI are given in (4.63).

$$i_C = \begin{cases} -i_{dc} & 0 \le t \le D_{st}T_s \quad ; STS \\ i_{dc} - i_{inv} & (1-D_{st})T_s \le t \le T_s \quad ; nSTS \end{cases} \tag{4.63}$$

Similarly, the required currents for calculating P_C of Type 2 SLC-ZSI are given in (4.64) and (4.65).

$$i_C = \begin{cases} -i_{L1} - i_{L2} & 0 \le t \le D_{st}T_s \quad ; STS \\ i_{L2} - i_{inv} & (1-D_{st})T_s \le t \le T_s \quad ; nSTS \end{cases} \tag{4.64}$$

$$i_{C1} = \begin{cases} -i_{L2} & 0 \le t \le D_{st}T_s \quad ; STS \\ i_{L1} - i_{L2} & (1-D_{st})T_s \le t \le T_s \quad ; nSTS \end{cases} \tag{4.65}$$

Based on the above power loss calculations, power losses in various elements of proposed SLC-ZSIs are calculated at rated load power and are shown in Fig. 4.22 as a percentage of total power losses. The considered non-ideal parameters of elements for power loss calculations are $r_{DCR} = 0.2\ \Omega$, $r_{ESR} = 0.035\ \Omega$, $V_{DS(on)} = 1.1$ V, $r_{DS(on)} = 0.15\ \Omega$, $V_{FD} = 0.8$ V and $r_{FD} = 0.1\ \Omega$. It can be observed from Fig. 4.22 that switches have more power losses as compared to other elements of proposed SLC-ZSIs. Further, efficiency variation of the proposed SLC-ZSIs is carried out at different loading conditions and is shown in Fig. 4.23. It can be observed from Fig. 4.23 that the Type 1 SLC-ZSI has maximum efficiency as 89.64% at a load power of 81.6 W and the Type 2 SLC-ZSI has maximum efficiency as 90.34% at a load power of 79.96 W.

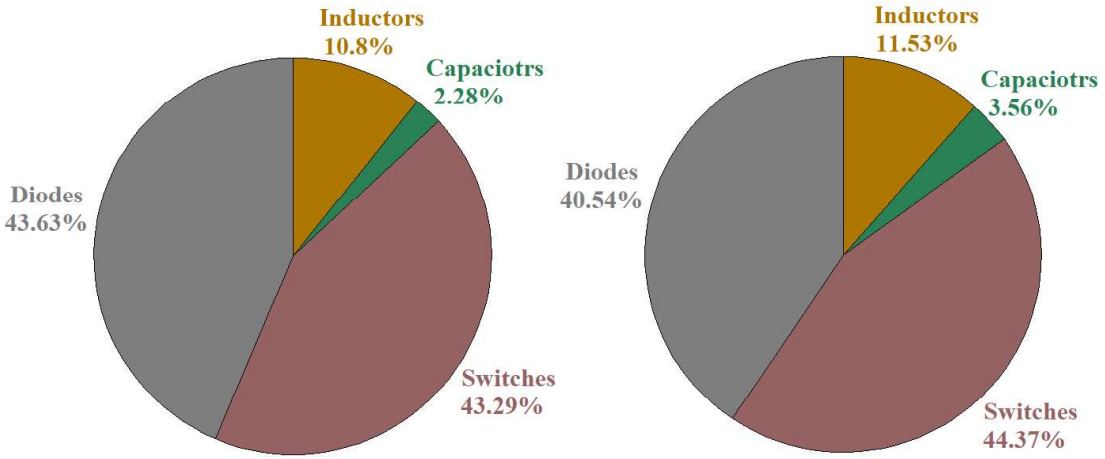


Fig. 4.22. Power loss distribution among the elements of proposed SLC-ZSIs **(a)** power losses in the elements of Type 1 SLC-ZSI **(b)** power losses in the elements of Type 2 SLC-ZSI.

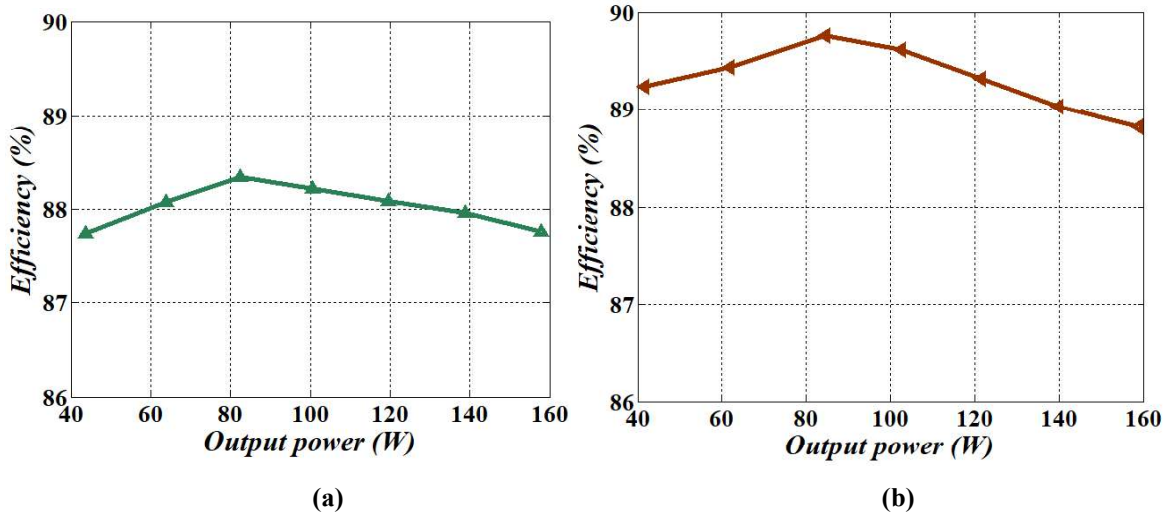


Fig. 4.23. Efficiency variation of proposed SLC-ZSIs at different loading conditions **(a)** efficiency variation in Type 1 SLC-ZSI **(b)** efficiency variation in Type 2 SLC-ZSI.

4.7 Summary

This chapter has been presented two single-phase SLC-ZSIs (Type 1 and Type 2) for a single-stage AC system operated by low voltage sources. The SLC-ZSIs high voltage gain at low values of D_{st} with reduced elements as compared to some reported SL based ZSIs. As D_{st} is low, M can be high (close to unity), which results in high gain inversion of SLC-ZSIs at permissible THD. Due to lesser number of elements, the volume of overall system is reduced and resulting in better power density as compared to reported ZSIs. Detailed mathematical modeling of proposed SLC-ZSIs is carried out based on developed switching logic. A

comparison is given among proposed SLC-ZSIs and reported ZSIs in terms of number of elements, voltage gain, current and voltage stresses on various elements. It can be concluded from the comparison that the proposed SLC-ZSIs have high voltage gain using lesser number of elements and have moderate voltage/current stresses on the elements. The obtained simulation and experimental results are aligned with the theoretical analysis of SLC-ZSIs. From the harmonic spectrum of SLC-ZSIs, it can be concluded that THD of AC output of SLC-ZSIs is within limits. Further, the effectiveness of SLC-ZSIs has been verified through power loss calculations and efficiency variation.

Although the proposed SLC-ZSIs are well suited for a single-stage AC system due to their merits as compared to reported SL based ZSIs, they also have a few demerits such as moderate ripple in input current and moderate voltage/current stresses on the elements. To take care of these issues, chapter 5 presents an enhanced high gain switched LC Z-source inverter (eSLC-ZSI) which is an improved version of Type 2 SLC-ZSI.