

1.1 Thesis Abstract

As the world progresses toward next-generation computing, achieving faster data processing and higher integration density while maintaining power efficiency remains challenging. Device scaling has been utilized in the complementary metal-oxide-semiconductor (CMOS) technology to improve performance, such as dynamic power dissipation, chip area, and delay. However, further miniaturization of devices introduces short-channel effects, resulting in substantial static leakage power. Consequently, researchers are seeking innovative alternatives to conventional CMOS technology that can overcome these scaling limitations to enhance computational performance.

Spintronics is an emerging field in modern memory and computing technology that utilizes the spin of electrons and their associated magnetic moments to store information. Unlike conventional CMOS technology, which relies on the charge of electrons that degrades due to static leakage current. Spintronics involves the magnetization state to represent binary data that can be retained almost indefinitely without a continuous power supply in spintronics-based circuits and memory, offering non-volatility. Furthermore, the magnetization state can be switched in the low energy budget through the spin transfer torque (STT) switching mechanism. Due to these advancements, the researchers have started to focus on the development of a spintronics device such as magnetic tunnel junction (MTJ) based computing architectures, which offer negligible static leakage, non-volatility, faster data processing, and higher integration density.

This thesis work pursues two main objectives: device modeling and logic circuit design for spin-based computing. Firstly, we developed a SPICE compatible STT-MTJ compact model, accurately capturing both tunnel magnetoresistance (TMR) and tunnel

magnetocapacitance (TMC) phenomena, which are essential for simulating next-generation spin-based devices and circuits. Further, we also develop an advanced micromagnetic simulation framework based on the non-equilibrium Green's function (NEGF) formalism to analyze the STT switching behaviour in MTJ devices. Secondly, we designed a novel STT-MTJ-based non-volatile latch with an auto-write termination (AWT) circuit, which eliminates redundant writing of the MTJ and stops the write operation once it is complete. This design enhances reliability, reduces area, and minimizes power dissipation. The simulations presented in this thesis were conducted using NGSPICE, HSPICE, Magic IC Layout, and OOMMF simulation tools. The thesis is organized into five chapters as follows:

Chapter 1 introduces the spintronics device, specifically the MTJ, highlighting its advantages in next-generation memory and computing technology. This chapter includes details on the remarkable properties of the MTJ device and explains its basic physics, including key properties such as MTJ structure, magnetic anisotropy, TMR, TMC, and STT switching techniques. Additionally, the chapter reviews the literature on device modeling and logic circuits, including compact modeling of MTJs, micromagnetic simulation frameworks that analyze the STT switching behaviour in MTJ devices, and hybrid CMOS/MTJ circuits such as non-volatile latches, flip-flops, and AWT circuits. At the end of the chapter, a brief summary is presented to support the formation of the problem statement for the thesis work.

In the next chapter, **Chapter 2**, we address the limitations of existing compact MTJ models that emulate the TMR effect and magnetization dynamics but lack the TMC effect. This chapter introduces a SPICE-based STT-MTJ compact model that incorporates both TMR and TMC effects. The voltage-induced TMC effect is modeled using a combination of the Debye-Fröhlich model, Zhang-sigmoid theory, parabolic barrier approximation, and

spin-dependent drift-diffusion model, which accurately emulates magnetocapacitance behaviour of MTJ device across different frequencies. The proposed model is validated through HSPICE simulations, showing good agreement with experimental data.

Chapter 3 presents an advanced micromagnetic simulation framework utilizing the NEGF formalism for modeling STT-MTJ devices. This simulation framework combines the TCL-based NEGF model for spin transport with the micromagnetic simulations for magnetization dynamics, enabling comprehensive analyses of the STT switching behaviour in MTJs.

In the next chapter, *Chapter 4*, we propose an STT-MTJ-based non-volatile latch with an AWT feature. This latch has a simple structure, improved stability, higher speed, and seamless integration with CMOS logic styles. It eliminates the need for an additional write driver circuit, resulting in a smaller footprint during MTJ writing. Consequently, the proposed latch consumes less power compared to previous designs, using fewer transistors for write operations and logic implementation. The AWT circuit continuously monitors the write operation, prevents redundant MTJ writing, and removes excessive write current flow, thereby saving power.

In *Chapter 5*, the thesis is concluded while highlighting the significant contributions and a summary of the results achieved in this research work. This chapter also contains the future scope of the thesis work.

1.2 Introduction

Spintronics is an emerging field in modern memory and computing technology that utilizes the spin of electrons and allied magnetic moments to store information. The conventional CMOS technology relies on the charge stored in capacitive nodes that depreciates due to static leakage current [1], [2], [3], [4], [5], [6], [7], [8], [9], [10]. Modern spin-based devices