Chapter 3

A Three-Level Dual-Output Active Neutral-Point Clamped (ANPC) Converter

3.1 Introduction

In response to the above literature, region of operation, DC-link capacitor voltage balancing, and compactness are the main concerns for a multilevel multi-output converter. This article presents a three-level dual output active neutral-point clamped (TLDO-ANPC) converter topology with a complete operating region and a simple PWM technique for capacitor voltage balancing. The output voltages can be independently controlled regardless of amplitude, frequency, and phase angle (phase difference).

3.2 Three-level dual output active neutral point clamped (TLDO-ANPC) converter

3.2.1 Topology of TLDO-ANPC converter

The three-phase circuit configuration of the proposed TLDO-ANPC converter is shown in Fig. 3.1. The schematic of the proposed topology looks similar to the five-level ANPC, which is a single-output converter, but the proposed topology is a dual-output three-level converter. TLDO-ANPC produces two sets of output voltages and offers complete

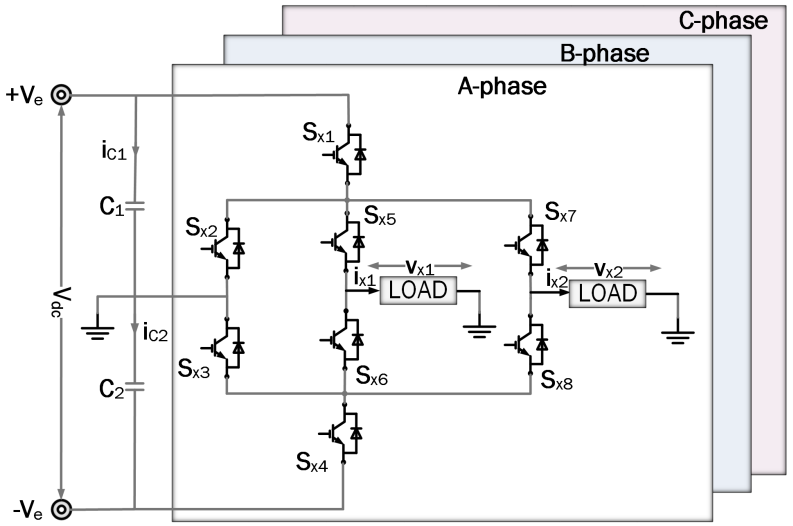


FIGURE 3.1: Proposed three-level dual-output ANPC converter.

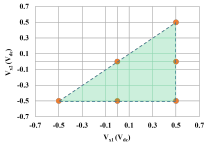
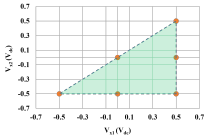
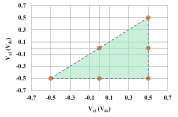
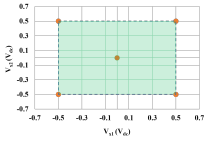
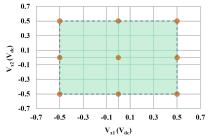
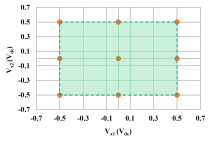
independent control of its output terminals during healthy operating conditions. The single phase TLDO-ANPC converter consists of eight switches (S_{x1} to S_{x8}) and two DC-link capacitors (C_1, C_2). Out of these eight switches, S_x1, S_{x2}, S_{x3} and S_{x4} are inner switches and S_{x5}, S_{x6}, S_{x7}, and S_{x8} are outer switches per leg. Where "x" mentioned in the following part is all x $\in$ {A, B, and C}.

The DC-link neutral point is connected to the midpoint of switches S_{x2} and S_{x3}. The output voltages v_{x1} and v_{x2} are the two distinct phase voltages obtained from the combination of inner and outer switches with respect to the neutral point. The two output load currents are the i_{x1} and i_{x2}.

Similar to NPC-DO in [26], TLDO-ANPC provides a full region of operation with higher switching states, improving redundancy and maximum DC-bus utilization without enforcing limitations on the region of operation.

For providing dual output per leg, the proposed TLDO-ANPC converter requires eight switches per leg compared to the conventional three-level ANPC (CTL-ANPC) [59, 60, 62] converter, which requires 12 switches. For driving a six-phase machine or two three-phase loads, CTL-ANPC requires 36 switches [62, 63], while TLDO-ANPC requires only 24 switches. CTL-ANPC and TLDO-ANPC allow the neutral current to be controlled, enabling the losses to be evenly distributed among devices. Table 3.1 lists the number of switches, devices, and operating region of TLDO-ANPC with three-level dual output topologies. Compared to other topologies, TLDO-ANPC provides advantages in terms of region of operation, cost, and volume and has zero clamping diodes.

TABLE 3.1: Comparison of Single-Phase Dual-Output Three-level Topologies

Topologies	NPP[64],[65]	DO-NPC-TLI [66]	DO-T-TLC[67, 53]	NPC-DO [68]	Dual CTL-ANPC [30, 31, 32]	Proposed
Type of Converter	ZSI/VSI	VSI	VSI	VSI	VSI	VSI
No. of Switches	21	20	18	18	36	24
No. of diodes	0	12	0	6	0	0
Capacitors*	0	0	0	0	0	0
Total Devices (active + passive)	21	32	18	24	36	24
Maximum voltage stress	V_{dc}	$V_{dc}/2$	V_{dc}	V_{dc}	$V_{dc}/2$	V_{dc}
Boundary Region						

*Not Considering DC-link Capacitor

3.2.2 State of Operation

The output voltages at two terminals of TLDO-ANPC are : -V_{dc}/2, 0, and V_{dc}/2. The phase output voltage across two AC (RL) loads are v_{x1} and v_{x2}. A few operating states for the single-phase configuration of the proposed topology are shown in Fig. 3.2(a)–(c) and are described as follows.

3.2.2.1 State of Operation 1

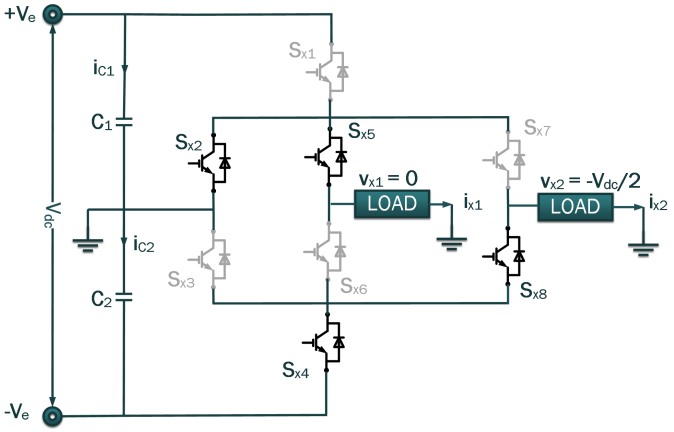
In this state, switches S_{x2}, S_{x4}, S_{x5} and S_{x8} are ON. The current flows between the DC-link and the loads, as shown in Fig. 3.2(a). In this stage, the terminal voltages v_{x1} and v_{x2} are 0 and -V_{dc}/2, and the blocking voltages of switches S_{x1}, S_{x3}, S_{x6} and S_{x7} is V_{dc}/2. C_1 maintains its previous voltage, and C_2 charges.

3.2.2.2 State of Operation 2

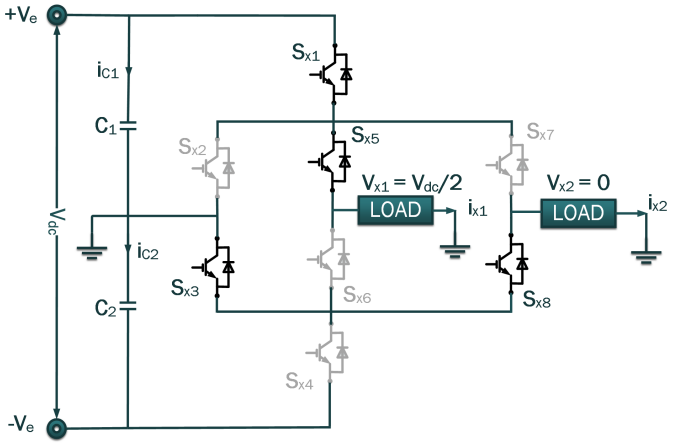
In this state, switches S_{x1}, S_{x3}, S_{x5} and S_{x8} are ON. The current flows between the DC-link and loads, as shown in Fig. 3.2(b). In this interval, the output voltages v_{x1} and v_{x2} are V_{dc}/2 and 0 and the voltage stress across switches S_{x2}, S_{x4}, S_{x6} and S_{x7} is V_{dc}/2. C_1 discharges and C_2 to maintain its previous voltage during this state.

3.2.2.3 State of Operation 3

Switches S_{x1}, S_{x4}, S_{x5} and S_{x8} are ON in this state. Fig. 3.2(c) shows the current flow between the DC-link and loads. At this time, the output voltages v_{x1} and v_{x2} are V_{dc}/2 and -V_{dc}/2, and the voltage stress across switches S_{x2}, S_{x3}, S_{x6} and S_{x7} are V_{dc}/2, V_{dc}/2, V_{dc} and V_{dc} respectively. During this state, C_1 discharges and C_2 charges.



(a)



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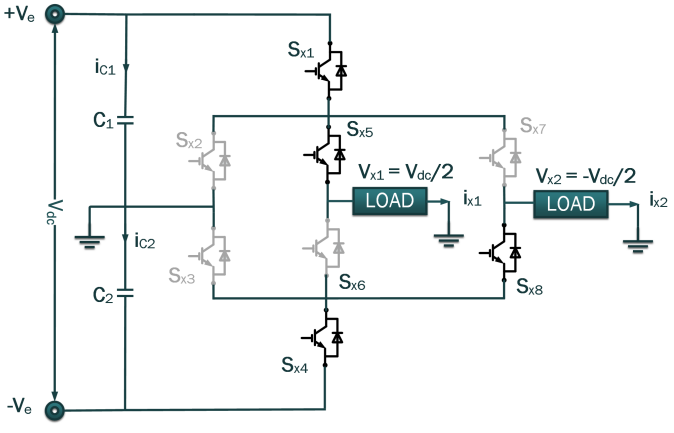


(c)

FIGURE 3.2: Operating states of the proposed TLDO-ANPC. (a) v_{x1}= 0 and v_{x2}= - V_{dc}/2. (b) v_{x1}= V_{dc}/2 and v_{x2}= 0. (c) v_{x1}= V_{dc}/2 and v_{x2}= - V_{dc}/2.

TABLE 3.2: Switching States, Corresponding Output Voltage and Capacitor Charging State of the TLDO-ANPC

S.No.	Switching Signals	Output Voltages (V_{dc})		Capacitor state ($i_{x1} > 0$, $i_{x2} > 0$)		Count
	S_{x1} S_{x2} S_{x3} S_{x4} S_{x5} S_{x6} S_{x7} S_{x8}	v_{x1}	v_{x2}	C_1	C_2	
1	0 1 0 1 1 0 1 0	0	0	NA	NA	6
	0 1 1 0 1 0 1 0	0	0	NA	NA	
	0 1 1 0 1 0 0 1	0	0	NA	NA	
	0 1 1 0 0 1 0 1	0	0	NA	NA	
	1 0 1 0 0 1 0 1	0	0	NA	NA	
	0 1 1 0 0 1 1 0	0	0	NA	NA	
2	1 0 1 0 0 1 1 0	0	0.5	↓	NA	1
3	0 1 0 1 1 0 0 1	0	-0.5	NA	↑	1
4	1 0 1 0 1 0 0 1	0.5	0	↓	NA	1
5	1 0 1 0 1 0 1 0	0.5	0.5	↓	NA	2
	1 0 0 1 1 0 1 0	0.5	0.5	NA	NA	
6	1 0 0 1 1 0 0 1	0.5	-0.5	↓	↑	1
7	0 1 0 1 0 1 1 0	-0.5	0	NA	↑	1
8	1 0 0 1 0 1 1 0	-0.5	0.5	↓	↑	1
9	0 1 0 1 0 1 0 1	-0.5	-0.5	NA	↑	2
	1 0 0 1 0 1 0 1	-0.5	-0.5	NA	↑	
Total						16

↑ is for charging, ↓ is for discharging state and NA = Not affected

It can be seen that the maximum blocking voltage of the switch is TLDO-ANPC is V_{dc}. All possible switching combinations of the single-phase TLDO-ANPC converter are shown in Table 3.2. Among sixteen valid states per phase of the converter, seven are redundant. These redundant switching states reduce the average device switching frequency and dynamic power loss while balancing the DC-link capacitor.

3.2.3 DC-Link Capacitor Voltage Balance

There are two DC-link capacitors in this configuration: the top capacitor (C_1) provides positive, and the bottom capacitor (C_2) provides negative voltage levels. Thus, the voltage deviations of the capacitors of C_1 and C_2 occur due to charging and discharging. Table 3.2 shows the C_1 and C_2 charge, discharge, and bypass states depending upon switching combinations. The currents into the load are taken positively. The designed PWM technique utilizes switching redundancies to balance capacitors C_1 and C_2. Let ΔV_{C1} and ΔV_{C2} represent the DC-link Voltage ripple. $V_{C1} = V_{DC}/2 + \Delta V_{C1}$ and $V_{C2} = V_{DC}/2 + \Delta V_{C2}$. The sum of V_{C1} and V_{C2} is V_{DC} and ΔV_{C2} = - ΔV_{C1}. The capacitor currents through C_1 and C_2 are i_{C1} and i_{C2}. The DC-link capacitor currents in terms of the load currents and the switching signals are as follows:

$$i_{C1} = -S_{x1}(S_{x5}i_{x1} + S_{x7}i_{x2}) \tag{3.1}$$

$$i_{C2} = S_{x4}(S_{x6}i_{x1} + S_{x8}i_{x2}) \tag{3.2}$$

The capacitor voltages depend on the load current as follows:

$$V_{C1} = \frac{1}{C_1}\int_0^t i_{C1}dt + V_{C10} \tag{3.3}$$

$$V_{C1} = -\frac{1}{C_1}\int_0^t (S_{x1}(S_{x5}i_{x1} + S_{x7}i_{x2}))dt \tag{3.4}$$

$$V_{C2} = \frac{1}{C_2}\int_0^t i_{C2}dt + V_{C20} \tag{3.5}$$

$$V_{C2} = \frac{1}{C_2}\int_0^t (S_{x4}(S_{x6}i_{x1} + S_{x8}i_{x2}))dt \tag{3.6}$$

$$V_{C2} = \frac{1}{C_2}\int_0^t i_{C2}dt + V_{C20} \tag{3.7}$$

where V_{C10} and V_{C20} are the initial voltages of capacitors C_1 and C_2 respectively and taking initial value to zero. To achieve balancing, the sum of currents injected or drawn

by the capacitors should result in zero net deviation over a switching period. The average current through C_1 over a T_{ref} switching period should be zero.

$$\int_0^{T_{ref}} i_{C1}dt = 0, \quad i_{C1} = C_1\frac{dV_{C1}}{dt}$$
$$C_1\int_0^{T_{ref}} \frac{dV_{C1}(t)}{dt}dt = 0 \Rightarrow \int_0^{T_{ref}} \Delta V_{C1}(t)dt = 0 \tag{3.8}$$

$$\int_0^{T_{ref}} i_{C2}dt = 0, \quad i_{C2} = C_2\frac{dV_{C2}}{dt}$$
$$C_1\int_0^{T_{ref}} \frac{dV_{C2}(t)}{dt}dt = 0 \Rightarrow \int_0^{T_{ref}} \Delta V_{C2}(t)dt = 0 \tag{3.9}$$

$$V_{C2} = V_{dc} - V_{C1}, \int_0^{T_{ref}} d(V_{dc} - V_{C1}(t)) = 0$$
$$\Rightarrow -\int_0^{T_{ref}} \Delta V_{C1}(t)dt = 0 \tag{3.10}$$

From (3.8) and (3.9), the integration of ΔV_{C1} and V_{C2} over a switching period of T_{ref} should be zero for balancing of DC-link capacitor voltage. As it can be observed from Fig. 3.3 that the charging and discharging times are the same, the DC-link capacitor gets balanced over a period of T_{ref}. In the proposed topology, the capacitor voltage always remains in a balanced state irrespective of the load type, modulation index, or load characteristics. Also, the proposed topology does not require any complicated methods to balance the capacitor voltages.

3.2.4 Capacitor Voltage Ripple Analysis

The DC-link capacitor voltage ripple for phase-A under CF mode with $m_1 = m_2 = 1$, $f_1 = f_2 = 50$ Hz are examined in the following analysis. Fig. 3.3 shows the gate pulses for switches using the proposed PWM and DC-link capacitor voltage ripple, assuming the load current flows into the load. It can be seen that the sequences C (charging) and D (discharging) cause the DC-link capacitor voltage ripple. When switches S_5 and S_7 are ON then V_{C1} discharges and reaches to V_{C1min} while V_{C2} charges and reaches to V_{C2max}. Similarly when switches S_5 and S_7 are OFF then V_{C1} charges and reaches to V_{C1max} while V_{C2} discharges and reaches to V_{C2min}. Since the charging and discharging times are the

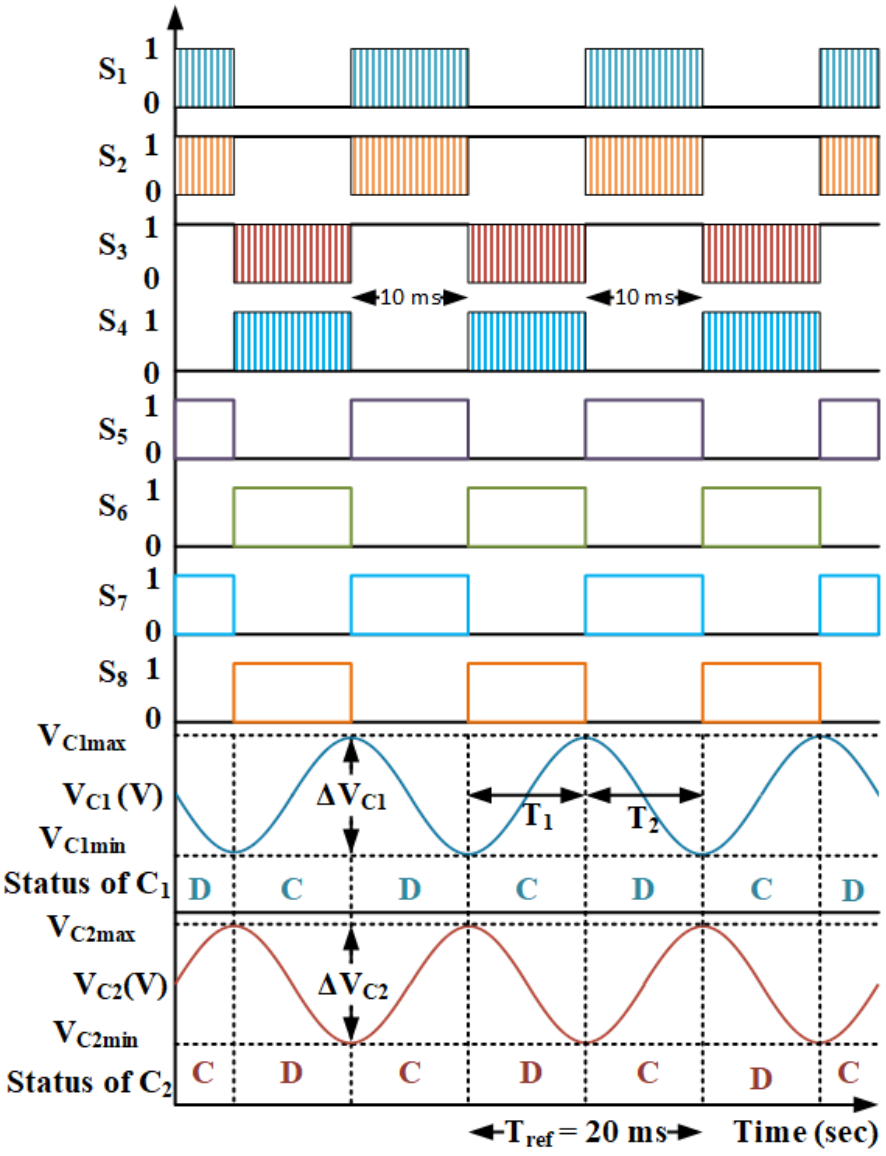


FIGURE 3.3: DC-link capacitor voltage ripple in few-cycle for C_1 and C_2 of the TLDO-ANPC converter through proposed PWM under CF mode with $m_1 = m_2 = 1$, $f_1 = f_2 =$ 50 Hz.

same, the voltage ripple is reset in each reference (fundamental or line) cycle. T_1 and T_2 are the duration of time for charging and discharging and $T_{ref} = T_1 + T_2$. The peak-to-peak value of capacitor voltage ripple ΔV_{C1} and ΔV_{C2} is defined to be the difference between its maximum and minimum value in one fundamental cycle as $\Delta V_{C1} = V_{C1max}$ - V_{C1min} and $\Delta V_{C2} = V_{C2max}$ - V_{C2min}. In the case of Fig. 3.3, $\Delta V_{C1} = \Delta V_{C2} = 204.5\text{-}195.5 = 9$ V.

The limitation of the capacitor balancing technique can be analyzed through the voltage

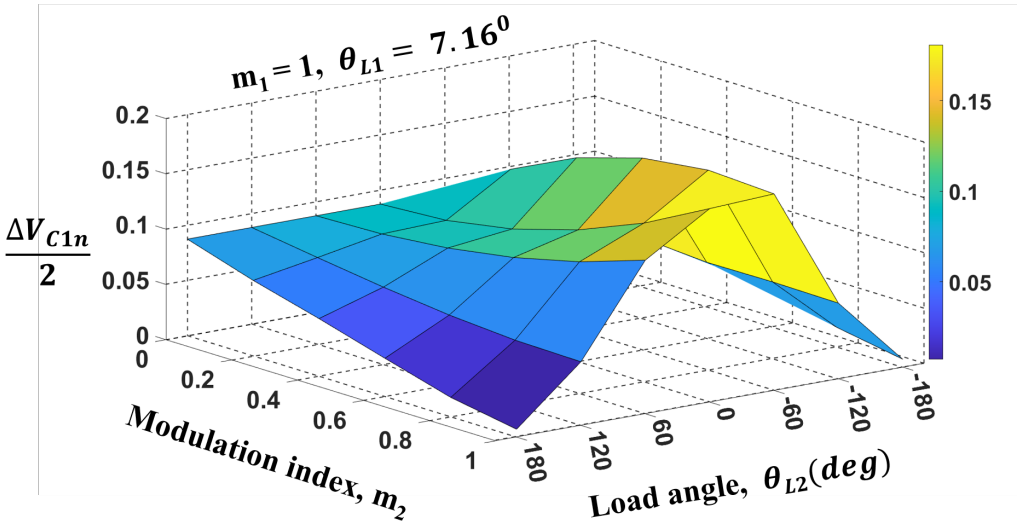


FIGURE 3.4: Normalized DC-link capacitor voltage ripple for C_1 of the TLDO-ANPC converter under CF mode with $m_1 = 1$ and $\theta_{L1} = 7.16°$.

ripple of the DC-link capacitor under various operating conditions [63, 69]. The capacitor voltage ripple in a power converter is mainly affected by two factors: 1. Output power $\propto$ modulation index (m), and 2. Phase current angle or AC load angle (θ_L). In the case of a dual output converter, the evaluation of four variables (m_1, m_2, θ_{L1}, θ_{L2}) is required to operate two loads. Since it consists of large multidimensional data, two variables (m_1 and θ_{L1}) are fixed while the other two are varied within their respective ranges in this evaluation. Converter is operated in CF mode by taking $m_1 = 1$ and $\theta_{L1} = 7.16°$ and by varying m_2 and θ_{L2}. The normalized magnitude of the voltage ripple is used, which may be applied to various applications and operating situations, and the equations are as follows:

$$\frac{\Delta V_{Cin}}{2} = \frac{\Delta V_{Ci}}{2} \Big/ \frac{I_{RMS}}{fC_i}, i = 1, 2 \tag{3.11}$$

where ΔV_{Ci} is the peak-to-peak low-frequency DC-link capacitor voltage ripple, 'f' is the fundamental output frequency, I_{RMS} is the RMS output current, and 'C' is the value of the DC-link capacitor.

Fig. 3.4 shows the results obtained with a fixed load 1 angle $\theta_{L1} = 7.16°$ and $m_1 = 1$. The evaluation is done for CF mode (f_1=f_2= 50 Hz), varying a m_2 and θ_{L2} with a fixed load current.

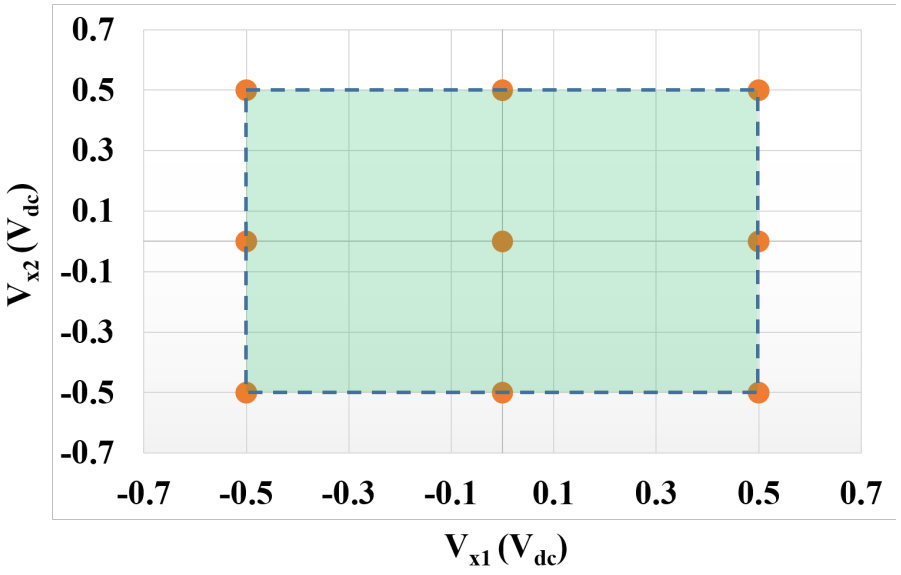


FIGURE 3.5: Graphical depiction of the region of operation and switching states.

3.3 Operation and Switching Scheme of TLDO-ANPC Converter

Most dual-output converters reduce the device count and overall size; however, they face a significant drawback in the operating region. Non-available switching combinations limit the modulation indices of the converter. For example, the NSI is known to have the limitation of $v_{ref1} \geq v_{ref2}$ at all times [70]. In the case of NPC-DO [26], most of the operating states requiring neutral or zero are unavailable. However, TLDO-ANPC does not suffer from this limitation, even with the reduced switch count, it maintains all the voltage states as that of conventional three-level ANPC. This section analyzes and investigates the region of operation of TLDO-ANPC.

3.3.1 Region of Operation

Fig. 3.5 provides a graphical representation of the switching states from Table 3.2. The graph displays the possible voltage levels simultaneously on the v_{x1} and v_{x2} output terminals. The following representation aids in understanding the converter's boundary region. The complete area enclosed by the voltage states depicts all configurations of the voltage reference signals that can be employed. As a result, an output voltage varying from -0.5 to 0.5 V_{dc} corresponds to a variation in the reference signal.

According to the boundary region of Fig. 3.5, there are no limits on one output reference to the other. Both reference signals are independent of each other.

3.3.2 Modulation Scheme

In reduced switch count dual output converters such as NSI, NPP, DO-TLC, and DO-NPC-TLI, the upper reference signal should be greater than the lower to prevent invalid switching states [21, 22, 24, 25, 70]. Therefore, DC offsets are added into two sets of reference signals. However, the TLDO-ANPC converter has no restriction between two reference signals, which provides the full region of operation. The in-phase disposition (IPD) PWM scheme is used for switching. In this scheme, the upper and lower reference signals for three phases are given as follows.

1. For A phase,

$$v_{refA1}(t) = m_1 sin(\omega_1 t + \theta_1) \tag{3.12}$$

$$v_{refA2}(t) = m_2 sin(\omega_2 t + \theta_2) \tag{3.13}$$

2. For B phase,

$$v_{refB1}(t) = m_1 sin(\omega_1 t - 2\pi/3 + \theta_1) \tag{3.14}$$

$$v_{refB2}(t) = m_2 sin(\omega_2 t - 2\pi/3 + \theta_2) \tag{3.15}$$

3. For C phase,

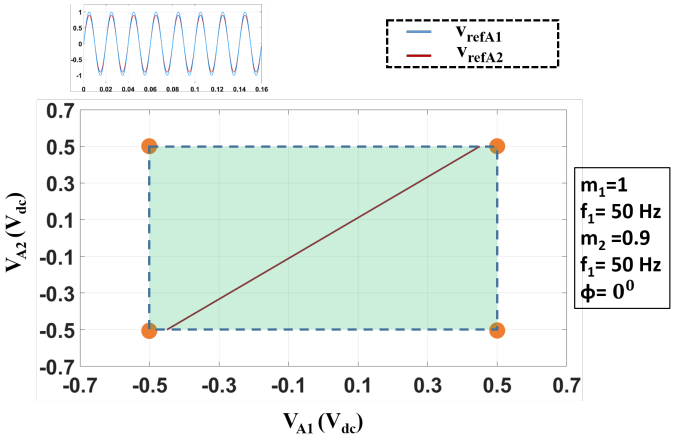
$$v_{refC1}(t) = m_1 sin(\omega_1 t + 2\pi/3 + \theta_1) \tag{3.16}$$

$$v_{refC2}(t) = m_2 sin(\omega_2 t + 2\pi/3 + \theta_2) \tag{3.17}$$

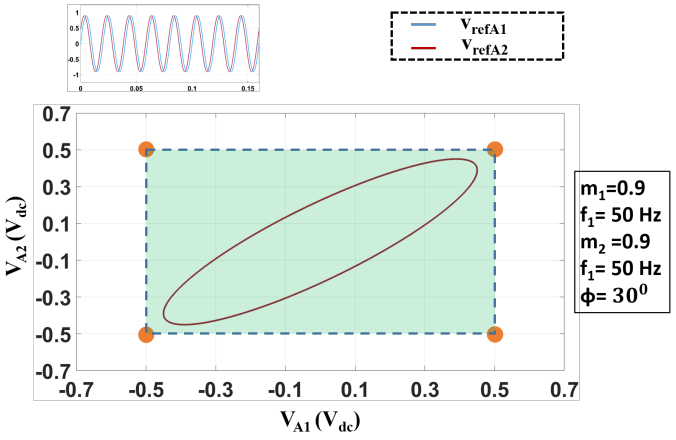
Where m_1 and m_2 are the modulation indices in the range of 0 to 1, $\omega_1 = 2\pi f_1$ and $\omega_2 = 2\pi f_2$ are the fundamental angular frequencies, θ_1 and θ_2 are the initial phase angles. The maximum value of the output line voltage is 0.866 V_{dc}. The complete operating region of the converter is shown in Fig. 3.6(a-c) by projecting the respective reference signals on the boundary space.

3.3.3 Operating modes of TLDO-ANPC

For the independent operation of a dual output converter, two operating modes are classified based on the modulating frequency of two outputs: common and different frequency



(a)



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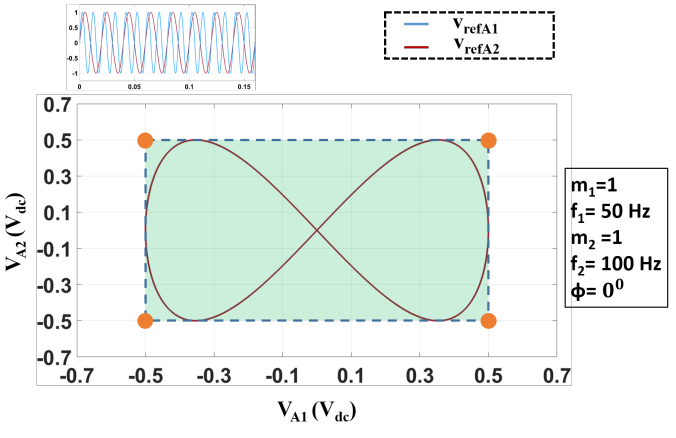
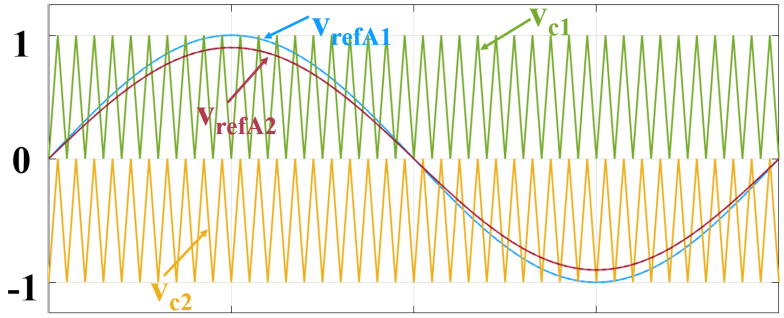
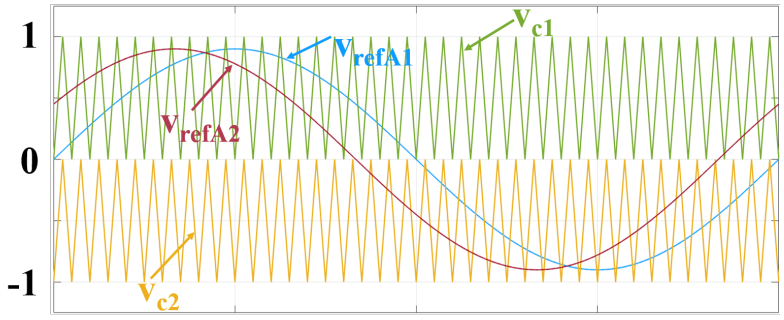


(c)

FIGURE 3.6: Projections of reference signals onto the TLDO-ANPC converter's boundary region under (a) CF with $m_1 = 1$, $m_2 = 0.9$, (b) CF with $m_1 = m_2 = 0.9$ and phase shift of 30°, (c) DF with $m_1 = m_2 = 1$.



(a)



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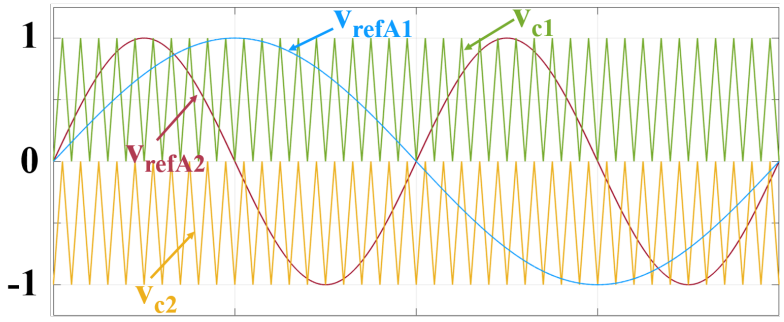


(c)

FIGURE 3.7: IPD PWM scheme for TLDO-ANPC in the (a) CF mode with m_1 =1, m_2 = 0.9 and $\phi = 0°$, (b) CF mode with $m_1 = m_2 = 0.9$ and $\phi = 30°$, (c) DF mode with $m_1 = m_2 = 1$,$f_1 = 50$ and $f_2 = 100$ Hz.

(CF & DF) modes. A dual-output converter should be capable of operating independently at both CF and DF modes. Common frequency (CF) mode of operation in dual output inverters typically refers to the two outputs of the inverter operating at the same frequency. In this, there are two types, i.e., with and without phase shift. Applications of CF mode are grid-tied inverters, UPS, UPQC systems, motor drives, etc. Different frequency (DF) operation in an inverter typically refers to the ability of the inverter to generate two output voltages at different frequencies; consequently, its currents are different. For example, different frequency operations are used in aircraft applications, limited to 400 Hz, dual motor variable speed drives (VSDs) operated at frequencies rated at 50Hz/60Hz, etc. Dual motor drives are also utilized in all-terrain electric vehicles (ATEVs).

The operation of the TLDO-ANPC converter in CF and DF modes is detailed as follows.

3.3.3.1 Common Frequency Mode

The converter is operated in CF mode with varying modulation indices ($m_{1,2}$) and a phase shift (ϕ), where $\phi = |\theta_2$ - $\theta_1|$. Let $f_1 = f_2 = f$ and $\theta_1 = \theta_2 \Rightarrow \phi = 0$, then the reference signal v_{refA1} and v_{refA2} of the A phase leg with two carriers are shown in Fig. 3.7(a). If the reference signal v_{refA1} is greater than the upper carrier and zero, the output voltage v_{A1} is $V_{dc}/2$. If the reference signal v_{refA1} is lesser than the lower carrier and zero, the output voltage v_{A1} is -$V_{dc}/2$. Otherwise, the output voltage v_{A1} equals zero. Following, the output voltage v_{A2} is $V_{dc}/2$ when the reference signal v_{refA2} is greater than the upper carrier and zero. When the reference signal v_{refA2} is lesser than the lower carrier and zero, the output voltage v_{A2} is -$V_{dc}/2$. Otherwise, the output voltage v_{A2} equals zero.

Let $f_1 = f_2 = f$ and $\theta_1 \neq \theta_2$, reference signals v_{refA1} and v_{refA2} of phase A with two carriers, as shown in Fig. 3.7(b). The phase angle shift, $\phi = |\theta_2$ - $\theta_1|$ between the two sets of output phase voltages. v_{refA1} and v_{refA2} are operated with modulation indices between 0 and 1. As it can be observed, there is no phase angle restriction in this case.

3.3.3.2 Different Frequency Mode

The converter can operate in DF mode at various load frequencies. When $f_1 \neq f_2$, reference signals v_{refA1} and v_{refA2} are compared with two carriers, as shown in Fig. 3.7(c). There is no restriction on the modulation index, and the TLDO-ANPC converter can operate with any value of f_1 and f_2. This is a significant advantage compared to other dual-output topologies listed in Table 3.1. Most of them have constrain of $0 < m_1 + m_2 \leq 1$ while

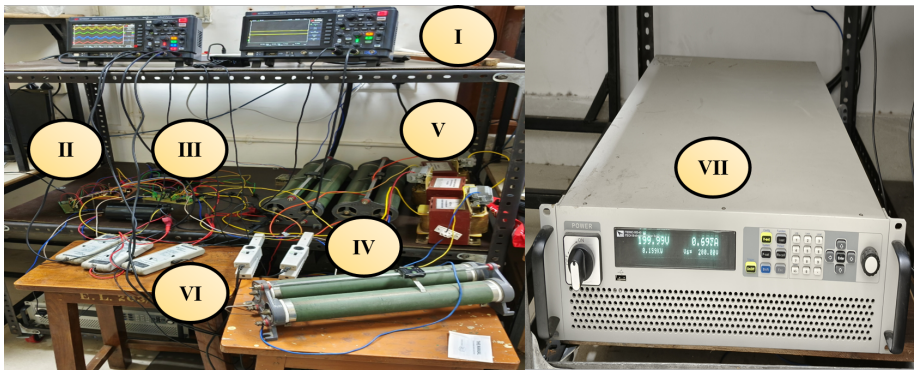


FIGURE 3.8: Hardware setup the proposed converter consisting of (I) Digital signal oscilloscope. (II) DSP TMS320F28335. (III) TLDOV-ANPC converter with its gate driver. (IV) Resistive loads. (V) Inductive loads. (VI) Voltage and current probe (VII) DC power supply.

choosing modulation indices of two outputs. The reference signal v_{refA2} is always smaller than the lower carrier for maintaining this constraint in different frequency modes. As a result, there are only two levels in the upper output voltage v_{A1}: 0 and $V_{dc}/2$ and in the lower output voltage v_{A2}: 0 and -$V_{dc}/2$. Low modulation indices reduce the levels in both phase and line voltage. TLDO-ANPC topology has no such restriction; with this advantage, it can generate the same value of output voltages with a 50% DC bus voltage compared to other dual-output topologies.

Similarly, the B and C phase leg output voltages are generated.

3.4 Simulation and Experimental Verification

MATLAB/Simulink is used to simulate the proposed TLDO-ANPC. The DC-link capacitor voltage is also balanced. Table 3.3 lists the system parameters considered for the simulation and hardware. The 2 kHz carrier frequency is used to implement the IPD-PWM. Identical resistive-inductive (RL) loads are connected at both output terminals. The hardware setup for the experiment is shown in Fig. 3.8. Digital signal processor TMS320F28335 generates the gate pulse signals for the TLDO-ANPC converter.

3.4.1 Common frequency (CF) mode

Fig. 3.9(a) shows the experimental results in CF ($f_1 = f_2 = 50$ Hz) mode for both output voltages (v_{A1},v_{A2}) and their corresponding load currents (i_{A1},i_{A2}). Both loads are operated

TABLE 3.3: Parameters for Simulation and Hardware

Parameter	Value
dc-link voltage (V_{dc})	400 V
dc-link capacitors ($C_1 = C_2$)	2200 μF
Load resistances ($R_1 = R_2$)	50 Ω
Load inductances ($L_1 = L_2$)	20 mH
Switching frequency (f_s)	2 kHz

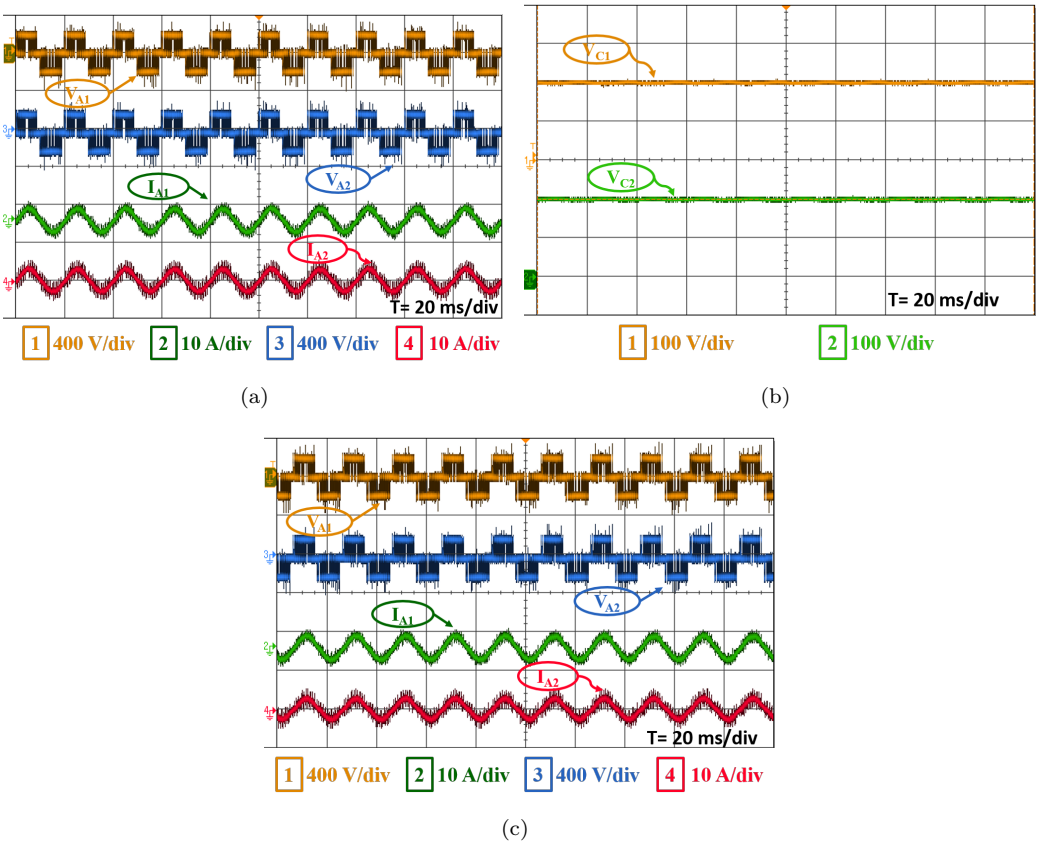


FIGURE 3.9: Experimental result in CF mode (a) output voltages (v_{A1},v_{A2}) and currents (i_{A1},i_{A2}) with $m_1 = m_2 = 1$, (b) DC-link capacitor voltage balancing with $m_1 = m_2 = 1$, (c) output voltages (v_{A1},v_{A2}) and currents (i_{A1},i_{A2}) with $m_1 = 1$, $m_2 = 0.9$.

with the same modulation indices $m_1 = m_2 = 1$. Fig. 3.9(b) depicts the DC-link capacitor voltage balancing under CF mode with the same modulation indices ($m_1 = m_2 = 1$). As it can be observed, V_{C1} and V_{C2} are balanced at 199.6 V and 201.2 V, respectively.

The experimental result for both output voltages (v_{A1},v_{A2}) and their corresponding load currents (i_{A1},i_{A2}) under CF mode of operation with the different modulation indices (m_1 = 1, m_2 = 0.9) is shown in Fig. 3.9(c). As observed, the converter generates three voltage levels at its output ports: -V_{dc}/2, 0, and +V_{dc}/2.

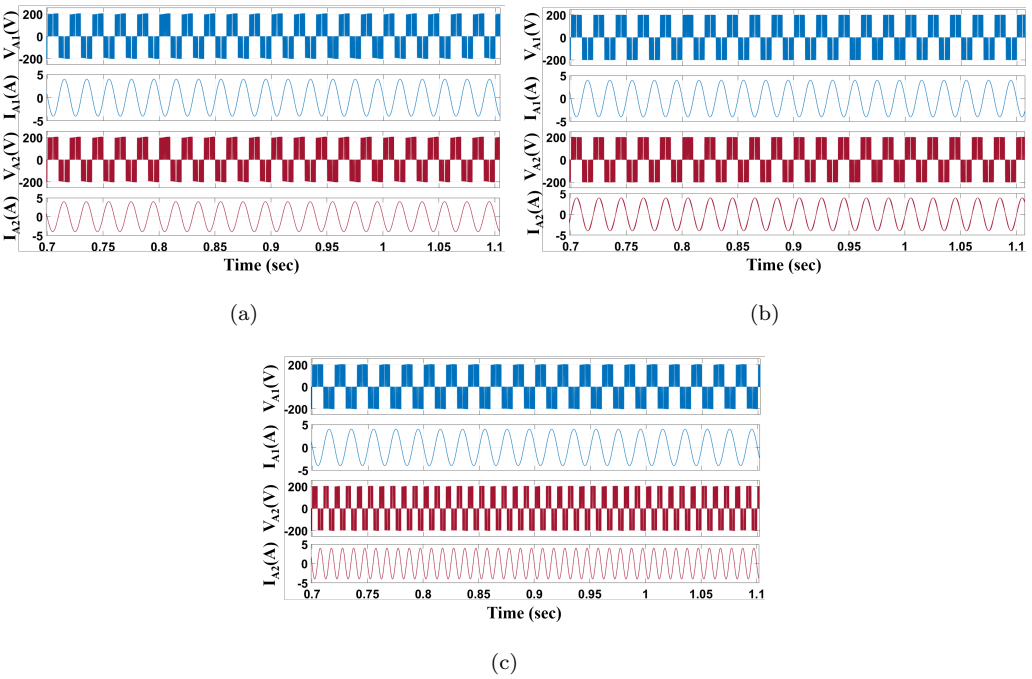
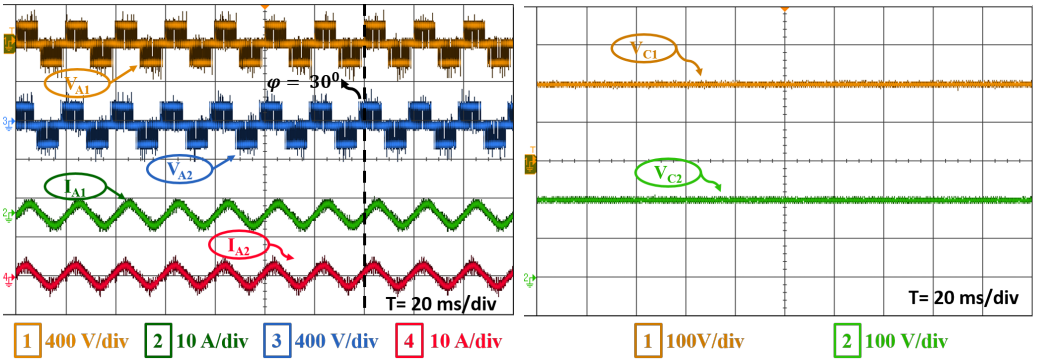


FIGURE 3.10: Simulation results for output voltages (v_{A1},v_{A2}) and currents (i_{A1},i_{A2}) (a) CF mode with $m_1 = m_2 = 1$, when both load currents are flowing from the output terminal to the DC-link capacitor, (b) CF mode with $m_1 = m_2 = 1$, when i_{A1} is flowing from the output terminal to the DC-link capacitor, and i_{A2} is flowing from DC-link to the load, (c) DF mode with $m_1 = m_2 = 1$ and $f_1 = 50$ Hz, $f_2 = 100$ Hz when both load current are flowing from the output terminal to the DC-link capacitor.

Fig. 3.10(a) shows the simulation result of the converter when both the load current flows towards DC-link under CF ($f_1 = f_2 = 50$ Hz) mode with $m_1 = m_2 = 1$. Fig. 3.10(b) shows the result of the converter when i_{A1} is flowing from the output terminal to the DC-link capacitor and i_{A2} is flowing from DC-link to the load under CF ($f_1 = f_2 = 50$ Hz) mode with $m_1 = m_2 = 1$.

Fig. 3.11(a) displays the experimental result of the voltages at both output terminals (v_{A1},v_{A2}) and its corresponding load currents (i_{A1},i_{A2}) under CF mode of operation with the same modulation indices ($m_1 = m_2 = 0.9$) and phase shift $\phi = 30°$.

Fig. 3.12(a) displays the experimental result for the voltages at both output terminals (v_{A1},v_{A2}) and its corresponding load currents (i_{A1},i_{A2}) under CF mode ($f_1 = f_2 = 50$ Hz) of operation with the modulation indices $m_1 = 0.8$, $m_2 = 0.7$ and phase shift $\phi = 30°$. Fig. 3.12(b) shows the experimental result for the voltages at both output terminals (v_{A1},v_{A2}), and its corresponding load currents (i_{A1},i_{A2}) under CF mode ($f_1 = f_2 = 50$ Hz) of operation with the same modulation indices ($m_1 = m_2 = 0.9$) and phase shift ϕ



(a) (b)

FIGURE 3.11: (a) Experimental result for output voltages (v_{A1},v_{A2}) and currents (i_{A1},i_{A2}) in CF mode, $m_1 = m_2 = 0.9$ and $\phi = 30°$. (b) Experimental result of DC-link capacitor voltage for three-phase in CF mode with $m_1 = 1$, $m_2 = 1$.

$= 60°$. This phase shift between two outputs is significant when operating multi-phase motors [71].

3.4.2 Different frequency (DF) mode

This section evaluates the converter's performance in the DF mode of operation. Fig. 3.10(c) shows the simulation result of the converter when load current flows from DC-link under DF mode ($f_1 = 50$ Hz, $f_2 = 100$ Hz) with $m_1 = m_2 = 1$. Fig. 3.12(c) shows the experimental result for the voltages at both output terminals (v_{A1},v_{A2}), and its corresponding load currents (i_{A1},i_{A2}) under DF mode of operation with the same modulation indices $m_1 = m_2 = 1$ and $f_1 = 50$ Hz, $f_2 = 60$ Hz. Fig. 3.13(a) presents the experimental results of voltages at both output terminals (v_{A1},v_{A2}), and its corresponding load currents (i_{A1},i_{A2}), the output frequencies of the converter at both terminals are kept $f_1 = 50$ Hz, $f_2 = 100$ Hz with modulation indices $m_1 = m_2 = 1$, respectively.

3.4.3 Load Change

The converter's performance is evaluated for sudden load changes in the lower output terminal in the CF mode of operation. Previously, R_1= 50 Ω, R_2 = 25 Ω and L_1= 20 mH, L_2 = 10 mH, after a sudden change in load in lower terminal R_2 and L_2 becomes 50 Ω and 20 mH, same as that of R_1 and L_1. Fig. 3.13(b) presents the experimental result for upper and lower output voltages (v_{A1},v_{A2}), and its corresponding load current (i_{A1},i_{A2}) under CF mode. In this case, the converter is operated at modulation indices $m_1 = m_2$

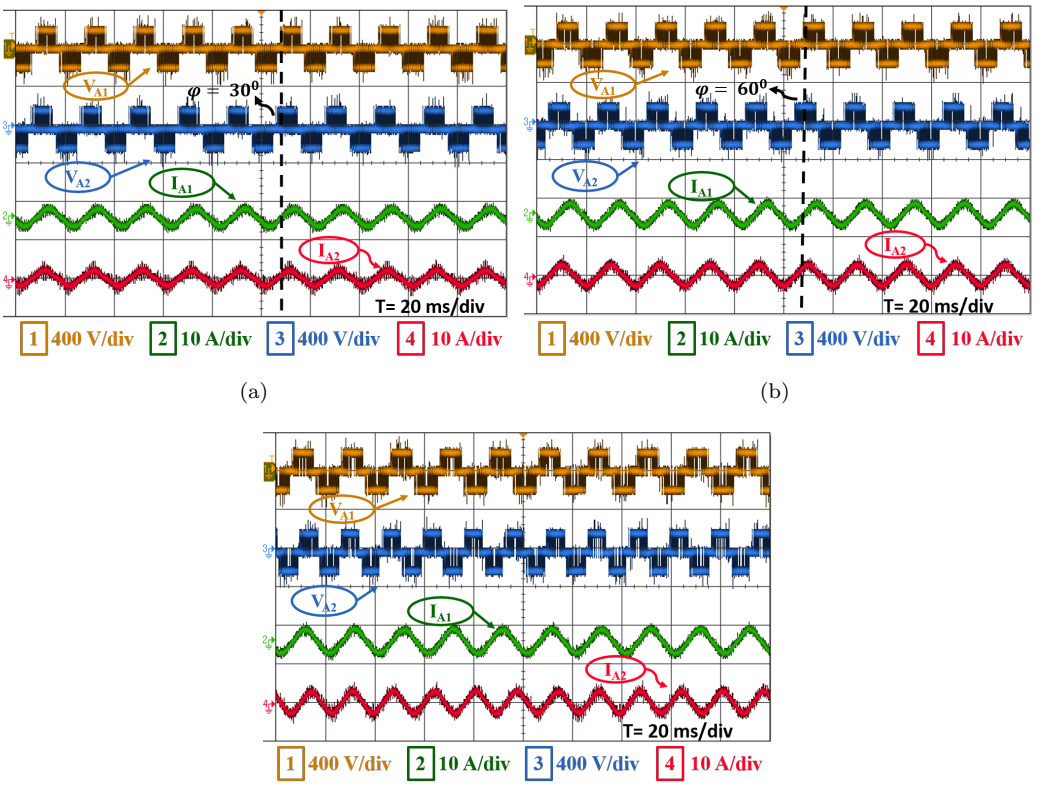
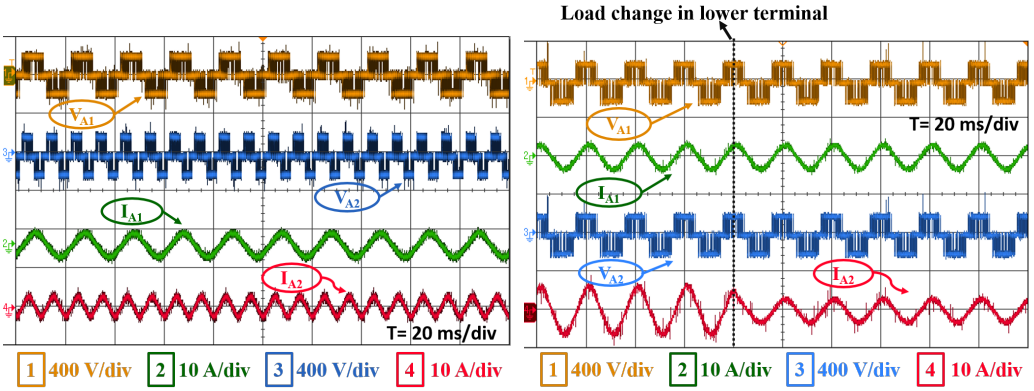


FIGURE 3.12: Experimental result (a) output voltages (v_{A1},v_{A2}) and currents (i_{A1},i_{A2}) in CF mode, m_1 =0.8, $m_2 = 0.7$ and $\phi = 30°$, (b) output voltages (v_{A1},v_{A2}) and currents (i_{A1},i_{A2}) in CF mode, $m_1 = m_2 = 0.9$ and $\phi = 60°$, (c) output voltages (v_{A1},v_{A2}) and currents (i_{A1},i_{A2}) in DF mode, $m_1 = m_2 = 1$ and $f_1 = 50$ Hz, $f_2 = 60$ Hz.

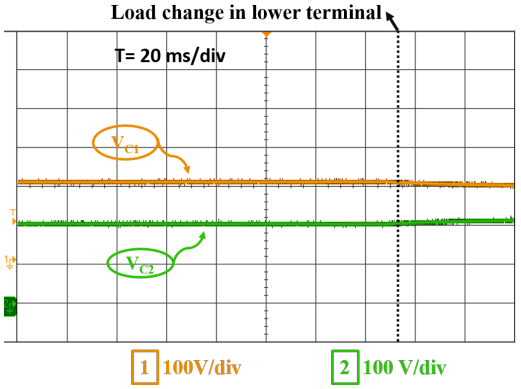
= 1. Fig. 3.13(c) depicts the DC-link capacitor voltage balancing under load changes. Initially, the DC-link capacitors V_{C1} and V_{C2} are balanced at 202.9 V and 197.1 V, after a sudden change in load in the lower terminal, the DC-link capacitors voltage V_{C1} and V_{C2} are balanced approximately to the previous voltage.

3.4.4 Three-phase operation

The experimental results for 'A' and 'C' phases have been recorded and presented to validate the three-phase operation of the proposed converter. Fig. 3.14 shows the three phase experimental result in CF mode ($f_1 = f_2 = 50$ Hz) with $m_1 = m_2 = 1$. Fig. 3.14(a) for output phase voltages (v_{A1},v_{A2},v_{C1},v_{C2}), Fig. 3.14(b) for output line voltages (v_{AC1},v_{AC2}) and currents (i_{A1},i_{A2}) and Fig. 3.14(c) for output currents (i_{A1},i_{A2},i_{C1},i_{C2}). Fig. 3.11(b) depicts the experimental result of DC-link capacitor voltage balancing for three-phase under CF mode ($f_1 = f_2 = 50$ Hz) with the same modulation indices (m_1



(a) (b)



(c)

FIGURE 3.13: Experimental result for (a) output voltages (v_{A1},v_{A2}) and currents (i_{A1},i_{A2}) in DF mode with $m_1 = m_2 = 1$ and $f_1 = 50$ Hz, $f_2 = 100$ Hz, (b) output voltages (v_{A1},v_{A2}) and currents (i_{A1},i_{A2}) for a sudden change in load under CF mode with same modulation indices $m_1 = m_2 = 1$, (c) DC-link capacitor voltage balancing for a sudden change in load under CF mode with same modulation indices $m_1 = m_2 = 1$.

$= m_2 = 1$). As it can be observed, V_{C1} and V_{C2} are balanced at 199.8 V and 200.2 V, respectively. The operating converter for three phases provides more states for balancing the DC-link capacitor as compared to a single phase.

3.5 Power Loss and Efficiency Comparison

Conduction and switching losses are two significant forms of power losses arising from power electronic devices [72]:

Conduction Loss (P_{con}): A standard power transistor (IGBT) and diode are used for the loss analysis of the proposed converter. Instantaneous conduction losses for a diode [P_{con},

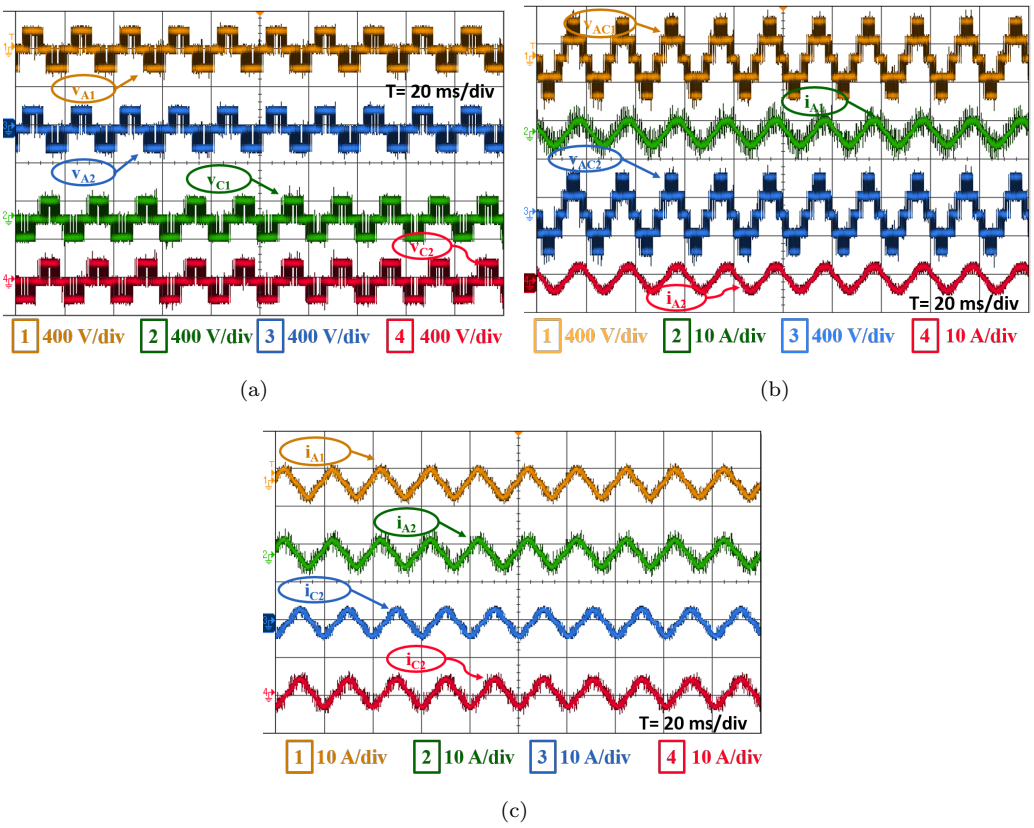


FIGURE 3.14: Experimental result in CF mode with $m_1 = m_2 = 1$ (a) output phase voltages (v_{A1},v_{A2},v_{C1},v_{C2}), (b) output line voltages (v_{AC1},v_{AC2}) and currents (i_{A1},i_{A2}), (c) output currents (i_{A1},i_{A2},i_{C1},i_{C2}).

D(t)] and IGBT [P_{con}, T(t)] are as follows:

$$P_{con}, T(t) = [V_T + R_T i^{\beta}(t)]i(t) \tag{3.18}$$

$$P_{con}, D(t) = [V_D + R_D i(t)]i(t) \tag{3.19}$$

where V_T and V_D are ON state voltages of IGBTs and the diodes, and R_T and R_D are their equivalent resistances, respectively. β is a constant associated with the transistor specification. The conduction losses of each device are calculated using (3.18) and (3.19), and total conduction loss is the sum of these two for a converter.

Switching Loss (P_{sw}): Turn-on and turn-off loss (E_{on}, E_{off}) are calculated for the switch and the anti-parallel diode as follows:

$$E_{off,m} = \int_0^{t_{off}} v(t)i(t)dt = \int_0^{t_{off}} [(\frac{v_{sw,m}}{t_{off}}t) (-\frac{I}{t_{off}}(t - t_{off}))dt = \frac{1}{6}v_{sw,m}It_{off} \tag{3.20}$$

$$E_{on,m} = \int_0^{t_{on}} v(t)i(t)dt = \int_0^{t_{on}} [(\frac{v_{sw,m}}{t_{on}}t) (-\frac{I'}{t_{on}}(t - t_{on}))dt = \frac{1}{6}v_{sw,m}I't_{off} \tag{3.21}$$

where $E_{off,m}$ and $E_{on,m}$ are the turn-off and turn-on losses, t_{off} and t_{on} are the turn-off and turn-on time of the 'm' switch respectively. 'I' is the current through the switch before turning off, and ' I'' is the current after turning on. $V_{sw,m}$ is the off-state voltage on the 'm' switch.

$$P_{sw} = f[\sum_{m=1}^{N_{switch}} (\sum_{j=1}^{N_{on,m}} E_{on,mj} + \sum_{j=1}^{N_{off,m}} E_{off,mj})] \tag{3.22}$$

Where 'f' is the fundamental frequency, $N_{off,m}$ and $N_{on,m}$ are the number of times switch 'm' turns OFF and ON during a period. Also, $E_{off,mj}$ and $E_{on,mj}$ are the energy loss of the 'm' switch during the j^{th} turn OFF and ON, respectively. The total losses of TLDO-ANPC will be;

$$P_{Loss} = P_{con} + P_{sw} \tag{3.23}$$

The parameters used for power loss calculation are listed in Table 3.3. The switching and conduction losses of TLDO-ANPC are calculated using the IGBT IKW50N60H3 for the loss model in PLECS software. The contribution of switching and conduction loss under the CF mode of operation with $m_1 = 1$, m_2 varying from 0.2 to 1, and $f_1 = f_2 = 50$ Hz is shown in Fig. 3.15(a). Figs. 3.15(b) and (c) show the distribution of the conduction and switching losses among the different switches of phase A under CF mode of operation having $m_1 = m_2 = 1$ and $f_1 = f_2 = 50$ Hz, where the conduction losses are the highest in S_{a1} and S_{a4}, and the lowest in S_{a2} and S_{a3}. On the other hand, S_{a1} and S_{a4} have the highest switching losses while S_{a5}, S_{a6}, S_{a7} and S_{a8} have the lowest switching losses. The efficiencies are compared in CF and DF mode as shown in Fig. 3.16. The efficiency comparison is made using the parameters listed in Table 3.3 between the

CTL-ANPC, NPP, RSC-DT(DO-T-TLC), and the proposed TLDO-ANPC converter. In the first scenario, Fig. 3.16(a) depicts the efficiency comparison under CF mode when modulation indices $m_1 = 1$ and m_2 vary from 0.2 to 1. It can be observed that the NPP has more efficiency compared to other dual output three-level converters, but CTL-ANPC and TLDO-ANPC also have an efficiency greater than 99 % for all values of m_2. In the second scenario, Fig. 3.16(b) compares the efficiency under CF mode with $m_1 = 0.8$ and phase shift, $\phi = 30°$ and varying m_2. As it can be seen, for a modulation index m_2 greater than 0.8, the reduced switch count converter (NPP, RSC-DT(DO-T-TLC), etc.) is unable to operate because of its constricted region of operation, so the graph shows zero efficiency. For m_2 less than 0.8, NPP has more efficiency than other dual output three-level converters, but CTL-ANPC and TLDO-ANPC have efficiency greater than 98 % and when m_2 lies between 0.8 and 1, then the efficiency of CTL-ANPC and TLDO-ANPC is greater than 99 %. In the third scenario, Fig. 3.16(c) shows the comparison of efficiency under DF mode ($f_1 = 50$ Hz, $f_2 = 100$ Hz) with $m_1 = 0.5$ and varying m_2. Because of limitations in the operating region, the NPP, RSC-DT (DO-T-TLC) cannot operate at m_2 greater than 0.5, and efficiency is zero for this region. For m_2 less than 0.5, NPP has more efficiency, but TLDO-ANPC has efficiency greater than 98.8 % up to $m_2 = 0.6$, and for m_2 greater than 0.6, TLDO-ANPC has the efficiency greater than 99 %. In the first scenario, the TLDO-ANPC has approximately the same efficiency as that of CTL-ANPC up to $m_2 = 0.6$, but for m_2 greater than 0.8, CTL-ANPC is more efficient than TLDO-ANPC. But for the second and third scenarios, TLDO-ANPC is more efficient than CTL-ANPC for all modulation indexes of m_2. This difference in efficiency is not considerably high. Note that the two loads are constant and modulation index m_1 is fixed.

The comparison of conduction and switching loss under the CF mode of operation with $m_1 = m_2 = 1$ for varying total output power ($P_{out} = P_{out1} + P_{out2}$) is shown in Fig. 3.17. Figs.3.17(a) and (b) show the conduction and switching losses comparison between the conventional CTL-ANPC, NPP, RSC-DT(DO-T-TLC), and the proposed TLDO-ANPC converter at output power varying from 56.59 W to 1414.74 W for phase A under CF mode of operation ($m_1 = m_2 = 1$ and $f_1 = f_2 = 50$ Hz). As the output power increases, the conduction and switching losses also increase. It can be observed that the NPP has lesser conduction loss compared to other dual output three-level converters, but RSC-DT (DO-T-TLC) has higher conduction loss. While the difference in conduction loss for CTL-ANPC and TLDO-ANPC at all output power values is similar. On the other hand, there is no such difference in switching loss among the dual-output converters.

Conduction Loss with its equivalent circuit (P_{con}): The equivalent series resistance (ESR)

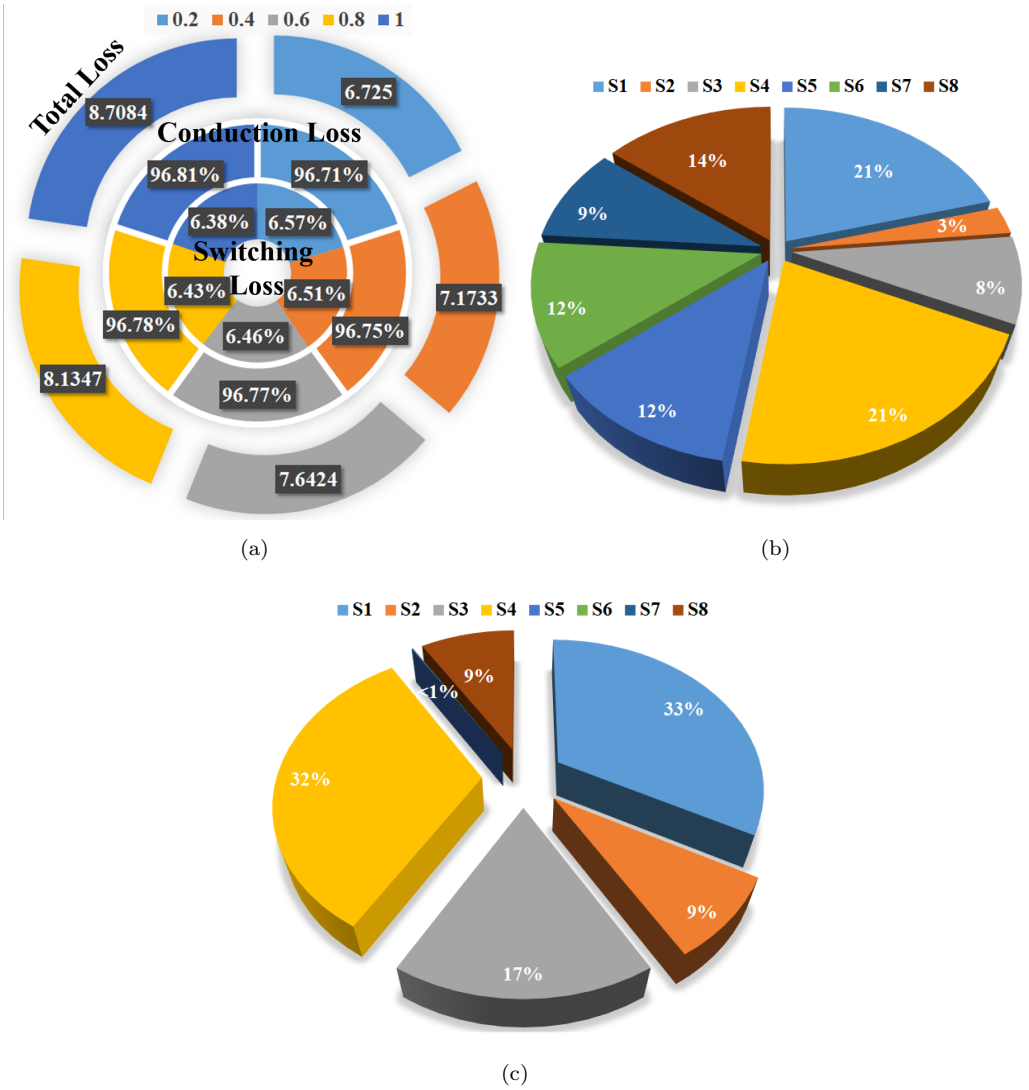


FIGURE 3.15: Switching, conduction, and total losses of the proposed TLDO-ANPC for A-phase under CF mode with $m_1 = 1$ and m_2 varying.

of the capacitors and the internal resistance of the switching device determines the conduction loss. The expression for the conduction loss is

$$P_{con} = \sum_{switches} i_x^2 R_x + \sum_{capacitor} i_C^2 R_C \tag{3.24}$$

where i_x, R_x, i_C, and R_C are load current, ON state resistance of the switch, capacitor current, and ESR of the capacitor, respectively. The ON state resistance of switches S_{x1}, S_{x2}, S_{x3}, S_{x4}, S_{x5}, S_{x6}, S_{x7}, and S_{x8} are R_{x1}, R_{x2}, R_{x3}, R_{x4}, R_{x5}, R_{x6}, R_{x7}, and R_{x8} where "x" mentioned in the following part is all x $\in$ {A, B, and C}. R_{C1} and R_{C2} are ESR of capacitance C_1 and C_2. $Z_1$and Z_2 are loads. From the Table 3.2 of TLDO-ANPC, all the

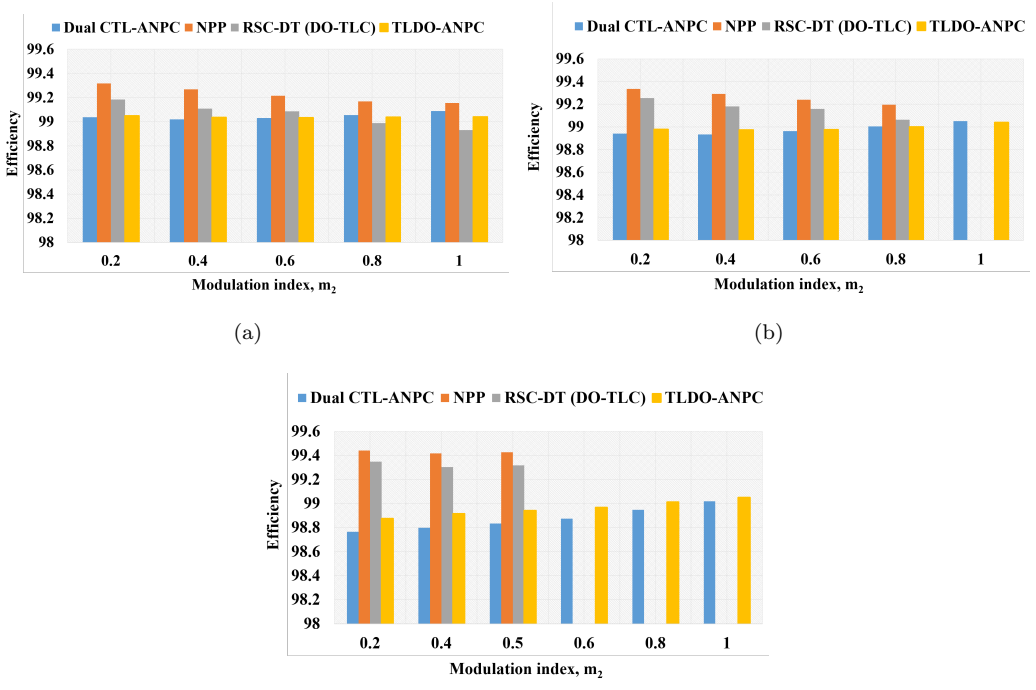


FIGURE 3.16: Efficiency comparison for (a) CF mode with $m_1 = 1$ (b) CF mode, $m_1 = 0.8$ and $\phi = 30°$, (c) DF mode with $m_1 = 0.5$ and $f_1 = 50$ Hz, $f_2 = 100$ Hz.

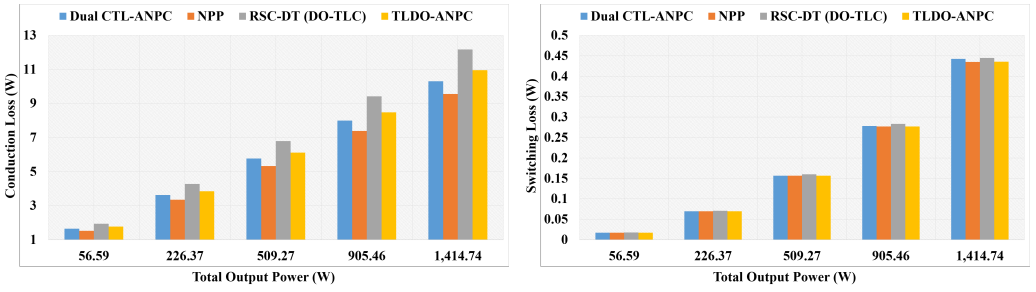


FIGURE 3.17: Conduction and switching loss comparison at different output powers under CF mode ($m_1 = m_2 = 1$).

states, including redundant states, are considered operating states. The equivalent circuit of the few operating states of Fig. 3.2 is shown in Fig. 3.18. There are eight switches with two DC-link capacitors and a DC source, enabling nine distinct and seven redundant switching states. For $v_{x1} = 0$ and v_{x2} = -V_{dc}/2, the equivalent circuit for this operating state is shown in Fig. 3.18(a). The capacitor and load currents are $i_{c1} = 0$, i_{c2} = -i_{x2} and $i_{x1} = 0$, $i_{x2} = \frac{-0.5V_{dc}}{R_{C2}+R_{x4}+R_{x8}+Z_2}$. The conduction loss for this state is $P_{con3} = i_{L2}^2(R_{C2}+R_{x4}+R_{x8})$. When v_{x1}= V_{dc}/2 and v_{x2}= 0, the equivalent circuit for this operating state

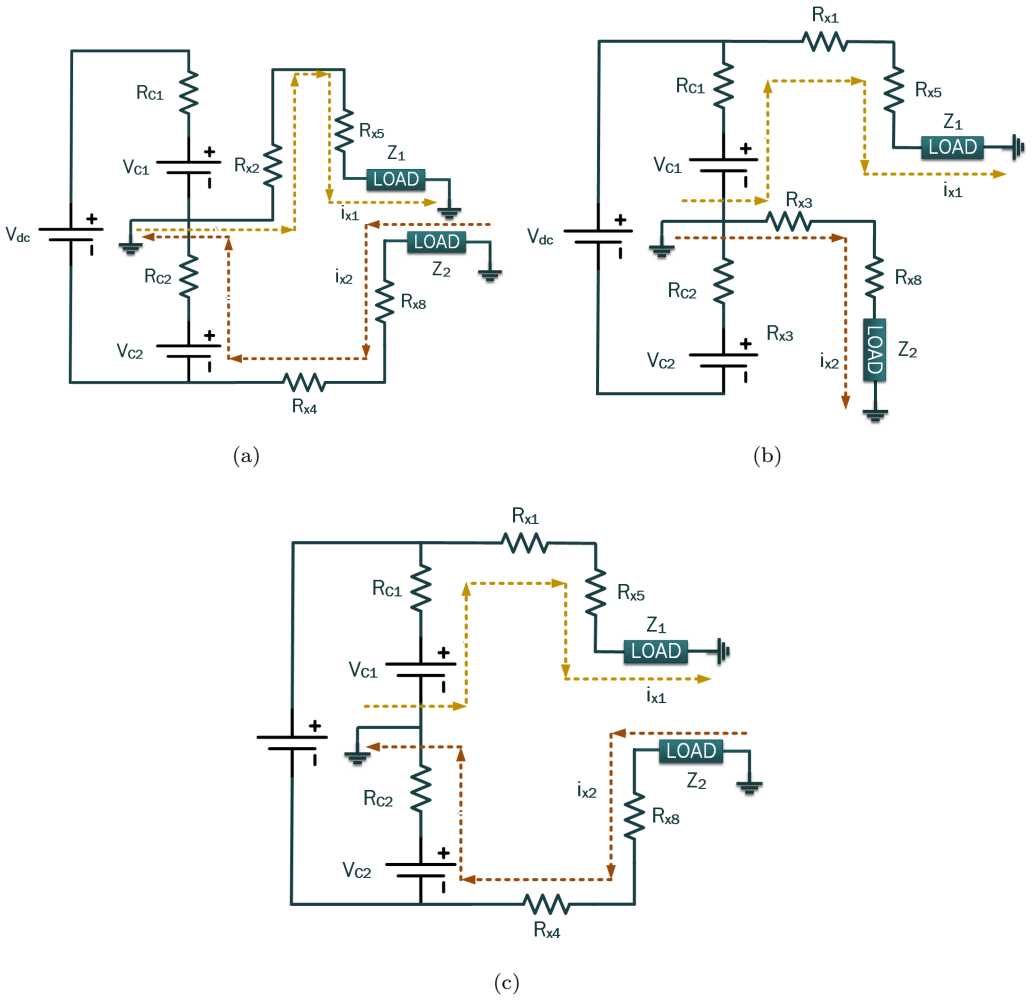


FIGURE 3.18: Equivalent circuit for the operating states of the proposed TLDO-ANPC (a) v_{x1}= 0 and v_{x2}= - $V_{dc}/2$ (b) v_{x1}= $V_{dc}/2$ and v_{x2}= 0 (c) v_{x1}= $V_{dc}/2$ and v_{x2}= - $V_{dc}/2$.

is shown in Fig. 3.18(b). The capacitor and load currents are i_{c1} = -i_{x1}, i_{c2} = 0 and $i_{x1} = \frac{0.5V_{dc}}{R_{C1}+R_{x1}+R_{x5}+Z_1}$, i_{x2} = 0. The conduction loss for this state is $P_{con4} = i_{L1}^2(R_{C1}+ R_{x1}+R_{x5})$. For v_{x1}= $V_{dc}/2$ and v_{x2}= - $V_{dc}/2$, the equivalent circuit for this operating state is shown in Fig. 3.18(c). The capacitor and load currents are i_{c1} = -i_{x1}, i_{c2} = -i_{x2} and $i_{x1} = \frac{0.5V_{dc}}{R_{C1}+R_{x1}+R_{x5}+Z_1}$, $i_{x2} = \frac{-0.5V_{dc}}{R_{C2}+R_{x4}+R_{x8}+Z_2}$. The conduction loss for this state is $p_{con6} = i_{x1}^2(R_{C1}+ R_{x1}+R_{x5}) + i_{x2}^2(R_{C2}+ R_{x4}+R_{x8})$. In a similar manner, the remaining switching states' conduction losses can be calculated. The overall conduction loss (P_{conT})

is therefore expressed as;

$$\begin{aligned} P_{conT} &= 6P_{con1} + P_{con2} + P_{con3} + P_{con4} \\ &+2P_{con5} + P_{con6} + P_{con7} + P_{con8} + 2P_{con9}. \end{aligned} \tag{3.25}$$

$$\begin{aligned} P_{conT} &= P_{con2} + P_{con3} + P_{con4} + 2P_{con5} \\ &+P_{con6} + P_{con7} + P_{con8} + 2P_{con9}. \end{aligned}$$