Chapter 5

Five-level Dual-Output Active Neutral Point Clamped Converter

5.1 Background

To further reduce the switch count of previously discussed FLSDO converter, a five-level dual-output active clamped neutral point clamped (5LDO-ANPC) converter is introduced in this chapter. 5LDO-ANPC also overcomes the major drawback of [20, 21, 23, 25, 26, 28, 73], reduced operating (boundary) region due to the unavailability of a few switching states. This topology achieves a lower number of power switches than the conventional five-level ANPC and FLSDO, while providing independent operation of dual three-phase loads without constraining modulation index or phase-shift. A mathematical model of the converter is developed and integrated into a multiobjective finite control set model predictive control (FCS-MPC) algorithm. FCS-MPC effectively controls the two independent three-phase load currents while ensuring balanced voltages across the DC-link and flying capacitors. The performance of this converter is improved through FCS-ANPC.

5.2 Five-Level Dual Output Active Neutral Point Clamped (5LDO-ANPC) Converter

The three-phase circuit configuration of the proposed 5LDO-ANPC converter is shown in Fig. 5.1.

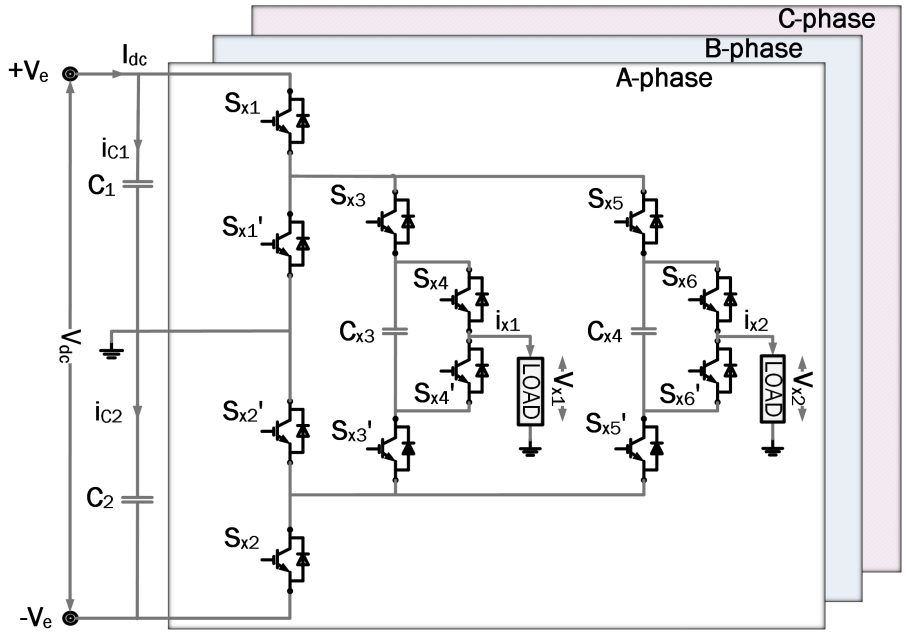

FIGURE 5.1: Proposed five-level dual output active neutral point clamped (5LDO-ANPC) converter.

5.2.1 Topology of 5LDO-ANPC

The 5LDO-ANPC produces two sets of output voltages and offers complete independent control of its output terminals. The converter consists of 36 semiconductor switches, two DC-link capacitors, and six flying capacitors. The DC-link and flying capacitors (FCs) are charged to "$V_{dc}/2$" and "$V_{dc}/4$". This flying capacitor is employed with the three-level converter as needed, thereby introducing two additional intermediate output voltage levels for both output terminals. The single-phase 5LDO-ANPC converter consists of 12 switches (S_{x1} to S_{x12}), two DC-link capacitors (C_1, C_2) and two flying capacitors (C_{x3}, C_{x4}). The input DC-link voltage V_{dc} is connected across the series connection of capacitors C_1 and C_2. Out of these twelve switches, four are inner switches, and eight are outer switches per leg which are S_x1, S'_{x1}, S_{x2}, S'_{x2} and S_{x3}, S'_{x3}, S_{x4}, S'_{x4}, S_{x5}, S'_{x5}, S_{x6}, S'_{x6} where "x" mentioned in the following part is, all x $\in$ {A, B, and C}.

ABB has added the active neutral-point clamped (ANPC) five-level topology to their medium-voltage (MV) drive portfolio as the advancement [78]. Similar to a conventional five-level ANPC (C5L-ANPC) in [78], 5LDO-ANPC also provides a full region of operation. It can drive two three-phase loads simultaneously. The elegance of this converter is that it has four fewer switches per leg than C5L-ANPC required to drive two loads simultaneously.

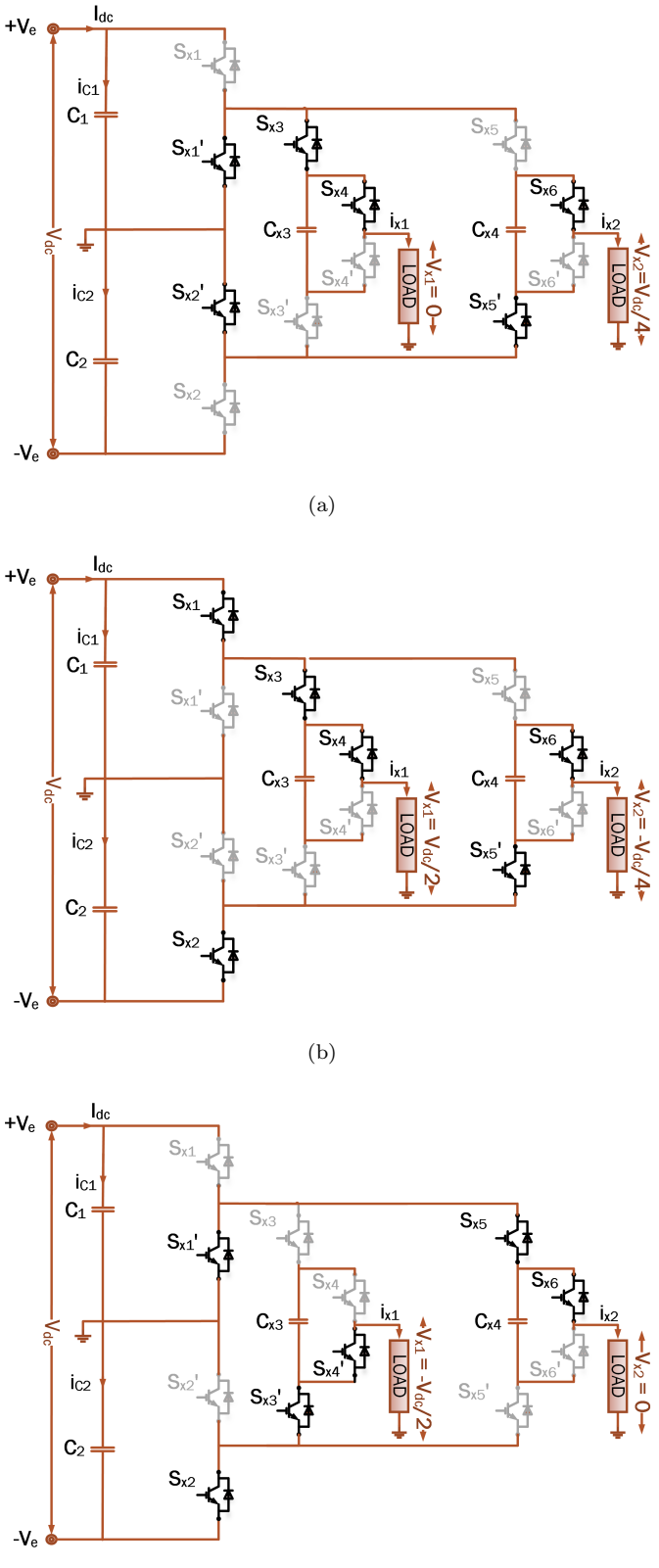

FIGURE 5.2: Various operating states of the proposed 5LDO-ANPC. (a) v_{x1}= 0 and v_{x2} = $V_{dc}/4$. (b) v_{x1}= $V_{dc}/2$ and v_{x2}= -$V_{dc}/4$. (c) v_{x1}= -$V_{dc}/2$ and v_{x2}= 0.

To drive a six-phase machine or two three-phase loads, the C5L-ANPC requires 48 switches [76], whereas the 5LDO-ANPC only needs 36 switches. Table 5.1 details the number of switches, devices, and operating regions for the 5LDO-ANPC with five-level dual output topologies. Compared to other topologies, the 5LDO-ANPC offers advantages in terms of reduction in component count while providing a full region of operation.

5.2.2 State of Operation

Each leg in the proposed converter consists of four inner and eight outer switches. The output voltages v_{x1} and v_{x2} are distinct values obtained from the combinations of the inner and outer switches with respect to the neutral point. These voltages are derived from the input-side voltage, the levels are $V_{dc}/2$, $V_{dc}/4$, 0, -$V_{dc}/2$, -$V_{dc}/4$. The voltages v_{x1} and v_{x2} correspond to the phase voltages of the two outputs, while i_{x1} and i_{x2} represent the load currents for each output. For the single-phase configuration of the proposed topology, the few operating states are illustrated in Fig. 5.2(a)–(c) and described as follows.

5.2.2.1 State of Operation 1

Switches S'_{x1}, S'_{x2}, S_{x3}, S_{x4}, S'_{x5}, and S_{x6} are turned ON, allowing current to flow between the DC-link and the loads, as illustrated in Fig. 5.2(a). In this state, the terminal voltages v_{x1} and v_{x2} are 0 and $V_{dc}/4$, respectively. The blocking voltages across switches S_{x1}, S_{x2}, S'_{x3}, S'_{x4}, S_{x5}, and S'_{x6} are $V_{dc}/2$, $V_{dc}/2$, $V_{dc}/4$, $V_{dc}/4$, $V_{dc}/4$, and $V_{dc}/4$, respectively. During this state, capacitors C_1, C_2, and C_{x3} retain their previous voltages, while C_{x4} discharges.

5.2.2.2 State of Operation 2

Switches S_{x1}, S_{x2}, S_{x3}, S_{x4}, S'_{x5}, and S_{x6} are turned ON, allowing current to flow between the DC-link and the loads, as illustrated in Fig. 5.2(b). During this interval, the output voltages v_{x1} and v_{x2} are $V_{dc}/2$ and -$V_{dc}/4$, respectively. The voltage stress across switches S'_{x1}, S'_{x2}, S'_{x3}, S'_{x4}, S_{x5}, and S'_{x6} are $V_{dc}/2$, $V_{dc}/2$, $3V_{dc}/4$, $3V_{dc}/4$, and $V_{dc}/4$, respectively. In this state, capacitor C_1 and C_{x4} discharges, C_2 charges, while C_{x3} retain its previous voltage.

5.2.2.3 State of Operation 3

Switches S'_{x1}, S_{x2}, S'_{x3}, S'_{x4}, S_{x5}, and S_{x6} are turned ON. As shown in Fig. 5.2(c), the current flows between the DC-link and the loads. During this interval, the output voltages v_{x1} and v_{x2} are -$V_{dc}/2$ and 0, respectively. The voltage stress across switches S_{x1}, S'_{x2}, S_{x3}, S_{x4}, S'_{x5}, and S'_{x6} are $V_{dc}/2$, $V_{dc}/2$, $V_{dc}/4$, $V_{dc}/4$, $V_{dc}/4$, and $V_{dc}/4$, respectively. In this state, capacitor C_2 charges, while C_1, C_{x3}, and C_{x4} maintain their previous voltages.

The maximum blocking voltage of the switch in the 5LDO-ANPC converter is $3V_{dc}/4$. Table 5.2 provides the maximum voltage and current stress values of each switch in the 5LDO-ANPC converter. The possible switching combinations for this converter are shown in Table 5.3. For simplicity, the switching states are represented in decimal format. These states can be converted to binary to generate the corresponding switching signals. For example, state $(28)_{10}$ is equivalent to $(011100)_2$, where each bit represents the switching signals S_{x1}, S_{x2}, S_{x3}, S_{x4}, S_{x5}, and S_{x6}, respectively. There are 25 valid states for controlling the converter, many of which include redundant combinations. These redundant states can be utilized to reduce the average switching frequency of the devices, thereby minimizing dynamic power losses and balancing both the DC-link and the flying capacitors.

TABLE 5.1: Comparison of Three-Phase Dual-Output Five-level Topologies

Topologies	DFC-ANPC[17, 38]	Dual C5L-ANPC [16, 36]	Dual 5L-NPC [37]	Modified CMOM[33]	Proposed
No. of Switches	60	48	48	30	36
No. of diodes	0	0	36	0	0
Total Devices (active + passive)	60	48	84	30	36
No. of DC-link Capacitors	2	2	4	2	2
Maximum voltage stress	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/4$	V_{dc}	$3V_{dc}/4$
Boundary Region					

TABLE 5.2: Maximum voltage and current stress on each switch of the 5LDO-ANPC.

S.No.	Switches	Max voltage stress	Max current stress
1	S_{x1}	$V_{dc}/2$	$I_{x1} + I_{x2}$
2	S'_{x1}	$V_{dc}/2$	$I_{x1} + I_{x2}$
3	S_{x2}	$V_{dc}/2$	$I_{x1} + I_{x2}$
4	S'_{x2}	$V_{dc}/2$	$I_{x1} + I_{x2}$
5	S_{x3}	$3V_{dc}/4$	I_{x1}
6	S'_{x3}	$3V_{dc}/4$	I_{x1}
7	S_{x4}	$V_{dc}/4$	I_{x1}
8	S'_{x4}	$V_{dc}/4$	I_{x1}
9	S_{x5}	$3V_{dc}/4$	I_{x2}
10	S'_{x5}	$3V_{dc}/4$	I_{x2}
11	S_{x6}	$V_{dc}/4$	I_{x2}
12	S'_{x6}	$V_{dc}/4$	I_{x2}

TABLE 5.3: 5LDO-ANPC Switching States, Corresponding Output Voltage, DC-Link and Flying Capacitor Charging State

S.No.	Switching Signals	Output Voltages (V_{dc})		Capacitor state ($i_{x1} > 0$), ($i_{x2} > 0$)				Count
	Decimal of [S_{x1} S_{x2} S_{x3} S_{x4} S_{x5} S_{x6}]	v_{x1}	v_{x2}	C_1	C_2	C_{x3}	C_{x4}	
1	47, 63	0.5	0.5	↓	-	-	-	2
2	62, 46, 45	0.5	0.25	↓, ↓, ↓	-, -, -	-, -, -	↑, ↑, ↓	3
3	44	0.5	0	↓	-	-	-	1
4	61	0.5	-0.25	↓	↑	-	↓	1
5	60	0.5	-0.5	↓	↑	-	-	1
6	39,43,59	0.25	0.5	↓, ↓,↓	-, -, -	↓, ↑, ↑	-, -,-	3
7	5, 37, 38, 41, 42, 58	0.25	0.25	-,-, -, -, ↓,↓	-, -, -, -, -, -	↓, ↓, ↓, ↑, ↑, ↑	↓, ↓, ↑, ↓, ↑, ↑	6
8	4, 7, 36, 40	0.25	0	-,-, -, ↓	-, -, -, -	↓, ↓, ↓, ↑	-, -, -, -	4
9	57	0.25	-0.25	↓	↑	↑	↓	1
10	56	0.25	-0.5	↓	↑	↑	-	1
11	35	0	0.5	↓	-	-	-	1
12	1, 13, 33, 34	0	0.25	-, -, - ↓	-	-	↓, ↓, ↓, ↑	4
13	0, 3, 12, 15, 31, 32	0	0	-	-	-	-	6
14	2, 14, 29, 30	0	-0.25	-	-, -,↑, -	-	↑, ↑, ↓, ↑	4
15	28	0	-0.5	-	↑	-	-	1
16	55	-0.25	0.5	↓	↑	↓	-	1
17	54	-0.25	0.25	↓	↑	↓	↑	1
18	8, 11, 23, 27	-0.25	0	-	-,-, ↑, -	↑, -, ↓, ↑	-	4
19	10, 21, 22, 25, 26, 53	-0.25	-0.25	-	-, ↑, ↑, ↑, -, ↑	↑, ↓, ↓, ↑, ↑, ↓	↑, ↓, ↑, ↓, ↑, ↓	6
20	20, 24, 52	-0.25	-0.5	-	↑, ↑, ↑	↓, ↑, ↓	-	3
21	51	-0.5	0.5	↓	↑	-	-	1
22	50	-0.5	0.25	↓	↑	-	↑	1
23	19	-0.5	0	-	↑	-	-	1
24	17, 18, 49	-0.5	-0.25	-	↑, ↑, ↑	-	↓, ↑, ↓	3
25	16, 48	-0.5	-0.5	-	↑	-	-	2
Total								62

(↑) charging, (↓) discharging and (-) NA. S'_{x1}, S'_{x2}, S'_{x3}, S'_{x4}, S'_{x5}, S'_{x6} are switched complementary to S_{x1}, S_{x2}, S_{x3}, S_{x4}, S_{x5}, S_{x6} respectively.

5.2.3 Operating Region

Most dual-output converters minimize device count and overall size; however, they encounter a significant limitation in their operating region. The unavailability of certain switching combinations restricts the modulation indices of the converter. For the operation of a dual output converter, two reference signals are required to generate switching signals. For three-phase operation, the reference signals for the A, B, and C phases are:

$$v_{refAj}(t) = m_j sin(\omega_j t + \theta_j)$$
$$v_{refBj}(t) = m_j sin(\omega_j t - 2\pi/3 + \theta_j)$$
$$v_{refCj}(t) = m_j sin(\omega_j t + 2\pi/3 + \theta_j)$$

. Where j = 1,2 and m_j is the modulation index in the range of 0 to 1, $\omega_j = 2\pi f_j$ is the fundamental angular frequencies, θ_j are the initial phase angles. In reduced switch count dual output converters such as NSI, NPP, RSC-DT (DO-T-TLC) and DO-NPC-TLI, the upper reference signal should be greater than the lower to prevent invalid switching states. Therefore, DC offsets are added into two sets of reference signals. For instance, the NSI imposes the condition that $v_{ref1} \geq v_{ref2}$ at all times [70]. In the case of (1) NPC-DO [26], many operating states requiring neutral or zero are unavailable, (2) NPP has only half of the operational region and imposes the same condition as that of NSI [21], and (3) CMOM and modified CMOM do not have a complete operational region [27, 28]. In contrast, 5LDO-ANPC does not face this limitation; despite having a reduced switch count, it retains all the voltage states characteristic of a conventional five-level ANPC. This section analyzes and explores the region of operation of 5LDO-ANPC. Fig. 5.3 offers a graphical depiction of the switching states outlined in Table 5.3. The graph illustrates the possible voltage levels at the v_{x1} and v_{x2} output terminals. This representation helps to clarify the converter's boundary region. The entire area enclosed by the voltage states represents all configurations of the voltage reference signals that can be utilized. Consequently, an output voltage ranging from -0.5 to 0.5 V_{dc} corresponds to variations in the reference signal. Based on the boundary region shown in Fig. 5.3, there are no restrictions on one output reference signal with respect to the other for 5LDO-ANPC. Both reference signals operate independently of each other.

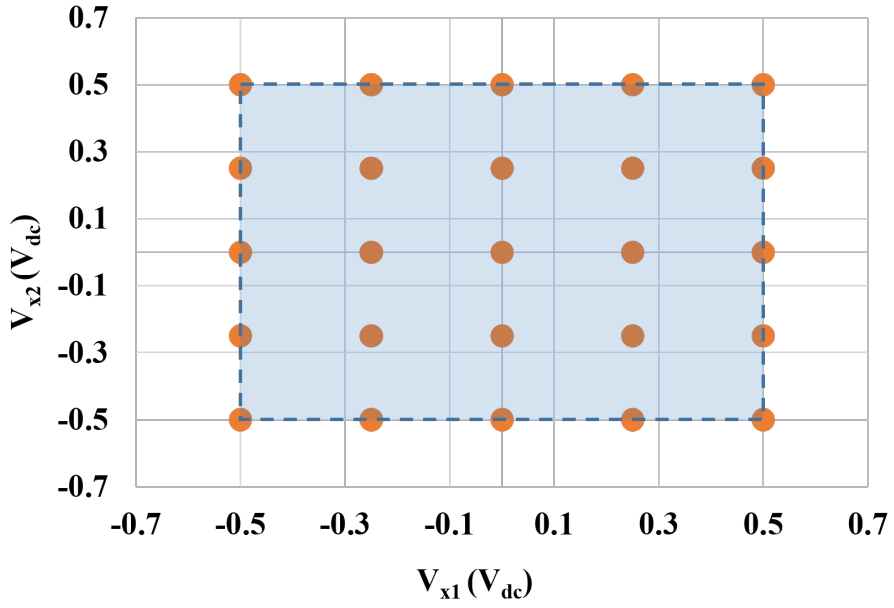

FIGURE 5.3: Graphical depiction of the region of operation and switching states.

5.2.4 Modes of Operation of 5LDO-ANPC

For the independent operation of a dual output converter, two operating modes are classified based on the modulating frequency of two outputs: common and different frequency (CF & DF) modes. A dual-output converter should be capable of operating independently at both CF and DF modes. The operation of the 5LDO-ANPC converter in CF and DF modes is detailed as follows.

5.2.4.1 Common Frequency Mode

The common frequency (CF) mode refers to the scenario where both outputs of the inverter operate at the same frequency. Within this mode, there are two variations: one with phase shift and one without. The converter is operated in CF mode with varying modulation indices ($m_{1,2}$) and a phase shift (ϕ), where $\phi = |\theta_2$ - $\theta_1|$. Let $f_1 = f_2 = f$ and $\theta_1 = \theta_2 \Rightarrow \phi = 0$, this for CF mode without phase shift. Fig. 5.4(a) shows the projection of reference signals onto the boundary region at $m_1 = 1$, $m_2 = 0.9$, and $f_1 = f_2 = 50$ Hz.

CF mode with phase shift is when, $f_1 = f_2 = f$ and $\theta_1 \neq \theta_2$. The phase angle shift, $\phi = |\theta_2$ - $\theta_1|$ between the two sets of output phase voltages. Fig. 5.4(b) shows the projection of reference signals onto the boundary region at $m_1 = m_2 = 0.9$ and $f_1 = f_2 = 50$ Hz with a phase shift of 30° and Fig. 5.4(c) shows the projection of reference signals in the boundary

region at $m_1 = m_2 = 0.8$ and $f_1 = f_2 = 50$ Hz with a phase shift of 60°. The reference signals v_{refA1} and v_{refA2} of phase A are operated with modulation indices between 0 and 1. As it can be observed, there is no phase angle restriction in this case. Applications of the CF mode are grid-tied inverters, UPS, UPQC systems, motor drives, etc. A phase shift between two outputs is significant when operating multi-phase motors [71].

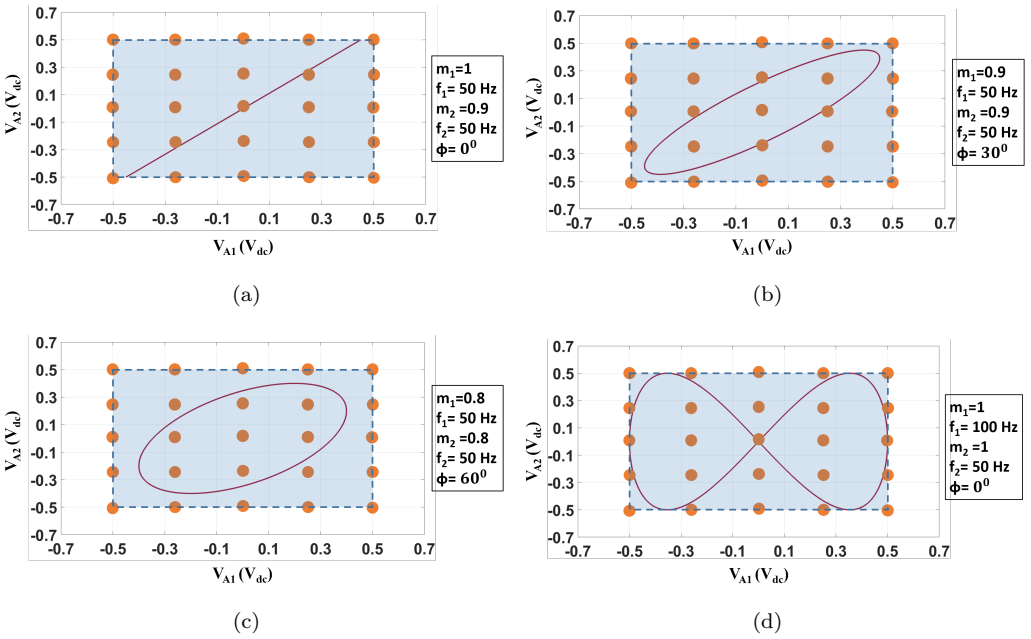

FIGURE 5.4: Projection of reference signals onto the 5LDO-ANPC converter's boundary region under (a) CF with $m_1 = 1$, $m_2 = 0.9$, (b) CF with $m_1 = m_2 = 0.9$ and phase shift of 30°, (c) CF with $m_1 = m_2 = 0.8$ and phase shift of 60° (d) DF with $m_1 = m_2 = 1$.

5.2.4.2 Different Frequency Mode

Different frequency (DF) operation in an inverter typically refers to the ability of the inverter to generate two output voltages at different frequencies ($f_1 \neq f_2$); consequently, its currents are different. The converter can operate in DF mode at various load frequencies. The projection of reference signal onto boundary region for $m_1 = m_2 = 1$ and $f_1 = 100$ Hz, $f_2 = 50$ Hz as shown in Fig. 5.4 (d). There is no restriction on the modulation index, and the 5LDO-ANPC converter can operate with any value of f_1 and f_2. This is a significant advantage compared to other reduced switch count dual-output topologies. Most of them have constrain of $0 < m_1 + m_2 \leq 1$ while choosing modulation indices of two outputs. The reference signal v_{refA2} is always smaller than the lower carrier for maintaining this constraint in different frequency modes. As a result, they provide reduced voltage levels.

Low modulation indices reduce the levels in both phase and line voltage. However, 5LDO-ANPC topology has no such restriction; with this advantage, it can generate the exact value of output voltages as that of conventional five-level ANPC. Different frequency operations find applications in more electric aircraft (MEA), limited to 400 Hz, dual motor variable speed drives (VSDs) operated at frequencies rated at 50Hz/60Hz, etc. Dual motor drives are also utilized in all-terrain electric vehicles (ATEVs).

5.3 Finite Control Set Model Predictive Control (FCS-MPC) of 5LDO-ANPC

FCS-MPC is effective at addressing multi-objectives and constraints of non-linear systems. With this approach, the converter's two independent three-phase load currents closely follow the reference signals while ensuring balanced voltages across the DC-link and flying capacitors. Additionally, the approach allows system nonlinearities and constraints to integrate seamlessly into the controller design.

5.3.1 Mathematical Model of 5LDO-ANPC

5.3.1.1 Continous Time Model

From Fig. 5.1, the dynamic equations of two outputs and capacitors in a continuous time model are derived as follows.

$$\frac{di_{xj}(t)}{dt} = \frac{[v_{xj}(t) - i_{xj}(t)R_{xj}]}{L_{xj}}, \frac{dv_{cj}(t)}{dt} = \frac{i_{cj}(t)}{C_j} \tag{5.1}$$

$$\frac{dv_{cx3}(t)}{dt} = \frac{i_{cx3}(t)}{C_{x3}}, \frac{dv_{cx4}(t)}{dt} = \frac{i_{cx4}(t)}{C_{x4}} \tag{5.2}$$

In this context, v_{xj} represents output voltages of the converter at j^{th} port (where j=1, 2), i_{cj} denotes the currents flowing through the DC-link capacitor C_j, i_{cx3} and i_{cx4} are the current through flying capacitors. Here, "x" refers to all x $\in$ {A, B, and C}. According to the relationships outlined in Table II, the output voltages v_{x1} and v_{x2} can be expressed

in terms of the capacitor voltages v_{c1}, v_{c2}, v_{cx3} and v_{cx4}, as well as the switching signals:

$$\begin{aligned} v_{x1}(t) = v_{c1}(t)S_{x1}(t)S_{x3}(t) - v_{c2}S_{x2}(t)(1 - S_{x3}(t)) - \\ v_{cx3}(t)(S_{x3}(t) - S_{x4}(t)) \end{aligned} \tag{5.3}$$

$$\begin{aligned} v_{x2}(t) = v_{c1}(t)S_{x1}(t)S_{x5}(t) - v_{c2}S_{x2}(t)(1 - S_{x5}(t)) - \\ v_{cx4}(t)(S_{x5}(t) - S_{x6}(t)) \end{aligned} \tag{5.4}$$

Similarly, the capacitor currents can be expressed in terms of the output currents and the switching signals:

$$i_{c1}(t) = \sum_x \Big(-S_{x1}(t)\Big(S_{x3}(t)i_{x1}(k) + S_{x5}(t)i_{x2}(t)\Big)\Big) \tag{5.5}$$

$$i_{c2}(t) = \sum_x \Big(S_{x2}(t)\Big(S'_{x3}(t)i_{x1}(k) + S'_{x5}(t)i_{x2}(t)\Big)\Big) \tag{5.6}$$

$$i_{cx3}(t) = (S_{x3}(t) - S_{x4}(t))i_{x1}(t) \tag{5.7}$$

$$i_{cx4}(t) = (S_{x5}(t) - S_{x6}(t))i_{x2}(t) \tag{5.8}$$

5.3.1.2 Discrete-time model

Using the Euler method, transforming the output current and capacitor voltages of continuous-time equations into their discrete forms as follows:

$$i_{xj}(k+1) = i_{xj}(k)\alpha_{xj} + \frac{T_s v_{xj}(k)}{L_{xj}} \tag{5.9}$$

DC-link and flying Capacitor :

$$v_{cj}(k+1) = v_{cj}(k) + \beta_j i_{cj}(k) \tag{5.10}$$

$$v_{cx3}(k+1) = v_{cx3}(k) + \beta_{x3} i_{cx3}(k) \tag{5.11}$$

$$v_{cx4}(k+1) = v_{cx4}(k) + \beta_{x4} i_{cx4}(k) \tag{5.12}$$

where, $\alpha_{xj} = (1 - \frac{T_s R_{xj}}{L_{xj}})$, $\beta_j = \frac{T_s}{C_j}, \beta_{x3} = \frac{T_s}{C_{x3}}$, $\beta_{x4} = \frac{T_s}{C_{x4}}$ and T_s is sampling period.
The state-space model of the converter in discrete form can be represented as follows,

$$z_x(k+1) = Az_x(k) + Bu(k) \tag{5.13}$$

where,

$z_x(k) = \begin{bmatrix} i_{x1}(k) & i_{x2}(k) & v_{c1}(k) & v_{c2}(k) & v_{cx3}(k) & v_{cx4}(k) \end{bmatrix}^T$,

$$u_x(k) = \begin{bmatrix} S_{x1}(k)S_{x3}(k) \\ S_{x2}(k)S'_{x3}(k) \\ S_{x3}(k) - S_{x4}(k) \\ S_{x1}(k)S_{x5}(k) \\ S_{x2}(k)S'_{x5}(k) \\ S_{x5}(k) - S_{x6}(k) \end{bmatrix} \tag{5.14}$$

$A_x = diag[\alpha_{x1}, \alpha_{x2}, 1, 1, 1, 1]$

$$B_x = \begin{bmatrix} \frac{v_{c1}}{L_{x1}} & -\frac{v_{c2}}{L_{x1}} & -\frac{v_{cx3}}{L_{x1}} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{v_{c1}}{L_{x2}} & -\frac{v_{c2}}{L_{x2}} & -\frac{v_{cx4}}{L_{x2}} \\ -\beta_1 i_{x1} & 0 & 0 & -\beta_1 i_{x2} & 0 & 0 \\ 0 & \beta_2 i_{x1} & 0 & 0 & \beta_2 i_{x2} & 0 \\ 0 & 0 & \beta_{x3} i_{x1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \beta_{x4} i_{x2} \end{bmatrix}$$

5.3.1.3 Control target

For optimal converter operation, the output currents must track the specified reference signals, and the DC-bus and flying capacitor voltages should be maintained at $V_{dc}/2$ and $V_{dc}/4$. Thus, the desired reference $z_x^*(k+1)$ can be given as follows:

$$z_x^*(k+1) = \begin{bmatrix} i_{x1ref}(k+1) & i_{x2ref}(k+1) & \frac{v_{dc}}{2} & \frac{v_{dc}}{2} & \frac{v_{dc}}{4} & \frac{v_{dc}}{4} \end{bmatrix}^T$$

where, $i_{xjref}(k+1)$ is the reference current. For A-phase $i_{Ajref}(k+1) = I_{Aj}(sin\omega_j(k+1)+\phi_j)$ and I_{Aj}, ω_j, ϕ_j are the amplitude, angular frequency and phase angle of the reference current at port j. The system state predictions can be obtained by directly evaluating the nonlinear system for each possible switching combination. Each predicted state is then assessed using a quadratic cost function $J_{xn}(k)$:

$$J_{xn}(k) = e_{xn}(k+1)^T Q e_{xn}(k+1) \tag{5.15}$$

where $e_{xn}(k+1) = z_{xn}(k+1) - z_{xn}^*(k+1)$ and Q is weighting matrix represented as

$$Q = diag[\lambda_{x1}, \lambda_{x2}, \lambda_3, \lambda_4, \lambda_{x5}, \lambda_{x6}] \tag{5.16}$$

where λ_{x1}, λ_{x2}, λ_3,λ_4, λ_{x5} and λ_{x6} serve as weighting factors for current, dc-link and flying capacitors respectively. They minimize tracking errors and achieve uniform tracking performance. The optimal switching combination is then calculated by minimizing the cost function, expressed as follows:

$$s_x^{opt}(k) = arg\{minJ_{xn}(k)\} \tag{5.17}$$

The block diagram in Fig. 5.5 summarizes the FCS-MPC.

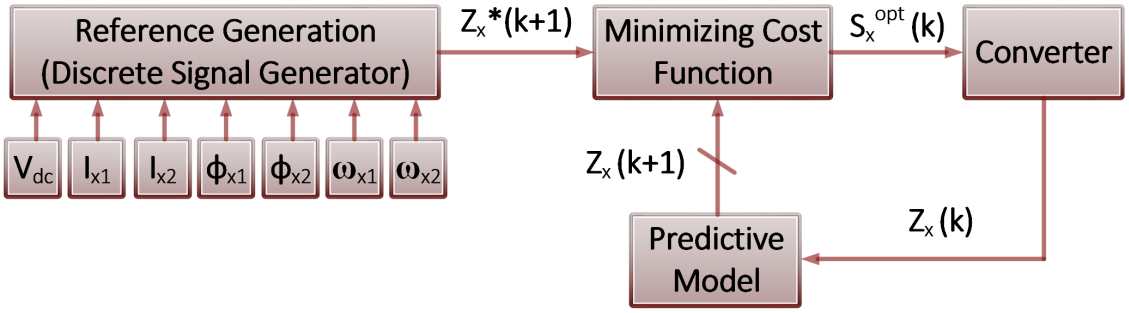

FIGURE 5.5: Block diagram of the FCS-MPC algorithm.

5.3.2 DC-Link and Flying Capacitor Voltage Balance

There are two DC-link and six flying capacitors for a three-phase configuration. According to Table 5.3 and by considering Fig. 5.1. The deviation between the capacitor voltages will cause an unbalanced output voltage. Thus, the voltage of C_1, C_2, C_{x3}, C_{x4} needs to be balanced. From the Table 5.3, for $(i_{x1} > 0)$, $(i_{x2} > 0)$ it can be seen that capacitors will charge, discharge, and bypass depending upon state numbers listed in the table. For 5LDO-ANPC several redundant switching combinations can produce the same output voltage but have different effects on the capacitor voltages. FCS-MPC exploits this redundancy by selecting switching states that help to balance the capacitor voltages while maintaining the desired output. The cost function of FCS-MPC is used to minimize the difference between the actual and desired capacitor voltages. The main objective is to reduce the load current error while effectively maintaining the charging and discharging of capacitors. At each sampling interval, FCS-MPC selects the switching state that minimizes the cost function, which in turn balances the capacitor voltages.

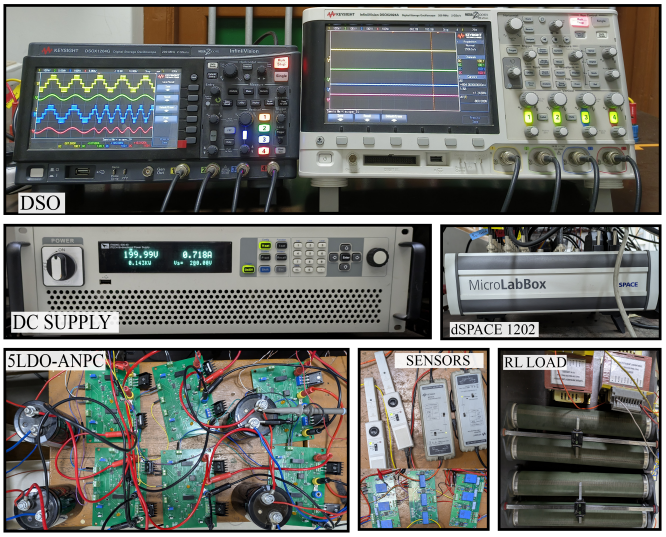

FIGURE 5.6: Experimental setup of 5LDO-ANPC.

TABLE 5.4: Parameters for Simulation and Hardware

Parameter	Value
DC-link voltage (V_{dc})	200 V
DC-Link capacitor ($C_1 = C_2$)	2200 μF
Flying Capacitor ($C_{x3} = C_{x4}$)	470 μF
Load Resistance ($R_{x1} = R_{x2}$)	50 Ω
Load Inductance ($L_{x1} = L_{x2}$)	20 mH
Sampling Time (T_s)	50 μs
Weighting Factor ($\lambda_{x(1,2)}$, $\lambda_{(3,4)}$, $\lambda_{x(5,6)}$)	2.5, 0.3, 0.1

5.4 Simulation and Experimental Verification

The proposed 5LDO-ANPC converter is implemented using MATLAB/Simulink and validated with hardware experiments. The FCS-MPC algorithm is programmed within a Simulink function block, utilizing a T_s of 50 μs. The model is validated through simulations of the CF and DF output modes with linear loads. Additionally, the converter DC-link and flying capacitor voltages are analyzed under these operating conditions. The hardware prototype of the converter is built in the laboratory, and a *dSPACE MicroLabBox* programmable controller is employed to generate the gate control signals. The complete hardware setup for the experiment is shown in Fig. 5.6. Table 5.4 lists the system parameters considered for the simulation. Identical RL loads, representing AC loads, are used across two output ports.

5.4.1 Simulation Results

5.4.1.1 Case 1: Common frequency (CF) mode

In CF mode, the two output frequencies are $f_1 = f_2 = 50$ Hz. Fig. 5.7(a) illustrates the simulation result for both output voltages (v_{A1}, v_{A2}) and their corresponding load currents (i_{A1}, i_{A2}) under CF mode of operation with equal modulation indices, $m_1 = m_2 = 0.8$. In contrast, Fig. 5.7(b) shows the simulation result of the DC-link and flying capacitor voltages balancing under CF mode with the same modulation indices, $m_1 = m_2 = 0.8$. Fig. 5.7(c) displays the outcomes for both output voltages (v_{A1},v_{A2}) and its corresponding load current (i_{A1},i_{A2}) under CF mode of operation with the same modulation indices $m_1 = m_2 = 0.8$ and phase shift $\phi = 30°$.

5.4.1.2 Different frequency (DF) mode

In this, two outputs of the 5LDO-ANPC converter are operated in DF modes, and performance is evaluated. Fig. 5.7(d) shows the simulation result for both output voltages (v_{A1},v_{A2}), and its corresponding load current (i_{A1},i_{A2}). The converter is operated with frequencies $f_1 = 50$ Hz, $f_2 = 100$ Hz with modulation indices $m_1 = m_1 = 0.8$.

5.4.1.3 Dual Drive

The performance of the proposed 5LDO-ANPC converter is evaluated using two identical PMSM motors. The parameters of each motor are as follows: number of pole pairs (p) = 2, stator phase resistance (R_s) = 4.765 Ω, stator phase inductance (L_s) = 0.014 H, magnetic flux linkage (ψ_f) = 0.1848 Wb, rotational inertia (J) = 0.0001051 kg·m^2, rated speed (N) = 3750 r/min, and rated torque (T) = 1.7 Nm. Fig. 5.8 presents the converter's performance while driving two motors operating at the same speed. The converter operates in common frequency (CF) mode with modulation indices $m_1 = m_2 = 0.8$ and output frequencies $f_1 = f_2 = 50$ Hz. The DC link voltage is set to $V_{dc} = 300$ V. Under these conditions, both motors maintain a speed of 1500 RPM and deliver a torque of 1 Nm. Fig. 5.9 shows the converter's performance when driving the two motors at different speeds. In this case, the converter operates in different frequency (DF) mode with $m_1 = m_2 = 0.8$, $f_1 = 50$ Hz, and $f_2 = 60$ Hz, while keeping $V_{dc} = 300$ V. Consequently, the motors run at different speeds: $N_1 = 1500$ RPM and $N_2 = 1800$ RPM, each delivering a torque of 1 Nm. As observed, motor 2 maintains its speed at 1800 RPM, and the performance of motor 1

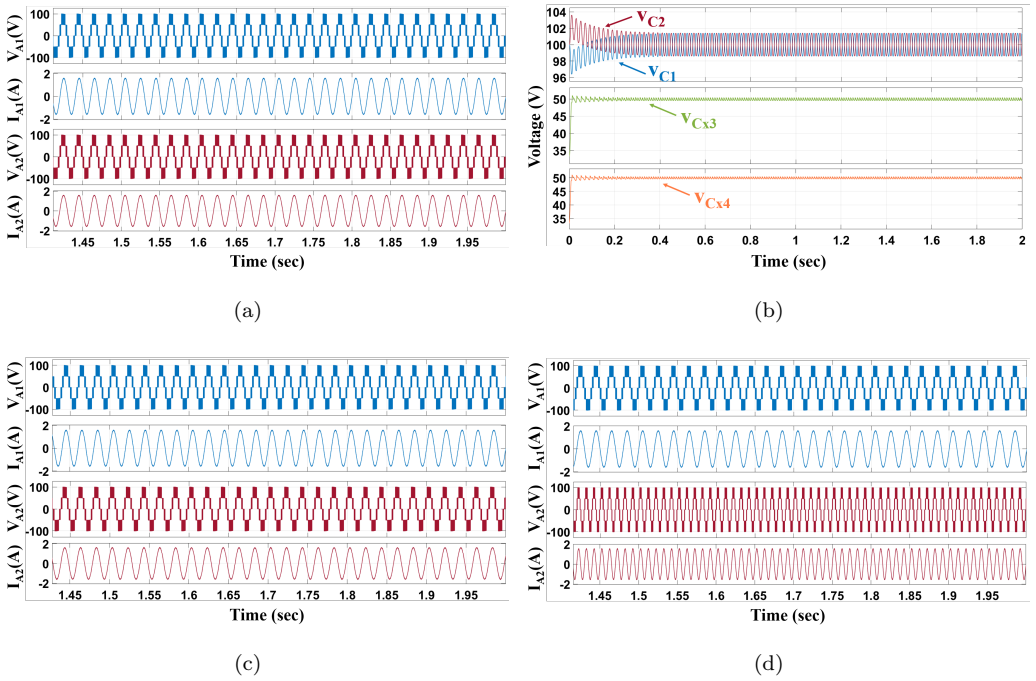

FIGURE 5.7: Simulation result (a) output voltages (v_{A1},v_{A2}) and currents (i_{A1},i_{A2}), under CF mode with $m_1 = m_2 = 0.8$, (b) DC-link and flying capacitors voltage balancing under CF mode with $m_1 = m_2 = 0.8$, (c) output voltages (v_{A1},v_{A2}) and currents (i_{A1},i_{A2}), under CF mode with $m_1 = m_2 = 0.8$ and phase shift $\phi = 30°$, (d) output voltages (v_{A1},v_{A2}) and currents (i_{A1},i_{A2}) under DF mode with $m_1 = m_2 = 0.8$.

remains unaffected, confirming that the two outputs of the 5LDO-ANPC converter operate independently.

5.4.2 Experimental Results

5.4.2.1 Case 1: Common frequency (CF) mode

In CF mode, the two output frequencies are $f_1 = f_2 = 50$ Hz. Fig. 5.10(a) illustrates the experimental result for both output voltages (v_{A1}, v_{A2}) and their corresponding load currents (i_{A1}, i_{A2}) under CF mode of operation with equal modulation indices, $m_1 = m_2 = 0.8$. In contrast, Fig. 5.10(b) shows the experimental result of the DC-link and flying capacitor voltages balancing under CF mode with the same modulation indices, $m_1 = m_2 = 0.8$. As can be observed from simulation and experimental results, V_{C1}, V_{C2}, V_{CA3}, and V_{CA4} are balanced at 99.96 V, 100.1 V, 49.65 V, and 49.65 V, respectively. Fig. 5.10(c) presents the experimental result for output voltages (v_{A1}, v_{A2}) and their corresponding load currents (i_{A1}, i_{A2}) under CF mode with different modulation indices,

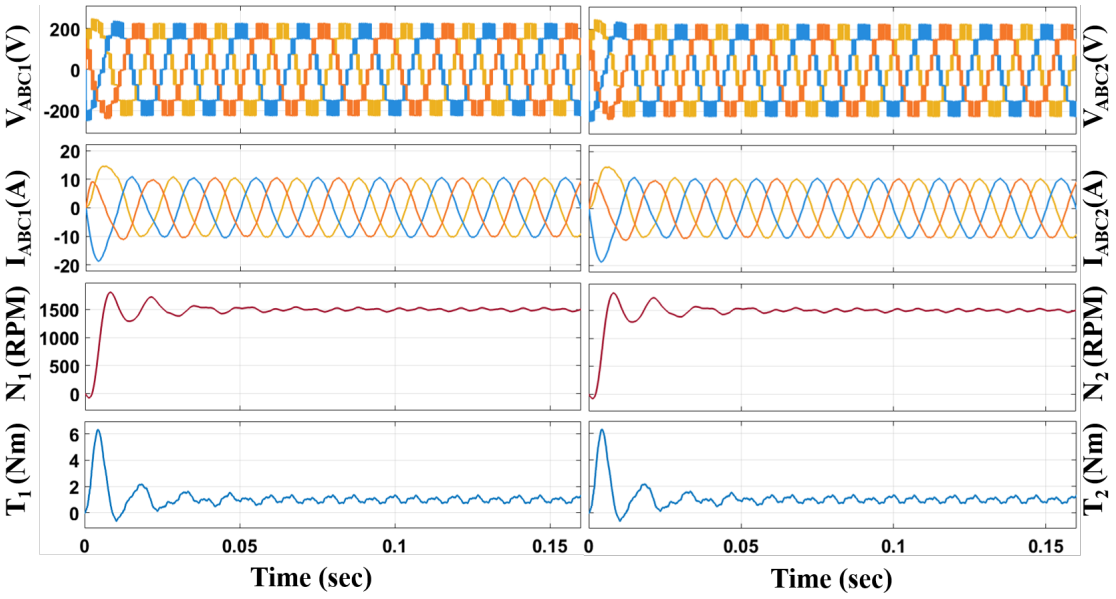

FIGURE 5.8: Simulation result for the output line voltages (v_{ABC1}, v_{ABC2}), currents (i_{ABC1},i_{ABC2}), speeds (N_1, N_2), and torque (T_1, T_2) for same speed of operation.

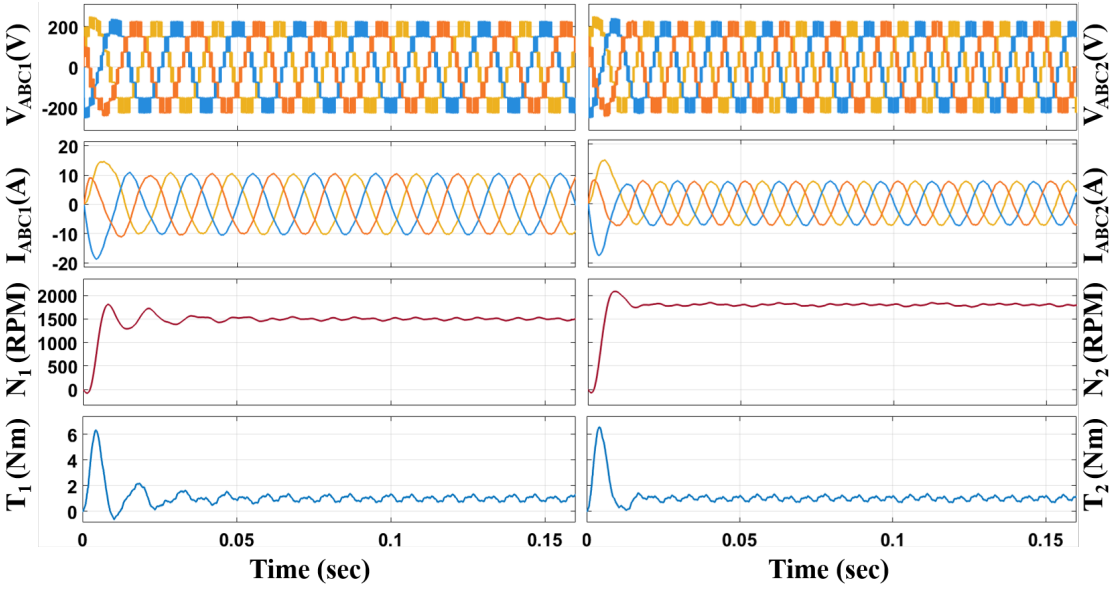

FIGURE 5.9: Simulation result for the output line voltages (v_{ABC1}, v_{ABC2}), currents (i_{ABC1},i_{ABC2}), speed (N_1, N_2), and torque (T_1, T_2) for different speed of operation.

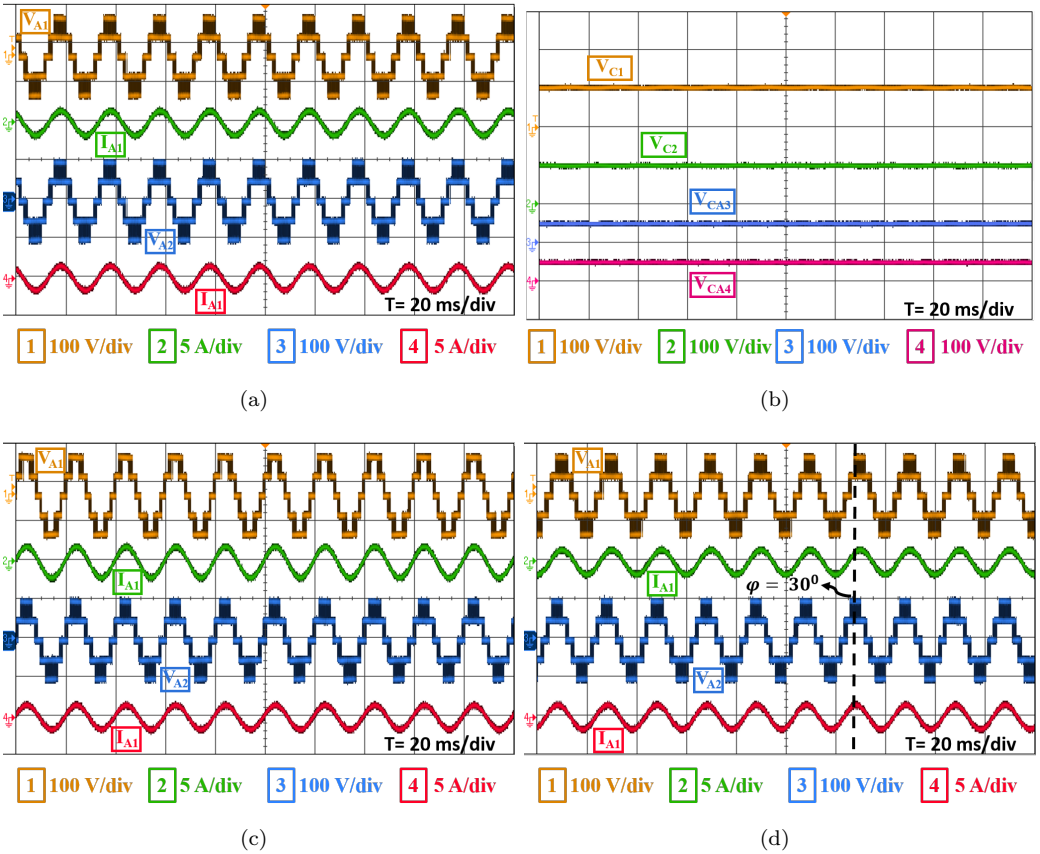

FIGURE 5.10: Experimental result (a) output voltages (v_{A1},v_{A2}) and currents (i_{A1},i_{A2}), $m_1 = m_2 = 0.8$, (b) DC-link and flying capacitors voltage balancing, CF mode $m_1 = m_2 = 0.8$, (c) output voltages (v_{A1},v_{A2}) and currents (i_{A1},i_{A2}), $m_1 = 1$, $m_2 = 0.8$, and (d) output voltages (v_{A1},v_{A2}) and currents (i_{A1},i_{A2}) having same modulation indices $m_1 = m_2 = 0.8$ and phase shift $\phi = 30°$.

$m_1 = 1$ and $m_2 = 0.8$. Fig. 5.10(d) displays the outcomes for both output voltages (v_{A1},v_{A2}) and its corresponding load current (i_{A1},i_{A2}) under CF mode of operation with the same modulation indices $m_1 = m_2 = 0.8$ and phase shift $\phi = 30°$. As observed, the converter generates five voltage levels at its output ports: -V_{dc}/2, -V_{dc}/4, 0, +V_{dc}/4, and +V_{dc}/2.

5.4.2.2 Different frequency (DF) mode

In this, two outputs of the 5LDO-ANPC converter are operated in different frequency modes, and performance is evaluated. Fig. 5.11(a) presents the experimental result for both output voltages (v_{A1},v_{A2}), and its corresponding load current (i_{A1},i_{A2}). The converter is operated with frequencies $f_1 = 50$ Hz, $f_2 = 100$ Hz with modulation indices $m_1 = m_1 = 0.8$.

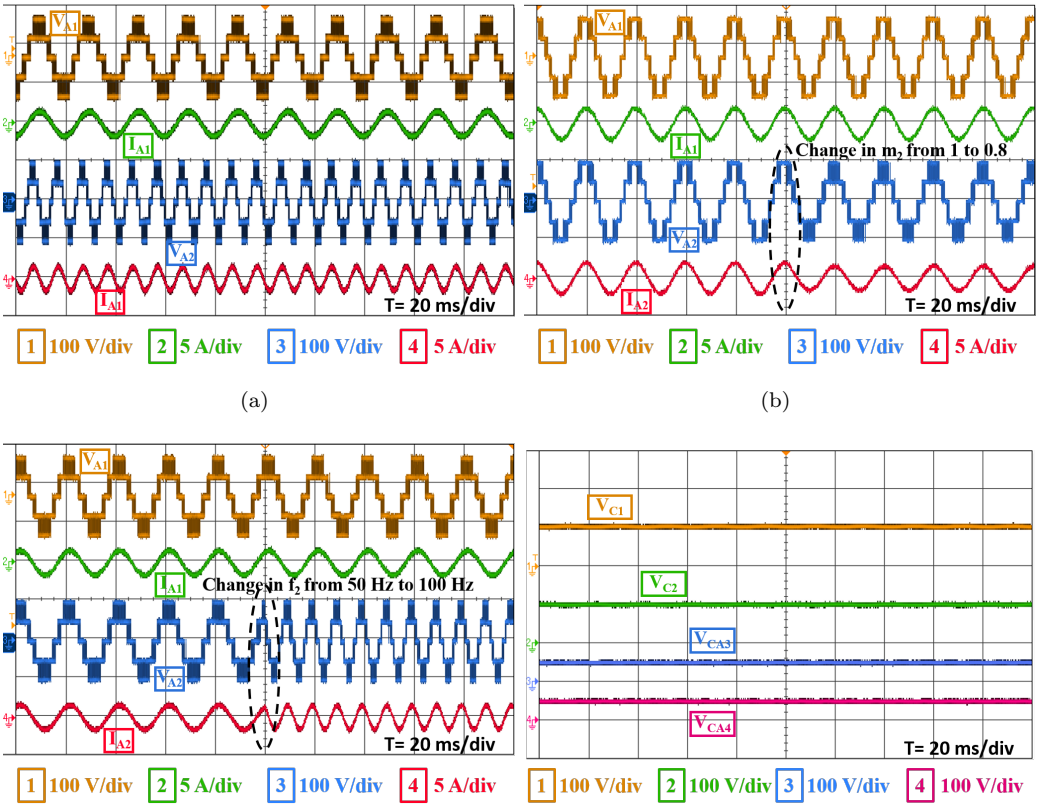

FIGURE 5.11: Experimental result (a) output voltages (v_{A1},v_{A2}) and currents (i_{A1},i_{A2}) with $m_1 = m_2 = 0.8$ under DF mode, (b) sudden change in modulation index of second output terminal under CF mode, (c) output voltages (v_{A1},v_{A2}) and currents (i_{A1},i_{A2}) for sudden change frequency of second output terminal with $m_1 = m_2 = 0.8$ and (d) DC-link and flying capacitors voltage balancing for sudden change in modulation index of the second output terminal.

5.4.2.3 Dynamic Performance

The converter's performance is evaluated across four scenarios: sudden changes in the modulation index, a mode transition, start-up, and shutdown.

(a) Modulation Change: In this scenario, the converter performance is evaluated under a sudden change in modulation index under the CF mode of operation with $m_1 = 0.8$ and m_2 changed from 1 to 0.8 and $f_1 = f_2 = 50$ Hz as shown in Fig. 5.11(b). Fig. 5.11(d) shows the balancing of the capacitors in this case. As can be observed, there is a negligible change in capacitor voltage.

(b) Mode Change: In this scenario, the converter's performance is assessed under the sudden change in mode. Initially, the converter is operating in CF mode, where $m_1 = m_2 = 0.8$, with $f_1 = f_2 = 50$ Hz. Then a sudden change in the frequency at the second terminal,

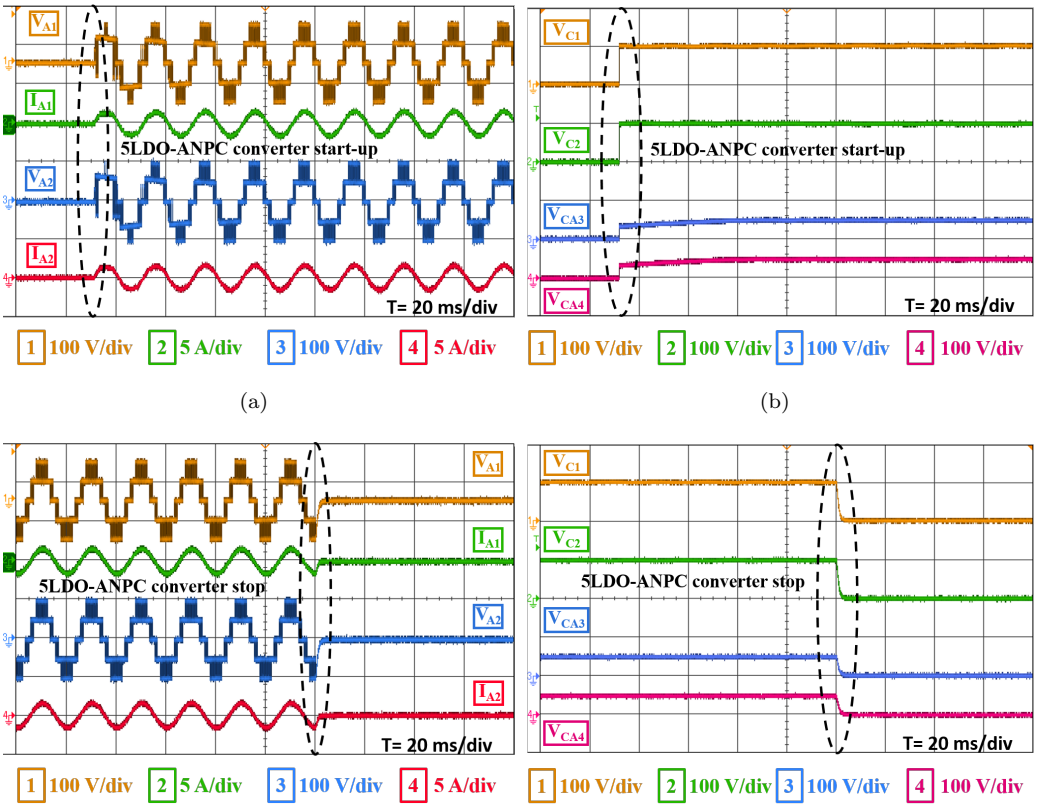

FIGURE 5.12: Experimental results under CF mode with modulation indices $m_1 = m_2 = 0.8$: (a) output voltages (v_{A1}, v_{A2}) and corresponding load currents (i_{A1}, i_{A2}) at the start-up, (b) voltage balancing of the DC-link and flying capacitors at the start-up (c) output voltages (v_{A1}, v_{A2}) and corresponding load currents (i_{A1}, i_{A2}) for the shut-down, (d) voltage balancing of the DC-link and flying capacitors for the shut-down.

from $f_2 = 50$ Hz to 100 Hz, with the same modulation index ($m_1 = m_2 = 0.8$) is observed. Fig. 5.11(c) presents the experimental result for both output voltages (v_{A1},v_{A2}), and its corresponding load current (i_{A1},i_{A2}) under sudden mode change. As can be seen, the two outputs of the converter operated independently.

(c) 5LDO-ANPC Converter Start-up: This scenario evaluates the performance of the 5LDO-ANPC converter during start-up. Fig. 5.12(a) presents the experimental results of the output voltages (v_{A1}, v_{A2}) and their corresponding load currents (i_{A1}, i_{A2}) under CF mode. The converter operates with modulation indices $m_1 = m_2 = 0.8$. Fig. 5.12(b) illustrates the DC-link and flying capacitor voltage balancing behavior during start-up. Initially, all capacitor voltages are at 0 V, i.e., $V_{C1} = V_{C2} = V_{CA3} = V_{CA4} = 0$ V. Once the 5LDO-ANPC converter begins operation, the capacitor voltages stabilize to their nominal

values: $V_{C1} = 99.96\,\text{V}$, $V_{C2} = 100.1\,\text{V}$, $V_{CA3} = 49.65\,\text{V}$, and $V_{CA4} = 49.65\,\text{V}$, demonstrating effective voltage balancing at start-up.

(d) 5LDO-ANPC Converter Shut-down: In this scenario, the converter's performance is analyzed during the shut-down phase of the 5LDO-ANPC converter. Fig. 5.12(c) shows the experimental waveforms of the output voltages (v_{A1}, v_{A2}) and the corresponding load currents (i_{A1}, i_{A2}) in CF mode, with modulation indices maintained at $m_1 = m_2 = 0.8$. Fig. 5.12(d) displays the behavior of the DC-link and flying capacitor voltages during the converter shut-down. Initially, the capacitors are balanced at their nominal operating values: $V_{C1} = 99.96\,\text{V}$, $V_{C2} = 100.1\,\text{V}$, $V_{CA3} = 49.65\,\text{V}$, and $V_{CA4} = 49.65\,\text{V}$. Upon stopping the converter, these voltages drop to $0\,\text{V}$, indicating a complete de-energization of the system and successful power-down operation.

5.5 Current Total Harmonic Distortion (THD)

TABLE 5.5: Comparison of Current THD

Topology/Scenario	Scenario 1		Scenario 2		Scenario 3	
	i_{A1}	i_{A2}	i_{A1}	i_{A2}	i_{A1}	i_{A2}
DFC-ANPC	2.17	2.17	3.24	3.24	2.17	3.35
Dual C5L-ANPC	2.27	2.27	3.36	3.36	2.27	3.41
Dual 5L-NPC	2.4	2.4	3.47	3.47	2.4	3.47
Modified CMOM	2.27	2.27	3.36	3.36	-	-
Proposed	2.27	2.27	3.36	3.36	2.27	3.41

In this comparative analysis, three operating scenarios are evaluated. In the first scenario, referred to as Common Frequency (CF) mode, both loads operate at the same frequency ($f_1 = f_2 = 50$ Hz) and with equal modulation indices ($m_1 = m_2 = 1$). The second scenario is also CF mode but with modulation indices $m_1 = m_2 = 0.8$ and a phase shift of $\phi = 30°$. The third scenario represents a Different Frequency (DF) mode, where the loads operate with different modulation indices and frequencies: $m_1 = 1$, $f_1 = 50$ Hz; $m_2 = 0.8$, $f_2 = 100$ Hz. Table 5.5 presents the current total harmonic distortion (THD) for both outputs under these scenarios using the IPD-PWM technique with a switching frequency of 4 kHz. The results indicate that DFC-ANPC exhibits slightly lower THD across the evaluated scenarios, while Dual 5L-NPC shows higher current THD at both outputs in all cases. Due to operational constraints, the CMOM topology is unable to function in Scenario 3; hence, the current THD values for this case are not reported. The proposed 5LDO-ANPC demonstrates similar THD performance to the Dual C5L-ANPC across all scenarios. Furthermore, when using the Finite Control Set Model Predictive Control

(FCS-MPC) strategy, the proposed 5LDO-ANPC achieves significantly lower THD due to its superior current tracking performance. The current THD values for FCS-MPC in the three scenarios are as follows: in Scenario 1, i_{A1} and i_{A2} have 0.42; in Scenario 2, i_{A1} and i_{A2} have 0.55; and in Scenario 3, i_{A1} have 0.42, whereas i_{A2} have 0.56. These results clearly demonstrate the effectiveness of the 5LDO-ANPC topology in maintaining low current distortion and enhancing dynamic performance when combined with advanced control techniques like FCS-MPC.

The THD performance of the 5LDO-ANPC converter under different load conditions has been analyzed by considering $R_{x1} = 50\ \Omega$, $R_{x2} = 25\ \Omega$, $L_{x1} = 20$ mH, and $L_{x2} = 10$ mH. Figure 5.13 illustrates the THD of both output voltages and currents at different load conditions with modulation indices $m_1 = m_2 = = 1$. The output voltage THD for v_{A1} and v_{A2} are 2.68% and 26.91%, respectively, while the corresponding output current THD values for i_{A1} and i_{A2} are 0.55% and 0.48%. It can be observed that the current THD for both outputs remains nearly identical, indicating effective current regulation by the proposed converter under varying load conditions.

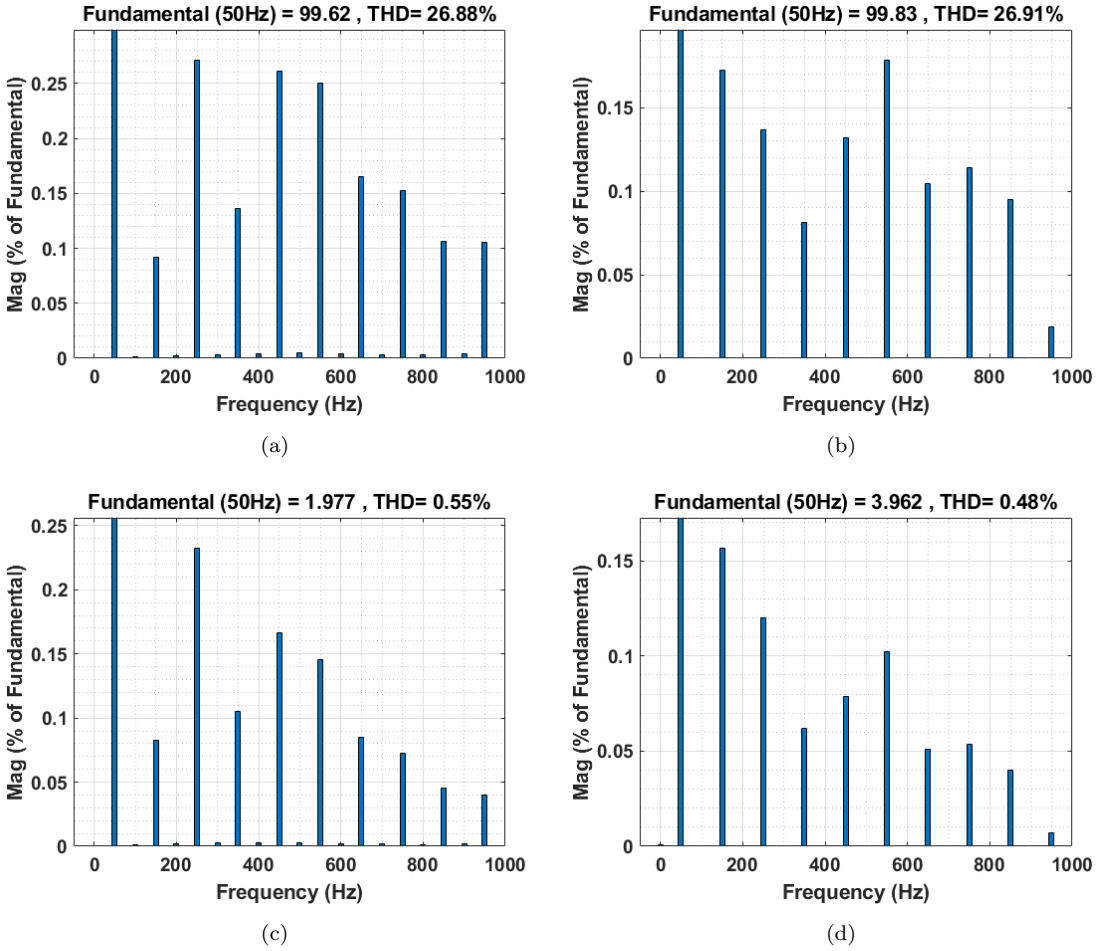

FIGURE 5.13: Total Harmonic Distortion of 5LDO-ANPC at different loads (a) v_{A1}, (b) v_{A2}, (c) i_{A1}, and (d) i_{A2}