Chapter 4

Active Switched Inductor based Converter

4.1 Introduction

The inductor current stress minimization is the challenge associated with high-voltage gain converters. In previous chapters, inductors' current stress is high for fixed power and input voltage. This leads to an increased inductor rating, consequently increasing the overall size of the converter. This chapter investigates the new structures that reduce the current stress of the inductors in high-gain converters. Low voltage stress across semiconductor devices, low component count, and high voltage gain at moderate duty cycle are some of the desirable features of high-gain DC-DC converters. With all these essential features, this chapter demonstrates new high-gain converters. Inserting a basic switched inductor (SL) cell in a boost converter slightly improves the gain by $\frac{1+D}{1-D}$ factor at the cost of three additional diodes in basic SL cells. Instead of three diodes in a basic SL cell, only two active switches are required in an active switched inductor (ASL) network. Several transformerless topologies are available in the literature to achieve high gain. Compared to converter [6], the ASL-based converters have the following advantages.

1. Two power devices are in the two different current-flow paths during switch ON time.

2. Voltage stresses across active switches are lower than the output voltage.

3. Input current division at the low voltage side allows for a low device rating.

Researchers have embraced various power electronics DC-DC converters with the advent of ASL networks, as illustrated in Figure 4.1 and Figure 4.2. Nonetheless, the attained gains from these converters have not been substantial. Delving deeper into the ASL network concept, the following section explores several ASL-derived converters.

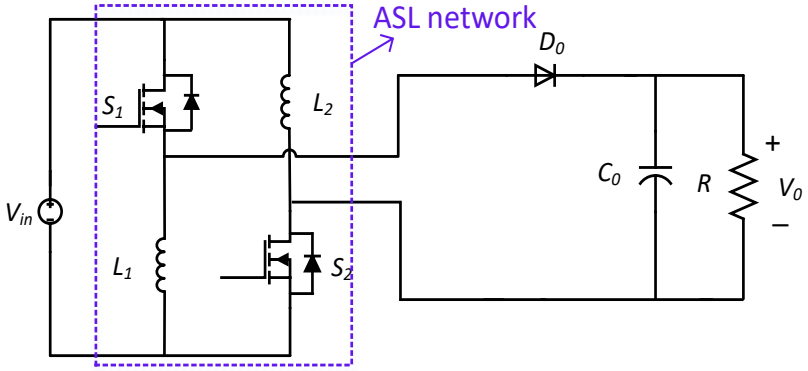

Figure 4.1: ASL based derived converter version-1 [10].

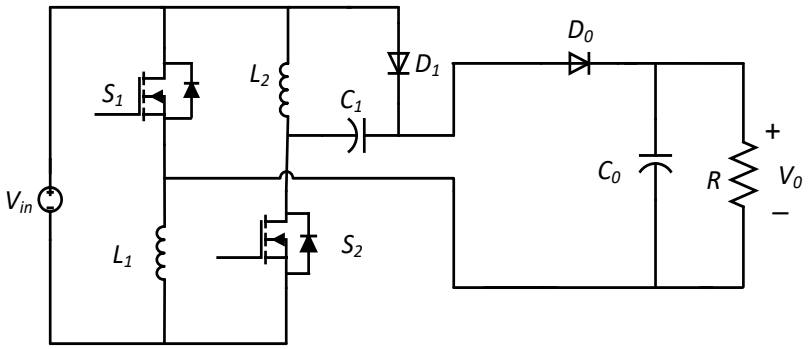

Figure 4.2: ASL based derived converter version-2 [10].

4.2 Proposed ASL derived converters

The ASL-based high gain converter consists of an active switched network composed of two switches and two inductors at the low voltage side and a switched capacitor (SC) network at the high voltage side, as shown in Figure 4.1. Based on this proposal, converter-3 is derived as shown in Figure 4.3.

4.2.1 Operation

The operation of an ASL-derived high gain converter is straightforward. It operates in two states. In the ON state of the switches, the inductors of the ASL network charge in parallel with the source voltage, and in the OFF state, they discharges in series to deliever their energy to the SC network. The used both inductor have same value of inductance ($L_1 = L_2$).

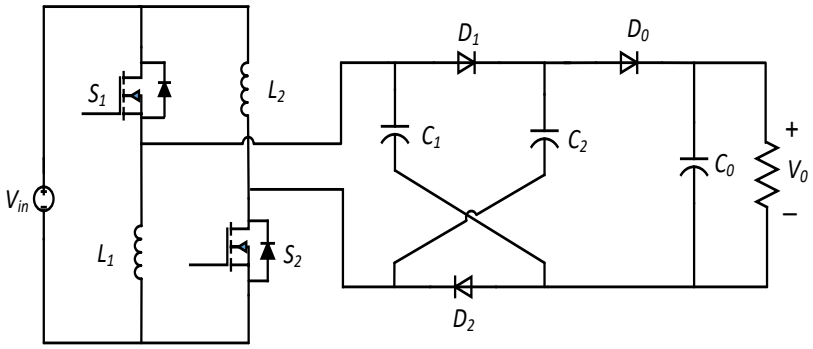

Figure 4.3: ASL derived proposed converter-3.

ON state

ON state is brought into the circuit by applying the gate pulse (V_G) to both switches. In this state, both inductor and capacitors are charged by source voltage V_{in}. The output Diode D_0 is reverse biased, and the output Capacitor C_0 is discharged into load resistance. The steady-state equations for this state are as follows:

$$v_{L1} = V_{L2} = v_{C1} = v_{C2} = V_{in} \tag{4.1}$$

$$v_{C0} = v_0 \tag{4.2}$$

OFF state

During this period, both inductors discharge in series, and their stored energy is transferred into SC to enhance the gain of the ASL converter as shown in Figure 4.5. The equation corresponding to OFF state are;

$$v_{L1} = v_{L2} = \frac{V_{in} + 2v_{C1} - V_0}{2} \tag{4.3}$$

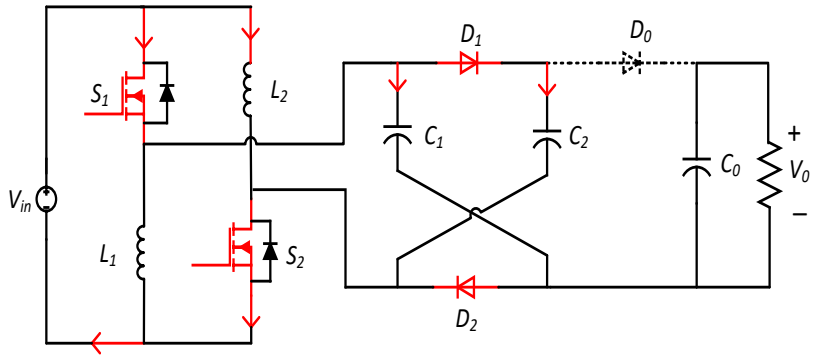

Figure 4.4: ON state operation of ASL based Converter.

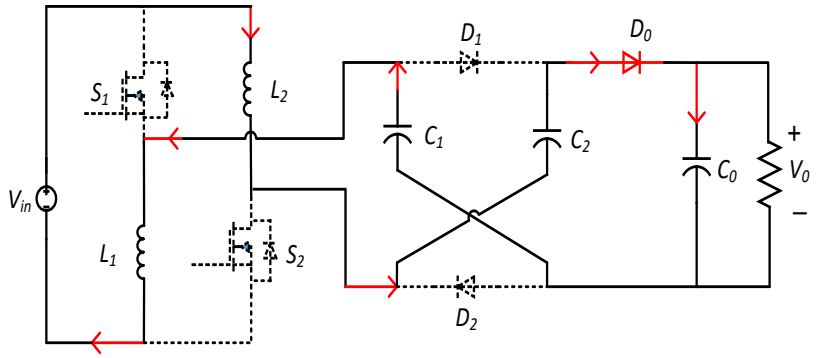

Figure 4.5: OFF state opeartion of ASL based converter.

Since the average inductor voltage is zero in each period, the volt-second law is applied across inductors to get the voltage gain. Hence, the voltage gain of the derived ASL converter is given as;

$$M_{ccm} = \frac{V_0}{V_{in}} = \frac{3-D}{1-D} \tag{4.4}$$

The voltage gain expressions shows the ASL converters has wide range of duty operation i.e, $0 < D < 1$.

4.2.2 ASL derived proposed converter-4

The proposed ASL-based converter is derived from the proposed converter-3. To derive ASL based converter-4 one pair of (CD) network (C_2, D_1) in Figure 4.3 is replaced by a new SC network (C_3, D_3, C_4, D_4). This converter consists of the same number of switches and inductors except for one additional capacitor and diode. For analysis of this version of the converter, all the components are assumed to be lossless, and its operation is considered in continuous conduction mode (CCM). The mathematical

equations and voltage gain expression for the ASL converter is described below and proposed converter-4 as shown in Figure 4.6.

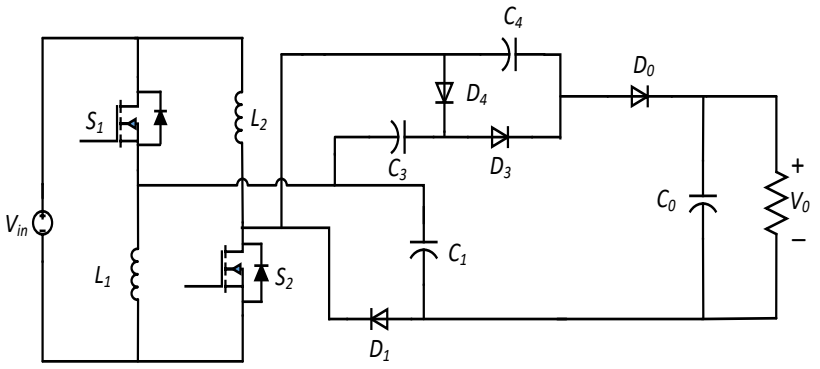

Figure 4.6: ASL based proposed converter-4.

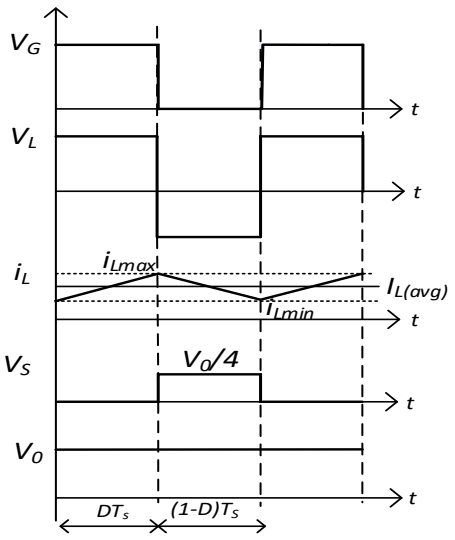

Figure 4.7: Operating CCM waveform.

4.2.3 Operation

In order to understand the operation of proposed converter-4, the steady state waveform is shown in Figure 4.7. ON and OFF time are represented by DT_s and $(1-D)T_s$, respectively. V_G represents the gate pulses for both switches S_1 and S_2, respectively. V_L denotes the voltages across both inductors, i_L represents the current through the inductors. Similarly, switch voltage stresses is represented by V_S. Finally the output voltage is shown by V_0. The static gain is derived under the following assumptions pertaining to the converter:

1. Parasitics effect of the components are neglected.

2. All capacitors are large enough to maintain ripple free operation.

3. Both inductor have a same value ($L_1 = L_2$).

Mode 1

Figure 4.8 presents the equivalent circuit diagram during ON time. During this period, both active Switches S_1 and S_2 are turned ON. Both inductors L_1 and L_2 are magnetized by input source V_{in}. Diodes D_1 and D_3 are forward biased while Diodes D_4 and D_0 are reversed biased. Capacitor C_1 is charged by input supply voltage V_{in}. Similarly, capacitor C_4 is charged by V_{C3} and V_{in} i.e. $(V_{C3}+V_{in})$. The output capacitor discharges its energy into load resistance. During this period, the steady-state equations are as follows:

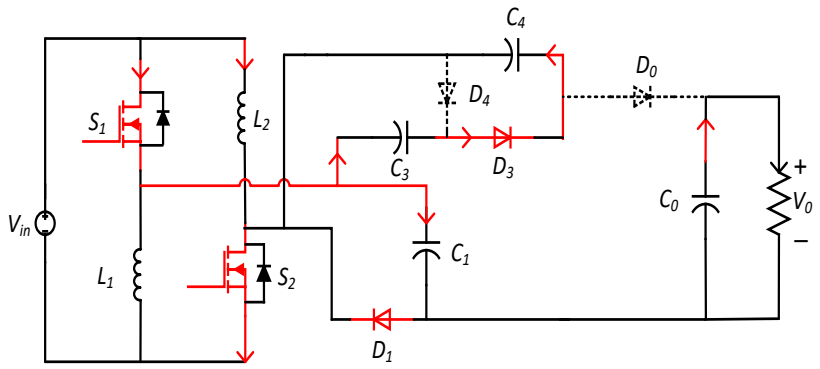

Figure 4.8: ON time equivalent circuit diagram.

$$v_{L1} = v_{L2} = V_{in} = v_{C1} \tag{4.5}$$

$$v_{C4} = v_{C3} + v_{in} \tag{4.6}$$

$$i_{C3} = -i_{C4} \tag{4.7}$$

$$i_{C0} = -i_0 \tag{4.8}$$

Mode 2

Figure 4.9 shows the equivalent circuit diagram during OFF period in which both Switches S_1 and S_2 are turned OFF, Diodes D_1 and D_3 are reversed biased. However, Diodes D_4 and D_0 are forward biased. Both inductor L_1 and L_2 releases their energy

through Diode D_4 to charge capacitor C_3 and through capacitor C_4, C_1 via Diode D_0 to charge the capacitor C_0. The steady state state equation can be obtained as following;

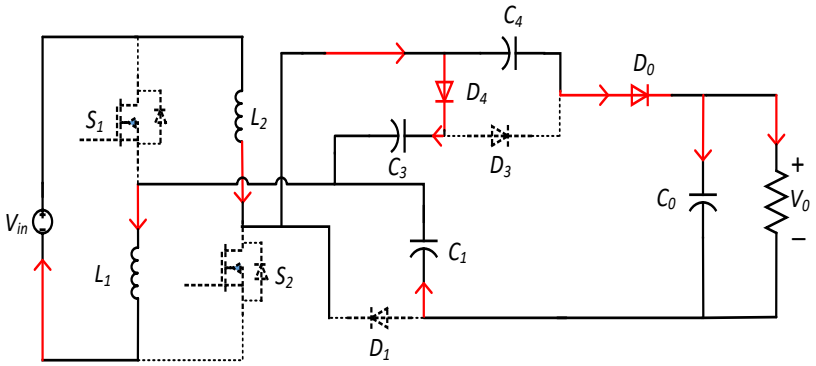

Figure 4.9: OFF time equivalent circuit diagram.

$$v_{L1} = \frac{v_{in} - v_{C3}}{2} \tag{4.9}$$

$$v_0 = v_{C1} + v_{C3} + v_{C4} \tag{4.10}$$

$$i_{C4} = -i_0 - i_{C0} \tag{4.11}$$

$$i_{C3} = i_{L1} - i_{C1} \tag{4.12}$$

$$i_{C1} = i_{C0} + i_0 \tag{4.13}$$

Voltage gain in CCM

According to energy conservation, average voltage across inductor L_1 is zero.

$$\int_0^{DT_s} v_{L1} dt + \int_{DT_s}^{T_s} v_{L1} dt = 0 \tag{4.14}$$

Here eq. (4.5) and eq. (4.9) are substituted in eq. (4.14) to obtain the voltage across the capacitor C_3 and C_4,

$$V_{C3} = \frac{1+D}{1-D} V_{in} \tag{4.15}$$

$$V_{C4} = \frac{2}{1-D} V_{in} \tag{4.16}$$

Using eq. (4.10) the output voltage of the proposed converter can be obtained,

$$V_0 = \frac{4}{1-D} V_{in} \tag{4.17}$$

Therefore, the voltage gain (M) expression for the proposed converter in CCM operation

$$M = \frac{V_0}{V_{in}} = \frac{4}{1-D} \tag{4.18}$$

DCM gain calculation

Three modes of operation occur for the derivation of voltage conversion ratio in discontinuous current mode (DCM). The operating waveform during DCM condition is shown in Figure 4.10. From Figure 4.10, current through the inductor reaches the boundary condition to enter DCM. The peak current of an inductor, I_{Lp} for Mode 1 and Mode 2, is given as;

$$i_{Lp_{mode1}} = \frac{V_{in} D T_s}{L} \tag{4.19}$$

$$i_{Lp_{mode2}} = \frac{[V_{in} + V_{C1} + V_{C4}] D_z T_s}{2L} \tag{4.20}$$

From eq. (4.19) and eq. (4.20) D_z can be derived as;

$$D_z = \frac{2DV_{in}}{[V_0 - 4V_{in}]} \tag{4.21}$$

The average current through C_0 for when switches are off can be derived as;

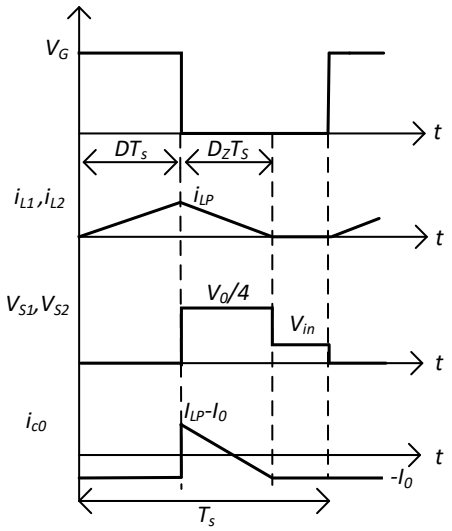

Figure 4.10: Operating waveform during DCM condition.

$$I_{C0} = \frac{\frac{1}{2}(D_z T_s I_{LP}) - I_0 T_s}{T_s} = 0 \tag{4.22}$$

$$I_{C0} = \frac{V_{in}^2 D^2 T_s}{[V_0 - 4V_{in}]L} = \frac{V_0}{R} = 0 \tag{4.23}$$

Solving eq. (4.23) voltage gain during DCM operation is given by,

$$\frac{V_0}{V_{in}} = \frac{4 \pm \sqrt{16 + \frac{4D^2}{\tau}}}{2} \tag{4.24}$$

Where, $\tau = \frac{L}{RT_s}$. Boundary condition from eq. (4.18) and eq. (4.24) can be derived.

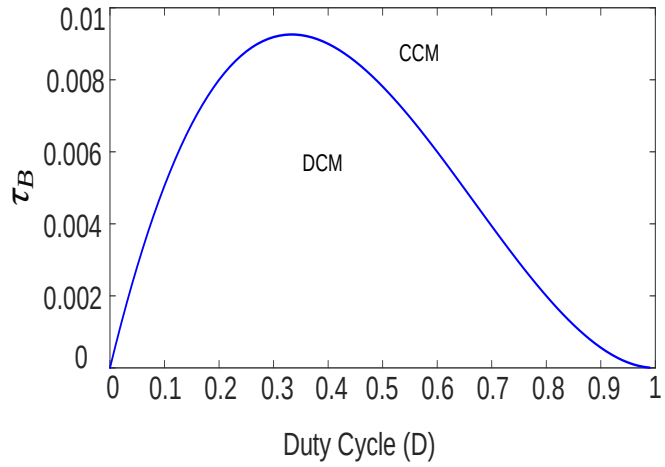

Figure 4.11: Boundary condition CCM/DCM.

Figure 4.11 shows the curve seprating CCM/DCM regions. The inductor time constant at the boundary is defined by τ_B and below boundary curve inductor currents operate in DCM. The inductor time constant τ_B at boundary of CCM/DCM is plotted as shown in Figure 4.11.

4.2.4 Current stress on diodes and switches

The device is stressed if there is a specific amount of current flowing through it. Hence applying KCL in Figure 4.8 and Figure 4.9 results current through capacitor during ON and OFF time.

$$\left.\begin{aligned} i_{C_3,ON} = -i_{C_4,ON}, \quad & i_{C_0,ON} = -I_0 \\ i_{C_1,OFF} = -I_0 - i_{C_0,OFF}, \quad & i_{C_4,OFF} = -I_0 - i_{C_0,OFF} \end{aligned}\right\} \tag{4.25}$$

By applying ampere-second balance principle to all capacitors C_1, C_3, C_4 and C_0

$$i_{C(ON)} \times DT_s + i_{C(OFF)} \times (1-D)T_s = 0 \tag{4.26}$$

where, D is the duty cycle and T_s is the switching period.

$$\left.\begin{aligned} i_{C_1,ON} = \frac{I_0}{D}, \quad i_{C_1,OFF} = -\frac{I_0}{1-D} \end{aligned}\right\} \tag{4.27}$$

$$\left.\begin{aligned} i_{C_3,ON} = -\frac{I_0}{D}, \quad & i_{C_3,OFF} = \frac{I_0}{1-D} \\ i_{C_4,ON} = \frac{I_0}{D}, \quad & i_{C_4,OFF} = -\frac{I_0}{1-D} \\ i_{C_0,ON} = -I_0, \quad & i_{C_0,OFF} = \frac{I_0 D}{1-D} \end{aligned}\right\} \tag{4.28}$$

The mean value current stress through each device is obtained as following: Using Figure 4.8 following equations hold to determine the current value through switches,

$$\left.\begin{aligned} i_{S_1} = i_{C4} - i_{C3} + i_{L2}, \quad i_{D_1} = i_{C1} \\ i_{S_2} = i_{C4} + i_{C1} + i_{L1}, \quad i_{D_3} = i_{C4} \end{aligned}\right\} \tag{4.29}$$

Using eq. (4.28) and eq. (4.29) mean value of current can be as folllows,

$$\left.\begin{aligned} I_{S_1} = I_{S_2} = \frac{2I_0}{D(1-D)} \times D + 0 \times (1-D) = \frac{2I_0}{(1-D)} \\ I_{D_1} = I_{D_3} = \frac{I_0}{D} \times D + 0 \times (1-D) = I_0 \\ I_{D_4} = I_{D_0} = \frac{I_0}{1-D} \times (1-D) = I_0 \end{aligned}\right\} \tag{4.30}$$

4.3 Performance comparison with wide duty range based converter

This section compares the proposed converter with the existing non-isolated converter in terms of voltage gain, number of devices being used, efficiency, and nature of input current; Table 4.1 is shown. Compared to the proposed converter, the SH-SLC reported in [11] has a higher device count and lower gain. Though converter-III and converter-I presented in [10] have a low number of device counts, the voltage gain achieved by these reported converters is not attractive as compared to the proposed converter. At higher gain, these converters suffer from inductor current saturation, and their efficiency deteriorates. The converter in [61] describes a four-stage Dickson converter that achieves higher gain at the expense of increased component count. Interestingly, the stress on the switch is equal to the proposed converter, and the stress on the diode

Table 4.1: Comparison of proposed converter-4 with existing topologies.

Topology	***L***	***C***	***S***	***Di***	**TC**	***Gain***	***Switch stress***	***Diode stress***	**Efficiency**	**input current**
SH-SLC [11]	4	1	2	7	14	$\frac{1+3D}{1-D}$	$V_{S1}=V_{S2}=\frac{1+D}{1+3D}V_0$	$V_{D1a}=V_{D1b}=\frac{D}{1+3D}V_0$ $V_{D2a}=V_{D2b}=\frac{D}{1+3D}V_0$ $V_{D1c}=V_{D2c}=\frac{1-D}{1+3D}V_0$ $V_D=\frac{2(1+D)}{1+3D}V_0$	93.9%	continuous
Converter-III [10]	2	3	2	3	10	$\frac{3-D}{1-D}$	$V_{S1}=V_{S2}=\frac{V_0}{3-D}$	$V_{D1}=V_{D2}=\frac{V_0}{3-D}$ $V_{D0}=\frac{2V_0}{3-D}$	89%	continuous
Converter-I [10]	2	1	2	1	6	$\frac{1+D}{1-D}$	$V_{S1}=V_{S2}=\frac{V_0}{1+D}$	$V_{D0}=\frac{2V_0}{1+D}$	91%	continuous
4-stage Dickson [61]	2	5	2	5	14	$\frac{5}{1-D}$	$V_{S1}=V_{S2}=\frac{V_0}{4}$	$V_{D1}=V_{D2}=\frac{2V_0}{5}$ $V_{D3}=V_{D4}=\frac{2V_0}{5}$ $V_{D0}=\frac{2V_0}{5}$	94%	continuous
Converter [62]	2	3	2	3	10	$\frac{3+D}{1-D}$	$V_{S1}=V_{S2}=\frac{V_0}{3+D}$	$V_{D1}=V_{D2}=\frac{2V_0}{3+D}$ $V_{D0}=\frac{2V_0}{3+D}$	96%	continuous
Converter [63]	3	3	2	2	10	$\frac{1+3D}{1-D}$	$V_{S1}=V_{S2}=\frac{V_0}{1+3D}$	$V_{D1}=V_{D2}=\frac{2V_0}{1+3D}$	95.5%	continuous
Converter [64]	1	3	1	3	8	$\frac{2}{1-D}$	$V_{S1}=\frac{V_0}{2}$	$V_{D1}=V_{D2}=\frac{V_0}{2}$ $V_{D3}=\frac{V_0}{2}$	93%	continuous
Converter V1 [65]	1	5	1	5	12	$\frac{3}{1-D}$	$V_S=\frac{V_0}{3}$	$V_{D1}=V_{D2}=\frac{V_0}{3}$ $V_{D3}=V_{D4}=V_{D0}=\frac{V_0}{3}$	88%	continuous
Converter [66]	2	3	1	6	12	$2\frac{1+D}{1-D}$	$V_S=\frac{V_0}{2}$	$V_{D1}=V_{D2}=V_{D3}=\frac{V_0}{2}$ $V_{D4}=V_{D5}=V_{D6}=\frac{V_0}{2}$	95.47%	continuous
Converter [67]	3	5	1	3	12	$\frac{3D}{1-D}$	$V_S=\frac{V_0+3}{3}$	$V_{D1}=V_{D3}=\frac{V_0}{3D}$ $V_{D2}=\frac{1-2D}{3D}V_0$	96%	discontinuous
Converter [68]	2	5	2	5	14	$\frac{5+D}{1-D}$	$V_{S1}=V_{S2}=\frac{V_0}{5+D}$	$V_{D1}=V_{D2}=V_{D3}=\frac{2V_0}{5+D}$ $V_{D4}=V_{D0}=\frac{2V_0}{5+D}$	97%	continuous
Proposed converter-3	2	3	2	3	10	$\frac{3-D}{1-D}$	$V_{S1}=V_{S2}=\frac{V_0}{3-D}$	$V_{D1}=V_{D2}=\frac{2V_0}{3-D}$ $V_{D0}=\frac{2V_0}{3-D}$	95.9%	continuous
Proposed converter-4	2	4	2	4	12	$\frac{4}{1-D}$	$V_{S1}=V_{S2}=\frac{V_0}{4}$	$V_{D1}=V_{D3}=\frac{V_0}{2}$ $V_{D3}=V_{D0}=\frac{V_0}{2}$	96.9%	continuous

Note1: In this table L=number of inductor, C=number of capacitor, S=number of switches, Di= number of diodes, TC= total count, D=Duty cycle of converter

Note2: Efficiency number calculated for 200 W power rating and Switching frequency $f_s = 40\ kHz$

is lower than the proposed converter. The ASL-based networks reported in [62] and [63] have a lower voltage gain and higher switch and diode stress. Converter in [64] shows a multilevel high gain system that has lower gain and fewer devices but more

voltage stress across the switch. The voltage gain of the converter [65], [67], and [66] is lower than that of the proposed converter despite having the same number of total components. Converter [68] achieves more voltage gain and low switch stress at the cost of a higher device count.

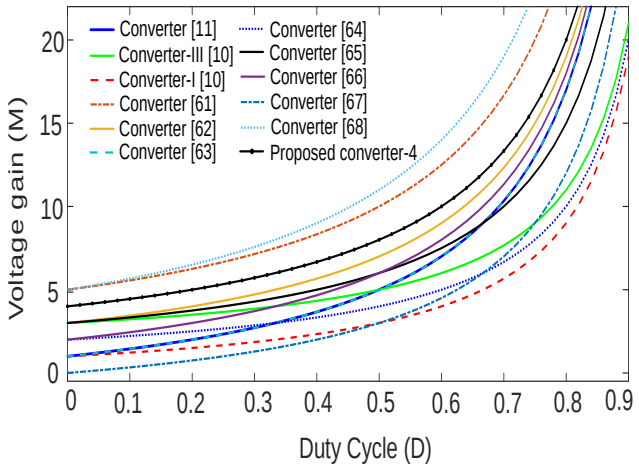

Figure 4.12: Boost factor of existing non-isolated converters with wide duty operation.

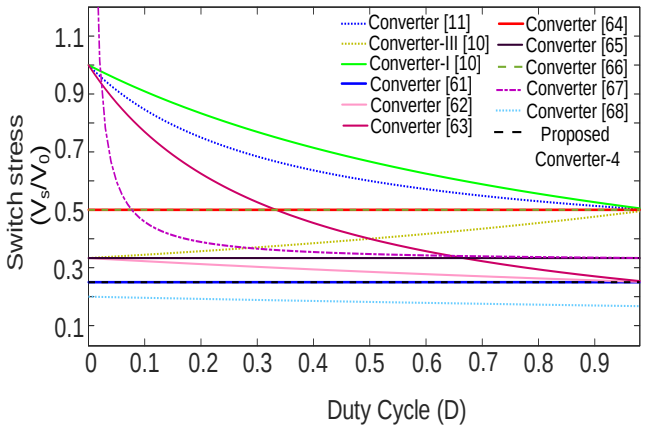

Figure 4.13: Normalized switch stress.

So broadly, the proposed converter switch voltage stress is lower than that of other converters hence a low device rating of switch is required. From the gain curve shown in Figure 4.12 it can be seen that proposed converter achieve higher gain at lower duty cycle as compared to its counterparts. Normalized switch stress for all compared converter is plotted in Figure 4.13 and it can be seen that modified ASL has low switch stress except [68] but this converter consist of more device count.

4.3.1 Small signal analysis of Proposed converter

Analyzing the converter for stability requires performing dynamic modeling based on a small-signal AC model. For this purpose inductor currents ($\hat{i}_{L1}$-$\hat{i}_{L2}$) and capacitor voltages ($\hat{v}_{c1}$, $\hat{v}_{c3}$, $\hat{v}_{c4}$, $\hat{v}_{c0}$) are taken as state variables. Both operating modes provide a set of equations during each period. The small signal ac model can be deduced by state space averaging techniques. The coupling between capacitor C_1 and C_4 is removed by putting the corresponding series resistance (r_{C_i}) (where $i = 1, 4$) within the same loop to avoid the incorrect state variables. The effect of parasitic resistance of both inductors are also considered. The state variable, the input variable, the output variable and the control variable can be described by small-signal disturbance. The disturbance terms is each state variables are added with the stedy state components of variable and is given by eq. (4.31).

$$\left.\begin{aligned} i_{L1}(t) &= I_{L1} + \hat{i}_{L1}(t) \\ i_{L2}(t) &= I_{L2} + \hat{i}_{L2}(t) \\ v_{C1}(t) &= V_{C1} + \hat{v}_{c1}(t) \\ v_{C3}(t) &= V_{C3} + \hat{v}_{c3}(t) \\ v_{C4}(t) &= V_{C4} + \hat{v}_{c4}(t) \\ v_{C0}(t) &= V_{C0} + \hat{v}_{c0}(t) \\ v_{in}(t) &= V_{in} + \hat{v}_{in}(t) \\ d(t) &= D + \hat{d}(t) \end{aligned}\right\} \tag{4.31}$$

Where I_{L1}, I_{L2}, V_{C1}, V_{C3}, V_{C4}, V_{C0}, V_{in} and D are the steady state components, $\hat{i}_{L1}(t)$, $\hat{i}_{L2}(t)$, $\hat{v}_{c1}(t)$, $\hat{v}_{c3}(t)$, $\hat{v}_{c4}(t)$, $\hat{v}_{c0}(t)$, $\hat{v}_{in}(t)$ and $\hat{d}(t)$ are the small-signal disturbances. After performing perturbation and linearization, the small-signal ac model of the proposed converter is given in matrix form eq. (4.32). Inside matrix various constant terms are presented. The details of these constant terms are represented by eq. (4.35).

$$\begin{bmatrix} \frac{d\hat{i}_{L1}}{dt} \\ \frac{d\hat{i}_{L2}}{dt} \\ \frac{d\hat{v}_{c1}}{dt} \\ \frac{d\hat{v}_{c3}}{dt} \\ \frac{d\hat{v}_{c4}}{dt} \\ \frac{d\hat{v}_{c0}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{K_1}{2L_1} & 0 & 0 & -\frac{D'}{2L_1} & 0 & 0 \\ 0 & -\frac{K_2}{2L_2} & 0 & -\frac{D'}{2L_2} & 0 & 0 \\ 0 & 0 & -\frac{K_3}{C_1} & -\frac{K_4}{C_1} & -\frac{K_4}{C_1} & \frac{K_4}{C_1} \\ D' & 0 & -\frac{K_4}{C_3} & -\frac{K_5}{C_3} & \frac{K_6}{C_3} & \frac{K_4}{C_3} \\ 0 & 0 & -\frac{K_4}{C_4} & \frac{K_6}{C_4} & \frac{K_5}{C_4} & \frac{K_4}{C_4} \\ 0 & 0 & \frac{K_4}{C_0} & \frac{K_4}{C_0} & \frac{K_4}{C_0} & -\frac{K_7}{C_0} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{v}_{c1} \\ \hat{v}_{c3} \\ \hat{v}_{c4} \\ \hat{v}_{c0} \end{bmatrix} + \begin{bmatrix} \frac{D+1}{2L_1} \\ \frac{D+1}{2L_2} \\ \frac{D}{C_1 R_{C1}} \\ \frac{-D}{C_3 R_{C4}} \\ \frac{D}{C_4 R_{C4}} \\ 0 \end{bmatrix} \hat{V}_{in}$$

$$+ \begin{bmatrix} \frac{-K_1'}{2L_1} & 0 & 0 & \frac{1}{2L_1} & 0 & 0 \\ 0 & \frac{-K_2'}{2L_2} & 0 & \frac{1}{2L_2} & 0 & 0 \\ 0 & 0 & \frac{K_3'}{C_1} & \frac{K_4'}{C_1} & \frac{K_4'}{C_1} & -\frac{K_4'}{C_1} \\ -1 & 0 & -\frac{K_4'}{C_3} & -\frac{K_5'}{C_3} & \frac{K_6'}{C_3} & -\frac{K_4'}{C_3} \\ 0 & 0 & \frac{K_4'}{C_4} & \frac{K_6'}{C_4} & \frac{K_5'}{C_4} & -\frac{K_4'}{C_4} \\ 0 & 0 & -\frac{K_4'}{C_0} & -\frac{K_4'}{C_0} & -\frac{K_4'}{C_0} & \frac{K_4'}{C_0} \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{C1} \\ V_{C3} \\ V_{C4} \\ V_{C0} \end{bmatrix} \hat{d}(t) \tag{4.32}$$

$$\hat{v_0} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \hat{i}_{L1} & \hat{i}_{L2} & \hat{v}_{c1} & \hat{v}_{c3} & \hat{v}_{c4} & \hat{v}_{c0} \end{bmatrix}^T \tag{4.33}$$

$$G_{vd}(s) = \frac{\hat{v_0}(s)}{\hat{d}(s)} = \frac{-4.66\times10^3 s^4 - 7.07\times10^{12} s^3 - 2.12\times10^{21} s^2 - 2.4\times10^{23} s + 2.51\times10^{27}}{1.25 s^5 + 1.89\times10^9 s^4 + 5.7\times10^{17} s^3 + 1.02\times10^{20} s^2 + 1.27\times10^{23} s + 8.52\times10^{24}} \tag{4.34}$$

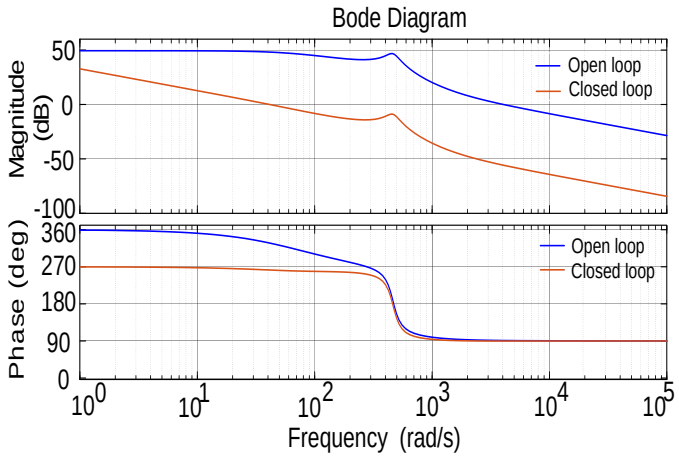

Figure 4.14: Bode plot of converter with and without controller.

$$\left.\begin{aligned}
K_1 &= 2Dr_{L1}+D'(r_{L1}+r_{L2}) \\
K_1' &= r_{L1}-r_{L2} \\
K_2 &= 2Dr_{L2}+D'(r_{L1}+r_{L2}) \\
K_2' &= r_{L2}-r_{L1} \\
K_3 &= \left(\frac{D}{r_{C1}}+\frac{D'}{r_{C1}+r_{C4}}\right) \\
K_3' &= \left(\frac{1}{(r_{C1}+r_{C4})}-\frac{1}{r_{C1}}\right) \\
K_4 &= \frac{D'}{(r_{C1}+r_{C4})} \\
K_4' &= \frac{1}{(r_{C1}+r_{C4})} \\
K_5 &= \left(\frac{D}{r_{C4}}+\frac{D'}{r_{C1}+r_{C4}}\right) \\
K_5' &= \left(\frac{1}{(r_{C1}+r_{C4})}-\frac{1}{r_{C4}}\right) \\
K_6 &= \left(\frac{D}{r_{C4}}-\frac{D'}{r_{C1}+r_{C4}}\right) \\
K_6' &= \left(\frac{1}{(r_{C1}+r_{C4})}+\frac{1}{r_{C4}}\right) \\
K_7 &= \left(\frac{1}{R}+\frac{D'}{r_{C1}+r_{C4}}\right)
\end{aligned}\right\} \tag{4.35}$$

From the transfer function presented in eq. (4.34), Bode plot of the proposed converter-4 is obtained and as shown in Figure 4.14. Bode plot suggests that both phase margin (PM) and gain margin (GM) are negative and the values are ($-88.9°$) and ($-46.4\ dB$), respectively. Therefore, single loop voltage control based on PI controller is adopted to make the system stable and control the output voltage. After using PI controller the phase margin is increased to a positive value of ($81.2°$) and the gain margin is improved to ($7.4\ dB$). The controller is the combination of proportional and integral term, which is mathematically given by

$$G_c(s) = K_p + \frac{K_i}{s} \tag{4.36}$$

4.3.2 Experimental validation

In order to validate the proposed converter-4 theoretical analysis, a laboratory prototype is built and tested with the specification listed in Table 4.2. For these values,

the circuit parameters are computed for capacitor voltage ripple and current ripple of 2% and 15%, respectively. The design of storing elements for rated power is discussed in detail. The design of the storing element is calculated for $P_0 = 200\ W$ of load power, keeping the load resistance $R = 200\ \Omega$, switching frequency f_s=40 kHz, and input voltage fixed to 24 V. The duty cycle calculation for all these values is given by eq. (4.38).

$$P_0 = \frac{V_0^2}{R}, \implies V_0 = 200\ V \tag{4.37}$$

$$\frac{V_0}{V_{in}} = \frac{4}{1-D}, \implies D = 0.519 \approx 0.52 \tag{4.38}$$

The calculation of both inductance can be done using eq. (4.5).

$$L = L_1 = L_2 = \left(\frac{V_{in}}{\Delta I_{L1,L2}}\right) DT_s, \implies L = \frac{24 \times 0.52}{40k \times 0.15} = 500\ \mu H \tag{4.39}$$

Same way using eq. (4.27) and eq. (4.28) the capcitance is calculated.

$$C_1 = \frac{I_0 T_s}{\Delta V_{C1}}, \implies C_1 = \frac{1}{0.02 \times 40k} = 52\ \mu F \tag{4.40}$$

$$C_3 = \frac{I_0 T_s}{\Delta V_{C3}}, \implies C_3 = \frac{1}{0.02 \times 40k} = 17\ \mu F \tag{4.41}$$

$$C_4 = \frac{I_0 T_s}{\Delta V_{C4}}, \implies C_4 = \frac{1}{0.02 \times 40k} = 11\ \mu F \tag{4.42}$$

$$C_0 = \frac{I_0 T_s}{\Delta V_{C0}}, \implies C_0 = \frac{1}{0.02 \times 40k} = 8\ \mu F \tag{4.43}$$

The specification and used final value of storing elemets for proposed converter is listed in Table 4.2 and experimental prototype for converter is shown in Figure 4.15. The inductors L_1 and L_2 are designed to prevent them from entering the discontinuous Conduction Mode (DCM), while the capacitors are chosen to minimize voltage ripple. Table 4.3 presents the components used for the experiment, along with their respective part numbers.

Case I: ($V_{in} = 22\ V$, $P_0 = 160\ W$)

The salient features offered by the proposed converter are high voltage gain and division of input current through inductors along with low voltage stress switches. The measured parameters V_0 and I_0 are 180 V and 0.89 A ,respectively, as shown in Figure 4.16 . The duty cycle is kept at 0.52. The inductors current profile is shown in Figure 4.18 with an average value I_{L1}=I_{L2}=3.82 A . The peak-to-peak ripple current

Table 4.2: Specification and Parameter of proposed Converter-4

Specification	
Input Voltage V_{in}	24 V
Output Voltage V_0	200 V
Output Power P_0	200 W
Switching frequency f_{sw}	40 kHz
Parameter	
Inductance L_1, L_2	500 μH
Capacitance C_1	63μF
Capacitance C_3, C_4, C_0	33μF

Table 4.3: Device and components used in experiment

Component/Device	**Part Number and Manufacturer**
DC Source	H3010, Aplab
MOSFET	IRFB4321PBF, Infineon
Diode	STPS60SM200CW, STElectectrnoics
Gate driver	HCPL3120 Avago Technology
Inductor	MCAP115018077A-561LU, Multicomp Pro
Capacitor	EEUEE2D680, Panasonic
Control board	eZdsp F28335 DSP board, Texas

ΔI_L, 0.66 A for L_1 and 0.68 A for L_2 is measured, which shows the percentage of ripple current is $\approx$ 17.1%. This percentage ripple is slightly more than the assumed value of 15%. The voltage stress across Diodes D_1 and D_4 is 89 V, almost half of the output voltage, as shown in Figure 4.20. The voltage stress across output Diode D_0, Switch S_1, and Switch S_2 is shown in Figure 4.22, and the switch's voltage is oscillatory in nature. This happens when the switch is turned off; the parasitic capacitance forms a series connection with the inductance, resulting in ringing across the switch, which makes it oscillatory in nature. The mean value of voltage across capacitors C_1, C_3, and C_4 are 22 V, 69 V, and 90 V, respectively as shown in Figure 4.24, which are close in agreement with the analytical value.

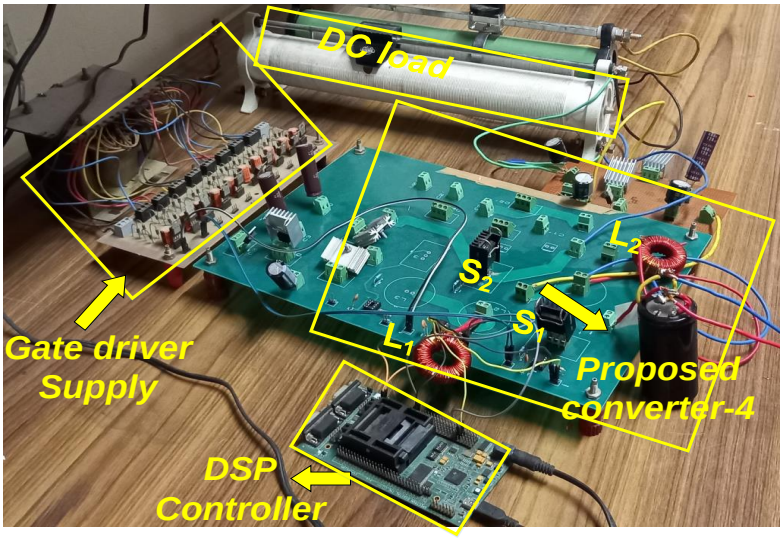

Figure 4.15: Experimental setup for proposed converter-4

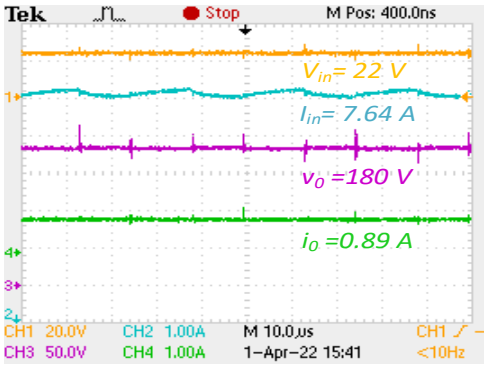

Figure 4.16: Measured steady state input-output voltage and current $V_{in} = 22\ V$.

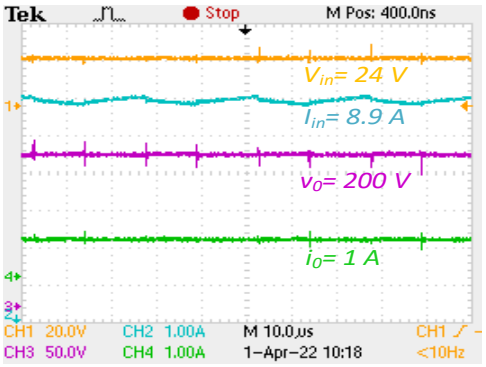

Figure 4.17: Measured steady state input-output voltage and current $V_{in} = 24\ V$.

Case II: ($V_{in} = 24\ V$, $P_0 = 200\ W$)

The input voltage is increased to 24 V for a power rating of 200 W, while the duty cycle is the same as in the previous case. The load resistance is 200 Ω, and the measured output voltage is 200 V. The measured values of input and output current are 8.9 A and 1 A, respectively. The input-output voltage and current waveform are shown in Figure 4.17. The zoomed inductor current profile is shown in Figure 4.19, and their mean value is 4.45 A. The measured peak-to-peak inductor current ripple is 0.75 A, which is nearly the preassumed value of 15% ripple. The voltage stress across Diode D_1, D_3, and D_4 is similar to the previous case (160 W power rating). However, their magnitudes are higher around $\approx$ 100 V as shown in Figure 4.21. The voltage stress for the output Diode D_0, Switch S_1, and Switch S_2 is depicted in Figure 4.23. In the

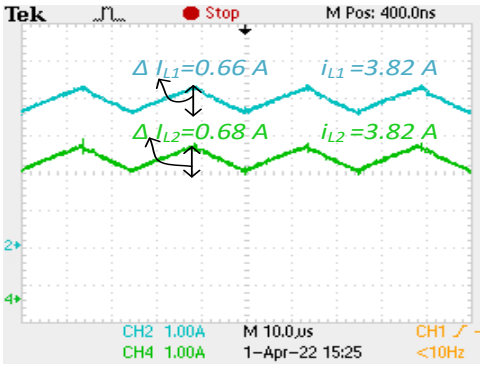

Figure 4.18: Zoomed inductor current of when $V_0 = 180\ V$.

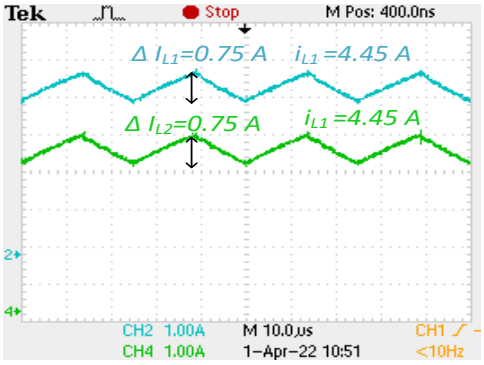

Figure 4.19: Zoomed inductor profile of ASL network for $V_0 = 200\ V$.

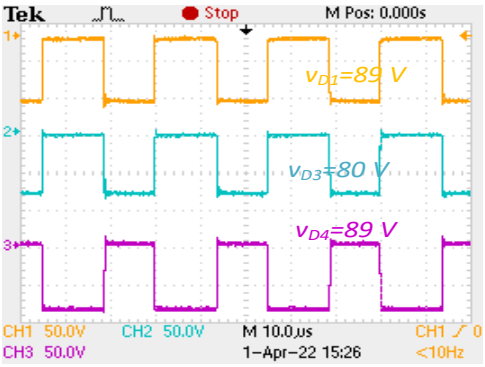

Figure 4.20: Voltage stress across diodes for $V_0 = 180\ V$.

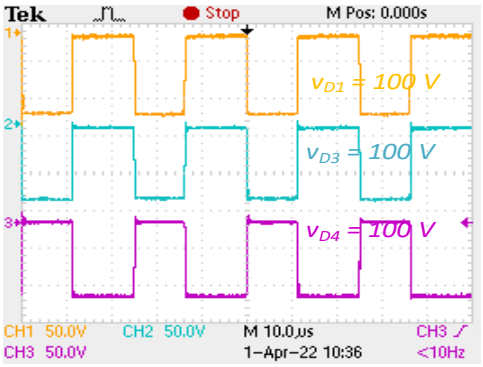

Figure 4.21: Voltage stress across diodes for $V_0 = 200\ V$.

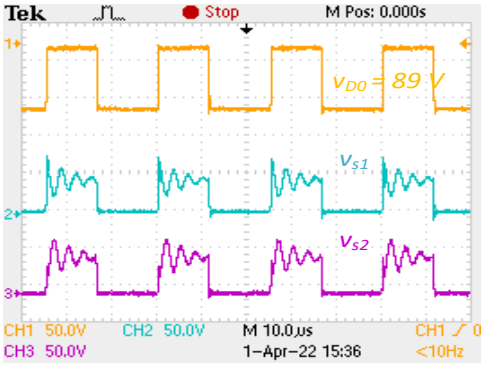

Figure 4.22: Switch and output diode stress for $V_0 = 180\ V$.

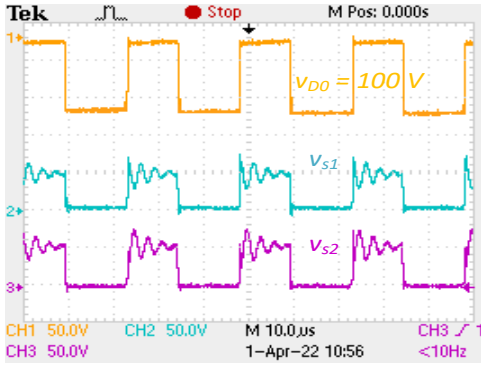

Figure 4.23: Switch and output diode stress for $V_0 = 200\ V$.

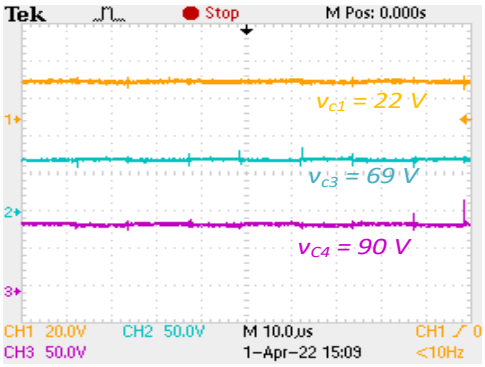

Figure 4.24: Measured mean value across capacitors when $V_0 = 180\ V$.

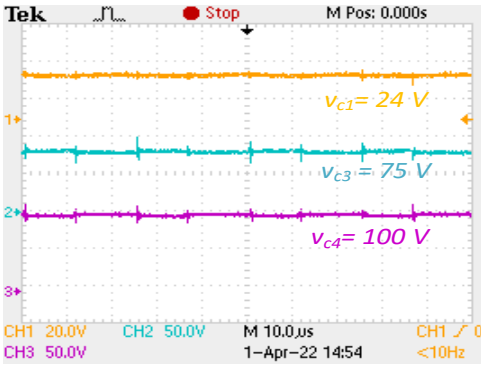

Figure 4.25: Mean value across capacitor $V_0 = 200\ V$.

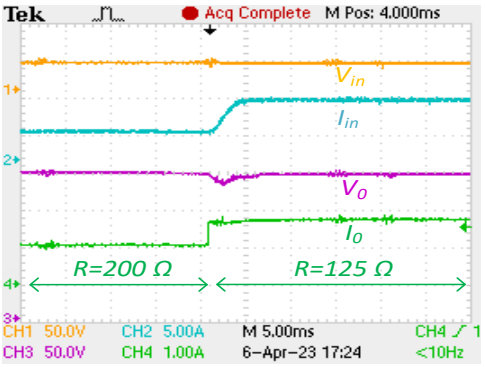

Figure 4.26: Measured dynamic response with load current variation.

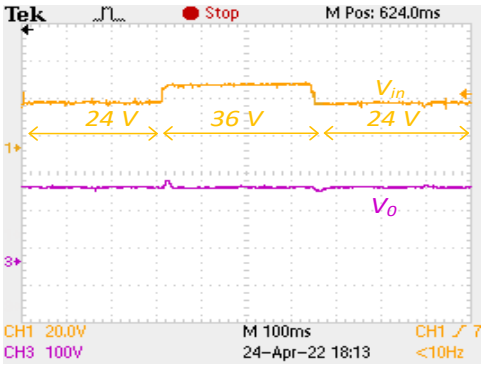

Figure 4.27: Measured dynamic response with source voltage variation.

same way, as in the previous case, the voltage across C_1, C_3, and C_4 is 24 V, 75 V, and 100 V, as illustrated in Figure 4.25.

Closed loop validation

To demonstrate the robustness aspect, the dynamic performance of the converter is captured for sudden load current and source voltage variation, as shown in Figure 4.26 and Figure 4.27, respectively. The dynamic response of load voltage against sudden variation in load R (200 $\Omega - 125\ \Omega$). Here, the output voltage settles within 5 ms. Figure 4.27 shows the response against the sudden change in supply voltage ($24 - 36\ V$), and the load voltage settles within 20 ms.

It can be concluded that the output voltage is maintain constant with variation of soure and load side. The performance of controller is also measured with the change in the reference-point voltage and its results are shown in Figure 4.28. The reference set point (V_{0ref})) of the closed loop system is varied from $210 - 250\ V$ in step. The

load voltage response effectively follows the new reference value within $\approx 25\ ms$, when using controller. This confirms the resilience of the designed controllers, as they are capable of maintaining the system's stability even when faced with changing reference set-points.

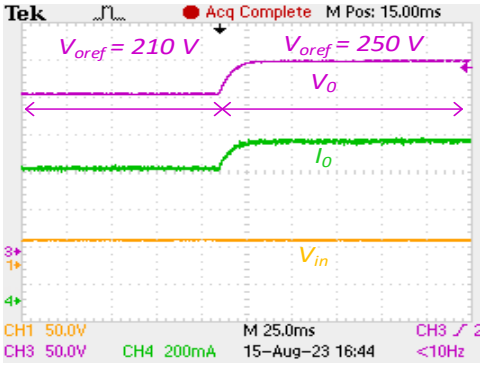

Figure 4.28: Voltage tracking performance with given reference voltage V_{0ref}. point

4.3.3 Power loss analysis

In the proposed converter-4, several diodes, switches, and storing elements are present. These elements contribute to power losses in the converter. The loss calculation of used elements is demonstrated below.

Inductor and capacitor losses

The inductor power loss consist of copper and core loss. The loss due to inductor is given as:

$$P_L = I_{L1}^2 r_{L1} + I_{L2}^2 r_{L2} \tag{4.44}$$

$$P_L = \frac{4I_0^2}{(1-D)^2}(r_{L1} + r_{L2}) \tag{4.45}$$

where, r_{L1} and r_{L2} are the DC resistance of inductor.
The loss due to the capacitor is given by;

$$P_C = I_{C1}^2 r_{c1} + I_{C3}^2 r_{c3} + I_{C4}^2 r_{c4} + I_{C0}^2 r_{c0} \tag{4.46}$$

where r_{C1}, r_{C3}, r_{C4} and r_{C0} are the effective series resistance of the capacitor. The rms value of current in various capacitor is given as

$$I_{C1} = I_{C4} = \sqrt{\left(\frac{I_0}{D}\right)^2 D + \left(\frac{-I_0}{1-D}\right)^2 (1-D)} \tag{4.47}$$

$$I_{C3} = \sqrt{\left(\frac{-I_0}{D}\right)^2 D + \left(\frac{I_0}{1-D}\right)^2 (1-D)} \tag{4.48}$$

$$I_{C0} = \sqrt{(-I_0)^2 D + \left(\frac{I_0 D}{1-D}\right)^2 (1-D)} \tag{4.49}$$

Diode loss

The loss due to diode depends upon the forward voltage drop and ON state resistance. It can be given as;

$$P_D = V_D I_{D1_{avg}} + V_D I_{D3_{avg}} + V_D I_{D4_{avg}} + V_D I_{D0_{avg}} + I^2_{D1_{rms}} r_d + I^2_{D3_{rms}} r_d + I^2_{D4_{rms}} r_d + I^2_{D0_{rms}} r_d \tag{4.50}$$

$$I_{D1_{avg}} = I_{D3_{avg}} = I_{D4_{avg}} = I_{D0_{avg}} = I_0 \tag{4.51}$$

$$I_{D1_{rms}} = I_{D3_{rms}} = \sqrt{\frac{I_0^2}{D}}, \quad I_{D4_{rms}} = I_{D0_{rms}} = \sqrt{\frac{I_0^2}{1-D}} \tag{4.52}$$

Switches power loss

The switches power loss is divided into two parts: conduction loss and switching loss. Conduction loss depends upon ON-state resistance and switching loss depends upon frequency and voltage across switch. The conduction loss and switching loss can be calculated as;

$$P_{CSW} = \left(\frac{4I_0^2}{D(1-D)^2} + \frac{4I_0^2}{D(1-D)^2}\right) r_{dson} \tag{4.53}$$

$$P_{SW} = \frac{1}{6} V_{DS} I_D (t_{on} + t_{off}) f_{sw} \tag{4.54}$$

For power loss distribution, parasitic effect of each component is considered: Inductors

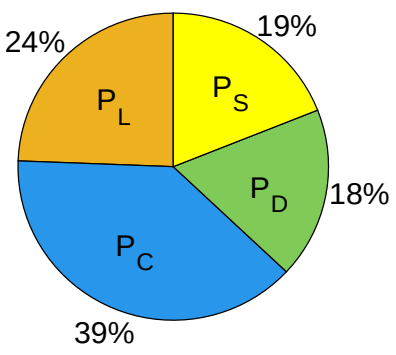

Figure 4.29: Distribution of power loss for the proposed converter at a 200 W load

resistance $r_{L1} = r_{L2} = 0.09\ \Omega$, capacitor resistance $r_{C1} = 0.15\ \Omega$, $r_{C3} = r_{C4} = r_{C0} = 0.5\ \Omega$, MOSFET ON-state resistance $r_{dson} = 0.015\ \Omega$, diode drop $V_f = 0.58$ V, diode resistance $r_d = 0.003\ \Omega$ and switching frequency $f_{sw} = 40$ kHz. According to these specifications at 200 W output power, the losses contributed by P_L, P_C, P_D, and P_S are 3 W, 5.5 W, 2.29 W, and 2.62 W, respectively. The core loss P_{core}= 80 mW is insignificant. The power loss distribution depicted in Figure 4.29 shows that major loss is contributed by the capacitor, which could be reduced by using a capacitor with low ESR. The proposed converter is tested experimentally at different power levels. Due to parasitics in the component, the experimental efficiency is lower than the theoretical efficiency. The maximum efficiency occurs at 120 W, which is 95.2%, and for 200 W, it is 93.6%. Figure 4.30 shows the efficiency curve for various power ratings.

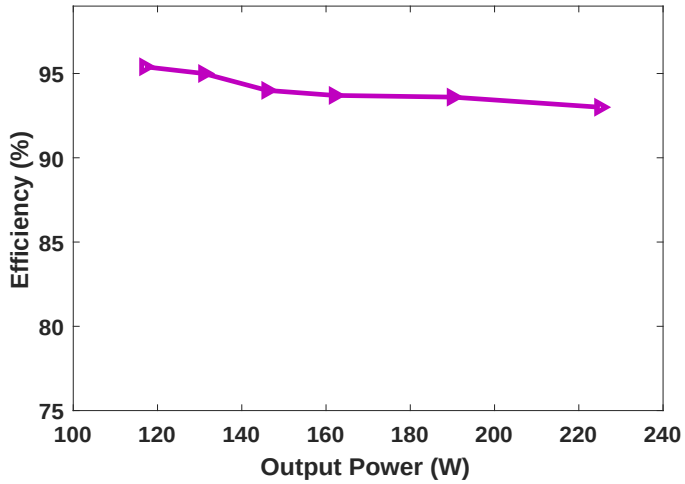

Figure 4.30: Experimental efficiency vs output power.

4.3.4 Soft switching in proposed converter-4

The proposed converter can achieve soft switching based on zero voltage switching (ZVS) to improve converter efficiency. Moreover, adopting soft switching brings the converter inductor currents into a discontinuous current mode (DCM). Here, the proposed converter-4 is simulated to achieve ZVS. During the OFF state of the switch, resonance behavior is observed for the proposed ASL converter. Parasitic capacitance C_{oss} of both the switches exhibits resonance with inductor L_1, L_2 as shown in Figure 4.31. When inductor current reaches zero, it starts oscillating due to parasitic capacitance of switches, as shown in Figure 4.33.

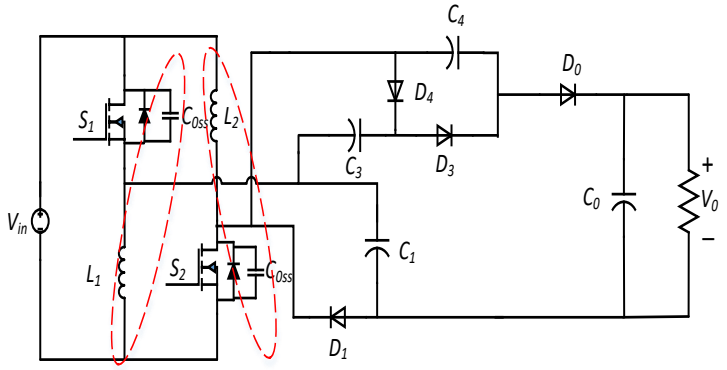

Figure 4.31: Proposed converter-4 with parasitic capacitance to achieve ZVS.

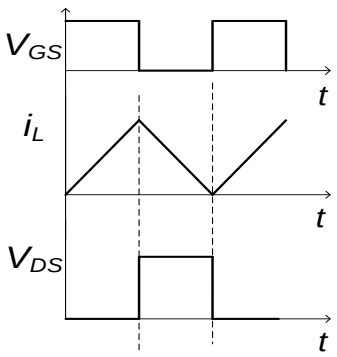

Figure 4.32: At Boundary condition of CCM/DCM [69].

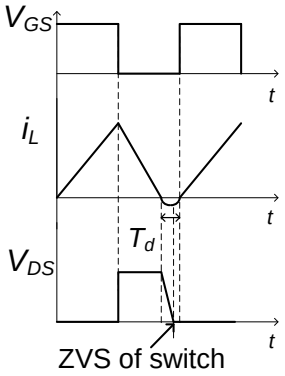

Figure 4.33: Operating in DCM to achieve ZVS [69].

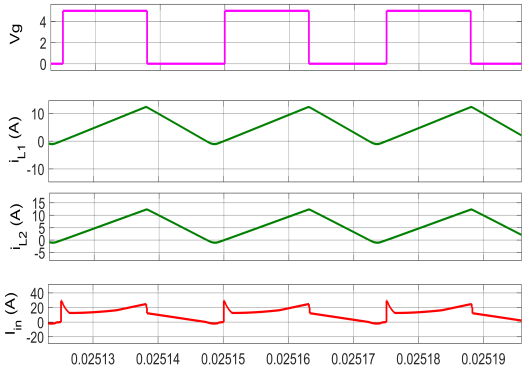

Figure 4.34: Proposed ASL converter with discontinuous inductor current.

The turn ON instant of both switches is delayed until the drain to source voltage reaches zero or resonates down to valley [69]. Here, key waveforms of the proposed converter at CCM/DCM boundary condition and DCM mode with delay T_d are shown in Figure 4.32 and Figure 4.33. Achieving ZVS requires operating the first converter at the boundary condition of CCM or DCM. The calculated critical value of inductance

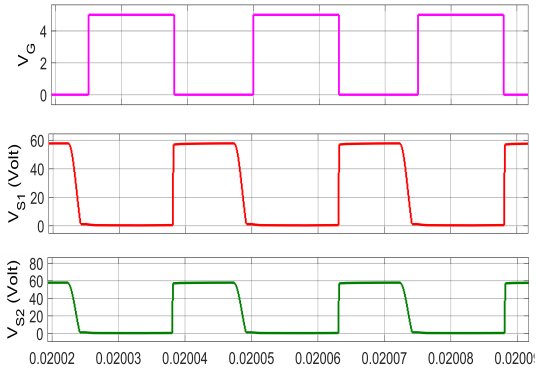

Figure 4.35: Proposed converter with parasitic capacitance to achieve ZVS.

for the converter allows it to operate in DCM operation, and as inductor current becomes zero, the voltage across switch S_1, S_2 decreases to zero before turning ON (V_{DS} settles to zero in T_d delay time). The proposed converter does not need extra passive elements to achieve ZVS. While the converter operates in ZVS, the source current becomes discontinuous, which is unsuitable for renewable applications. The MATLAB simulation is carried out to verify the [69] analysis, and the inductor currents are shown in Figure 4.34. The voltage across both switches with ZVS operation is shown in Figure 4.35. Hence, the proposed converter is modified with the interleaving concept along with ZVS and continuous input current. In the following section, an interleaved-based converter is proposed to achieve ZVS.

4.4 Proposed interleaved converter

In this section, switches of the ASL network are arranged like interleaved structures at the low voltage side. The converter uses an interleaved principle to drive the switches. The proposed interleaved converter is shown in Figure 4.36. The switching pattern for both the switches for interleaving operation is presented in Figure 4.37.

4.4.1 Operation

The converter can work in three states, and the steady-state equations for each state are used to calculate the voltage gain. Here, the operation and workings of the proposed converter are summarized.

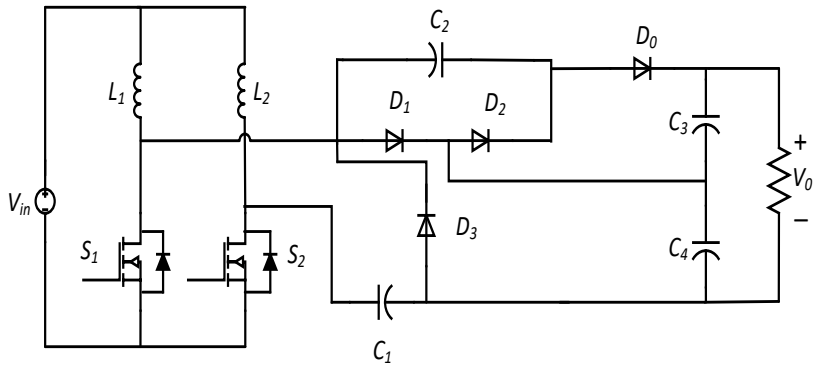

Figure 4.36: Proposed interleaved high gain converter.

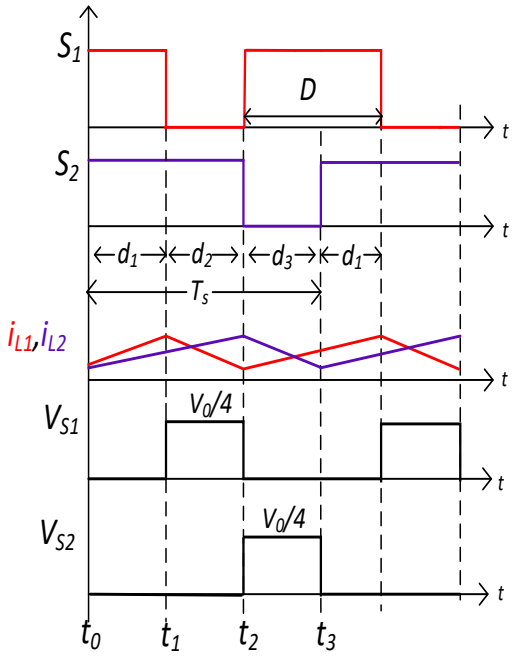

Figure 4.37: Switching pattern and waveform of two phase interleaved converter.

State-1 $(t_0 < t < t_1)$

Both switches are turned ON during this state, and the inductors L_1 and L_2 are magnetized by the input source V_{in}. All the diodes are in the blocking condition, and the capacitors are discharging their energy to the load R. Using Figure 4.38, the following equations can be found;

$$v_{L1} = v_{L2} = V_{in} \tag{4.55}$$

$$v_0 = v_{C3} + v_{C4} \tag{4.56}$$

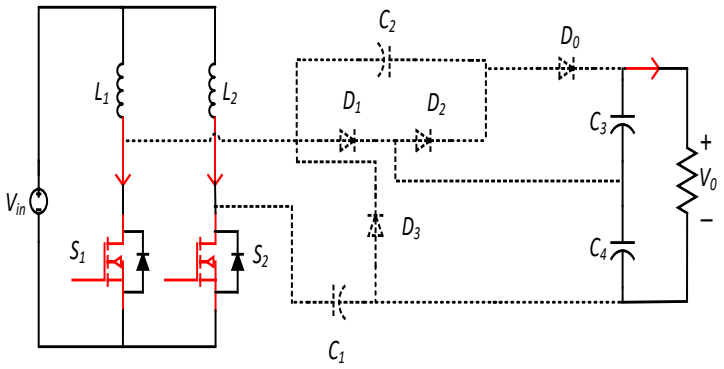

Figure 4.38: State-1 switches S_1, S_2 ON.

State-2 $(t_1 < t < t_2)$

During this state, Switch S_1 is turned-OFF and Switch S_2 is still turned ON. Inductor L_1 demagnetizes its energy through Diode D_1 and charges capacitor C_4. Capacitor C_2 discharges its energy to charge C_3 through output diode. Inductor L_2 is still being magnetised by the input source V_{in}, therefore current is still increasing in nature. Kirchhoff's voltage law (KVL) can be used to get the following equation:

$$v_{L2} = V_{in} \tag{4.57}$$

$$v_{L1} = v_{C1} + V_{in} - v_{C4} \tag{4.58}$$

$$v_{C2} = v_{C3} \tag{4.59}$$

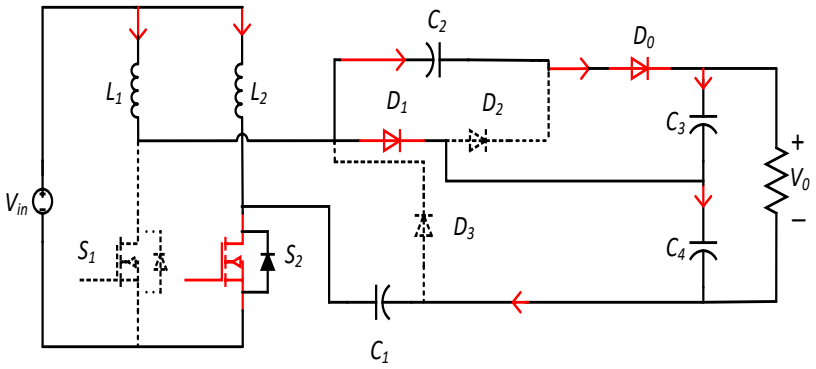

Figure 4.39: State-2 switches S_1 OFF, S_2 ON.

State-3 $(t_2 < t < t_3)$

During this state Switch S_1 is again turned-ON, while Switch S_2 is turned-OFF. Inductor L_1 is again magnetizes by the input source V_{in} and current is rising in nature. Inductor L_2 demagnetizes its energy and charge the capacitor C_1 and forward biased the Diode D_3. Simlilarly C_4 discharges its energy to charge C_2 and Diode D_2 in forward biased. The steady state equations are as following:

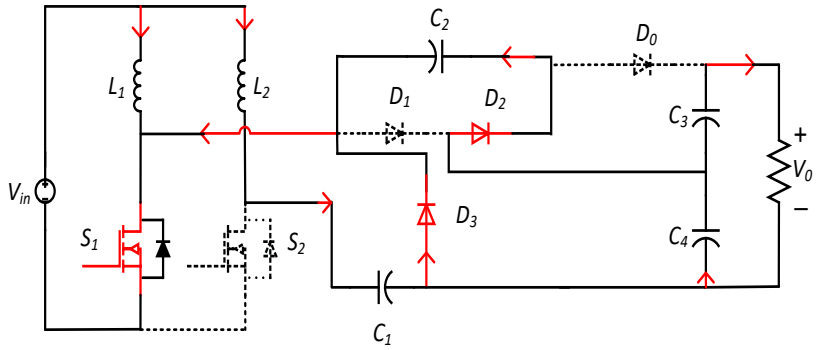

Figure 4.40: State-3 switches S_1 ON, S_2 OFF.

$$v_{L1} = V_{in} \tag{4.60}$$

$$v_{L2} = V_{in} - v_{C1} \tag{4.61}$$

$$v_{C2} = v_{C3} \tag{4.62}$$

Using energy conservation across both inductors L_1 and L_2 to determine the mean value across used capacitors,

$$(V_{C4} - V_{C1}) = \frac{V_{in}}{1-D} \tag{4.63}$$

$$V_{C1} = \frac{V_{in}}{1-D} \tag{4.64}$$

The voltage gain of the proposed interleaved converter is similar to proposed ASL converter-4.

$$\frac{V_0}{V_{in}} = \frac{4}{1-D} \tag{4.65}$$

4.4.2 Experimental validation

The proposed interleaved converter is validated through hardware. The boosting factor of proposed interleaved converter is tested for 100 W of power rating. The specification

Table 4.4: Specification of interleaved converter

Specification	
Input Voltage V_{in}	18 V
Output Voltage V_0	174 V
Output Power P_0	100 W
Switching frequency f_{sw}	40 kHz
Inductance L_1, L_2	500 μH
Capacitance C_1,C_2	63μF
Capacitance C_3, C_4	47μF

is listed in Table 4.4. The measured steady state waveforms for the proposed interleaved converter presented in Figure 4.41 and Figure 4.42. The measured input and output

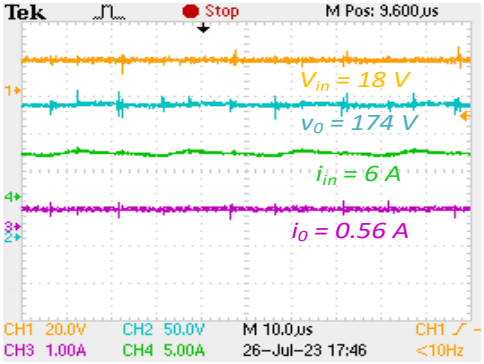

Figure 4.41: Measured input-output waveform of interleaved converter.

voltage is $V_{in} = 18\ V$ and $V_0 = 174\ V$, respectively, corresponding to duty cycle $D = 60\%$ satisfy the eq. (4.65). The inductor current and input current profile are shown in Figure 4.42. The measured values of both inductors and input current are 3.0 A and 6.0 A, respectively. The measured peak value across both switches is 44 V, almost one-fourth of the output voltage shown in Figure 4.43.

4.4.3 Soft switching based ZVS operation

To accomplish ZVS, the proposed interleaved converter inductor current is brought into DCM. Using an interleaved structure on the low voltage side, the input current remains continuous throughout ZVS. The critical value of the inductance for the interleaved

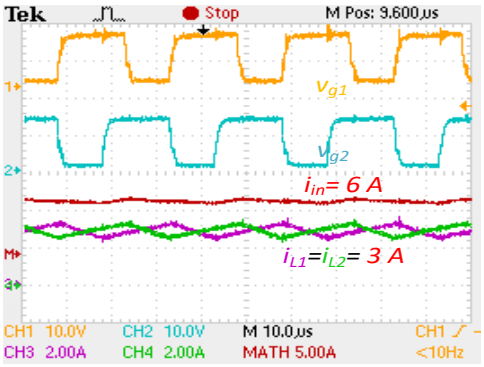

Figure 4.42: Measured value of inductor current with gate signal.

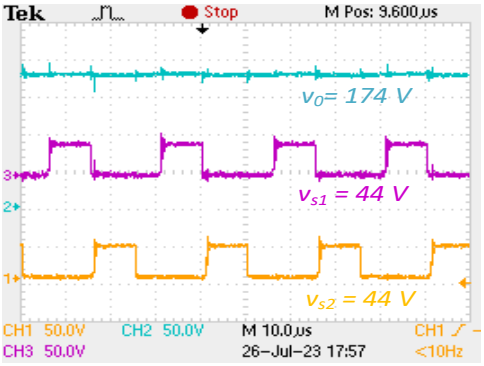

Figure 4.43: Measured value of switch stress and output voltage.

converter is as following:

$$I_{L_{min}} = I_L - \frac{\Delta I_L}{2} = 0 \tag{4.66}$$

$$L_1 = L_2 = L_{critical} = \frac{V_{in} D(1-D)}{4 I_0 f_s} \tag{4.67}$$

The critical inductance value is calculated to be 45 μH based on the load current of $I_0 = 0.56\ A$. The value of both inductance is 22 μH to bring down the inductor current in DCM. Parasitic capacitance of switch creats resonance during OFF state and inductor current becomes negative for certain period of time. Figure 4.44 illustrates the simulated waveform during discontinuous conduction Mode (DCM) in order to achieve zero voltage switching (ZVS). The inductor current and input current profile are presented in Figure 4.45.

Experimental validation

The proposed converter accomplishes soft-switching-based zero voltage switching (ZVS) capability, which is validated through experimental testing. During experimental testing, the measured input voltage is recorded as $V_{in} = 14.5\ V$, and the output voltage

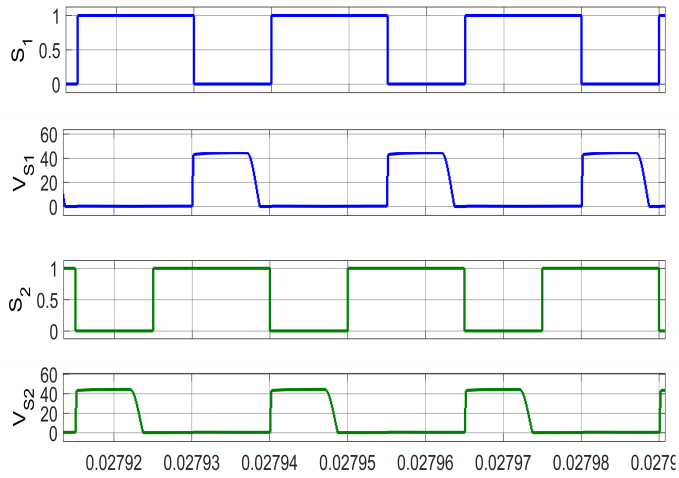

Figure 4.44: Turn ON ZVS for both switches.

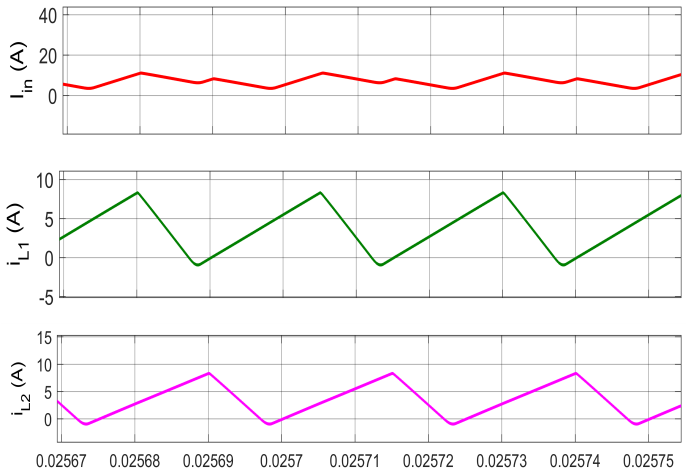

Figure 4.45: Input current and inductor current waveform during ZVS.

as $V_0 = 173\ V$, while the converter delivers an output power of 100 W. The ZVS operation waveform for the switches and inductor current profile is demonstrated in Figure 4.46 and Figure 4.47. From Figure 4.47, the measured value of both inductor currents is 3.73 A, and the nature of the currents is discontinuous.

Power loss calculation

Efficiency is calculated using real parameters used in the experiment setup. This brief includes final expressions of power loss calculation for different components. The analytical expression without soft switching for 100 W, $V_0 = 174\ V$, $V_{in} = 18\ V$ and

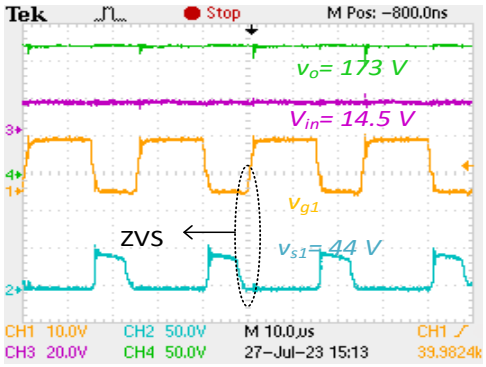

Figure 4.46: Input-output voltage and switch voltage in ZVS operation.

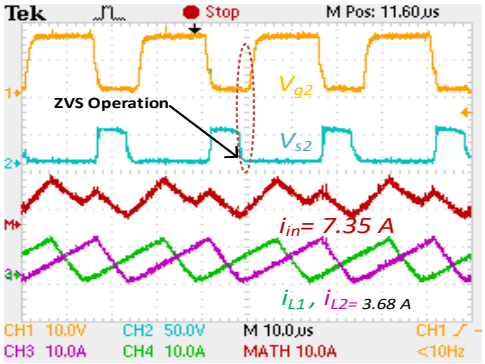

Figure 4.47: Measured inductor and input current waveform during ZVS.

$I_0 = 0.58\ A$, the losses are as follows;

$$P_L = \frac{8}{(1-D)^2} I_0^2 r_L = 1.5\ W \quad (r_L = 0.09\Omega) \tag{4.68}$$

$$P_C = \frac{5+(1-D)^2+(2-D)^2}{D(1-D)} I_0^2 r_c = 5.4\ W \quad (r_c = 0.5\Omega) \tag{4.69}$$

$$P_D = 4V_D I_O + \frac{2}{D(1-D)} I_0^2 r_D = 1.34\ W \quad (V_D = 0.58\ V) \tag{4.70}$$

$$P_S = \frac{8}{D(1-D)^2} I_0^2 r_{ds} + \frac{1}{6} V_{DS} I_D (t_{on} + t_{off}) f_{sw} = 0.34\ W \quad (r_{ds} = 0.0.015\Omega) \tag{4.71}$$

Similarly, the losses contributed by components during ZVS operation are estimated. The expressions with soft switching for 100 W, $V_0 = 173\ V$, $V_{in} = 14.5\ V$ and $I_0 = 0.57\ A$, the losses are as follows;

$$P_L = \frac{8}{(1-D)^2} I_0^2 r_L = 0.24\ W \quad (r_L = 0.015\Omega) \tag{4.72}$$

$$P_C = \frac{5+(1-D)^2+(2-D)^2}{D(1-D)} I_0^2 r_c = 4.8\ W \quad (r_c = 0.5\Omega) \tag{4.73}$$

$$P_D = 4V_D I_0 + \frac{2}{D(1-D)} I_0^2 r_D = 1.32\ W \quad (V_D = 0.58\ V) \tag{4.74}$$

$$P_S = \frac{8}{D(1-D)^2} I_0^2 r_{ds} + \frac{1}{6} V_{DS} I_D (t_{on} + t_{off}) f_{sw} = 0.21\ W \quad (r_{ds} = 0.0.015\Omega) \qquad (4.75)$$

Where P_L = Inductor loss, P_C = Capacitor loss, P_D = Diode loss, P_S = Switching loss, respectively. From the loss distribution graph, it can be seen that the capacitors

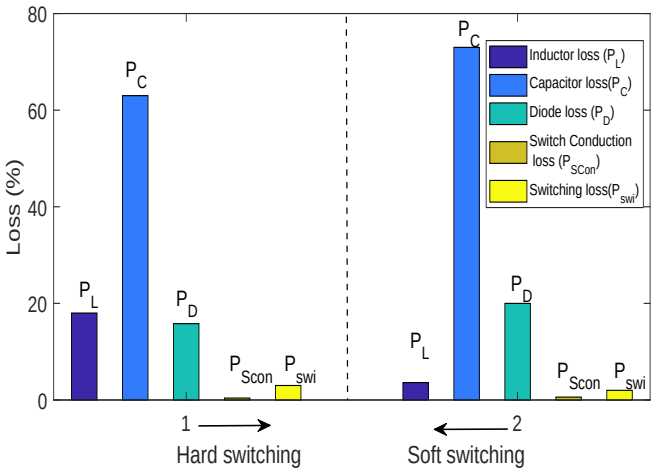

Figure 4.48: Loss distribution of plot without ZVS and with ZVS.

contribute the majority of losses. Converter without ZVS and with ZVS operation, total losses contributed by components are 8.58 W and 6.57 W, respectively. The reduction in loss occurs mainly in inductors and switches. The measured efficiency without ZVS and with ZVS for 100 W output power is 92.16% and 93.5%, respectively.

4.4.4 Conclusion

This chapter discusses a high-voltage gain converter with a wide-duty operating range by utilizing the idea of an active switched inductor network. This overcomes the duty limitations and limited output voltage of the impedance source converter. While analyzing the boosting operation, both inductors of the ASL network share an equal amount of current for a whole range of duty cycles and low current stress with respect to Z-source topologies. Experimental results are in agreement with analytical calculation. Compared to contemporary converters, the proposed converter has fewer passive elements and high voltage gain advantages. In addition, the proposed converter is simulated with soft switching-based ZVS techniques to achieve better efficiency, and it found that while operating during ZVS, the input current becomes discontinuous, which is not suitable for PV renewable applications. To resolve the issue of ASL net-

works, the new interleaved converter is proposed and simulated to achieve ZVS with continuous input current with improved efficiency.

Although, the gain of ASL-based converters highly depends on the duty cycle of the two switches. To achieve a higher conversion ratio, switches of ASL networks have to operate at a high duty ratio, contributing to more conduction losses. In the subsequent chapter, a new topology is deliberated to alleviate the challenge posed by high duty ratios.