
References

- [1] Zener Clarence, "A theory of the electrical breakdown of solid dielectrics," Proc. R. Soc. Lond., Series A, 145 (855), pp. 523-529, 193, 1934.
- [2] W. Shockley, and W.T. Read, "Statistics of the Recombination of Holes and Electrons", Phys. Rev. 87, 835-842, 1952.
- [3] R. N. Hall, "Electron Hole Recombination in Germanium", Phys. Rev. 87, 387, 1952.
- [4] E. O. Kane, "Zener tunneling in semiconductors," J. Phys. Chem. Solids, vol. 12, no. 2, pp. 181-188, Jan. 1960.
- [5] D. Kahng, and M. M. Atalla. "Silicon-Silicon Dioxide Field Induced Surface Devices." In IRE Solid-State Device Res. Conf., Carnegie Institute of Technology, Pittsburgh., 1960.
- [6] R. N. Noyce, "Semiconductor device-and-lead structure," U.S. Patent 2981877; Filed July 30, 1959, Issued April 25, 1961.
- [7] R.L. Anderson, "Experiments on Ge-GaAs heterojunctions", Solid-State Electronics, vol. 5, no. 5, pp. 341-351, 1962.
- [8] W.G. Oldham, A.G. Milnes, "Interface states in abrupt semiconductor heterojunctions", Solid-State Electronics, vol. 7, no. 2, pp. 153-165, 1964.
- [9] J. S. Kilby, "Miniaturized Electronic Circuits," U.S. Patent 3138747; Filed Feb. 6, 1959, Issued June 23, 1964.
- [10] A. M. Cowley, and S. M. Sze, "Surface states and barrier height of metal-semiconductor systems," Journal of Applied Physics, vol. 36, no. 10, pp. 3212-3220, 1965.
- [11] G. E. Moore, "Cramming More Components onto Integrated Circuits," Electronics, pp. 114-117, 1965.
- [12] R. H. Dennard, F. H. Gaenssle., H.-N. Yu, V. L. Rideout, E. Bassous, and A. R. Leblanc, "Design of ion-implanted MOSFETs with very small physical dimensions," *IEEE J. Solid-State Circuit.*, vol. 9, pp. 256-268, 1974.
- [13] G. E. Moore, "Progress in Digital Integrated Electronics," Technical Digest 1975: *IEEE International Electron Devices Meeting*, pp. 11-13, 1975.

- [14] L. Esaki, "Discovery of the tunnel diode", *IEEE Trans. Electron Devices*, vol. 23, no. 7, pp. 644-647, 1976.
- [15] J. Dzierwior and W. Schmid, "Auger Coefficient for Highly Doped and Highly Excited Silicon", *Appl. Phys. Lett.* vol. 31 pp. 346-348, 1977.
- [16] J. Quinn, G. Kawamoto, and B. Mc Combe, "Subband Spectroscopy by Surface Channel Tunneling," *Surface Science*, vol. 73, pp. 190-196, 1978.
- [17] S. M. Sze, *Physics of Semiconductor Devices*, New York: Wiley, 1981.
- [18] D.J. Roulston, N.D. Arora, and S.G. Chamberlain, "Modeling and Measurement of Minority-Carrier Lifetime versus Doping in Diffused Layers of $n \pm p$ Silicon Diodes", *IEEE Trans. Electron Devices* vol. 29, 284-291, Feb. 1982.
- [19] S. Banerjee, W. Richardson, J. Coleman, and A. Chatterjee, "A new three-terminal tunnel device," *IEEE Electron Device Lett.*, EDL-8, pp. 347-349, 1987.
- [20] M. E. Law *et. al.*, Self-Consistent Model of Minority-Carrier Lifetime, Diffusion Length, and Mobility, *IEEE Electron Device Letters* vol. 12, No. 8, 1991.
- [21] T. Baba, "Proposal for Surface Tunnel Transistors," *Jpn. J. Appl. Phys.*, vol. 31, pp. L455-L457, 1992.
- [22] Y. N. Bapat, *Electronic Circuits and Systems: Analog and Digital*, *1e.* Tata McGraw-Hill Education, pp. 119, 1992.
- [23] N. D. Arora, "MOSFET Models for VLSI Circuit Simulations: Theory and Practice," *Springer-Verlog Wien*, New York, 1993.
- [24] Y. Omura, S. Horiguchi, M. Tabe, and K. Kishi, "Quantum-mechanical effects on the threshold voltage of ultrathin-SOI nMOSFETs," *IEEE Electron Device Lett.*, vol. 14, no. 12, pp. 569-571, 1993.
- [25] W. Reddick and G. Amaratunga, "Silicon surface tunnel transistor," *Appl. Phys. Lett.*, vol. 67, no. 4, pp. 494-496, 1995.
- [26] A. R. Beattie, and A.M. White, "An Analytical Approximation with a Wide Range of Applicability for Electron Initiated Auger Transitions in Narrow-gap Semiconductors." *J. Appl. Phys.* Vol. 79, no. 12, pp. 802-813, 1996.
- [27] J. Koga and A. Toriumi, "Negative differential conductance in three-terminal silicon tunneling device," *Appl. Phys. Lett.*, vol. 69, no. 10, pp. 1435-1437, 1996.
- [28] E. Takeda, H. Matsuoka, Y. Igura, and S. Asai, "A band to band tunneling MOS device B2TMOSFET," *in IEDM Tech. Dig.*, pp. 402-405, 1998.

- [29] Y. Taur, and T. H. Ning, "Fundamentals of Modern VLSI Devices" Cambridge University Press, 1998.
- [30] X. Zhou and W. Long, "A Novel Hetero-Material Gate (HMG) MOSFET for Deep-Submicron ULSI Technology," *IEEE Trans. Electron Devices*, vol. 45, no. 12, pp. 2546-2548, 1998.
- [31] W. Long, H. Ou, J-M. Kuo, and K. K. Chin, "Dual-Material Gate (DMG) Field Effect Transistor," *IEEE Trans. Electron Devices*, vol. 46, no. 5, pp. 865–870, 1999.
- [32] W. Hansch, C. Fink, J. Schulze, and I. Eisele, "A vertical MOS-gated Esaki tunneling transistor in silicon," *Thin Solid Films*, vol. 369, pp. 387-389, 2000.
- [33] Xing Zhou, "Exploring the Novel Characteristics of Hetero-Material Gate Field-Effect Transistors with Gate-Material Engineering," *IEEE Trans. Electron Device*, vol. 47, no.1, pp. 113-120, Jan. 2000.
- [34] K. Kim and J. Fossum, "Double-gate CMOS: Symmetrical-versus asymmetrical-gate devices," *IEEE Trans. Electron Devices*, vol. 48, no. 2, pp. 294–299, 2001.
- [35] G. E. Moore, "No exponential is forever: but "Forever" can be delayed! [semiconductor industry]," *2003 IEEE International Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC.*, vol.1, pp. 20-23, 2003.
- [36] J. Appenzeller, Y.-M. Lin, J. Knoch, and Ph. Avouris, "Band-to-Band Tunneling in Carbon Nanotube Field-Effect Transistors," *Phys. Rev. Lett.*, vol. 93, no. 19, pp. 196805-1-4, 2004.
- [37] Y. Taur, X. Liang, W. Wang, and H. Lu, "A continuous, analytic drain current model for DG MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 2, pp. 107–109, Feb. 2004.
- [38] C. Aydin, A. Zaslavsky, S. Luryi, S. Cristoloveanu, D. Mariolle, D. Fraboulet, and S. Deleonibus, "Lateral interband tunneling transistor in silicon-on-insulator," *Appl. Phys. Lett.*, vol. 84, no. 10, pp. 1780-1782, 2004.
- [39] K. Bhuwarka, J. Schulze, I. Eisele, "Performance Enhancement of Vertical Tunnel Field-Effect Transistor with SiGe in the dp+ Layer," *Jap. J. Appl. Phys.*, vol. 43, no. 7A, pp. 4073-4078, 2004.
- [40] J. Appenzeller, Y. Lin, J. Knoch, Z. Chen, P. Avouris, "Comparing Carbon Nanotube Transistors –The Ideal Choice: A Novel Tunneling Device Design," *IEEE Trans. Electron Devices*, vol. 52, no.12, pp. 2568-2576, 2005.

- [41] K. K. Bhuiwarka, J. Schulze, and I. Eisele, "Scaling the vertical tunnel FET with tunnel bandgap modulation and gate work function engineering," *IEEE Trans. Electron Devices*, vol. 52, no. 5, pp. 909–917, May 2005.
- [42] B. Meyerson, *Semico Impact Conference*, Taiwan, January 2004.
- [43] Q. Zhang, W. Zhao, and A. Seabaugh. "Analytic expression and approach for low subthreshold-swing tunnel transistors." In *63rd Device Research Conference Digest, 2005. DRC'05.*, vol. 1, pp. 161-162. IEEE, 2005.
- [44] K. Bhuiwarka, J. Schulze, and I. Eisele, "Scaling the vertical tunnel FET with tunnel bandgap modulation and gate work function engineering," *IEEE Trans. Electron Devices*, vol. 52, no. 5, pp. 909–917, May 2005
- [45] K. K. Bhuiwarka, M. Born, M. Schindler, M. Schmidt, T. Sulima, and I. Eisele, "P-Channel Tunnel Field-Effect Transistors down to Sub-50 nm Channel Lengths," *Jap. J. Appl. Phys.*, vol. 45, no. 4, pp. 3106-3109, 2006.
- [46] S. M. Sze, and K. K. Ng, *Physics of semiconductor devices*, John Wiley & sons, 2006.
- [47] B. G. Streetman, and S. K. Banerjee, *Solid State Electronic Devices*, Pearson Prentice Hall India, 2006.
- [48] P. Nilsson, "Arithmetic Reduction of the Static Power Consumption in Nanoscale CMOS," *IEEE Int. Conf. on Electronics, Circuits and Systems*, pp. 656-659 2006.
- [49] B. Sviličić, and A. Kraš, "CMOS technology: challenges for future development", Pomorstvo, *Journal of Maritime Studies*, vol. 20, no. 2, pp. 97-104, 2006.
- [50] P. Packan, "Device and Circuit Interactions," *IEEE International Electron Device Meeting (IEDM '07) Short Course: Performance Boosters for Advanced CMOS Devices*, December 2007.
- [51] K. Boucart and A. M. Ionescu, "Threshold voltage in Tunnel FETs: physical definition, extraction, scaling and impact on IC design," in *Proc. ESSDERC*, pp. 299-302, 2007.
- [52] K. Boucart and A. M. Ionescu, "Length scaling of the Double Gate Tunnel FET with a high- k gate dielectric," *Solid-State Elec.*, vol. 51, no. 11-12, pp. 1500-1507, Nov.-Dec. 2007.
- [53] W. Y. Choi, B. G. Park, J. D. Lee, and T.-J. King Liu, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec," *IEEE Trans. Electron Devices*, vol. 28, no. 8, pp. 743–745, 2007.

- [54] K. Boucart and A. M. Ionescu, "Double-gate tunnel FET with high- κ gate dielectric," *IEEE Trans. Electron Devices*, vol. 54, no. 7, pp. 1725–1733, Jul. 2007.
- [55] K. Boucart and A. M. Ionescu, "A new definition of threshold voltage in Tunnel FETs," *Solid-State Electronics*, vol. 52, pp. 1318-1323, May 2008.
- [56] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano Lett.*, vol. 8, no. 2, pp. 405–410, 2008.
- [57] M. Fulde, A. Heigl, M. Weis, M. Wirnshofer, K. V. Arnim, T. Nirschl, M. Sterkel *et al.*, "Fabrication, Optimization and Application of Complementary Multiple-Gate Tunneling FETs," In *2008 2nd IEEE International Nanoelectronics Conference*, pp. 579-584, 2008.
- [58] H. Kam, T.-J. K.-Liu, E. Alon, and M. Horowitz. "Circuit-level requirements for MOSFET-replacement devices." In *2008 IEEE International Electron Devices Meeting*, pp. 1-1., 2008.
- [59] T. Krishnamohan, D. Kim, S. Raghunathan, and K. Saraswat, "Double-Gate Strained-Ge Hetero structure Tunneling FET (TFET) With Record High Drive Currents and $\ll 60$ mV/dec Subthreshold Slope," *IEEE Int. Electron Dev. Meeting (IEDM)*, 2008.
- [60] C. Hu, "Green Transistor as a Solution to the IC Power Crisis," in *Proc. 9th Int. Conf. Solid-State Int. Circuit Technol.*, pp. 16–20, 2008.
- [61] V. Nagavarapu, R. Jhaveri, and Jason C. S. Woo, "The Tunnel Source (PNPN) n-MOSFET: A Novel High Performance Transistor," *IEEE Trans. Electron Devices*, vol. 55, pp. 1013-1019, Apr. 2008.
- [62] Y. Khatami and K. Banerjee, "Steep Subthreshold Slope n- and p-Type Tunnel-FET Devices for Low-Power and Energy-Efficient Digital Circuits," *IEEE Trans. Electron Devices*, vol. 56, no. 11, pp. 2752-2761, 2009.
- [63] S. O. Koswatta, M. S. Lundstrom, and D. E. Nikonov, "Performance comparison between pin tunneling transistors and conventional MOSFETs." *IEEE Transactions on Electron Devices*, vol. 56, no. 3, pp. 456-465, 2009.
- [64] M. Luisier and G. Klimeck, "Atomistic Full-Band Design Study of InAs Band-to-Band Tunneling Field-Effect Transistors," *Electron Device Lett.*, vol. 30, no. 6, pp. 602-604, 2009.

- [65] Z. Chen, H. Y. Yu, N. Singh, N. S. Shen, R. D. Sayanthan, G. Q. Lo, and D-L. Kwong. "Demonstration of tunneling FETs based on highly scalable vertical silicon nanowires." *IEEE Electron Device Letters*, vol. 30, no. 7, pp. 754-756, 2009.
- [66] S. Mookerjea, R. Krishnan, S. Datta, and V. Narayanan. "Effective capacitance and drive current for tunnel FET (TFET) CV/I estimation." *IEEE Transactions on Electron Devices*, vol. 56, no. 9, pp. 2092-2098, 2009a.
- [67] D. Kim, Y. Lee, J. Cai, I. Lauer, L. Chang, S.J. Koester, D. Sylvester and D. Blaauw, "Low power circuit design based on heterojunction tunneling transistors (HETTs)," *Proceedings of International Symposium on Low Power Electronics and Design*, pp. 219-224, 2009.
- [68] S. Mookerjea, D. Mohata, R. Krishnan, J. Singh, A. Vallett, A. Ali, T. Mayer, C. Schlom, A. Liu, S. Datta, "Experimental demonstration of 100 nm Channel Length In_{0.53}Ga_{0.47}As-Based Vertical Inter-Band Tunnel Field Effect Transistors (TFETs) for ultra low-power logic and SRAM applications," In *2009 IEEE International Electron Devices Meeting (IEDM)*, pp. 1-3, 2009b.
- [69] C. Hu, *Modern semiconductor devices for integrated circuits*. vol. 2. Upper Saddle River, NJ: Prentice Hall, 2010.
- [70] W. Y. Choi and W. Lee, "Hetero-gate-dielectric tunneling field effect transistors," *IEEE Trans. Electron Devices*, vol. 57, no. 9, pp. 2317– 2319, Sep. 2010.
- [71] Y. Yang, X. Tong, L. Yang, P. Guo, L. Fan, and Y. Yeo, "Tunneling Field-Effect Transistor: Capacitance Components and Modeling," *IEEE Electron Device Lett.*, vol. 31, no. 7, pp. 752–754, 2010
- [72] K. Boucart, "Simulation of Double-Gate Silicon Tunnel FETs with a High-k Gate Dielectric," *École Polytechnique Fédérale De Lausanne*, 2010.
- [73] C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proc. IEEE*, vol. 98, no. 12, pp. 2095–2110, Dec. 2010.
- [74] S. Mookerjea, D. Mohata, T. Mayer, V. Narayanan and S. Datta, "Temperature-Dependent I–V Characteristics of a vertical In_{0.53}Ga_{0.47}As Tunnel FET," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 564–566, 2010.
- [75] J. Singh, K. Ramakrishnan, S. Mookerjea, S. Datta, N. Vijaykrishnan, and D. Pradhan. "A novel Si-Tunnel FET based SRAM design for ultra low-power 0.3 V

- VDD applications." *IEEE 15th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 181-186, 2010.
- [76] S. H. Kim, S. Agarwal, Z. A. Jacobson, P. Matheu, C. Hu, and Tsu-Jae King Liu, "Tunnel Field Effect Transistor with Raised Germanium Source," *IEEE Electron Device Lett.*, vol. 31, no. 10, pp. 1107–1109, Oct. 2010.
- [77] S. Datta, S. Mookerjee, D. Mohata, L. Liu, V. Saripalli, V. Narayanan, and T. Mayer. "Compound semiconductor based tunnel transistor logic." In *Proc. 20th CS MANTECH Conf.*, pp. 203-206. 2010.
- [78] R. Jhaveri, V. Nagavarapu, and J.C. Woo, "Effect of pocket doping and annealing schemes on the source-pocket tunnel field-effect transistor," *IEEE Transactions on Electron Devices*, vol. 58, no.1, pp.80-86, 2011.
- [79] S. Cho, M.-C. Sun, G. Kim, T. I. Kamins, B.-G. Park, and J. S. Harris, "Design optimization of a type-I heterojunction tunneling field-effect transistor (I-HTFET) for high performance logic technology," *J. Semiconductor Technology and Science*, vol. 11, no. 3, pp. 182-189, 2011.
- [80] J. Zhuge, A. S. Verhulst, W. G. Vandenberghe, W. Dehaene, R. Huang, Y. Wang, and G. Groeseneken. "Digital-Circuit Analysis of Short-Gate Tunnel FETs for Low-Voltage Applications." *Semiconductor Science and Technology*, vol. 26, no. 8, 085001, 2011.
- [81] R. Gandhi, Z. Chen, N. Singh, K. Banerjee, and S. Lee. "Vertical Si-Nanowire n - p -Type Tunneling FETs With Low Subthreshold Swing (≤ 50 mV/decade) at Room Temperature", *IEEE Electron Device Letters*, vol. 32, no. 4, pp. 437-439, 2011.
- [82] V. Saripalli, S. Datta, V. Narayanan, and J. P. Kulkarni. "Variation-tolerant ultra low-power heterojunction tunnel FET SRAM design", *IEEE/ACM International Symposium on Nanoscale Architectures*, pp. 45-52, 2011.
- [83] A. Tura, Z. Zhang, P. Liu, Y.-H. Xie, and J. CS Woo. "Vertical silicon pnpn tunnel nMOSFET with MBE-grown tunneling junction," *IEEE transactions on electron devices*, vol. 58, no. 7, pp. 1907-1913, 2011.
- [84] W. Cao, C. J. Yao, G. F. Jiao, D. Huang, H. Y. Yu, and M.-F. Li. "Improvement in reliability of tunneling field-effect transistor with p-n-i-n structure," *IEEE transactions on electron devices*, vol. 58, no. 7, pp. 2122-2126, 2011.

- [85] J. T. Smith, S. Das, and J. Appenzeller. "Broken-gap tunnel MOSFET: A constant-slope sub-60-mV/decade transistor." *IEEE electron device letters*, vol. 32, no. 10, pp. 1367-1369, 2011.
- [86] S. Saurabh and M. J. Kumar, "Novel attributes of a Dual Material Gate Nanoscale Tunnel Field-effect Transistor," *IEEE Trans. Electron Devices*, vol. 58, no. 2, pp. 404–410, Feb. 2011.
- [87] G. Dewey, B. Chu-Kung, J. Boardman, J. M. Fastenau, J. Kavalieros, R. Kotlyar, W. K. Liu et al. "Fabrication, characterization, and physics of III–V heterojunction tunneling field effect transistors (H-TFET) for steep sub-threshold swing." In *IEEE 2011 International Electron Devices Meeting*, pp. 33-6, 2011.
- [88] Pal, A. B. Sachid, H. Gossner, and V. R. Rao "Insights into the design and optimization of tunnel-FET devices and circuits" *IEEE Transactions on Electron Devices*, vol. 58, no. 4, pp. 1045-1053, 2011.
- [89] M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy efficient electronic switches," *Nature*, vol. 479, no. 7373, pp. 329–337, Nov. 2011.
- [90] L. Liu, D. Mohata, and S. Datta, "Scaling Length Theory of double-gate interband tunnel field-effect transistors," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 902–908, Apr. 2012.
- [91] R. Narang, M. Saxena, R. S. Gupta, and M. Gupta, "Assessment of Ambipolar Behavior of a Tunnel FET and Influence of Structural Modifications", *Journal of Semiconductor Technology and Science*, vol. 12, no. 4, pp. 482–491, 2012.
- [92] J. M. Lee, and W. Y. Choi. "Effects of device geometry on hetero-gate-dielectric tunneling field-effect transistors." *IEEE electron device letters*, vol. 33, no. 10, pp. 1459-1461, 2012.
- [93] Arnab Biswas, Surya Shankar Dan, Cyrille Le Royer, Wladyslaw Grabinski, Adrian M. Ionescu, "TCAD simulation of SOI TFETs and calibration of non-local band-to-band tunneling model", *Microelectronic Engineering*, vol. 98, pp. 334-337, 2012.
- [94] Sung Hwan Kim, "Germanium-Source Tunnel Field Effect Transistors for Ultra-Low Power Digital Logic," Electrical Engineering and Computer Sciences University of California at Berkeley May. 2012.
- [95] H.-Y. Chang, B. Adams, P.-Y. Chien, J. Li, and J. CS Woo, "Improved Subthreshold and Output characteristics of Source-Pocket Si Tunnel FET by the Application of

- Laser Annealing," *IEEE transactions on electron devices*, vol. 60, no. 1, pp. 92-96, 2012.
- [96] H. Riel, K. E. Moselund, C. Bessire, M. T. Björk, A. Schenk, H. Ghoneim, and H. Schmid. "InAs-Si heterojunction nanowire tunnel diodes and tunnel FETs." In *IEEE 2012 International Electron Devices Meeting*, pp. 16-6, 2012.
- [97] G. Lee, J.-S. Jang, and W. Y. Choi, "Dual-dielectric-constant spacer hetero-gate dielectric tunneling field-effect transistors," *Semiconductor Science and Technology*, vol. 28, no. 5, p. 052001, Mar. 2013.
- [98] Y. Chen, M. Fan, V. P. Hu, P. Su and C. Chuang, "Design and Analysis of Robust Tunneling FET SRAM," in *IEEE Transactions on Electron Devices*, vol. 60, no. 3, pp. 1092-1098, March 2013.
- [99] Rakhi Narang, M. Saxena, R. S. Gupta, and M. Gupta, "Drain current model for a gate all around (GAA) p-n-p-n tunnel FET," *Microelectronics Journal*, vol. 44, pp. 479-488, May 2013.
- [100] D. Verreck, A. S. Verhulst, K.-H. Kao, W. G. Vandenberghe, K. D. Meyer, and G. Groeseneken. "Quantum mechanical performance predictions of p-n-i-n versus pocketed line tunnel field-effect transistors." *IEEE transactions on electron devices*, vol. 60, no. 7, pp.2128-2134, 2013.
- [101] Y. Lee, D. Kim, J. Cai, I. Lauer, L. Chang, S. J. Koester, D. Blaauw, and D. Sylvester. "Low-power circuit analysis and design based on heterojunction tunneling transistors (HETTs)." *IEEE transactions on very large scale integration (VLSI) systems*, vol. 21, no. 9 pp. 1632-1643, 2013.
- [102] D. Sharma, and S. K. Vishvakarma, "Precise Analytical Model for Short-Channel Quadruple-Gate Gate-All-Around MOSFET", *IEEE Transactions on Nanotechnol*, vol. 12, no. 3, pp. 378-385, 2013.
- [103] H. Lu and A. Seabaugh, "Tunnel field-effect transistors: State-of-the-art," *IEEE J. Electron Devices Soc.*, vol. 2, no. 4, pp. 44-49, Jul. 2014
- [104] H. Liu, S. Datta and V. Narayanan, "Steep switching tunnel FET: A promise to extend the energy efficient roadmap for post-CMOS digital and analog/RF applications," *International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 145-150, 2013

- [105] R. Rooyackers, A. Vandooren, A. S. Verhulst, A. M. Walke, E. Simoen, K. Devriendt, S. Lo-Corotondo et al. "Ge-source vertical tunnel FETs using a novel replacement-source integration scheme." *IEEE Transactions on Electron Devices*, vol. 61, no. 12, pp. 4032-4039, 2014.
- [106] S. Datta, H. Liu, and V. Narayanan, "Tunnel FET technology: A reliability perspective," *Microelectron. Reliab.*, vol. 54, no. 5, pp. 861–874, 2014.
- [107] D. H. Morris, U. E. Avci, R. Rios, S. Member, and I. A. Young, "Design of Low Voltage Tunneling-FET Conduction Characteristics," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 4, no. 4, pp. 380–388, 2014.
- [108] E. Baravelli, E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, "TFET inverters with n-/p-devices on the same technology platform for low-voltage/low-power applications," *IEEE Transactions on Electron Devices*, vol. 61, no. 2, pp. 473-478, 2014.
- [109] K. Tomioka and T. Fukui, "Current increment of tunnel field-effect transistor using InGaAs nanowire/Si hetero junction by scaling of channel length," *Applied Physics Lett.*, vol. 104, pp. 073507-4, 2014.
- [110] D. B. Abdi and M. J. Kumar, "In-built N⁺ Pocket p-n-p-n tunnel field-effect transistor", *IEEE Electron Device Lett.*, vol. 35, no. 12, pp. 1170–1172, 2014.
- [111] M. Graef, T. Holtij, F. Hain, A. Kloes, Benjamín Iñíguez, "A 2-D closed form model for the electrostatics in hetero-junction double-gate tunnel-FETs for calculation of band-to-band tunneling current," *Microelectronics Journal*, vol. 45, pp. 1144-1153, Mar. 2014.
- [112] Upasana, R. Narang, M. Saxena, and M. Gupta, "Modeling and TCAD assessment for gate material and gate dielectric engineered TFET architectures: Circuit-level investigation for digital applications," *IEEE Trans. Electron Devices*, vol. 62, no. 10, pp.3348-3356, 2015.
- [113] S. Chander, and S. Baishya, "A Two-Dimensional Gate Threshold Voltage Model for a Heterojunction SOI-Tunnel FET With Oxide / Source Overlap," *IEEE Electron Device Letters*, vol. 36, no. 7, pp. 714–716, 2015.
- [114] M. Kumar and S. Jit, "A Novel Four-Terminal Ferroelectric Tunnel FET for Quasi-Ideal Switch," *IEEE Trans. Nanotechnology*, vol. 14, pp. 600-602, 2015.

- [115] S. Strangio *et al.*, "Impact of TFET Unidirectionality and Ambipolarity on the Performance of 6T SRAM Cells," in *IEEE Journal of the Electron Devices Society*, vol. 3, no. 3, pp. 223-232, May 2015.
- [116] N. Dagtekin and A.M. Ionescu, "Impact of Super-Linear Onset, Off-Region Due to Uni-Directional Conductance and Dominant C_{GD} on Performance of TFET-Based Circuits," *Journal of the Electron Devices Society*, vol. 3, no. 3, pp. 233–239, 2015.
- [117] S. Sant, and A. Schenk. "Methods to enhance the performance of InGaAs/InP heterojunction tunnel FETs," *IEEE Transactions on Electron Devices*, vol. 63, no. 5, pp. 2169-2175, 2015.
- [118] P. Wang, Yi Qi Zhuang, Cong Li, Zhi Jiang, and YuQi Liu, "Drain current model for double-gate tunnel field-effect transistor with hetero-gate-dielectric and source-pocket," *Microelectronics Reliability*, vol. 59, pp. 30-36, Feb. 2016.
- [119] F. Neves, S. Felipe, P. GD Agopian, J. A. Martino, B. Cretu, R. Rooyackers, A. Vandooren, E. Simoen, A. V.-Y. Thean, and C. Claeys. "Low-frequency noise analysis and modeling in vertical tunnel FETs with Ge source." *IEEE Transactions on Electron Devices*, vol.63, no. 4, pp. 1658-1665, 2016.
- [120] S. Strangio, P. Palestri, M. Lanuzza, F. Crupi, D. Esseni, and L. Selmi. "Assessment of InAs/AlGaSb Tunnel-FET Virtual Technology Platform for Low-Power Digital Circuits." *IEEE Transactions on Electron Devices* vol. 63, no. 7, pp. 2749-2756, 2016.
- [121] D. S. Yadav, D. Sharma, B. Ram Raad, and Varun Bajaj, "Impactful study of dual work function, underlap and hetero gate dielectric on TFET with different drain doping profile for high frequency performance estimation and optimization," *Superlattices and Microstructures*, vol. 96, pp. 36-46, Aug. 2016.
- [122] W. Y. Choi and H. K. Lee, "Demonstration of hetero-gate-dielectric tunneling field effect transistors (HG TFETs)," *Nano Convergence*, vol. 3, no. 1, pp. 1-15, 2016.
- [123] ATLAS: 3-D Device Simulator, SILVACO Int., Santa Clara, CA, USA, 2016.
- [124] SILVACO® (2016) ATLAS™ User's Manual.
<https://dynamic.silvaco.com/dynamicweb/jsp/downloads/>
- [125] S. Ahish, D. Sharma, Y. B. Nithin Kumar, and M. H. Vasantha, "Performance Enhancement of Novel InAs/Si Hetero Double-Gate TFET Using Gaussian Doping," *IEEE Trans. Electron Devices*, vol. 63, pp. 288-295, Jan. 2016.

- [126] A. Sharma, A. A. Goud, and K. Roy, "source underlapped GaSb-InAs TFETs with application to gain cell embedded DRAMs," *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2563–2569, 2016.
- [127] S. Kumar, E. Goel, K. Singh, B. Singh, M. Kumar, and S. Jit, "A Compact 2-D Analytical Model for Electrical Characteristics of Double-Gate Tunnel Field-Effect Transistors with a SiO₂/High-K Stacked Gate-Oxide Structure," *IEEE Transactions on Electron Devices*, vol. 63, no. 8 pp. 3291-3299, 2016.
- [128] Gopi, and S. S. Chauhan. "Double-gate Ge, In As-based tunnel FETs with enhanced ON-current." In *IEEE 2016 International Conference on Communication and Signal Processing (ICCSP)*, pp. 0639-0641, 2016.
- [129] S. Ahish, D. Sharma, M. H. Vasantha, and Y. B. N. Kumar. "Design and analysis of novel InSb/Si Heterojunction double gate tunnel field effect transistor." In *2016 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 105-109, 2016.
- [130] B. Abdi and M J Kumar, "Suppressing Amplipolar Conduction using Dual-Material in Tunnel-FETs Having Heavily Doped Drain," *Int. J. of Electronics and Communication Engineering*, vol. 10, no.5, pp. 594-598, 2016.
- [131] P. Wang, Y. Zhuang, C. Li, Z. Jiang, and Y. Q. Liu, "Drain current model for double-gate tunnel field-effect transistor with hetero-gate-dielectric and source-pocket," *Microelectronics Reliability*, vol. 59, pp. 30-36, 2016.
- [132] S. Kumar, E. Goel, K. Singh, B. Singh, P. K. Singh, K. Baral, and S. Jit, "2-D Analytical Modeling of the Electrical Characteristics of Dual-Material Double-Gate TFETs With a SiO₂/HfO₂ Stacked Gate-Oxide Structure," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 960–968, 2017.
- [133] J.-S. Liu, M. B. Clavel, and M. K. Hudait. "An energy-efficient tensile-strained Ge/InGaAs TFET 7T SRAM cell architecture for ultralow-voltage applications," *IEEE Transactions on Electron Devices*, vol. 64, no. 5, pp. 2193-2200, 2017.
- [134] L. Goroshko, E. A. Chusovitin, I. M. Chernev, A. V. Shevlyagin, K. N. Galkin, and N. G. Galkin, "Solid phase epitaxy formation of silicon-GaSb based heterostructures," in *Proc. JJAP Conf.*, vol. 5, Art. no. 011108, 2017.

- [135] P. N. Kondekar, K. Nigam, S. Pandey, and D. Sharma, "Electrically Doped Tunnel FET with Bandgap Engineering for Analog/RF Applications," *IEEE Trans. Electron Devices*, vol. 64, no. 2, pp. 412–418, 2017.
- [136] D. Kurniawan, S. Yang, and V. Thirunavukkarasu, 'Analysis of Ge-Si Heterojunction Nanowire Tunnel FET: Impact of Tunneling Window of Band-to-Band Tunneling Model', *Journal of the Electrochemical Society*, vol. 164, no. 11, pp. 3354–3358, 2017
- [137] Q. Wang, S. Wang, H. Liu, W. Li, and S. Chen, "Analog / RF performance of L- and U-shaped channel tunneling field-effect transistors and their application as digital inverters', *Jpn. J. Appl. Phys.* 56, 064102, 2017.
- [138] D. Gracia, D. Nirmal, A. Nisha Justeena, "Investigation of Ge based double gate dual metal tunnel FET novel architecture using various hetero dielectric materials," *Superlattices and Microstructures*, vol. 109, pp. 154-160, 2017.
- [139] Nupur Navlakha and Abhinav Kranti, "Insights into operation of planar tri-gate tunnel field effect transistor for dynamic memory application," *Journal of Applied Physics*, vol. 122, pp. 044502-1-9, May 2017.
- [140] *International Technology Roadmap for Semiconductors*. Accessed: 2018. [Online]. Available: <http://www.itrs2.net>
- [141] Fiore, J. Franco, M. Cho, F. Crupi, S. Strangio, P. J. Roussel, R. Rooyackers, N. Collaert, and D. Linten. "Single Defect Discharge Events in Vertical-Nanowire Tunnel-FETs." *IEEE Transactions on Device and Materials Reliability*, vol. 17, no. 1, pp. 253-258, 2017.
- [142] J. Madan, and R. Chaujar. "Temperature associated reliability issues of heterogeneous gate dielectric—Gate all around—Tunnel FET," *IEEE Transactions on Nanotechnology*, vol. 17, no. 1, 41-48, 2017.
- [143] Settino *et al.*, "Understanding the Potential and Limitations of Tunnel FETs for Low-Voltage Analog/Mixed-Signal Circuits," in *IEEE Transactions on Electron Devices*, vol. 64, no. 6, pp. 2736-2743, 2017
- [144] P. Xu, H. Lou, Lining Zhang, Z. Yu, and Xinnan Lin, "Compact Model for Double-Gate Tunnel FETs With Gate–Drain Underlap," *IEEE Trans. Electron Devices*, vol. 64, pp. 5242-5248, Dec. 2017.

- [145] E. Memisevic, J. Svensson, E. Lind and L. Wernersson, "Vertical Nanowire TFETs With Channel Diameter Down to 10 nm and Point SMIN of 35 mV/Decade," in *IEEE Electron Device Letters*, vol. 39, no. 7, pp. 1089-1091, July 2018.
- [146] Y. Guan, Z. Li, W. Zhang, Y. Zhang, and F. Liang, "An analytical model of gate-all-around heterojunction tunneling FET," *IEEE Transactions on Electron Devices*, vol. 65, no. 2, pp. 776-782, 2018.
- [147] E. Chusovitina, S. Dotsenko, S. Chusovitina, and D. Goroshko, 'Formation of a Thin Continuous GaSb Film on Si (001) by Solid Phase Epitaxy', *nanomaterials*, no.8, 987, pp. 7-9, 2018.
- [148] S. Shekhar, J. Madan, and R. Chaujar. "Source/gate material-engineered double gate TFET for improved RF and linearity performance: a numerical simulation." *Applied Physics A*, vol. 124, no. 11, 2018.
- [149] C. Convertino, C. B. Zota, H. Schmid, A. M. Ionescu, and K. E. Moselund. "III-V heterostructure tunnel field-effect transistor." *Journal of Physics: Condensed Matter*, vol. 30, no. 26, 264005, 2018.
- [150] S. Ahmad, B. Iqbal, N. Alam and M. Hasan, "Low Leakage Fully Half-Select-Free Robust SRAM Cells with BTI Reliability Analysis," in *IEEE Transactions on Device and Materials Reliability*, vol. 18, no. 3, pp. 337-349, Sept. 2018.
- [151] S. Ahmad, N. Alam, and M. Hasan, "Robust TFET SRAM cell for ultralow power IoT applications," *AEU Int. J. Electron. Commun.*, vol. 89, pp. 70-76, 2018.
- [152] S. Strangio, F. Settino, P. Palestri, M. Lanuzza, F. Crupi, D. Esseni, and L. Selmi. "Digital and analog TFET circuits: Design and benchmark." *Solid-State Electronics*, vol. 146, 50-65, 2018.
- [153] Seema, S. S. Chauhan, "Design of double gate vertical tunnel field effect transistor using HDB and its performance estimation," *Superlattice and Microstructures*, vol. 117, pp. 1-8, 2018.
- [154] Wang, G. Han, X. Jiang, Y. Liu, J. Zhang, and Y. Hao, "Improved performance in GeSn/SiGeSn TFET by hetero-line architecture with staggered tunneling junction," *IEEE Transactions on Electron Devices*, vol. 66, no. 4, pp. 1985-1989, 2019.

- [155] Kumar and M. M. De Souza, "A p-Channel GaN Heterostructure Tunnel FET with High ON/OFF Current Ratio," *IEEE Trans. Electron Devices*, vol. 66, no. 7, pp. 2916–2922, 2019.
- [156] S. Song, K. Lønsethagen, F. Laurell, T. W. Hawkins, J. Ballato, M. Fokine, and U. J. Gibson. "Laser restructuring and photoluminescence of glass-clad GaSb/Si-core optical fibres." *Nature communications*, vol. 10, no. 1, pp. 1-7, 2019.
- [157] M. Nogueira, P. GD Agopian, and J, A. Martino. "Silicon Nanowire Tunnel-FET Differential Amplifier Using Verilog-A Lookup Table Approach." In *2019 IEEE 34th Symposium on Microelectronics Technology and Devices (SBMicro)*, pp. 1-4. 2019.
- [158] K. Kato, K.-W. Jo, H. Matsui, H. Tabata, T. Mori, Y. Morita, T. Matsukawa, M. Takenaka, and S. Takagi, "p-Channel TFET Operation of Bilayer Structures with Type-II Heterotunneling Junction of Oxide-and Group-IV Semiconductors," *IEEE Transactions on Electron Devices*, vol. 67, no. 4, pp. 1880-1886, 2020.

IR1: <http://pubs.rsc.org/en/content/articlehtml/2015/NR/C4NR01600A>

IR2: http://www.slideshare.net/varun_bansal90/power-7535521

AUTHOR'S RELEVANT PUBLICATIONS

Journals:

1. **Manas Ranjan Tripathy**, Ashish Kumar Singh, A Samad, Sweta Chander, Kamalaksha Baral, Prince Kumar Singh and Satyabrata Jit, "Device and Circuit-Level Assessment of GaSb/Si Heterojunction Vertical Tunnel-FET for Low-Power Applications", *IEEE Transactions on Electron Devices*," *IEEE Transactions on Electron Devices*, vol. 67, no. 3, pp. 1285-1292, Feb. (2020).
2. **Manas Ranjan Tripathy**, Ashish Kumar Singh, Kamalaksha Baral, Prince Kumar Singh and Satyabrata Jit, "III-V/Si Staggered Heterojunction Based Source-Pocket Engineered Vertical TFETs for Low Power Applications," *Elsevier Superlattice and Microstructures*, Vol. 142, 2020, 106494, April (2020).
3. **Manas Ranjan Tripathy**, Ashish Kumar Singh, A Samad, Prince Kumar Singh, Kamalaksha Baral, and Satyabrata Jit, "Impact of Heterogeneous Gate Dielectric on DC, RF and Circuit-Level Performance of Source-Pocket Engineered Ge/Si Heterojunction Vertical TFET," *IOP Semiconductor Science and Technology*, vol. 35, 2020, 105014, Sept. (2020).
4. **Manas Ranjan Tripathy**, and Satyabrata Jit, "Lateral and Vertical Gate Oxide Stacking Effect on Noise Margins and Delays for the 8T SRAM Designed with Source Pocket Engineered GaSb/Si Heterojunction Vertical TFET," *IEEE Transactions on Device and Materials Reliability*, vol. 21, no. 3, Sept. (2021).

International/National Conferences:

1. **Manas Ranjan Tripathy**, Ashish Kumar Singh, and Satyabrata Jit, "TCAD Assessment Based Device to Circuit-Level Performance Comparison Study of Source Pocket Engineered All-Si Vertical Tunnel FET and GaSb/Si Heterojunction Vertical Tunnel FET," *2020 17th IEEE India Council International Conference (INDICON)*, New Delhi, India, 2020.
2. **Manas Ranjan Tripathy**, A Samad, Ashish Kumar Singh, Prince Kumar Singh, Kamalaksha Baral, and Satyabrata Jit, "Device and Circuit-Level Performance Comparison of Vertically Grown All-Si and Ge/Si Hetero-Junction TFET," *2020 IEEE International Conference on Electronics, Computing and Communication Technologies*

Author's Relevant Publications

(*CONECCT*), Bangalore, India, pp. 1-6, 2020. [**Overall Best Paper Award (Academia)** and **Best Paper Award** in the category of VLSI]

3. **Manas Ranjan Tripathy**, Ashish Kumar Singh, A Samad, Kamalaksha Baral, Prince Kumar Singh, and Satyabrata Jit, "Performance Comparison of Ge/Si Hetero-Junction Vertical Tunnel FET with and Without Gate-Drain Underlapped Structure with Application to Digital Inverter," *2020 4th IEEE Electron Devices Technology & Manufacturing Conference (EDTM)*, Penang, Malaysia, 2020.
4. **Manas Ranjan Tripathy**, Ashish Kumar Singh, Sweta Chander, Prince Kumar Singh, Kamalaksha Baral, and Satyabrata Jit, "Device-Level Performance Comparison of Some Pocket Engineered III-V/Si Hetero-Junction Vertical Tunnel Field Effect Transistor," *2020 5th International Conference on Devices, Circuits and Systems (ICDCS)*, Coimbatore, India, 2020, pp. 180-183.