CERTIFICATE

It is certified that the work contained in the thesis titled **"Performance Investigation of Some Heterojunction TFETs on SELBOX Substrates: Application to Dielectric Modulated Label-Free Biosensors"** by **"Ashish Kumar Singh"** has been carried out under my supervision and that this work has not been submitted elsewhere for a degree.

It is further certified that the student has fulfilled all the requirements of Comprehensive Examination, Candidacy and SOTA for the award of Ph. D. Degree.

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DECLARATION BY THE CANDIDATE

I, Ashish Kumar Singh, certify that the work embodied in this Ph. D. thesis is my own bonafide work and carried out by me under the supervision of Prof. S. Jit from "25/07/2017" to "06/07/2022", at the Department of Electronics Engineering, Indian Institute of Technology (Banaras Hindu University), Varanasi. The matter embodied in this Ph. D. thesis has not been submitted for the award of any other degree/diploma.

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It is certified that the above statement made by the candidate is correct to the best of my knowledge.

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Ashish Kumar Singh

Date: 6/7/2022 **(Ashish Kumar Singh)**

Dedicated

To

My Beloved Son

“Suryansh Singh”

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LIST OF ABBREVIATIONS

Abbreviation	Details
BTBT	Band-to-band Tunneling
TFET	Tunnel Field Effect Transistor
2-D	Two Dimensional
3-D	Three Dimensional
SCEs	Short Channel Effects
DG	Double Gate
BG	Back Gate
MOS	Metal Oxide Semiconductor
FET	Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
SOI	Silicon-on-Insulator
IC	Integrated Circuit
SS	Subthreshold Swing
SMG	Single Material Gate
TMG	Triple Material Gate
DMG	Dual/Double Material Gate
CMOS	Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
TEM	Tunneling Electron Microscope
BOX	Buried Oxide
SELBOX	Selective Buried Oxide
TCAD	Technology Computer-Aided Design

ITRS	International Technology Roadmap for Semiconductors
EOT	Equivalent Oxide Thickness
NW	Nanowire
ALD	Atomic Layer Deposition
L-BTBT	Lateral-Band to Band Tunneling
DM	Dual Material
JLFET	Junctionless Field Effect Transistor
SRAM	Static Random-Access Memory
TFP	Transconductance Frequency Product

LIST OF SYMBOLS

Symbol	Details
f_T	Unity Gain Frequency
f_{max}	Maximum Frequency of Oscillation
E_g	Energy Band Gap
Vel_0	Ballistic Velocity
E_C	Conduction Band energy
E_V	Valance Band Energy
q	Electronic Charge
T	Temperature in Kelvin
KT	Thermal Energy
V_T	Thermal Voltage
V_{th}	Threshold Voltage
I_D	Drain Current
$N_{S/D}$	Source/Drain Doping
N_{ch}	Channel Doping
g_m	Transconductance
g_d	Output-Conductance
I_{ON}	ON Current
I_{OFF}	OFF Current
I_{leak}	Leakage Current
V_{GS}	Gate-to-Source Voltage
V_{DS}	Drain-to-Source Voltage
t_{si}	Channel Thickness
w_{si}	Width of the Channel
t_{ox}	Oxide Thickness

LIST OF SYMBOLS

R	Radius of the Channel
L	Length of the Channel
ψ	Potential Function
nm	Nanometer
V	Voltage
L	Channel Length
eV	Electron Volt
mA	Milli Ampere
µm	Micro Meter
V_f	Quasi-fermi Level
ni	Intrinsic Concerntration
m_e	Effective Mass
h	Plank Constant
λ	Wave Function
U	Potential Energy
E	Discreatized Energy
r	Radial Coordinate
z	z-Coordinate
θ	Radial Coordinate
μ	Mobility
V_{tL}	Long Channel Threshold Voltage
SS	Subthreshold Slope

Abstract

The semiconductor industry has been on the lookout for alternative to MOSFETs due to the inability of MOSFETs to remain immune to downscaling in the term of performance. The ultimate objective at present is to design devices with principle of operation different from MOSFETs. Researchers have proposed novel devices which possess promising prospects as compared to MOSFETs in terms of performance from the perpective of present requirements of the semiconductor industry. This thesis presents work on one such emerging device, the Tunnel Field Effect Transistor (TFET). The device geomentry of TFET is similar to MOSFET except that its source and drain regions are oppositely doped with an intrinsic channel. The device operates by interband (Zener) tunneling caused by electric field modulation at source/channel junction by a controlling electrode. In this thesis work till chapter 5, I have done the performance investigation of some heterojunction TFETs on SELBOX substrate with and without back gated. All chapters contain extensive electrostatic analysis such as DC, RF/analog, and linearity parameters. In chapter 6 and chapter 7, I have studied the dielectric modulation-based label-free biosensor of the proposed structure and compared it to state-of-art sensors. The works presented in the different chapters are summarized below.

Chapter 1 this chapter introduces the thesis by briefly presenting the drawbacks of the MOSFET including the effects of scaling, and the emergence of novel semiconductor devices. Various emerging device structures have been introduced to sustain MOSFET scaling for future generation IC technology. It has been discussed that tunnel field-effect transistors (TFETs) have a huge potential for reducing short channel effects (SCEs) that occur when MOS devices have been scaled. It comments on the working principle of TFETs and their suitability for low-power electronics applications. The general review of some important state-of-the-art literatures related to TFETs shows that there are ample opportunities for theoretical investigation of the electrical performance of TFET on SELBOX substrate with gate oxide engineering as well as low bandgap engineering. Circuit level-based study was also reviewed in order to make a better understanding of the TFETs in circuit-level applications. In the addition, Furthermore, we conducted a literature review on dielectric modulated biosensors based on the TFET technology.

Based on the literature survey, the scopes of the present thesis have been outlined in the last section of this chapter.

Chapter 2 this chapter proposes an electrostatic comparison between conventional fully depleted SOI TFET and proposed Heterojunction TFET on SELBOX Substrate. This chapter discusses the advantages of the proposed TFET structure over the conventional fully depleted SOI TFET structure. The major observations can be given as follows:

- This work investigates the DC and Analog/RF performance of a newly suggested GSHJ-STFET-based TFET structure with stacked HfO_2/SiO_2 gate and Ge (source)/Si (channel) heterojunction.
- The rapid rate of BTB tunneling of carriers from the source to the channel region is due to the presence of germanium (a low bandgap material) in the source region.
- It has been shown that the SELBOX structure demonstrates the advantages over SOI and bulk structures. So, it can be considered a good option while selecting between SOI and bulk structures. This is mainly due to the gap present in the buried oxide in the SELBOX structure.
- The SELBOX substrate has been used in the proposed TFET to reduce the lattice heat and improve the I_{ON}/I_{OFF} ratio.
- Vertical gate stacked SiO_2/HfO_2 is highly responsible for the reduction of the gate leakage current due to the higher physical thickness of the gate oxide layer. The proposed TFET structure with SELBOX improves both DC and RF characteristics.

Chapter 3 In this chapter, we have investigated the influence of both the donor and acceptor type interface trap charges (ITCs) on the reliability of LS-STFET and VS-STFET in terms of their DC, analog/RF, and linearity parameters. This is a comparative analysis work based on their DC/RF and linearity parameters. The major observations in chapter 3 are given following.

- The presence of ITCs causes more severe effects on the performance degradation of VS-STFET than the LS-STFET structure. Thus, the proposed LS-STFET is more reliable than the VS-STFET device structure.

- Therefore, the LS-STFET device structure can be considered a promising MOS device for low-power and high-frequency applications.

Chapter 4 this chapter reports the design and device-level simulation analysis of a back-gated Ge/Si heterojunction TFET on SELBOX substrate (BG-HJ-STFET). There are some major points listed below about chapter 4:

- The proposed structure implements a stacked gate oxide where the conventional SiO2 is replaced by a SiO_2/HfO_2 in a stacked manner to increase its On-current.
- A back gate (BG) is also considered in the proposed TFET to enhance the device-level performance.
- Investigation of DC, RF, and linearity parameters such as drain current, transconductance, electric field, parasitic capacitance, cut-off frequency (fT), gain-bandwidth product (GBP), intrinsic delay (ꚍ), higher-order of gm (gm2, gm3), VIP2, VIP3, IIP3, IMD3, and 1-dB compression point are carried out for the proposed TFET and the results are compared with other conventional structures.
- Finally, we have discussed back gate effects on the performance of the proposed TFET.
- Performance evaluation shows that BG-HJ-STFET is a suitable candidate for distortionless and high-frequency applications.

Chapter 5 this chapter reports the device-level performance of a back gated ferroelectric heterojunction TFET on SELBOX substrate (BG-Fe-HJ-STFET). The proposed structure implements a stacked gate oxide where the conventional SiO_2 is replaced by a SiO_2/ferroelectric oxide in a stacked manner to increase its on-current. The following major points of this chapter are listed below.

Investigation of DC, RF, and linearity parameters such as drain current, transconductance, electric field, parasitic capacitance, cut-off frequency (f_T), gain-bandwidth product (GBP), intrinsic delay (ꚍ), higher-order of g_m (g_{m2}, and g_{m3}), VIP2, VIP3, IIP3, IMD3, and 1-dB compression point are carried out for the proposed TFET and the results are compared with other conventional structures.