Chapter 4

Pseudo DC-link based Two-Stage Topology for Solar PV to Grid-Tied System

4.1 Introduction

In the earlier chapter, the power generated from the solar panels is harnessed using an electrolytic capacitor-less dual half-active bridge resonant converter (DHABRC) at maximum power point. This solar power can now be fed to the grid using a three-phase voltage source inverter cascaded to the DHABRC. So, in this chapter, the control of a grid-tied inverter for a pseudo-DC-link-based two-stage topology is discussed. To feed the solar power to the grid, inverters' synchronization is necessary for safe and efficient integration. Grid synchronization is a process where the inverter's phase, frequency, and voltage are matched with the grid system before connecting it. The control strategy utilizes a cascaded control structure for the two-stage topology, as shown in Fig. 4.1. The inner current control is responsible for the precise control of the grid current, thereby enhancing the power quality and protecting the system from the overcurrent conditions. The outer voltage control loop regulated the DC-link voltage, ensuring balanced power flow in the system.

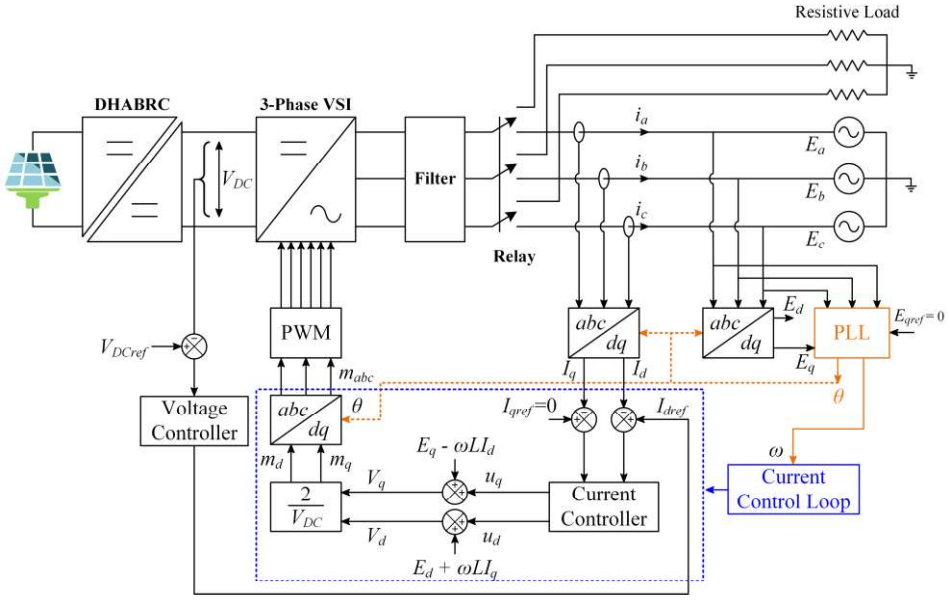


Fig. 4.1 Control structure of a grid-tied three-phase voltage source inverter.

4.2 Design of the Phase Locked Loop (PLL)

To ensure stable and efficient power transfer from solar PV to the grid, the inverter's AC output must be synchronised with the grid. The grid operates at a specific voltage, frequency (50 or 60 Hz), and phase. Since the direct measurement of the phase angle is not possible, a specific approach is required to extract the parameter. A synchronous reference frame (SRF) based phase locked loop (PLL) is employed in this work. In the SRF method, the grid voltage goes through two simple transformations: Clark and Park transformations. These transformations convert a three-phase stationary reference frame into a two-phase rotating reference frame. The grid voltage's phase angle (θ) is determined using its angular frequency (ω). The block diagram representation of the PLL is shown in Fig. 4.2.

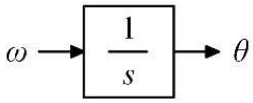


Fig. 4.2 Block diagram representation of the Phase Locked Loop (PLL).

4.2.1 Transformation of Reference Frames/ Coordinate Systems

In SRF, there are two transformations-

a. Conversion of a three-phase *a-b-c* stationary reference frame to a two-phase α-β stationary reference frame.

b. Conversion of a two-phase α-β stationary reference frame to a *d-q* rotating reference frame.

The first conversion uses Clark's transformation, and another uses Park's transformation. The conversion of the coordinate systems or reference frames is shown in Fig. 4.3, and the corresponding transformation matrices are shown in Table 4.1.

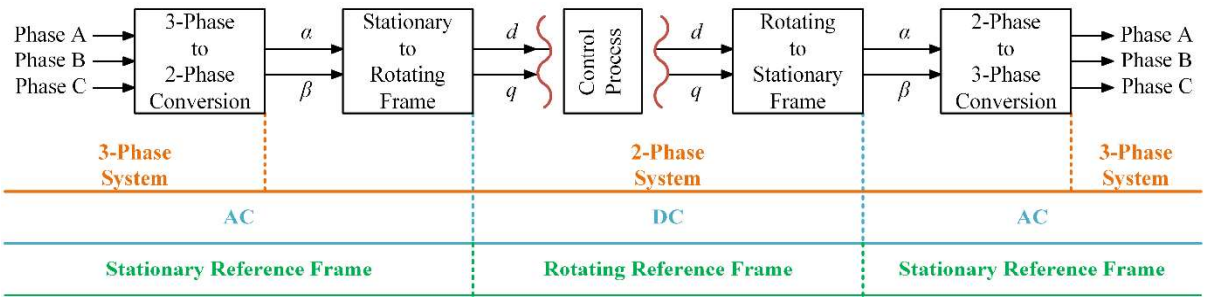


Fig. 4.3 Conversion of the coordinate systems.

Table 4.1 Clark and Park transformation and their inverse transformation

Transformation	Transform's	Transformation Matrices
Clark Transformation	From *a-b-c* to *α-β*	$\frac{2}{3}\cdot\begin{bmatrix}1 & -1/2 & -1/2\\ 0 & \sqrt{3}/2 & -\sqrt{3}/2\end{bmatrix}$
Inverse Clark Transformation	From *α-β* to *a-b-c*	$\begin{bmatrix}1 & 0\\ -1/2 & \sqrt{3}/2\\ -1/2 & -\sqrt{3}/2\end{bmatrix}$
Park Transformation	From *α-β* to *d-q*	$\begin{bmatrix}\cos\theta & \sin\theta\\ -\sin\theta & \cos\theta\end{bmatrix}$
Inverse Park Transformation	From *d-q* to *α-β*	$\begin{bmatrix}\cos\theta & -\sin\theta\\ \sin\theta & \cos\theta\end{bmatrix}$

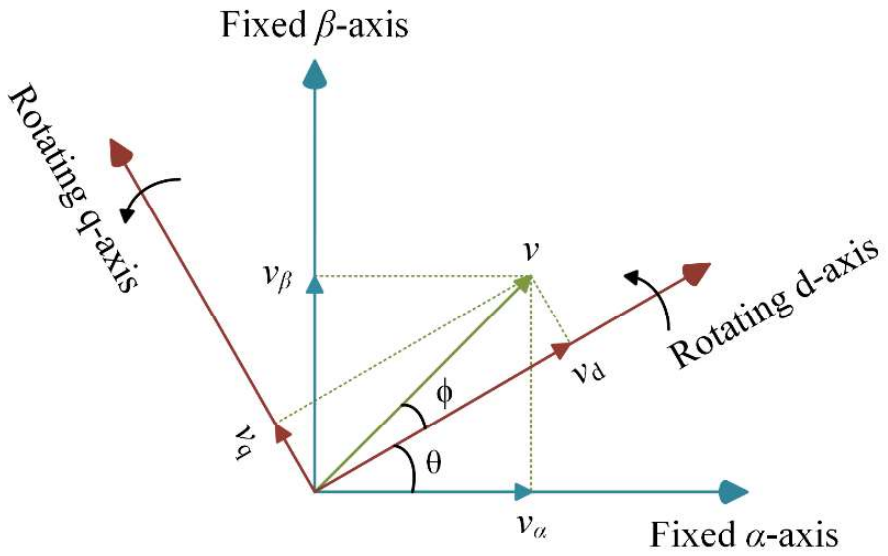


Fig. 4.4 Transformation of axes from *α-β* to *d-q* reference frame.

To ease the calculation, the *α*-axis of the *α-β* stationary reference frame is placed in such a way that it aligns with the *a*-axis of the three-phase *a-b-c* stationary reference frame. The *d-q* rotating reference frame is rotating at synchronous speed '*ω*' with respect to the *α-β* stationary reference frame. At a given instant, the d-axis of the *d-q* rotating reference frame is leading

ahead of the α-axis of the α-β stationary reference frame by an angle θ. It can be defined as (4.1). The transformation of the axes is shown in Fig. 4.4.

$$\theta = \tan^{-1}\left(\frac{v_\beta}{v_\alpha}\right) \tag{4.1}$$

Here, v_α and v_β are the voltage components of the α-β stationary reference frame. Using the angle θ, the switching devices of the inverter are controlled, and the inverter's output is synchronised with the grid.

Now, the process of determining the phase angle associated with the grid data will be discussed. For the given system, the three-phase grid voltages v_a, v_b, and v_c can be presented as (4.2) - (4.4).

$$v_a = V_m \cos(\omega_g t) \tag{4.2}$$

$$v_b = V_m \cos(\omega_g t + 120^o) \tag{4.3}$$

$$v_c = V_m \cos(\omega_g t + 240^o) \tag{4.4}$$

Here, $\omega_g t = \theta_g$. Now, by subjecting the grid voltages, represented as (4.2) - (4.4), to Clark's transformation for axis transformation, we get (4.5).

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \cdot \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}$$

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = V_m \begin{bmatrix} \cos\theta_g \\ \sin\theta_g \end{bmatrix} \tag{4.5}$$

Now, transforming the (4.5) into a d-q rotating reference frame using Park's transformation, we get (4.6).

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix}$$

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = V_m \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} \cos\theta_g \\ \sin\theta_g \end{bmatrix}$$

$$\begin{aligned} v_d &= V_m \cos(\theta_g - \theta) \\ v_q &= V_m \sin(\theta_g - \theta) \end{aligned} \tag{4.6}$$

Now, the controller for PLL is designed so that θ becomes equal to the θ_g. From (4.6), it can be observed that even after the transformation, the output of the inverter has the same frequency and phase as that of grid voltage. So, for synchronization, the difference between θ and θ_g will be very small, and then (4.6) can be rearranged as (4.7).

$$v_d = V_m$$
$$v_q = V_m(\theta_g - \theta) \tag{4.7}$$

The PLL's angular frequency can be defined as

$$\omega = \frac{d\theta}{dt} = G_{CP} V_q \tag{4.8}$$

Here, G_{CP} denotes the PLL's controller transfer function. Applying the Laplace transform on (4.8) will result in (4.9).

$$s\theta(s) = G_{CP}(s) V_m(\theta_g(s) - \theta(s)) \tag{4.9}$$

Using (4.9), the block diagram representation of the linearised model of the PLL is shown in Fig. 4.5.

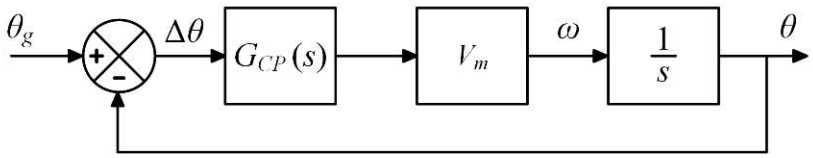


Fig. 4.5 Block diagram representation of the SRF-based PLL.

To achieve synchronisation, the reference value of the q-axis (v_{qref}) is subjected as zero, as shown in the block diagram representation of the control system for the PLL in Fig. 4.6. In Fig. 4.6. ω_o denotes the fundamental frequency of the grid in radian/seconds. The plant transfer function ($G_P(s)$) for the PLL can be given using Fig. 4.5 as (4.10). The voltage V_m for a grid system with a phase voltage of V_{ph} can be calculated as $\sqrt{2}*V_{\text{ph}}$ Volts. The bode plot for $G_P(s)$ is shown in Fig. 4.7. For the PLL, two controllers are discussed below: PI controller and K-factor-based -controller.

$$G_P(s) = \frac{V_m}{s} \tag{4.10}$$

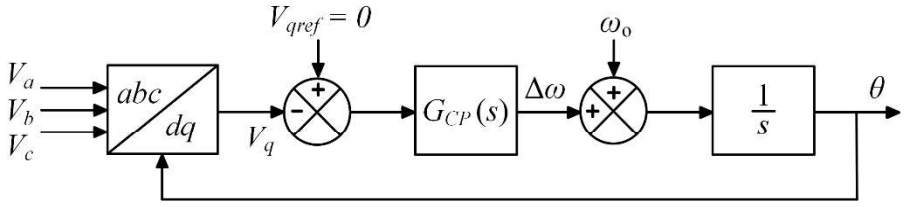


Fig. 4.6 Block diagram representation of the control system for the PLL.

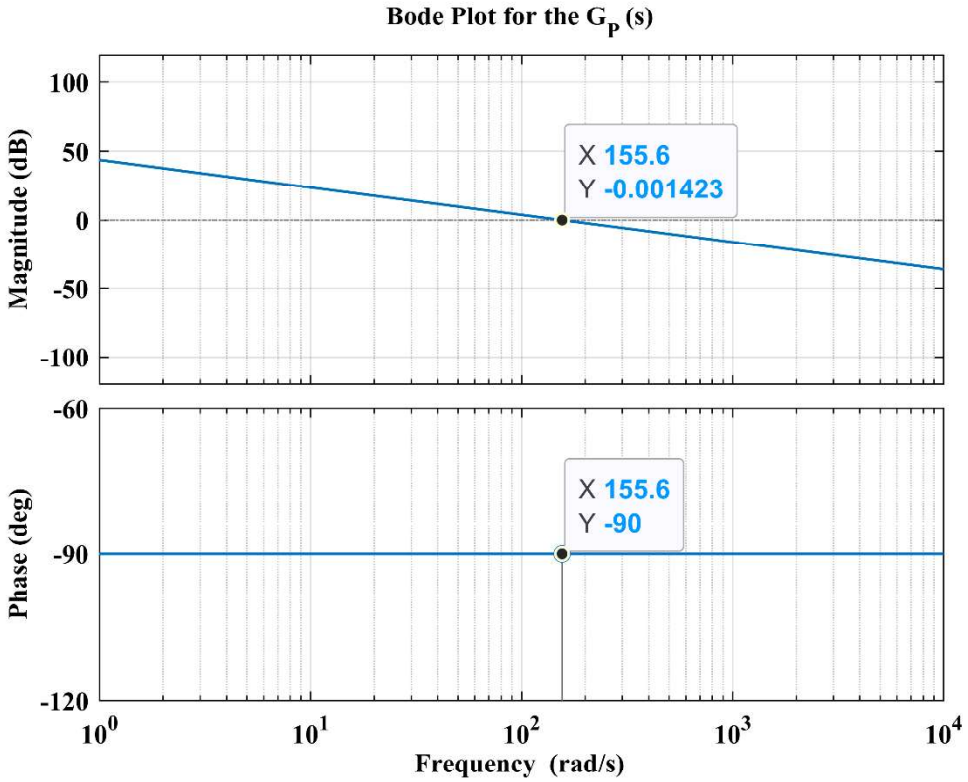


Fig. 4.7 Bode plot of the PLL's transfer function.

4.2.2 Design of the PLL control using the PI controller

To synchronize the inverter's output with the grid system, a proportional-integral (PI) controller can be used. A PI controller can be represented in s-domain as (4.11).

$$TF_{PI}(s) = K_p + \frac{K_i}{s} = K_p\left(\frac{1+sT}{sT}\right) \tag{4.11}$$

Here, K_p, K_i, and T denote the proportional gain, integral gain, and integral time constant. The open loop transfer function (OLTF) for PLL with PI controller can be given as (4.12).

$$G_{P1}(s) = G_P(s).TF_{PI}(s) = \frac{V_m}{s}\left(K_p + \frac{K_i}{s}\right) \tag{4.12}$$

The characteristics equation for the OLTF G_{PI}(s) can be given as (4.13).

$$s^2 + sK_pV_m + K_iV_m = 0 \tag{4.13}$$

The PLL's bandwidth is tuned to achieve a settling time of 4 ms for a steady state error of 2%. The bandwidth is calculated to be 1000 rad/sec for the required error and settling time. Let the

control loop have a damping ratio $\xi = 0.7$. These constraints will lead to controller gains to be as (4.14). The bode plot of the OLTF with PI controller is shown in Fig. 4.8.

$$K_p = \frac{2\xi\omega_n}{V_m} \text{ and } K_i = \frac{\omega_n^2}{V_m} \tag{4.14}$$

Using the above method, the controller provides the PM of 65.1° at the gain cross-over frequency (ω_{gc}) of 1000 rad/sec. Although the response of the PLL is satisfactory with the PI controller, we can use a K-factor-based controller to achieve a better response.

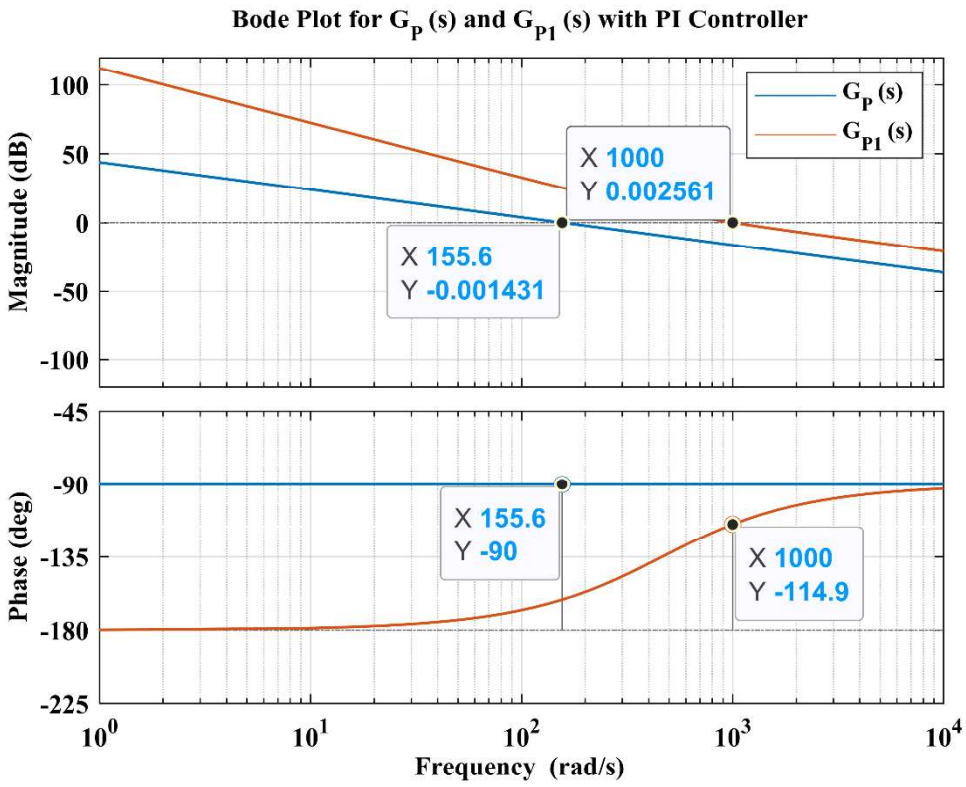


Fig. 4.8 Bode plot of the PLL (G_P(s)) and open loop transfer function of the PLL (G_{PI}(s)) with PI controller.

4.2.3 Design of the PLL control using K-factor Controller

The K-factor controller is a type-II compensator with a phase boost of 0° to 90°. The pole and zero are placed so that their ratio is always '*K*', hence, the name K-factor controller. In the s-domain, the K-factor can be given as (4.15).

$$TF_K(s) = K_c\left(\frac{1+s/\omega_z}{1+s/\omega_p}\right) \tag{4.15}$$

Let the gain cross-over frequency required for designing the controller is $\omega_{gc} = 1000$ rad/sec with a phase boost of $\phi_b = 60^o$. So, the phase boost, location of the pole, zero, and gain K_C can be calculated as (4.16) - (4.18).

$$K = \tan\left(\frac{\phi_b}{2} + 45^o\right) \tag{4.16}$$

$$\omega_p = K\omega_{gc} \text{ and } \omega_z = \frac{\omega_{gc}}{K} \tag{4.17}$$

$$K_c = \frac{\omega_z}{G_{gc}} \tag{4.18}$$

Here G_{gc} is the PLL gain observed at the $\omega_{gc} = 1000$ rad/sec. The following data is used to design the K-factor controller for the given PLL.

$$K = 3.732,\ \omega_p = 3732.1,\ \omega_z = 267.94, \text{ and } K_c = 1772.4$$

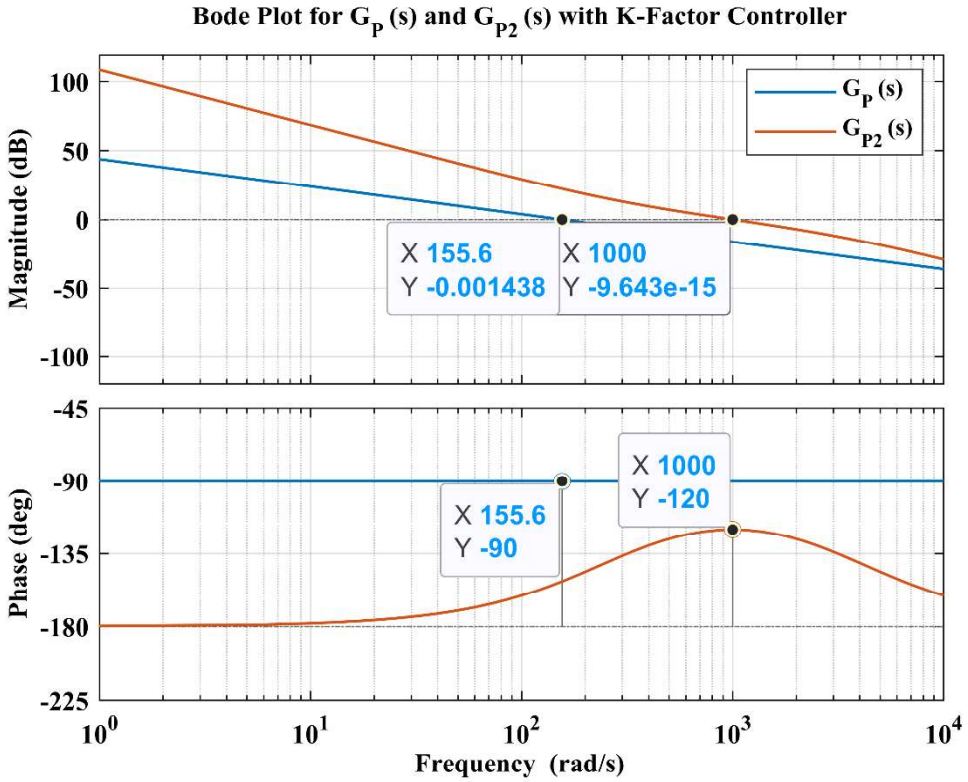


Fig. 4.9 Bode plot of the PLL (G_P(s)) and open loop transfer function of the PLL (G_{P2}(s)) with K-factor controller.

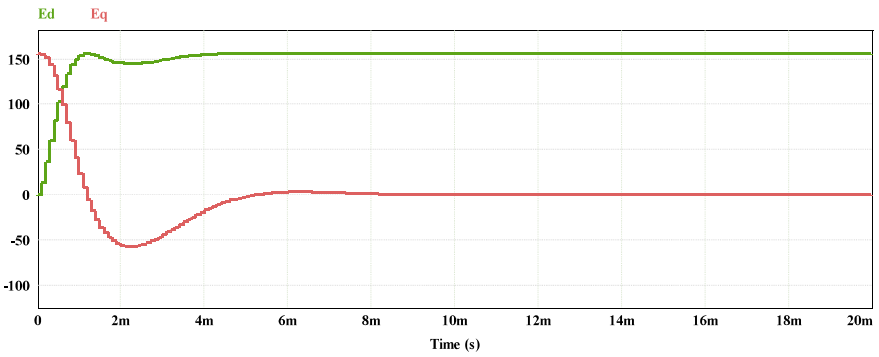
The open loop transfer function for PLL with K-factor controller can be given as (4.19).

$$G_{P12}(s) = G_P(s).TF_K(s) = \frac{V_m}{s} K_c \left(\frac{1 + s/\omega_z}{1 + s/\omega_p} \right) \tag{4.19}$$

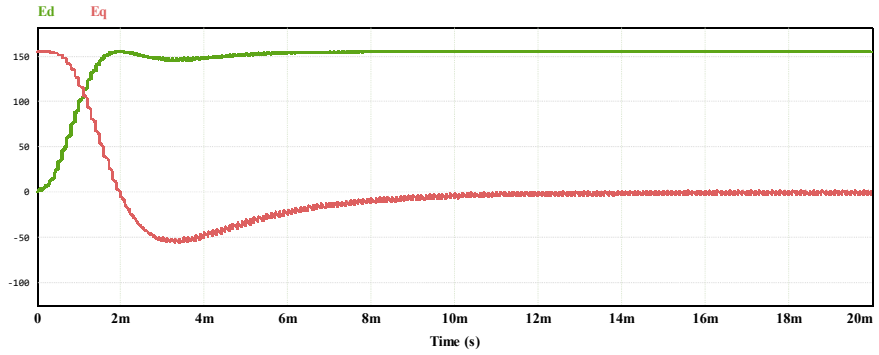
The bode plot of the open loop transfer function with the K-factor controller is shown in Fig. 4.9. Using this method, the controller provides the PM of 60° at the gain cross-over frequency of 1000 rad/sec.

4.2.4 Simulation Results Corresponding the PI and the K-factor Controller

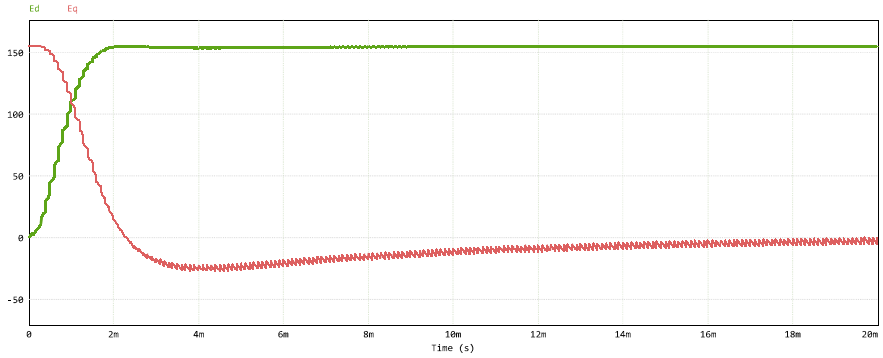
The simulation results corresponding to the controller mentioned above are shown in Fig. 4.10 using the simulation software PSIM. In Fig. 4.10 (a), the grid voltages in *dq*- frame are demonstrated for the PI controller. The settling time for E_q is approximately 10 ms., and it goes through an overshoot of 57.3 V. In Fig. 4.10 (b), the grid voltages in *dq*- frame are shown for the K-factor controller. The settling time for E_q is approximately 14 ms. and goes through an overshoot of 54.25 V when designed for a phase margin of 60°. Also, if we try to increase the phase margin to 75°, then the settling time for E_q can be observed to be approximately 20 ms., and overshoot of 25.1 V as shown in Fig. 4.10 (c).



(a)



(b)



(c)

Fig. 4.10 Simulation results for the d-axis and q-axis voltages (a) With PI controller, (b) With K-factor controller (PM = 60º), and (c) With K-factor controller (PM = 75º).

4.3 State-space Modelling of the Voltage Source Inverter (VSI)

The state space modeling of a voltage source inverter provides a mathematical framework to analyze and design the behavior of a dynamic system. Fig. 4.11 shows a simple circuit diagram of the inverter connected to the 3-phase grid system. The three-phase grid voltages and inverter voltages are denoted as E_a, E_b, E_c and V_a, V_b, V_c, respectively. Per-phase resistance and inductances are denoted as R and L. The current injected into the grid system is denoted as i_a, i_b, and i_c.

Applying the KVL in Fig. 4.11 will result in (4.20).

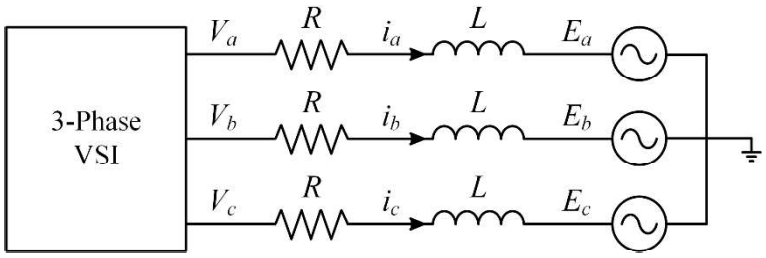


Fig. 4.11 Circuit diagram representation of the VSI integrated with grid system.

$$\begin{aligned} V_a &= E_a + L\frac{di_a}{dt} + Ri_a \\ V_b &= E_b + L\frac{di_b}{dt} + Ri_b \\ V_c &= E_c + L\frac{di_c}{dt} + Ri_c \end{aligned} \tag{4.20}$$

Rearranging (4.20) into state-space form will give (4.21).

$$
\begin{aligned}
L\frac{di_a}{dt} &= -Ri_a + (V_a - E_a) \\
L\frac{di_b}{dt} &= -Ri_b + (V_b - E_b) \\
L\frac{di_c}{dt} &= -Ri_c + (V_c - E_c)
\end{aligned}
\tag{4.21}
$$

Now, using the Clarks and Parks transformation discussed earlier, converting (4.21) into dq-reference frame as

$$
\begin{bmatrix} \frac{di_d}{dt} \\ \frac{di_q}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -\omega \\ \omega & -\frac{R}{L} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{1}{L} \begin{bmatrix} V_d - E_d \\ V_q - E_q \end{bmatrix}
\tag{4.21}
$$

Expanding (4.21) will result in (4.22).

$$
\begin{aligned}
\frac{di_d}{dt} &= -\frac{R}{L} i_d - \omega i_q + \frac{1}{L}\left(V_d - E_d\right) \\
\frac{di_q}{dt} &= -\frac{R}{L} i_q + \omega i_d + \frac{1}{L}\left(V_q - E_q\right)
\end{aligned}
\tag{4.22}
$$

It can be observed from (4.22) that the *d*-axis current contains some terms of the *q*-axis and *q*-axis, and the current contains some terms of the *d*-axis, which means both currents are cross-coupled. The cross-coupling terms are considered to be a disturbance to the system. To achieve smooth control, we need to decouple the axis currents, and the final inverter equations should be in the form shown in (4.23).

$$
\begin{aligned}
\frac{di_d}{dt} &= -\frac{R}{L} i_d + \frac{1}{L} u_d \\
\frac{di_q}{dt} &= -\frac{R}{L} i_q + \frac{1}{L} u_q
\end{aligned}
\tag{4.23}
$$

Here, u_d and u_q are the intermediate terms required to decouple the inverter currents. Comparing (4.22) and (4.23) will give (4.24) as follows:

$$
\begin{aligned}
u_d &= V_d - E_d - L\omega i_q \\
u_q &= V_q - E_q + L\omega i_d
\end{aligned}
\tag{4.24}
$$

From (4.24), it can be concluded that the inverter output voltage must be regulated to achieve the decoupled *dq*-axis current. The inverter voltages should provide output voltages of (4.25).

$$
\begin{aligned}
V_d &= u_d + E_d + L\omega i_q \\
V_q &= u_q + E_q - L\omega i_d
\end{aligned}
\tag{4.25}
$$

The compensation required in the inverter voltage to achieve decoupled axis currents is called voltage feed-forward compensation. The compensation is necessary to achieve better performance for the closed-loop control. A conventional sinusoidal pulse width modulation (SPWM) technique is adapted for the given system. In SPWM, the relationship between the DC-link voltage and the inverter output voltage can be given as (4.26).

$$V_d = m_d \frac{V_{dc}}{2}$$
$$V_q = m_q \frac{V_{dc}}{2} \tag{4.26}$$

In (4.26), m_d and m_q denote the modulation index in the dq- reference frame.

4.4 Design of the Inner Current Control Loop

Based on the relationship derived using the system model presented via (4.23), the inner current control loop can be presented in dq-frame. The inner current control loop incorporates PI controllers, decoupling elements, and feed-forward terms for both the axis's currents i_d and i_q. The block diagram representation of the inner current control loop is shown in Fig. 4.12.

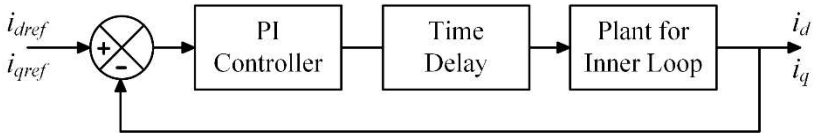


Fig. 4.12 General block diagram representation of the inner current control loop.

In the inner loop, there are two PI controllers corresponding to each d and q-axis current. The error in each axis current is used to generate the required voltage value. The overview of each block is discussed below.

4.4.1 Plant Transfer Function for the Current Control

From the decoupling control, the plant transfer function for the current control can be given using the Laplace transform of the (4.23) as (4.27) below, and it will be the same for both the d-axis and q-axis currents.

$$u(s) = \frac{1}{R(1+s\tau)} i(s) \tag{4.27}$$

In (4.27), the constant τ denotes the line time constant defined as $\tau = L/R$. The block diagram representation of the current control can be given in Fig. 4.13.

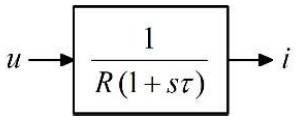


Fig. 4.13 Block diagram representation of the current control.

From the control perspective, a converter is considered an ideal transformer with a time delay. This time delay occurs between the control input and converter output due to the PWM switching. For three-phase VSI, the inverter's output voltage is assumed to follow a voltage reference with an average digital control delay (caused by the ADC sample and the PWM update) equal to 1.5 times the sampling period. For a switching frequency of 10 kHz, the time delay (T_w) will be 150 μs. The expression for the time delay can be given as follows:

$$v(t) = u(t - T_w) \tag{4.28}$$

Applying the Laplace transform will result in (4.29).

$$v(s) = \frac{1}{1 + sT_w} u(s) \tag{4.29}$$

So, the complete plant transfer function of the current control can be presented as (4.30)

$$G_I(s) = \frac{1}{1 + sT_w} \frac{1}{R(1 + s\tau)} \tag{4.30}$$

The plant transfer function of the current loop can be analyzed from (4.30). The plant has one dominating time constant (Line time constant τ) and another minor time constant (Due to delay). The bode plot for the plant is shown in Fig. 4.14. The plant has a phase margin of 130^o at a gain cross-over frequency of 16.12 Hz, and the gain margin is infinity.

4.4.2 PI Controller for Current Control

In the s-domain, the transfer function for the PI controller can be given as (4.31)

$$T_i(s) = K_{pi} + \frac{K_{ii}}{s} = K_{pi}\left(\frac{1 + sT_i}{sT_i}\right) \tag{4.31}$$

K_{pi}, K_{ii}, and T_i denote the proportional gain, integral gain, and integral time constant for the current control loop.

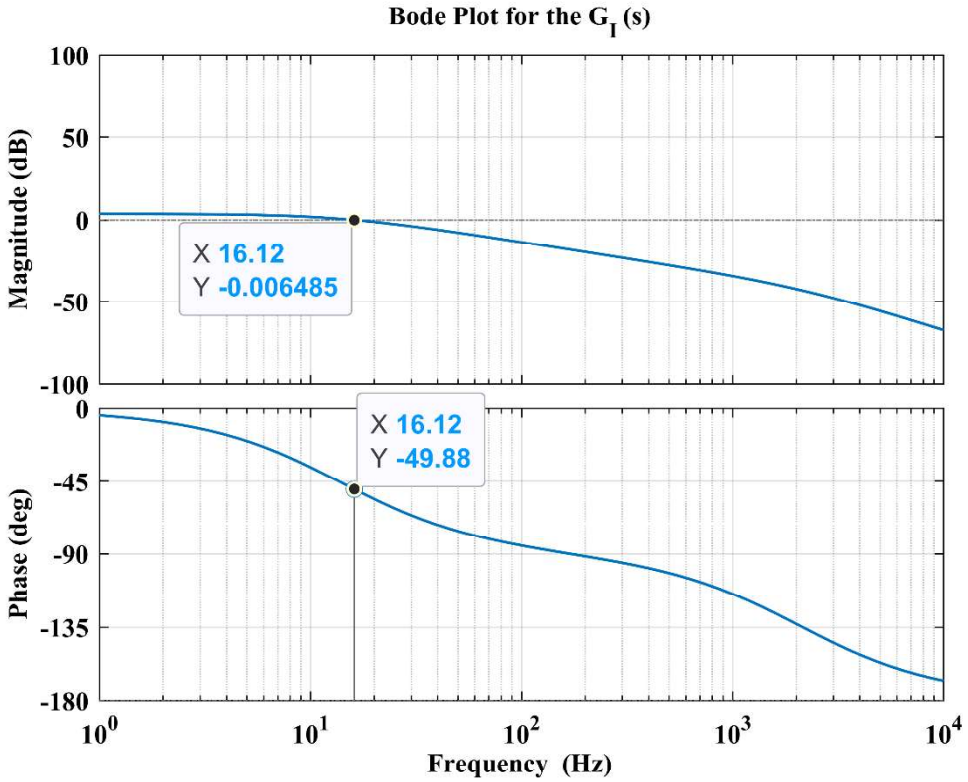


Fig. 4.14 Bode plot of the plant transfer function of the current control.

4.4.3 Complete Open Loop Transfer function

The complete open loop transfer function-based block diagram representation of the current control loop can be given in Fig. 4.15.

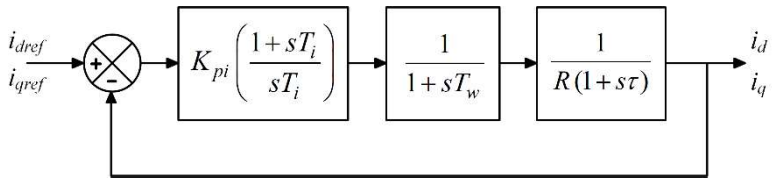


Fig. 4.15 Block diagram presentation of the inner current control loop.

In cascaded control, the inner control loop is generally required to be faster than the outer control loop. To achieve a faster response of the inner loop, the controller is tuned to have a bandwidth between 1/10 and 1/20 of the switching frequency. Also, to mitigate the harmonics around the switching frequency, the amplitude curve should cross the 0db line in such a way that it provides a phase margin of approximately more than 45°. A modulus optimum tuning

method is employed to optimize the loop's performance, resulting in a non-oscillatory and rapid closed-loop response.

4.4.4 Modulus Optimum Tuning Criterion

The modulus optimum tuning criterion (MOTC) is applied when the plant transfer function has one dominant and one minor time constant. For such plants, the dominant time constant is eliminated by the controller's zero to achieve a faster closed-loop response, and the closed-loop gain is maintained above unity for higher frequencies. Since this criterion offers a simple and effective solution with a fast response time, it has become popular for various applications. For the current control loop, the line time constant (τ) dominates in nature; it is canceled out with the PI controller's time constant (T_i). From Fig. 4.15, the open loop transfer function of the current control loop can be given as (4.32).

$$G_{I1}(s) = T_i(s).G_I(s) = K_{pi}\left(\frac{1+sT_i}{sT_i}\right)\frac{1}{1+sT_w}\frac{1}{R(1+s\tau)} \tag{4.32}$$

Now, as per the tuning criterion, eliminating the dominating time constant with the adjustable time constant of the PI controller $T_i = \tau$ will give (4.33).

$$G_{I1}(s) = T_i(s).G_I(s) = \frac{K_{pi}}{s\tau R}\left(\frac{1}{1+sT_w}\right) \tag{4.33}$$

The current control loop's closed-loop transfer function (CLTF) can be given as (4.34).

$$G_{CLI}(s) = \frac{K_{pi}/\tau RT_w}{s^2 + \frac{s}{T_w} + \frac{K_{pi}}{\tau RT_w}} \tag{4.34}$$

Comparing the denominator of (4.34) with the standard second-order characteristic equation will give the following damping factor and natural frequency.

$$\xi = \frac{1}{2}\sqrt{\frac{\tau R}{K_{pi}T_w}} \text{ and } \omega_n = \sqrt{\frac{K_{pi}}{\tau RT_w}}\,.$$

For a damping factor of $\xi = 1/\sqrt{2}$ and unity closed loop gain, the controller gains can be given as follows.

$$K_{pi} = \frac{\tau R}{2T_w} \text{ and } T_i = \tau \tag{4.35}$$

Based on the controller gains derived, the OLTF and CLTF of the current control loop can be given as (4.36) and (4.37).

$$G_{I1}(s) = \frac{1}{2T_w s}\left(\frac{1}{1+T_w s}\right) \tag{4.36}$$

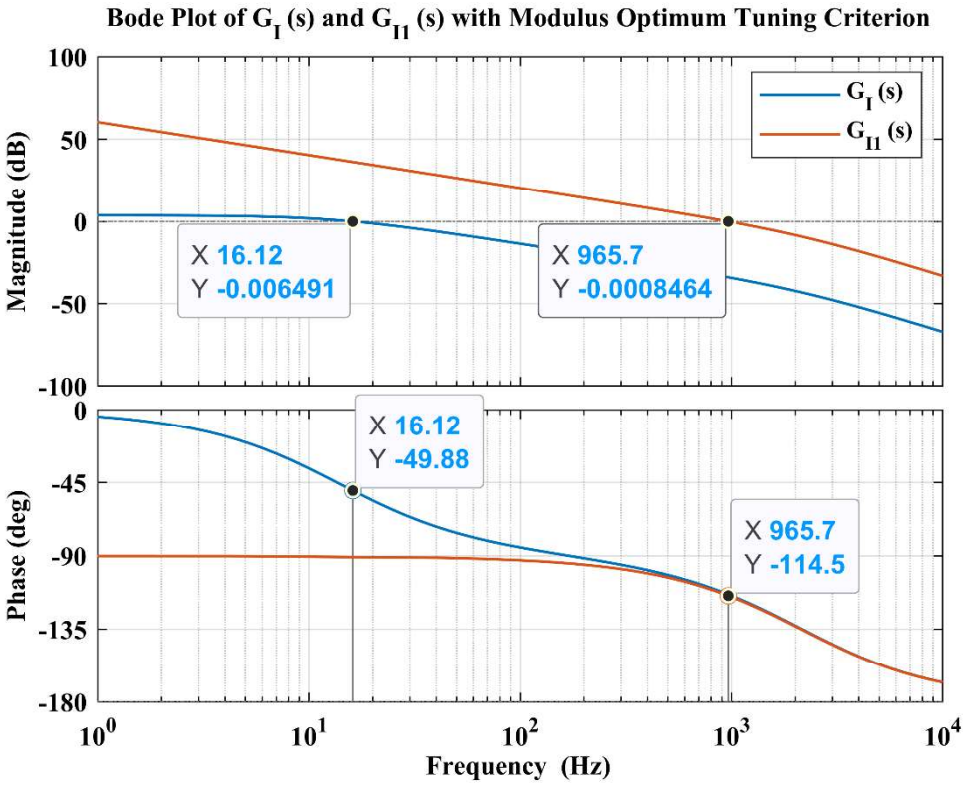


Fig. 4.16 Bode plot of the current control loop with MOTC.

The bode plot of the OLTF of the current control is shown in Fig. 4.16. With the designed controller based on MOTC, the OLTF has a phase margin of 65.53° at a gain cross-over frequency of 965.7 Hz. The gain margin for G_{I1} is infinity.

$$G_{CLI}(s) = \frac{1}{2T_w s^2 + T_w s + 1} \tag{4.37}$$

To analyze the transient and steady-state response of the controller designed, the step response of the designed control is given in Fig. 4.17. The step response has a peak overshoot of 4.32 %. The settling for the designed controller is 0.6 ms.

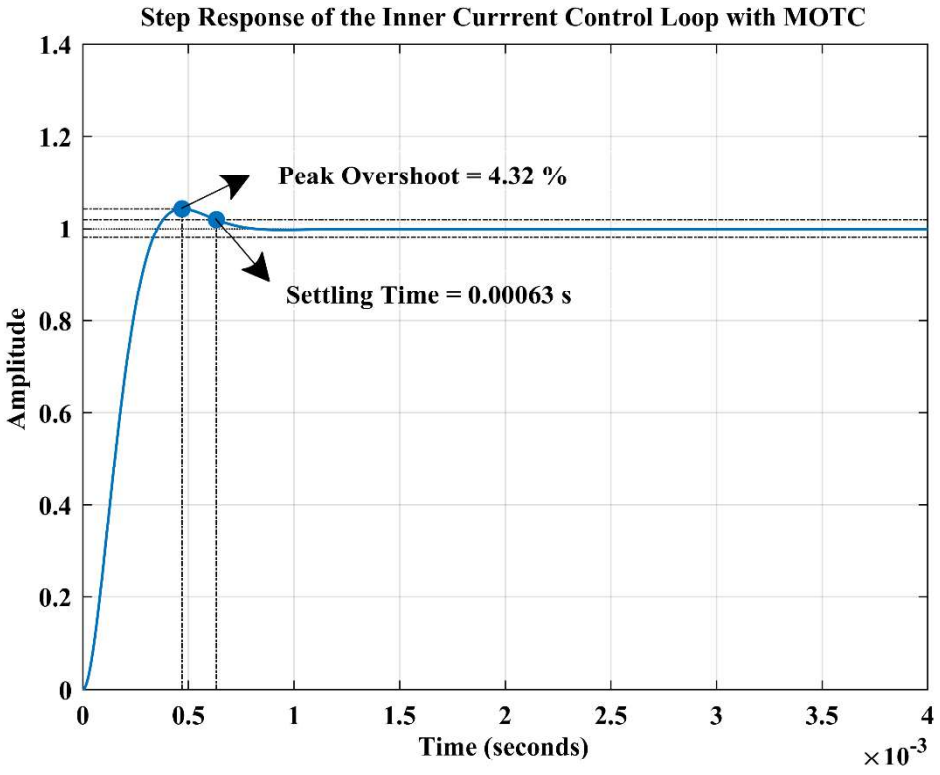


Fig. 4.17 Step Response of the current control loop with MOTC.

4.5 Design of the Outer Voltage Control Loop

The output from the solar PV panel is fluctuating in nature and depends upon the atmospheric conditions and temperature. To ensure optimal power extraction, the earlier proposed isolated DC-DC resonant converter tracks maximum power points. However, the output of the DC-DC converter or DC-link voltage also varies. By maintaining a constant DC-link voltage, the inverter can supply power to the grid with a current depending on solar PV's power. Since the inverter is grid-connected, its output voltage remains fixed, resulting in variations in the grid current to accommodate changes in solar power generation. So, the DC link voltage output acts as a reference for the inner current control loop. Since solar PV is required to feed only active power, the reactive part of the current reference (I_{qref}) is set to zero. The plant transfer function for the voltage control can be derived using the power balance between the DC link and the grid side. Let the power at the DC-link be the P_{DC}; at the grid side, it is P_{ac}. For balanced power transfer function-

$$P_{DC} = P_{ac} \tag{4.38}$$

For the fixed DC-link voltage V_{dc} and inverter side DC current I_{dc},

$$P_{DC} = V_{dc} I_{dc} \tag{4.39}$$

$$I_{dc} = C \frac{dV_{dc}}{dt} \tag{4.40}$$

The grid side power in the *dq*-frame can be given as (4.41).

$$P_{ac} = \frac{3}{2}(E_d I_d + E_q I_q) \tag{4.41}$$

For active power transfer, only $E_q = 0$, so (4.41) will be modified as (4.42).

$$P_{ac} = \frac{3}{2} E_d I_d \tag{4.42}$$

From (4.39) and (4.42),

$$I_{dc} = \frac{3E_d}{2V_{dc}} I_d = \frac{3}{2} K I_d \tag{4.43}$$

Applying the Laplace transform on (4.40) will result in the plant transfer function of the voltage control as (4.44).

$$sCV_{dc}(s) = 1.5KI_d(s)$$

$$V_{dc}(s) = \frac{K}{sT} I_d(s) \tag{4.44}$$

Here, $T = 2C/3$. The block diagram representation of the outer voltage control loop can be shown in Fig. 4.18. The control loop consists of a PI controller, a current loop, and the plant transfer function of the voltage control.

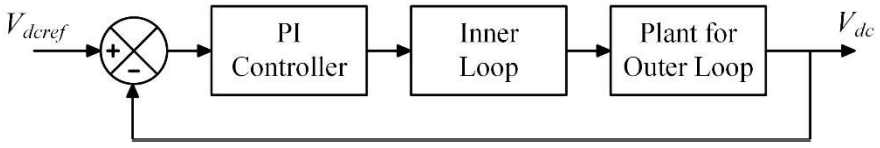


Fig. 4.18 General block diagram representation of the outer voltage control loop.

4.5.1 Plant Transfer Function for the Voltage Control

From (4.44), the plant transfer function for the voltage control can be given in Fig. 4.19. The bode plot for the plant is shown in Fig. 4.20. The plant has a phase margin of 90° at a gain cross-over frequency of 5.171 kHz, and the gain margin is infinity.

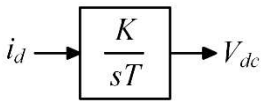


Fig. 4.19 The block diagram representation of the voltage control plant.

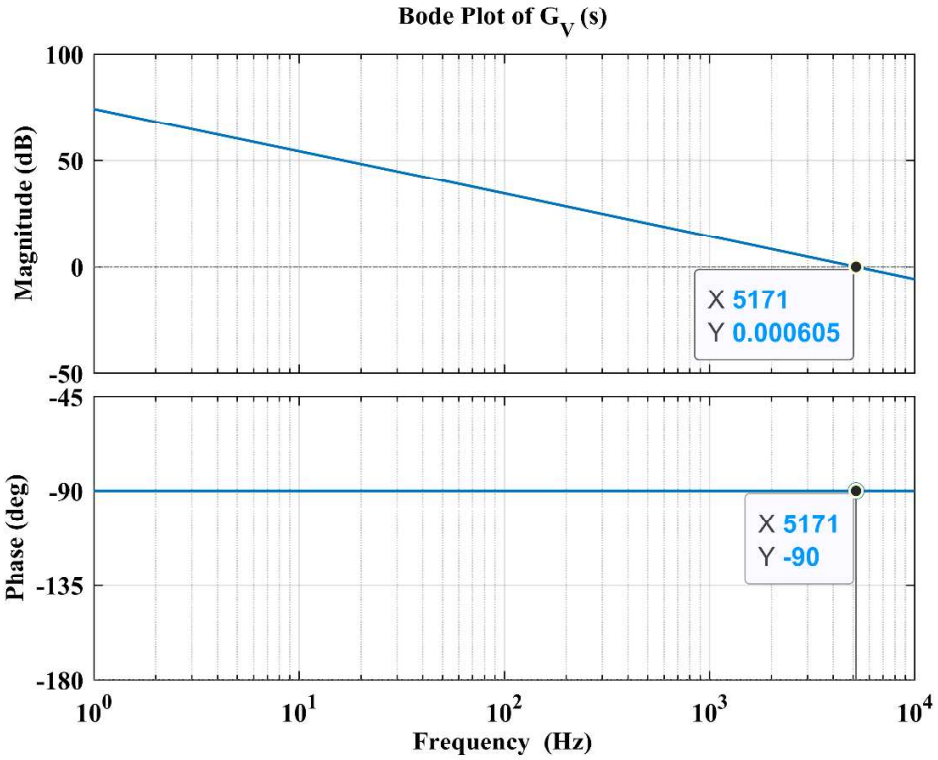


Fig. 4.20 The bode plot of the plant transfer function of the voltage control.

4.5.2 PI Controller for Voltage Control

In the s-domain, the transfer function for the PI controller can be given as (4.45)

$$T_o(s) = K_{po} + \frac{K_{io}}{s} = K_{po}\left(\frac{1+sT_o}{sT_o}\right) \tag{4.45}$$

K_{po}, K_{io}, and T_o denote the proportional gain, integral gain, and integral time constant for the voltage control loop.

4.5.3 Equivalent Inner Current Control Loop

While designing the voltage control loop, the inner current control loop may be considered as constant as it is too fast compared to the voltage control loop. However, if

included within the voltage loop, their closed-loop form must be considered as given in (4.37). Including the current controller within the voltage loop will increase the transfer function's order. To reduce the order of the system caused by the inner loop, a first-order equivalent transfer function of the current control loop is utilized instead of the second-order closed-loop transfer function. A second-order transfer function can be written as first-order only if the steady-state error caused by both is similar. Let the equivalent first-order transfer function be given as (4.46).

$$G_{CLIe}(s) = \frac{1}{1+sT_e} \tag{4.46}$$

The steady-state error caused by (4.46) and (4.37) for the step input can be calculated as (4.47). In (4.47), R(s) and C(s) denote the input and output transfer function with step input.

$$e_{SS}(s) = \lim_{s\to 0}\left(R(s) - C(s)\right) \tag{4.47}$$

Equating the error caused by the two-transfer function-

$$e_{SS}(s) \Rightarrow \lim_{s\to 0}\left(\frac{1}{s} - \frac{1}{s}\frac{1}{1+sT_e}\right) = \lim_{s\to 0}\left(\frac{1}{s} - \frac{1}{s}\frac{1}{2T_w^2 s^2 + 2T_w s + 1}\right)$$

$$\Rightarrow \lim_{s\to 0}\left(\frac{T_e}{1+sT_e}\right) = \lim_{s\to 0}\left(\frac{2T_w^2 s + 2T_w}{2T_w^2 s^2 + 2T_w s + 1}\right)$$

$$\Rightarrow T_e = 2T_w \tag{4.48}$$

So, the current control loop can be presented as an equivalent first-order transfer function with a constraint (4.48). Since the voltage loop is required to be at least 10 times slower than the current loop, the sample delay with the current loop is also added to the equivalent time constant. So,

$$T_e = 2T_w + 10T_{sample} \tag{4.49}$$

4.5.4 Revised Open Loop Transfer function

The complete open loop transfer function-based block diagram representation of the voltage control loop can be given in Fig. 4.21. The outer voltage control loop is designed to have lower bandwidth than the inner loop. The inner loop handles fast dynamics, and the outer loop is responsible for achieving accurate tracking. For the proposed system, the bandwidth of

the outer loop is limited to 1/50 to 1/10 of the inner loop's bandwidth. With this much bandwidth, the inner loop seldom affects the outer loop.

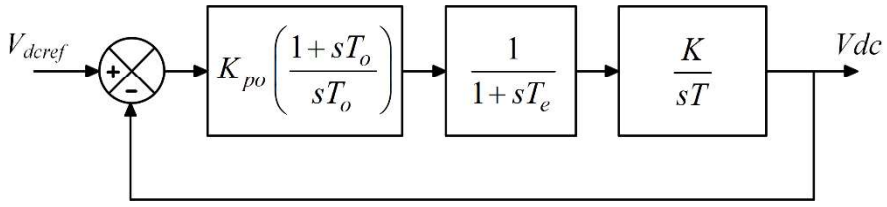


Fig. 4.21 Block diagram presentation of the outer voltage control loop.

4.5.5 Symmetrical Optimum Tuning Criterion (SOTC)

From Fig. 4.21, it can be observed that the outer loop has two poles at the origin, so the MOTC can't be applied here. So, a symmetrical optimum tuning criterion (SOTC) is used that forces the controller's frequency response towards the lower frequencies. The criterion also maximizes the system's bandwidth so that delays associated with the control loop can be avoided. From Fig. 4.21, the complete open loop transfer function of the voltage control loop can be given as

$$G_{V1}(s) = K_{po}\left(\frac{1+sT_o}{sT_o}\right)\frac{1}{1+sT_e}\frac{K}{sT} \tag{4.50}$$

The Nyquist criteria for the stability can be given as follows:

$$G_{V1}(j\omega)|=1 \tag{4.51}$$

$$\angle G_{V1}(j\omega) = -180^o + \phi_{PM}$$

From (4.50), the maximum phase margin can be achieved when

$$\omega_{gc} = \frac{1}{\sqrt{T_o T_e}} \tag{4.52}$$

The transfer function will provide a maximum phase margin of ϕ_{PM} at ω_{gc} symmetrically distributed between $1/T_o$ and $1/T_e$, which can be given as

$$T_o = a^2 T_e \tag{4.52}$$

Here, 'a' is the symmetricity coefficient for the SOTC. Now, from the unity magnitude condition of the Nyquist criteria at ω_{gc},

$$|G_{V1}(j\omega)| = \frac{K_{po}K}{\omega_{gc}^2 T_o T}\sqrt{\frac{1+\left(\omega_{gc}T_o\right)^2}{1+\left(\omega_{gc}T_e\right)^2}} = 1$$

$$K_{po} = \frac{T}{K\sqrt{T_e T_o}} \tag{4.53}$$

Using (4.52) and (4.53), the open loop transfer function can be modified as (4.54).

$$G_{V1}(s) = \frac{1}{s^2 a^3 T_e^2}\left(\frac{1+sa^2T_e}{1+sT_e}\right) \tag{4.54}$$

The bode plot of the open loop transfer function (OLTF) of the voltage control is shown in Fig. 4.22. With the designed controller based on SOTC, the OLTF achieves a phase margin of 53.13° at a gain cross-over frequency of 81.62 Hz. The gain cross-over frequency of the voltage control loop false within the desired range of the operation for stable control. The gain margin for G_{V1} is infinity.

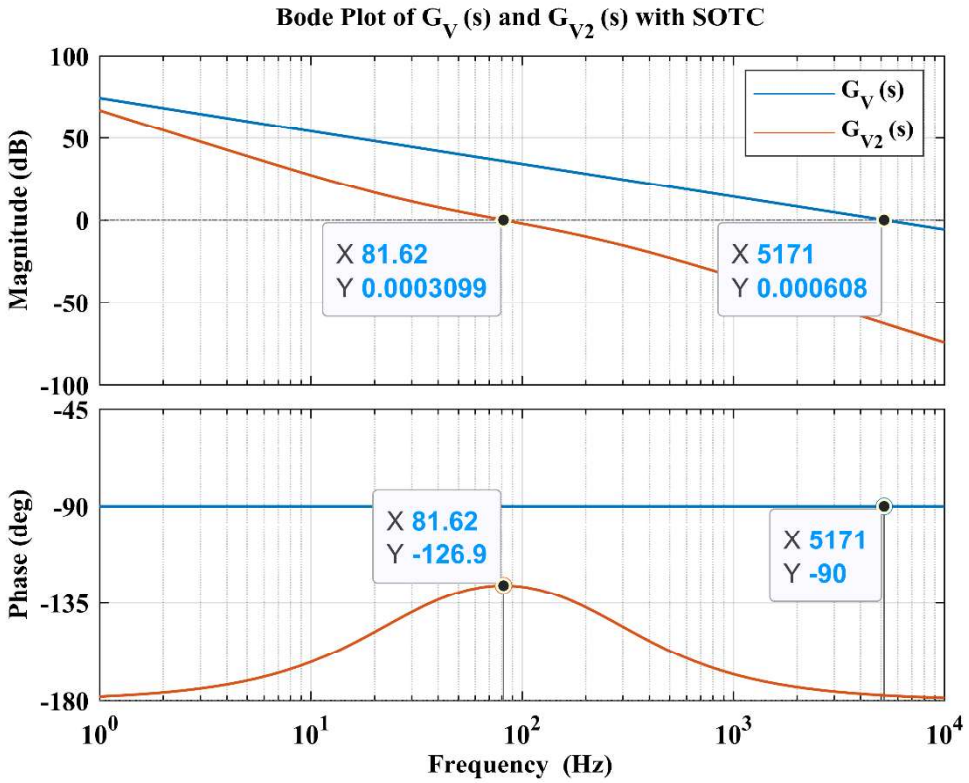


Fig. 4.22 Bode plot of the voltage control loop with SOTC.

For different values of the symmetricity coefficient 'a', the performance of the voltage control is shown in Table 4.2. As the value of the coefficient 'a' increases, the phase margin for the voltage control increases; however, the gain cross-over frequency f_{gc} decreases.

Table 4.2 Effect of the symmetricity coefficient on outer voltage control loop

Coefficient	K_{po}	K_{io}	GM	PM	f_{gc} (Hz)	Stable
a = 2	0.0237	9.1062	- ∞	36.9°	122.42	Yes
a = 3	0.0158	2.6981	- ∞	53.1°	81.61	Yes
a = 4	0.0118	1.1383	- ∞	61.9°	61.21	Yes

4.6 Design of the LC Filter

The sinusoidal pulse width modulation (SPWM) based switching process generates undesirable high-frequency harmonics in the output waveforms. To avoid them, an *LC* filter has been used to attenuate these high-frequency harmonics while allowing the fundamental frequency (f_g = 50 Hz) signals to pass through it. The filtering inductor (L_f) can be calculated assuming the voltage drop of 2% of the grid voltage as (4.55).

$$L_f = \frac{0.02V_g}{2\pi f_g I_o} \tag{4.55}$$

Properly selecting the filtering capacitor C_f is necessary to prevent unwanted resonance from the grid. AC Capacitor (C_f) provides a low impedance path for the high-frequency current, and its value depends upon the cut-off frequency (f_c) of the low-pass filter formed using an LC filter. For a given switching frequency (f_{sw} =10 kHz), the cut-off frequency can be selected using the criterion given as (4.56).

$$10 f_g < f_c < 0.5 f_{sw} \tag{4.56}$$

For a cut-off frequency of 1 kHz, the filtering capacitor can be calculated using (4.57).

$$C_f = \frac{1}{4\pi^2 f_c^2 L_f} \tag{4.57}$$

The value of the filtering passive components is designed using the (4.55) and (4.57).

4.7 Pseudo DC Link Capacitor Required

The film capacitors are known to carry higher rms current than the electrolytic capacitor. The ripple current required to be carried by a DC link capacitor for SPWM switching can be given as follows.

$$I_{DC} = I_{pk}\sqrt{\left[m\left\{\frac{\sqrt{3}}{4\pi}+\cos^2\delta\left(\frac{\sqrt{3}}{\pi}-\frac{9}{16}m\right)\right\}\right]} \tag{4.58}$$

$$C_{DC,\min} = \frac{I_{DC}}{2\pi f_s V_{ripple}} \tag{4.59}$$

Here, m denotes the modulation index, cos ϕ is the load power factor, and I_{pk} is the peak value of AC current. For the given value of the ripple current, the minimum value of the film capacitance required can be calculated using (4.59). Based on the power rating of the proposed topology, the suitable value of FCs (C_2 and C_3) is chosen to be 20 μF.

Table 4.3 Used design specifications of the topology

Parameters	Value
Input Voltage (V_{in})	140 V
Output Power (P_o)	500 W
Switching Frequency (F_s)	50 kHz
Resonant Inductor (L_r)	44.6 μH
Parallel Inductor (L_m)	122.6 μH
Resonant Capacitor (C_r)	227.25 nF
Turns Ratio (n_t)	28:25
Film Capacitance (C_1 - C_4)	20 μF
L_f	4 mH
C_f	15 μF

Table 4.4 Parameters of the shading patterns chosen for simulation results

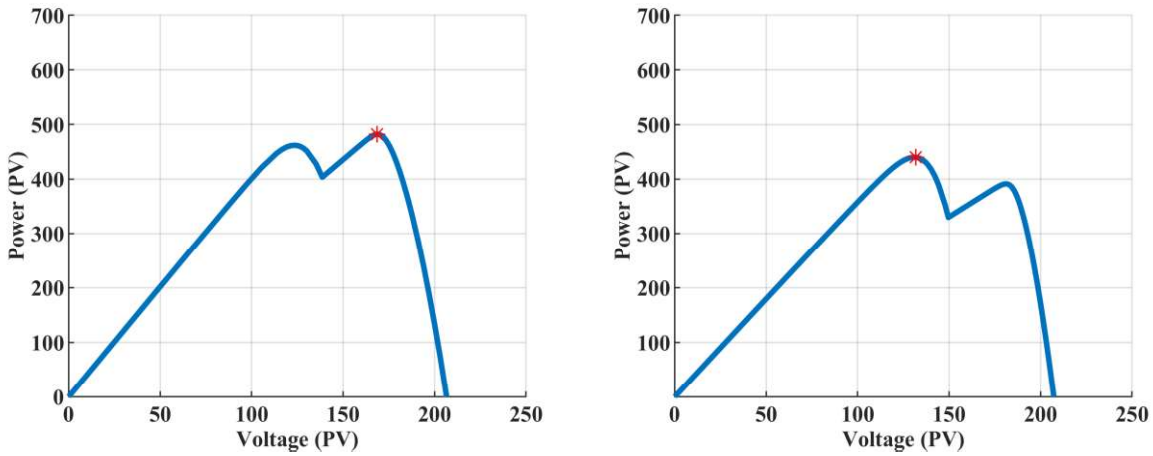
Shading Patterns	Global Peak (GP)		Open Circuit Voltage V_{oc}	Local Peak (LP)		Tracking Time (sec.)	Tracking Efficiency (%)
	Peak Power	Peak Voltage		Power	Voltage		
SP-1	482.5	168.5	206.6	461.9	123.8	0.205	99.12
SP-2	439.9	131.8	207.2	391.1	181.4	0.3	99.28

4.8 Simulation Results Under PSCs With Resistive Load

The parameters topology for testing the resistive load and parameters of the shading pattern are shown in Table 4.3 and Table 4.4. The shading pattern-1 (SP-1) has two peaks with a global peak (GP) power of 482.5 watts at 168.5 volts, as shown in Fig. 4.23 (a). The local peak (LP) can be observed at 461.9 watts at 123.8 volts. SP-2 also has a two-peak PV curve, as shown in Fig. 4.23 (b). The global peak (GP) can be observed at 439.9 watts with a voltage of 131.8. The local peak (LP) can be observed at 391.1 watts with 181.4 volts. Fig. 4.24 (a)-(d) shows the simulation results for the above two shading patterns.

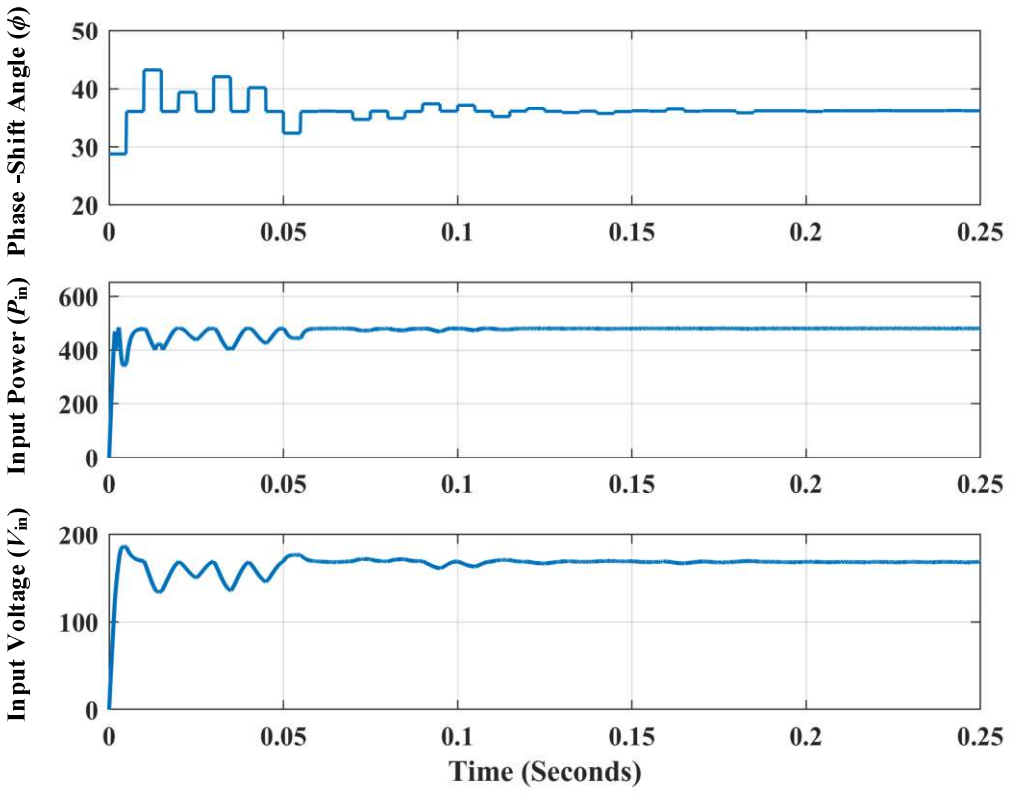
In Fig. 4.24 (a), the simulation shows the variation of phase shift angle (ϕ), input power (P_{PV}), and input voltage V_{in} for SP-1. In Fig. 4.24 (b), the simulation shows the variation of DC link voltage (V_{DC}), phase voltages (V_{an}, V_{bn}, and V_{cn}), and phase currents (I_a, I_b, and I_c) for SP-1. The PSO-based MPPT algorithm takes approximately 0.205 seconds to track the global peak power for SP-1.

In Fig. 4.24 (c), the simulation shows the variation of phase shift angle (ϕ), input power (P_{PV}), and input voltage V_{in} for SP-2. In Fig. 4.24 (b), the simulation shows the variation of DC link voltage (V_{DC}), phase voltages (V_{an}, V_{bn}, and V_{cn}), and phase currents (I_a, I_b, and I_c) for SP-2. The PSO-based MPPT algorithm takes approximately 0.3 seconds to track the global peak power for SP-2. From Fig. 4.24 (a) - (d), it can be seen that the PSO-based MPPT algorithm works satisfactorily for the given input voltage range, and the steady-state voltages are oscillation-free.

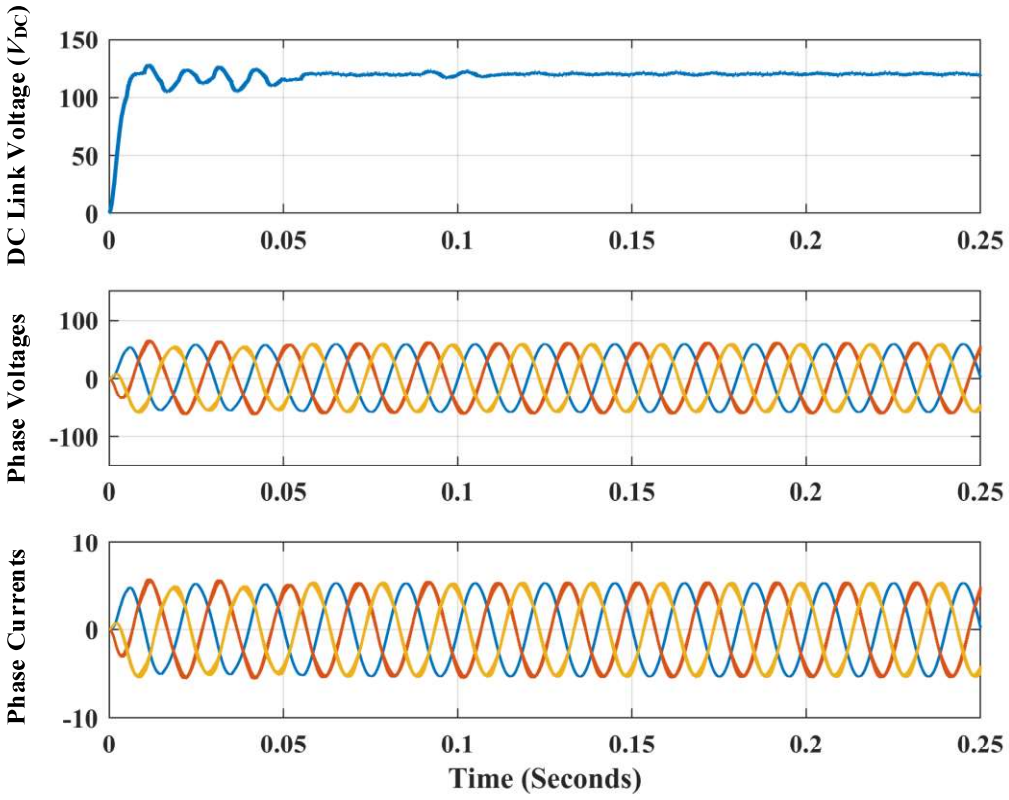


(a) (b)

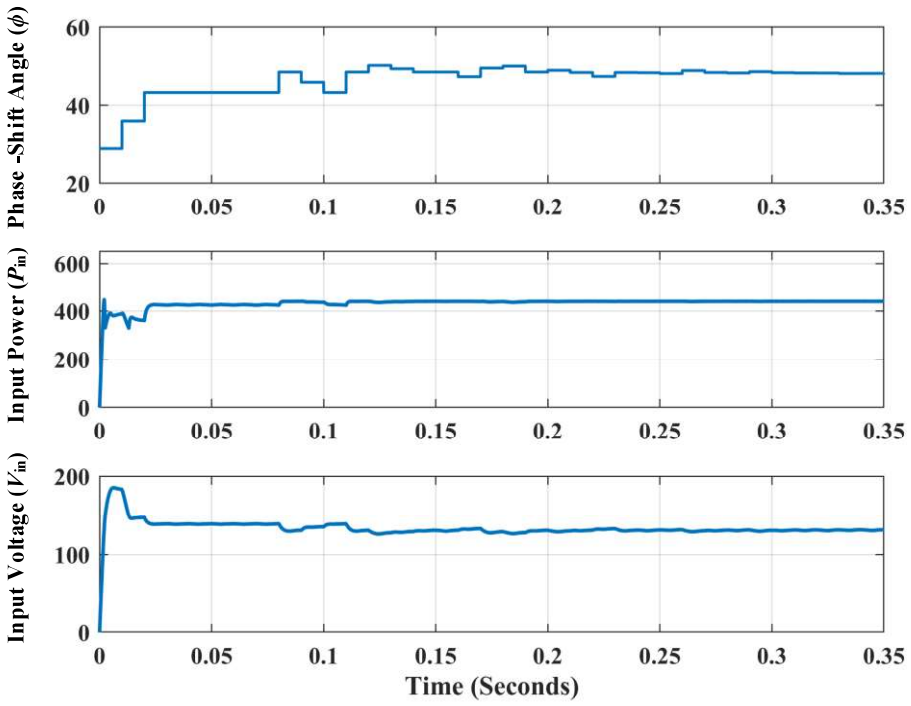
Fig. 4.23 Shading Patterns chosen for simulation results (a) SP-1 and SP-2.


Phase -Shift Angle (ϕ)
50
40
30
20
0
0.05
0.1
0.15
0.2
0.25
Input Power (P_{in})
600
400
200
0
Input Voltage (V_{in})
200
100
0
Time (Seconds)

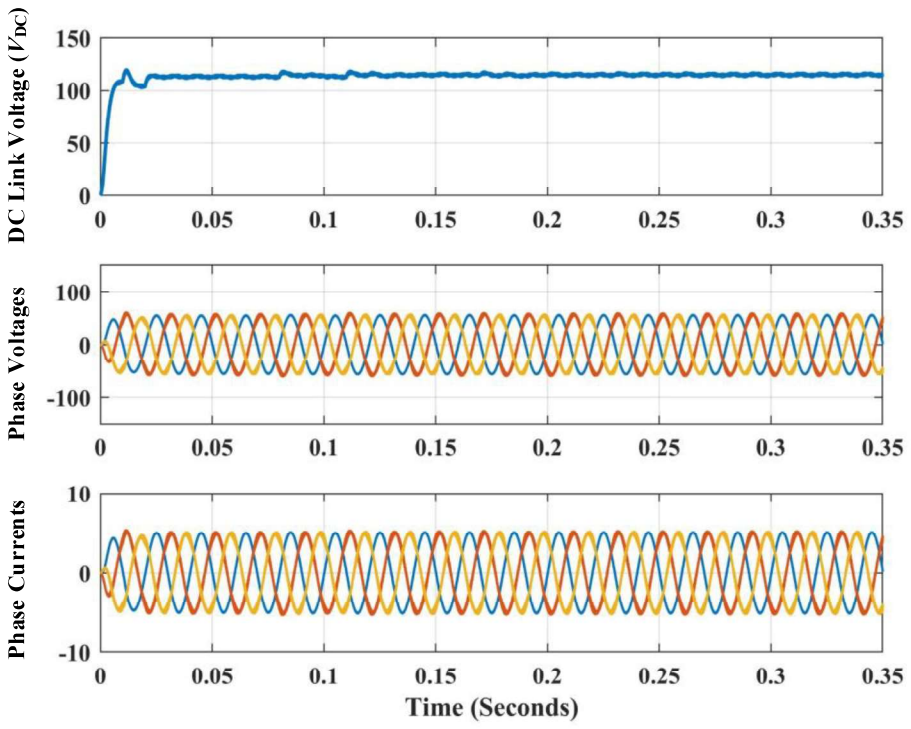
(a)


DC Link Voltage (V_{DC})
150
100
50
0
Phase Voltages
100
0
-100
Phase Currents
10
0
-10
0
0.05
0.1
0.15
0.2
0.25
Time (Seconds)

(b)



(c)



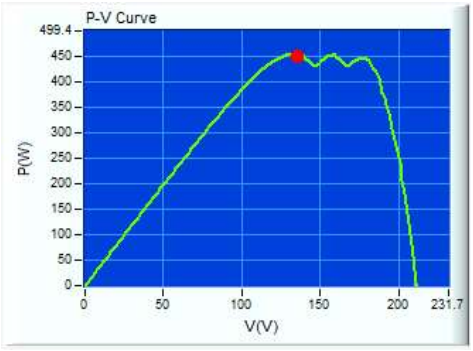
(d)

Fig. 4.24 Simulation results showing phase shift angle (ϕ), input power (P_{PV}), input voltage V_{in}, DC link voltage (V_{DC}), phase voltages (V_{an}, V_{bn}, and V_{cn}) phase currents (I_a, I_b, and I_c) for (a)-(b) SP-1. (c)-(d) SP-2.

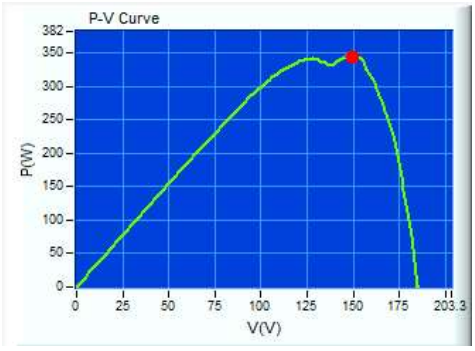
Fig. 4.25 Photograph of the experimental setup

4.9 Experimental Results Under PSCs with Resistive Load

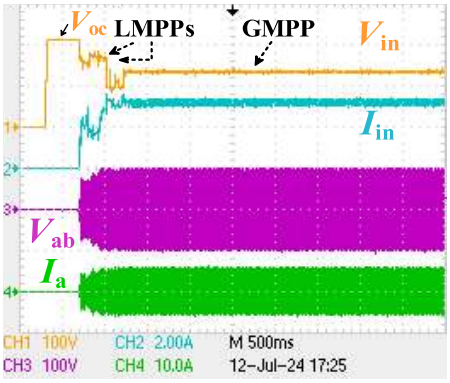
The photograph of the experimental setup is shown in Fig. 4.25. Two multi-peak PV curves representing shading patterns (PVC-1 to PVC-2) are formed to test PSCs. The parameters of the PV curves, tracking time, and tracking efficiency observed from hardware testing are given in Table 4.5. To ensure noise-less sensing for the input PV voltage and current, the MPPT sampling time interval is set to 20 ms. Fig. 4.26 (a) depicts PVC-1 with a global maxima power point (GMPP) of 454 W at 134.4 V and two local minima power points (LMPPs) of 442.9 W at 175 V and 449.4 W at 158.5 V. The algorithm locates the GMPP in 0.54 s with a tracking efficiency of 99.72 % as shown in Fig. 4.26 (b). The inverter line-to-line voltages (V_{ab}, V_{bc}, and V_{ca}) are 69.1 V, and the current (I_a) is 3.61 A, as shown in Fig. 4.26 (c). Fig. 4.26 (d) depicts PVC-2 with a GMPP of 347.2 W at 148.4 V and an LMPP of 339.1 W at 128.9 V.



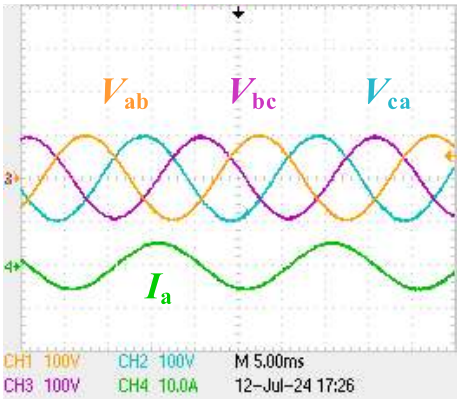
(a)



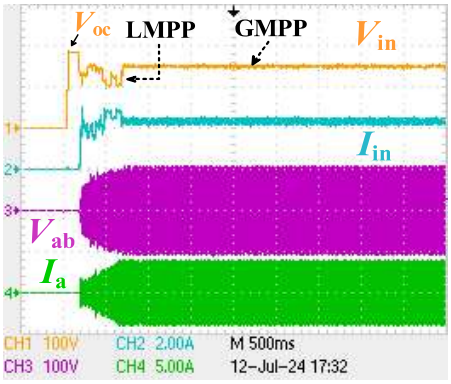
(b)



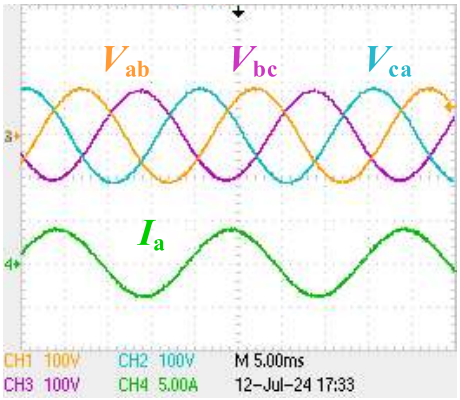
(c)



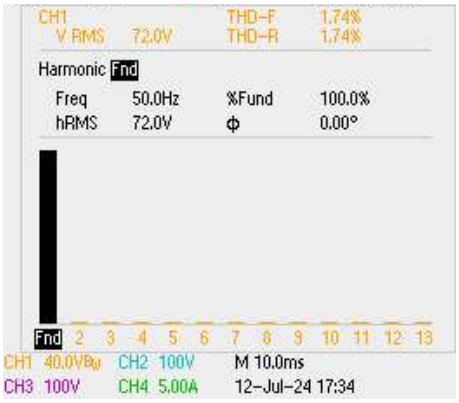
(d)



(e)



(f)



(g)

Fig. 4.26 Experiment results for shaded conditions with resistive load showing PV curves with input voltage V_{PV} and current I_{PV}, inverter voltages (V_{ab}, V_{bc}, and V_{ca}) and current (I_a) with zoomed view for (a)-(c) PVC-1. (d)-(f) PVC-2 (g) THD in line voltage Vab of PVC -2.

Table 4.5 Parameters of the PV-curves for experimental results

Shading Patterns	Global Peak (GP)		Local Peak (LP)		Tracking Time	Tracking Efficiency
	Peak Power	Peak Voltage	Power	Voltage		
PVC-1	454	134.4	442.9 449.4	175 158.5	0.54 s	99.72 %
PVC-2	347.2	148.4	339.1	128.9	0.52 s	99.76 %

Fig. 4.26 (e) shows that the algorithm locates the GMPP in 0.52 s with a tracking efficiency of 99.76 %. The inverter line-to-line voltages (V_{ab}, V_{bc}, and V_{ca}) are 71.9 V and the current (I_a) is 2.65 A as shown in Fig. 4.26 (f). The THD of line-to-line inverter voltage (V_{ab}) for PVC-2 is shown in Fig. 4.26 (g), which is observed to be 1.74%. The experimental results depict fast GMP tracking with negligible steady-state oscillations in the voltage and current waveforms.

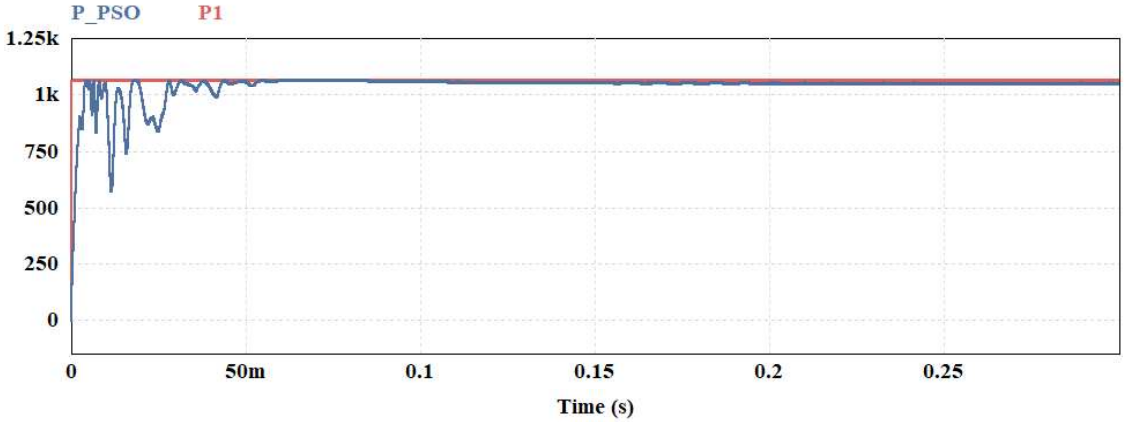
Table 4.6 Used design specifications of the ADABRC based two-stage topology

Parameters	Value
Input Voltage (V_{in})	120 V
Output Power (P_o)	1000 W
Grid Line Voltage (V_g)	110 V
Switching Frequency (F_s)	50 kHz
Resonant Inductor (L_r)	89.16 μH
Parallel Inductor (L_m)	163.26 μH
Resonant Capacitor (C_r)	517.68 nF
Turns Ratio (n_t)	240:264
Film Capacitance (C_1 - C_3)	47 μF
L_f and C_f	2.3 mH and 10 μF

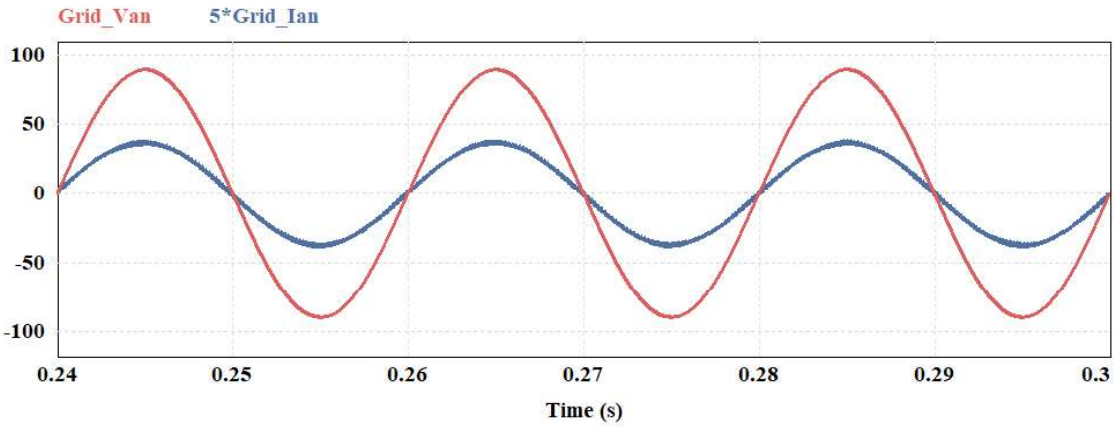
4.10 Simulation Results for Solar PV to Grid-Tied Condition

The design specification of the ADABRC-based pseudo DC-link two-stage topology is shown in Table 4.6. The grid line voltage is 110 V (rms). The PV curve used to feed the power to the grid-tied condition has a peak power of 1067 W at 125.6 V. To ensure noise-less sensing for the input PV voltage and current, the MPPT sampling time interval is set to 5 ms. The DC link voltage is set to be 240 V. The simulation results for the same is shown in Fig. 4.27.

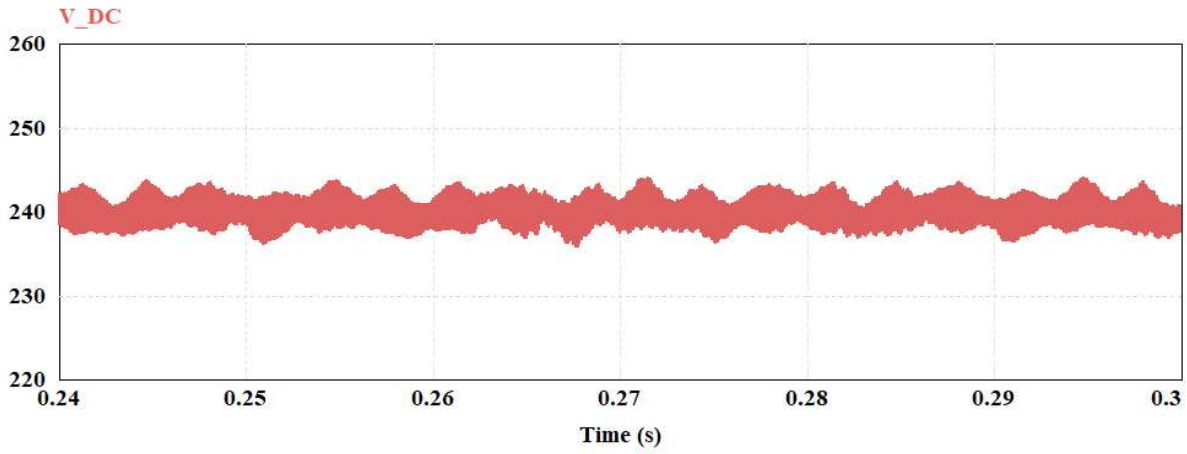
Fig. 4.27 (a) depicts the actual PV power and PV power tracked due to the PSO-based MPPT algorithm. Fig. 4.27 (b) depicts grid phase voltage (V_{an}) of 63.5 V and phase current (I_{an}) of 5.31 Amps. The DC link voltage (V_{DC}) of 240 V is shown in Fig. 4.27 (c), and it has a ripple of 6 V. The primary bridge and corresponding bridge current are shown in Fig. 4.27 (d). Fig. 4.27 (e) shows the secondary bridge and corresponding bridge current. From the simulation results, it can be seen that the DC link voltage is fixed at 240 V. The THD in the grid current is 2.18 %. All the active switches are operating with zero voltage switching.



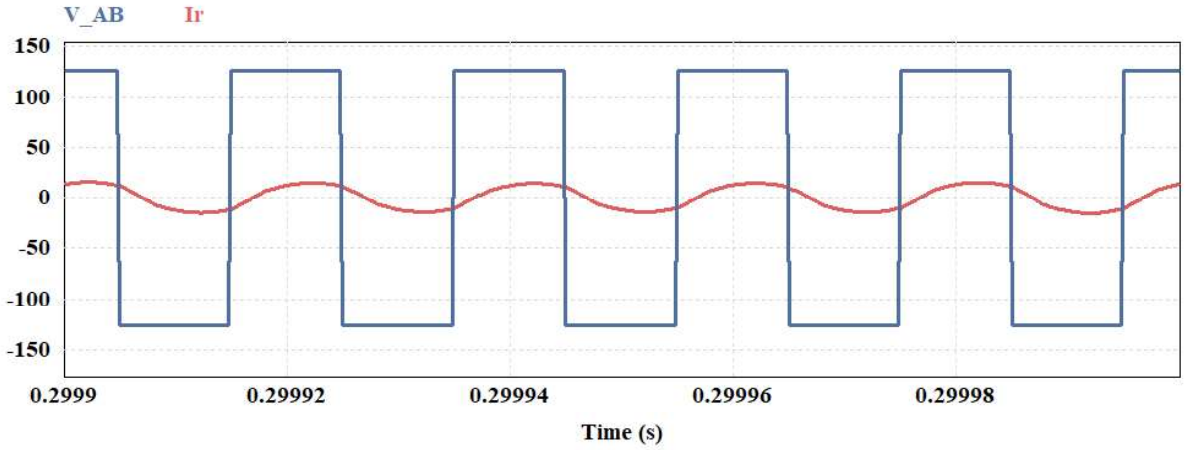
(a)



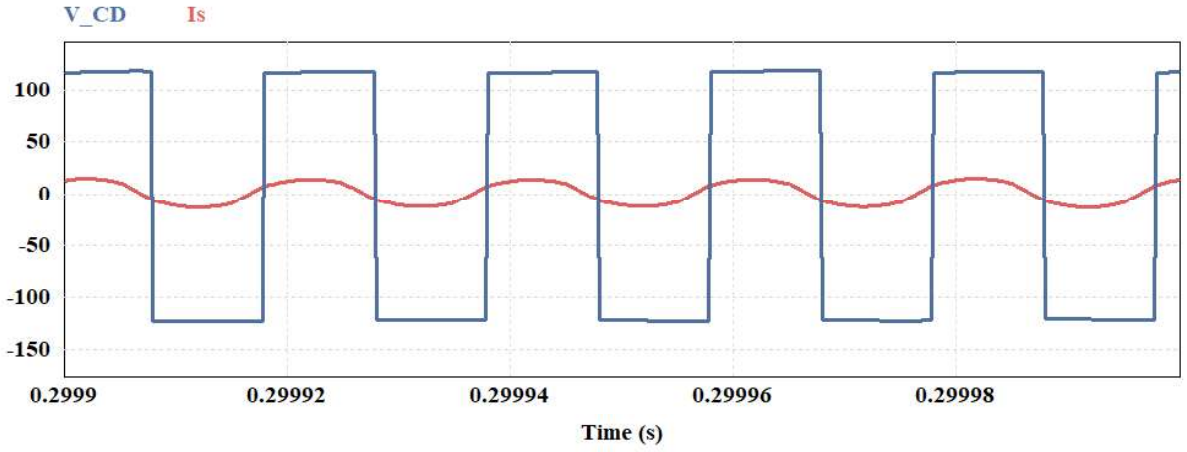
(b)



(c)



(d)



(e)

Fig. 4.27 The simulation results for grid-tied conditions showing (a) Actual power and PV power tracked, (b) Grid phase voltage and current for phase A, (c) DC link voltage, (d) Primary bridge voltage and current, and (e) Secondary bridge voltage and current.

4.11 Conclusion

The electrolytic capacitor-less converter proposed in Chapter 2 forms a pseudo-DC link-based two-stage topology. The topology utilizes its outer film capacitor leg to act like a DC link capacitor for the topology. The cascaded control loop for the two-stage topology is designed and tuned using the modulus optimum tuning criterion and the symmetrical optimum tuning criterion. The topology feeds the solar power to the AC grid with THD in grid current within the IEEE-519 standards. The topology is first tested for resistive load using simulation and hardware setup. The topology is then tested on a simulation platform for 1 kW to feed the solar PV power to a three-phase AC grid.

Now, since the dual half-active bridge resonant converter operates with soft-switching near unity voltage gain, a high voltage gain network may utilized at the input side to increase its gain further. In the next chapter, an expandable impedance source network is connected at the front end of the electrolytic capacitor-less dual half active bridge resonant converter to boost the voltage gain further. The proposed converter is then integrated with solar PV using particle swarm optimization based MPPT algorithm.