Performance Investigation of Back Gated SiO_2/Ferroelectric Stacked Gate Oxide Ge/Si Heterojunction STFET

5.1 Introduction

As we have discussed in the review section of chapter 1, ferroelectric oxides-based TFETs are another class of devices in which ferromagnetic material is used as the gate dielectric in the conventional tunnel field-effect transistor, which helps to reduce the subthreshold swing (SS) and improve the conduction current [67]-[71], [199]. When ferroelectric oxides are connected in series with conventional oxides, internal voltage amplification proportionate to the charge in the ferroelectric oxide occurs, resulting in an increase in drain current and a reduction in *SS* [199]–[205]. Therefore, if we combine the effect of both BTBT and ferroelectric oxide, we can get remarkable results for the lowering of *SS*. Lattanzio *et al.* [201] first proposed the ferroelectric gate oxide tunnel field-effect transistor (Ferro-TFET), observed *SS* of about 880 mV/dec using the principles of P(VDE-TrFE), and thus widely investigated over the years [206]–[208]. Jain and Alam [209] have reported that the minimum SS limit depends on various stability constraints of ferroelectric FETs (Fe-FETs).

In chapter-4 we observed that adding back gate to VSG-HJ-STFET increases the device drive current. Therefore in this chapter on the basis of the above discussion we have inserted ferroelectric oxide in place of HfO_2 in BG-HJ-STFET to enhance its performance. Present chapter analyses the device-level performance of a back gated ferroelectric gate dielectric engineered heterojunction TFET on SELBOX (BG-Fe-HJ-STFET) and performance metrics are compared with (BG-HJ-STFET) of chapter-4.

5.2 Device Under Study

5.2.1 Schematic Structure of the Device

The 2D-cross-sectional view of the proposed back gated ferroelectric gate dielectric engineered heterojunction TFET on SELBOX (BG-Fe-HJ-STFET) and back gated heterojunction TFET on SELBOX without any ferroelectric gate dielectric structure (BG-HJ-STFET) is shown in Figure 5.1. There are two gate terminals in the proposed structure which can be named as front gate and back gate. Device dimensions are shown in the same figure along with the symbols and some other device dimensions and doping concentration values are listed in table 5.1. The gap in the SELBOX structure increases the availability of density of state (DOS) of the carriers (electrons) so that some carriers can be trapped by the gap of the SELBOX structure, which decreases the availability of carriers in the OFF-state and it is responsible to reduce the ambipolarity current in the device [46], [74].

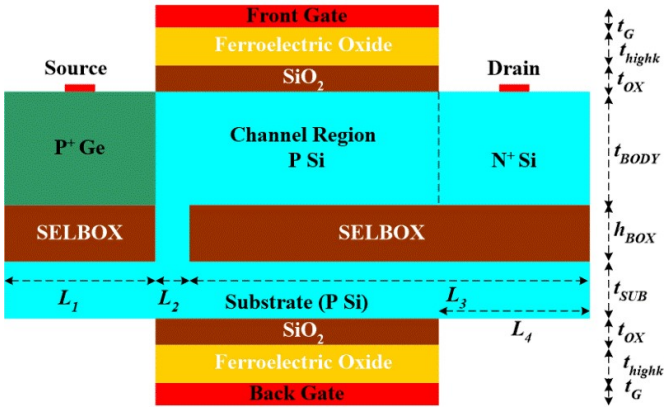

Figure 5.1 2D Schematic structure of BG-Fe-HJ-STFET.

5.2.2 Fabrication Process Flows

The fabrication feasibility of BG-Fe-HJ-STFET is given below. Thus, the BG-Fe-HJ-STFET can be fabricated by using below process flows [109], [189]. SILVACO ATLAS™ TCAD tool has been used for the simulation of all the aforementioned

structures [157]. The models which are included in this simulation are already discussed in the chapter-1.

Table 5.1: List of device dimensions and structural parameters.

Parameters	**BG-Fe-HJ-STFET**	**BG-HJ-STFET**
Source doping concentration (N_S)	1×10^{19} cm^{-3}	$1\times10^{19}$$cm^{-3}$
Channel doping concentration (N_{ch})	1×10^{16} cm^{-3}	1×10^{16} cm^{-3}
Drain doping concentration (N_D)	5×10^{18} cm^{-3}	5×10^{18} cm^{-3}
The thickness of the channel (t_{Si})	15 nm	15 nm
The thickness of SiO_2 gate oxide (t_{ox})	1 nm	1 nm
The thickness of High-k gate oxide (t_{ox})	2 nm	2 nm
Effective Oxide Thickness (EOT)	1.312 nm	1.312 nm
Gate length (L_G)	40 nm	40 nm
Source length (L_S)	30 nm	30 nm
Drain length (L_4)	30 nm	30 nm
Thickness of buried oxide (BOX) (t_{BOX})	10 nm	10 nm
Length of SELBOX gap (L_2)	2 nm	2 nm
Hole tunnel mass in silicon (m_{htSi})	0.24mo	0.24mo
Hole tunnel mass in germanium (m_{htGe})	0.044mo	0.044mo
Electron tunnel mass in silicon (m_{etSi})	0.20mo	0.20mo
Electron tunnel mass in germanium (m_{etGe})	0.082mo	0.044mo
Lattice constant of Ge	5.656 ^{0}A	5.656 ^{0}A
Lattice constant of Si	5.429 ^{0}A	5.429 ^{0}A
Bandgap energy Ge	0.70 eV	0.70 eV
Bandgap energy Si	1.12 eV	1.12 eV
Electron affinity Ge	4.01 eV	4.01 eV
Electron affinity Si	4.05 eV	4.05 eV
Dielectric Constant of ferroelectric material	1495	------
Front Gate Metal Work Function (eV), ψ_{sf}	4.1 eV	4.1 eV
Back Gate Work Function (eV), ψ_{sb}	4.1 eV	4.1 eV

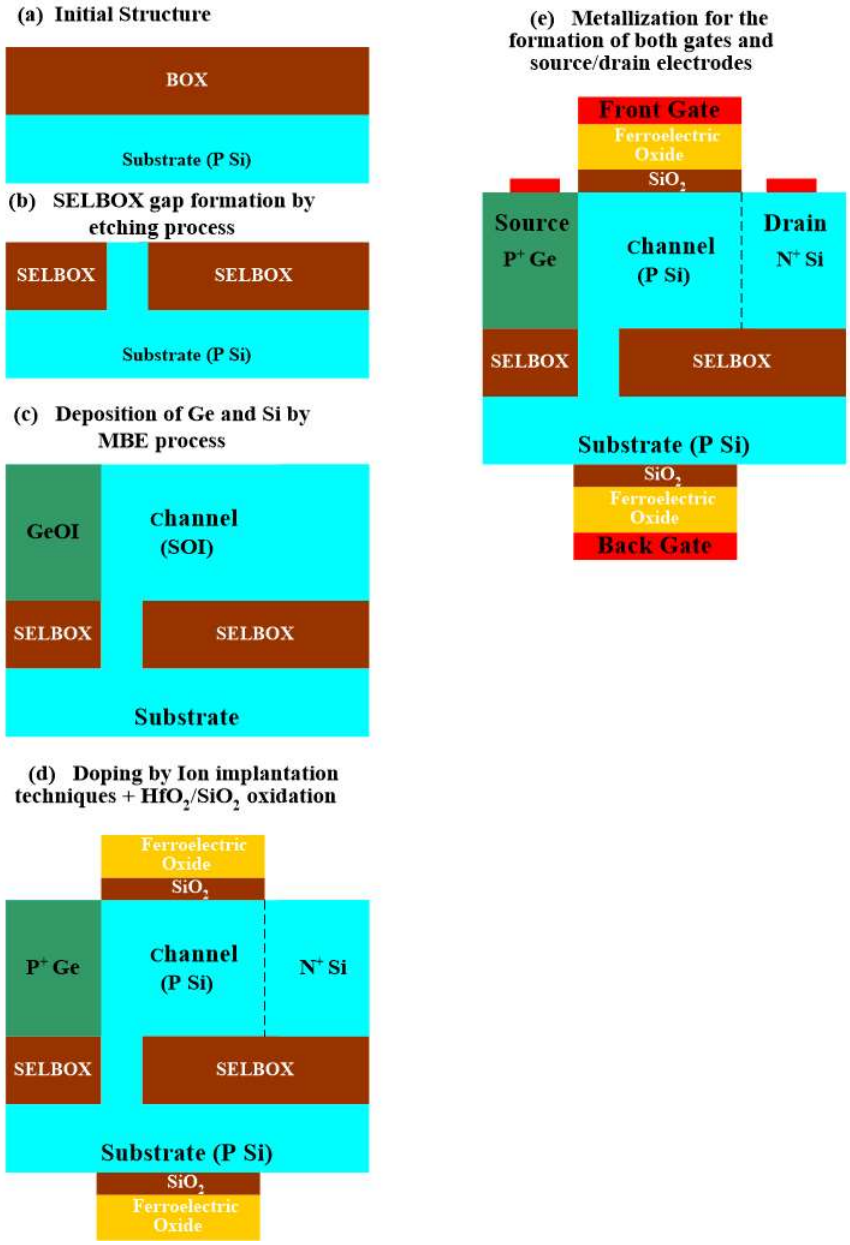

Figure 5.2 Fabrication Steps of BG-Fe-HJ-STFET.

Figure 5.2 shows the fabrication processes steps includes (a) choosing a clean silicon substrate and formation of a structure with SOI region on silicon substrate using oxidation method, (b) etching of required region to form a SELBOX structure in the SOI structure, (c) epitaxial growth of silicon on SELBOX structure to form drain and channel region of the TFET, (e) epitaxial growth of Ge as a source to form heterojunction at

source-channel junction, (d) N^+ drain region and P^+ source region (Ge) formation using ion implantation and heterogeneous gate dielectric formation using SiO_2 and ferroelectric oxide in a lateral stacked manner using atomic layer deposition (ALD) method, and finally (e) metallization is done to form a dual material gate, source and drain electrode terminals.

5.2.3 Models Validation

All the models are calibrated with a reported paper [158] where model validation is done considering the BG-Fe-HJ-STFET device which has been simulated with the same measurements and device parameters as appeared in Figure 5.3. Figure 5.3 demonstrates the transfer characteristics plots for different drain voltages obtained from the simulation. The outcome acquired is closeness with prior announced work [158] which confirms the validity of the selected models for simulations.

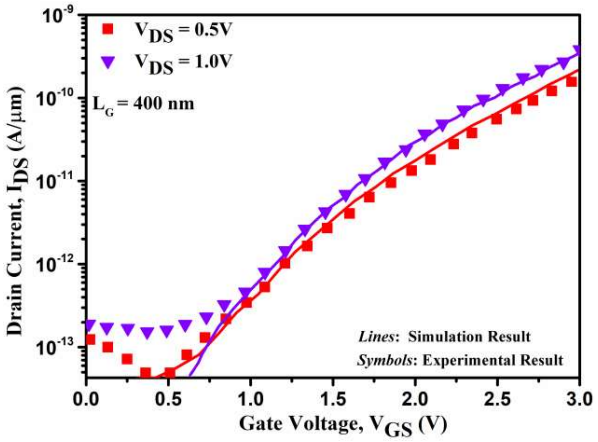

Figure 5.3 Calibrated transfer characteristics of the BG-Fe-HJ-STFET with the experimental data [158].

5.3 Results and Discussion

5.3.1 DC Analysis

Figure 5.4 (a) and Figure 5.4 (b) show the energy band diagrams of BG-Fe-HJ-STFET and BG-HJ-STFET vs. device length where both ON, as well as OFF-state of energy band diagrams along with the Quasi-Fermi-Level (QFL) of electrons and holes, are plotted.

The tunnel distance [D_{Tun}] is also included in the same figure, which is the minimum distance between the valence band to the conduction band. Tunnel distance decreases with an increase in the gate bias voltage [44]. Figure 5.4 (c) shows the equivalent circuit diagram of a Ferroelectric oxide Fe-TFET including the C_{FE}, C_{SiO2}, and C_s for the TFET where m and n can be found using Eqn: 5.1. Figure 5.5 (a) shows the logarithmic drain current plots of both BG-Fe-HJ-STFET and BG-HJ-STFET, here we can see that our proposed structure is showing higher I_{ON} current ($1.12\text{x}10^{-5}$ A/μm) as compared to without ferroelectric gate oxide TFET ($7.74\text{x}10^{-6}$ A/μm) at V_{DS} = 0.5 V. The I_{ON}/I_{OFF} ratio obtained by BG-Fe-HJ-STFET ($5.81\text{x}10^{10}$) is higher than that of BG-HJ-STFET ($3.86\text{x}10^{10}$) as shown in Figure 5.5 (a). Subthreshold swing (SS) plays an important role for low power applications of CMOS devices [207]. The SS of ferroelectric related MOS devices is expressed by Eqn: 5.1:

$$SS \approx \frac{\partial V_{GS}}{\partial\left(\log I_{DS}\right)} = \frac{\partial V_{GS}}{\partial \psi_s}\frac{\partial \psi_s}{\partial\left(\log I_{DS}\right)} = \underbrace{\left(1+\frac{C_s}{C_{ox}}\right)}_{m}\underbrace{\frac{\partial \psi_s}{d\left(\log_{10} I_d\right)}}_{n} \tag{5.1}$$

where C_{ox}, C_s, ψ_s and I_d are the gate oxide capacitance, channel-depletion capacitance, surface potential and drain current respectively. Factor m is known as transistor body's factor which depends on silicon body and gate oxide capacitance. For conventional oxide (i.e., SiO_2 and HfO_2), $m > 1$ whereas it can be reduced ($m < 1$) by using negative gate capacitance oxide at the place of conventional oxide. Charge transport mechanism of MOSFETs totally depends upon factor n which can be minimized by using TFET, because in TFET carriers transport is through band-to-band tunneling rather than thermally excitation of charge transport [44]. *SS* value obtained by the proposed device is very low (38.6 mV/dec) as compared to the Boltzmann limit (60 mV/dec) which makes the proposed device more suitable for low power operations [44]. Figure 5.5 (b) shows the plots of I_D-V_D for different gate voltage.

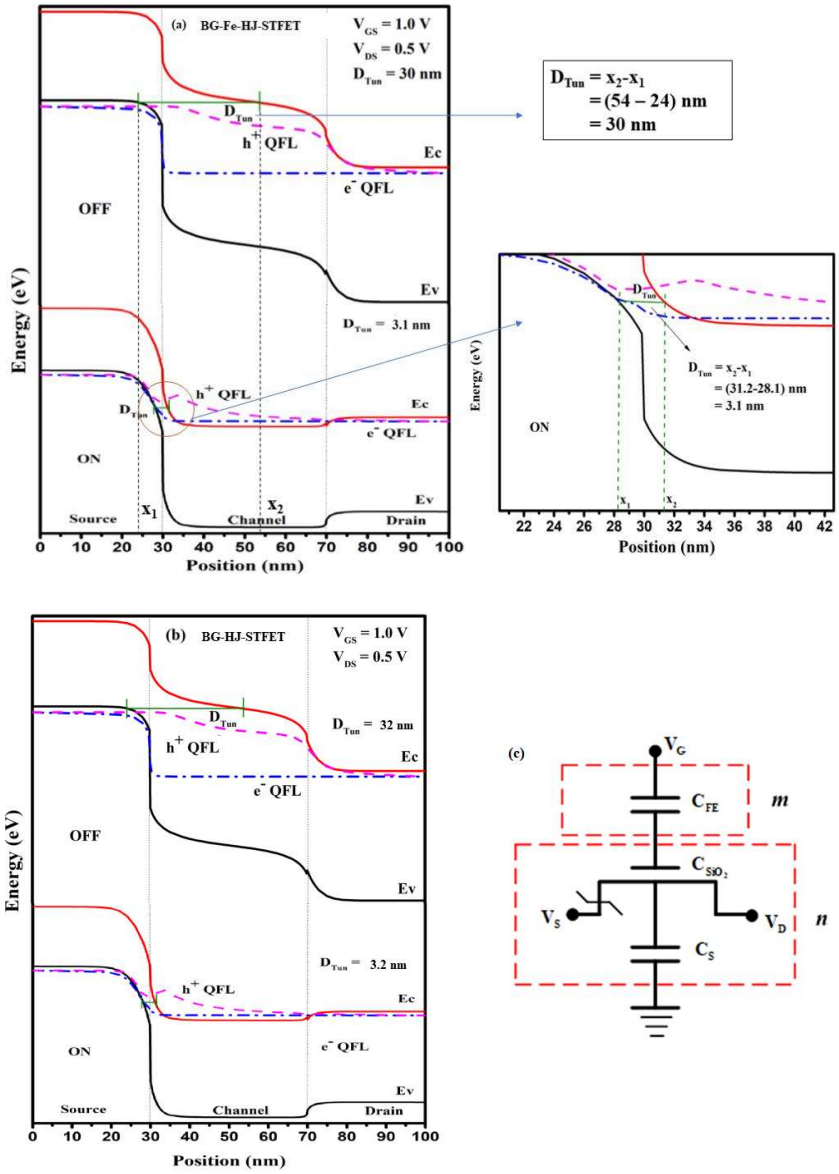

Figure 5.4 Energy band diagrams of (a) BG-Fe-HJ-STFET, (b) BG-HJ-STFET with respect to the device length in on and off-state and (c) The circuit diagram of ferroelectric oxide Fe-TFET including the C_{FE}, C_{SiO2} and C_S for the TFET.

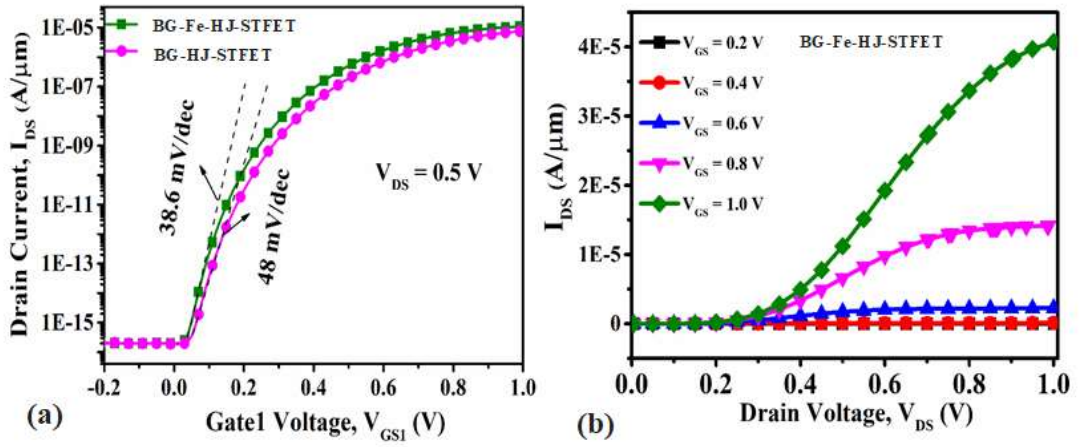

Figure 5.5 Plots of (a) I_{DS}-V_{GS} of BG-Fe-HJ-STFET and BG-HJ-STFET, and (b) I_{DS}-V_{DS} of the proposed TFET.

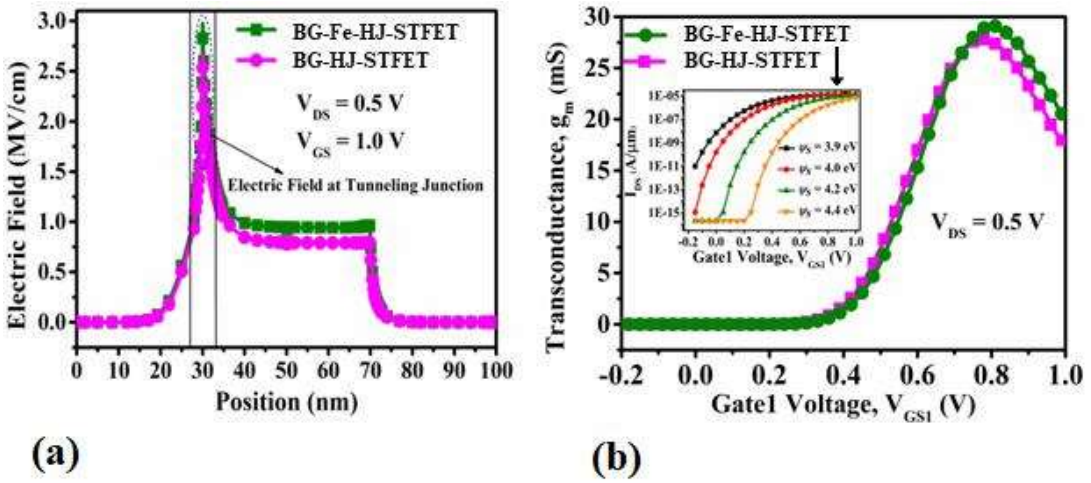

Figure 5.6 Plots of (a) Electric Field and (b) transconductance (inset I_D-V_{GS} graph of the proposed device at different gate material work function values, Ψs) of BG-Fe-HJ-STFET and BG-HJ-STFET w.r.t V_{GS} at V_{DS} =0.5 V.

Figure 5.6 (a) demonstrates the comparative plots of the electric field in the thermal equilibrium condition. The maximum value of the electric field at the junction in the BG-Fe-HJ-STFET structure is 3.013×10^6 V/cm, which is higher than the BG-HJ-STFET structure. Therefore, ferroelectric oxide as a gate oxide is responsible for increasing the electric field at the junction of source and channel region. A high electric field improves the performance of the device such as it increases the tunneling probability of the carriers from source to channel region [44]. Figure 5.6 (b) depicts the plots of the

transconductance of both the BG-Fe-HJ-STFET and the BG-HJ-STFET with respect to V_{GS}, with V_{DS} fixed to 0.5 V. BG-Fe-HJ-STFET is showing the higher value of maximum transconductance than BG-HJ-STFET because of increase in tunneling volume in the channel [44]. The inset image in Figure 5.6 (b) shows the drain current plots at various work functions value of the gate material where at Ψ_S = 4.2 eV better outcome is observed compared to other values of work function.

5.3.2 RF/Analog Analysis

The switching operation of the device can be analyzed by RF analysis which includes some important parameters like parasitic capacitances (C_{gg}, C_{gd}, and C_{gs}) for the prediction of the charge conduction mechanism; cut-off frequency (f_T) to predict the operating frequency of the device [210]. The plots of parasitic capacitances of BG-Fe-HJ-STFET and BG-HJ-STFET are shown in Figure 5.7 (a). Because of the higher dielectric constant value of ferroelectric oxide (k=1495), the proposed structure BG-Fe-HJ-STFET has a higher value of parasitic capacitances. Figure 5.7 (b) depicts the cut-off frequency variations, with the peak value of the proposed device's cut-off frequency (4.2 GHz) being higher than that of the BG-HJ-STFET (3.9 GHz) due to the higher transconductance value [44]. The expression of cut-off frequency is given by Eqn: 5.2:

$$f_T = \frac{g_m}{2\pi C_{gg}} \tag{5.2}$$

where g_m is the transconductance, and C_{gg} is the total gate capacitance.

Transit time (ɛ) is a prominent RF parameter, which is defined as the time for charge carriers to reach from source to drain region shown in Figure 5.7 (c) and this reflects the behavior of device speed of performance. The expression of transit time is expressed by Eqn: 5.3. The proposed device BG-Fe-HJ-STFET has a lower value of transit time over the entire range of V_{GS} compared to BG-HJ-STFET. Figure 5.7 (d) shows the plots of the gain-bandwidth product (GBP) and can be formulated as Eqn: 5.4 [210]. BG-Fe-HJ-

STFET has a higher value of GBP than BG-HJ-STFET.

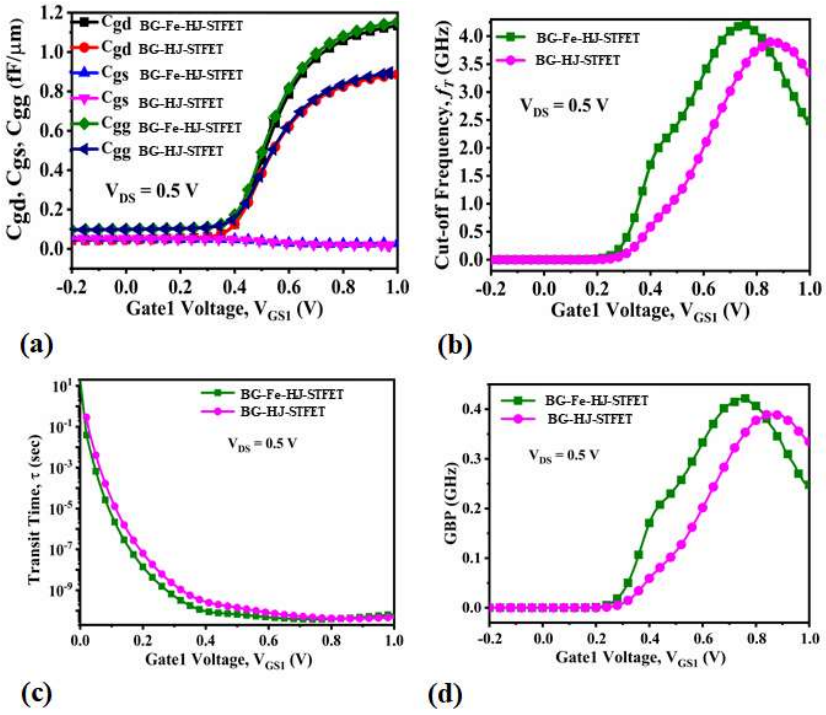

Figure 5.7 Plots of (a) C_{gd}, C_{gs} and C_{gg}, (b) cut-off frequency, f_T, (c) transit time, τ and (d) GBP of BG-Fe-HJ-STFET and BG-HJ-STFET vs. V_{GS} at V_{DS} = 0.5 V.

$$\tau = \frac{1}{2\pi f_T} \tag{5.3}$$

$$GBP = \frac{g_m}{20\pi C_{gd}} \tag{5.4}$$

5.3.3 Nonlinearity Distortion Analysis

Today is the era of digital communication and for the distortionless communication from the transmitter to the receiver, the devices connected to the system should be as linear as possible [211]. The linearity analysis of the TFET can be determined by observing some parameters such as gm3, zero crossover point, VIP2, VIP3, IIP3, IMD3, and 1-dB compression point. g_{m3} is the third order derivative of drain current with respect to V_{GS} as shown in Figure 5.8 (a) and the proposed device is found to be a higher value of g_{m3}. Zero crossover point (ZCP) indicates the best suitability of the biasing voltage, it should be as low as possible. The proposed device exhibits a low value of ZCP as shown in Figure 5.8

(b). The second-order voltage intercept point (VIP2) is the voltage where the first and second harmonics voltages are the same whereas the third-order voltage intercepts point (VIP3) is the voltage where the first and third harmonics voltages are the same. The peak value of VIP2 and VIP3 determine the linearity behavior of the device and it should be as high as possible. IMD3 defines the first and third, inters modulation harmonic power to be equal and IMD3 should be as low as possible because it refers to degeneracy in the wireless communication system [211]. There is another linearity FOM is IIP3. The overshoot of IIP3 is presenting the suitability of the device for distortion less applications [211]. The mathematical expressions of all the linearity parameters are given by equation (5.5 to 5.8) [211].

$$VIP2 = 4X\left(\frac{g_m}{g_{m2}}\right) \tag{5.5}$$

$$VIP3 = \sqrt{24X\left(\frac{g_m}{g_{m3}}\right)} \tag{5.6}$$

$$IIP3 = \frac{2}{3}X\left(\frac{g_m}{g_{m3} \times R_s}\right) \tag{5.7}$$

$$IMD3 = \left[\frac{9}{2} \times (VIP3)^3 \times g_{m3}\right]^2 \times R_s \tag{5.8}$$

Where Rs = 50 Ω [211]

Figure 5.9 shows all the graphs of linearity parameters, they are VIP2, VIP3, IIP3, and IMD3, the BG-Fe-HJ-STFET is showing a better response as compared to BG-HJ-STFET. So, the BG-Fe-HJ-STFET structure is more suitable for distortion-less applications. The 1-dB compression point is another important linearity parameter that measures the upper limit of linear operation. It is the input power when output power linearity shifts 1-dB [211].

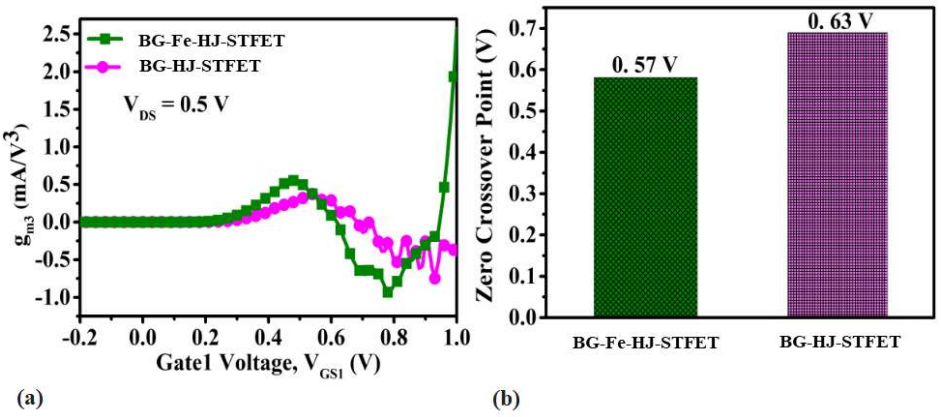

Figure 5.8 Variations of (a) gm3 and (b) zero crossover point at V_{DS}=0.5V of both studied TFETs.

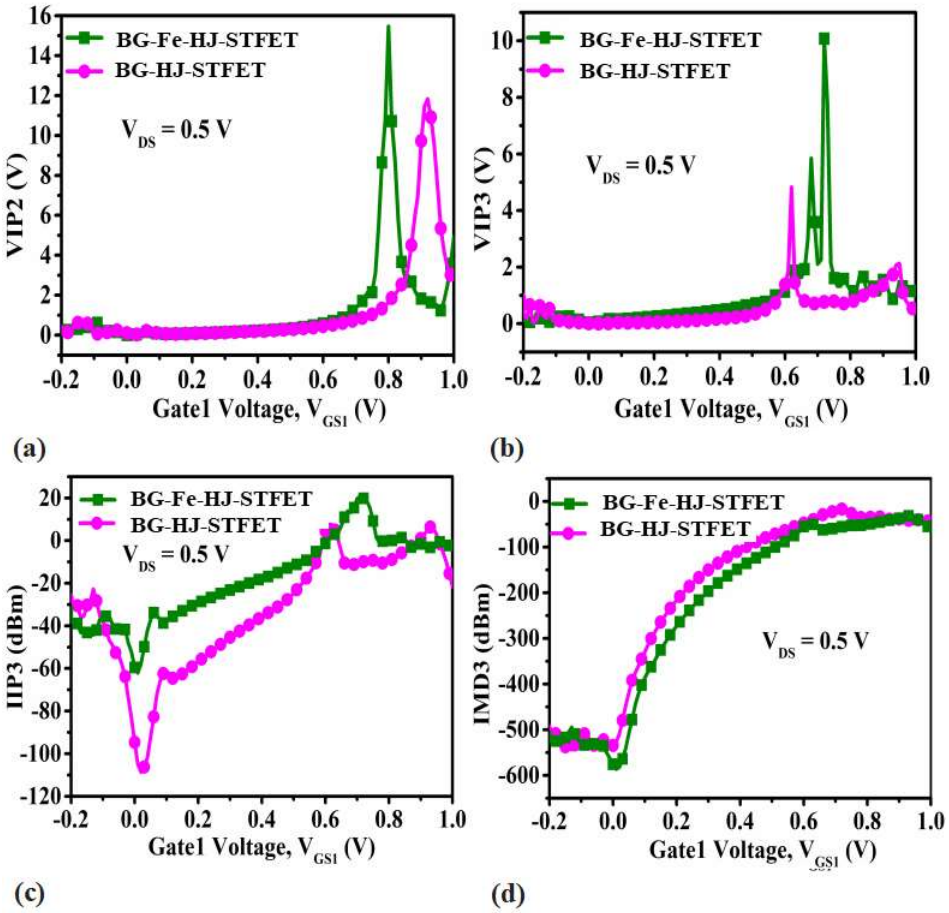

Figure 5.9 Variations of (a) VIP2, (b) VIP3, (c) IIP3, and (d) IMD3 with V_{GS} at V_{DS}=0.5V of both TFETs.

Figure 5.10 shows the plots of 1-dB compression point where the proposed structure has a maximum value of -22 dB at V_{GS1} =0.75 V. It is expressed as,

$$\text{1-dB Compression Point} = 0.22\sqrt{\frac{g_m}{g_{m3}}} \tag{5.9}$$

where g_m and g_{m3} are first and third differentiators of drain current vs. V_{GS}. Table 5.2 contains the performance comparison of BG-Fe-HJ-STFET and BG-HJ-STFET at V_{DS} = 0.5 V. All the performance parameters of BG-Fe-HJ-STFET are better than that of BG-HJ-STFET, so ferroelectric oxide as a gate oxide can be chosen for improvement in device-level performance.

Table 5.2: Comparison of the results of the mentioned TFET structures with the published article [76, 212].

Parameters	Units	BG-Fe-HJ STFET	BG-HJ STFET	Published article (SEBOX TFET) [76]	Published Article (PNPN TFET) [212]
I_{ON}	A/µm	1.77×10^{-5}	7.62×10^{-6}	----------	----------
I_{OFF}	A/µm	1.92×10^{-16}	1.92×10^{-16}	----------	----------
I_{ON}/I_{OFF}	Unitless	$9.22\text{x}10^{10}$	$3.96\text{ x}10^{10}$	$1\text{ x}10^{10}$	6×10^{7}
SS_{av}	mV/dec	38.6	48	61.5	62
E_{max}	MV/cm	3.013	2.70	----------	----------
V_{th}	V	0.4	0.47	0.7	----------
f_{Tmax}	GHz	4.2	3.9	0.0225	----------
$(GBP)_{max}$	GHz	0.41	0.38	----------	----------
ZCP	V	0.57	0.63	----------	----------

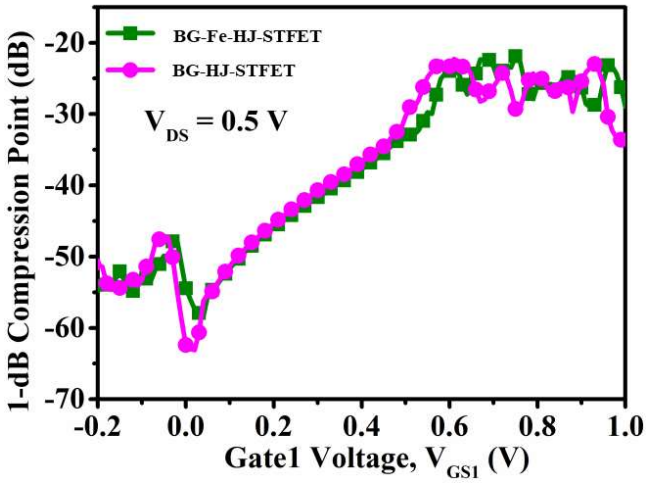

Figure 5.10 Plots of 1-dB compression point at V_{DS}=0.5V of both TFETs.

5.4 Conclusion

In this chapter, a novel back gated ferroelectric gate dielectric engineered Si/Ge heterojunction TFET on SELBOX (BG-Fe-HJ-STFET) is found to have an average subthreshold swing (SS) of 38.6 mV/dec which is much below the Boltzmann limit (60 mV/dec). Extensive TCAD-based simulation results show that BG-Fe-HJ-STFET is showing better device-level performance in terms of higher ON-current, higher I_{ON}/I_{OFF} ratio, lower SS, higher g_m, g_d, f_T, and *GBP* over BG-HJ-STFET. Therefore, the proposed structure is more suitable for low-power applications. In RF analysis, the maximum value of cut-off frequency (f_T) exhibited by our proposed device structure is very high (4.3 GHz), which in turn reduces the response time of the device. This makes it suitable for the designing of high-speed integrated circuit switches. Linearity analysis of the presented TFET indicates the ability of the proposed device to perform excellently in distortion-less switching operations. Keeping these think in mind the next chapter is based on the application of the proposed TFET (BG-Fe-HJ-STFET) as a dielectric modulated label-free biosensor.