Chapter 4

Dynamic Analysis and Loop Operation of Transformerless Hybrid Converter with Reduced Leakage Current

4.1 Introduction

In chapter 3, the mathematical modelling and small signal analysis of transformerless minimum phase hybrid converter (TLMPHC) and transformerless interleaved hybrid converter (TLIHC) have been presented. The verification and analysis of all the key features of both the proposed hybrid converters TLMPHC and TLIHC during the steady-state conditions have been discussed in the previous chapter. Also, in chapter 3, the simulation and experimental verifications of TLMPHC and TLIHC have been carried out. From the previous two chapters, it can be observed that the TLMPHC operates only in the operating condition of $D + M_i \leq 1$ and it is not suitable for higher power applications, as both the magnetically coupled inductor coils are charged and discharged simultaneously. In this chapter the verification and analysis of all the key features of the proposed TLIHC during the dynamic conditions are presented. The detailed design of both DC and AC side controllers and their advantageous features are discussed in this chapter. The behaviour of the controller used in the proposed TLIHC, for variations in passive components values are also presented. The cross-regulation behaviour of TLIHC is conferred during the dynamic loading conditions. The close-loop simulation and experimental verifications are carried out for validating the performance of the proposed TLIHC.

4.2 Close Loop Control of TLIHC

The controller of the proposed TLIHC has been implemented in digital domain using Nexys 4 DDR FPGA kit. The field programmable gate array (FPGA) has a built-in 12-bit analog-to-digital converter which accepts analog feedback signals (V_{DC}, V_{AC} and i_{Lf}) from the proposed TLIHC and convert them into digital domain for generating the gate signals for the controlled switches. The overall control structure of the proposed TLIHC is shown in Fig. 4.1. In this control architecture, the task of the controller is to generate gate control signals (S, S_1, S_2, S_3, S_4, S_5 and S_6) for the proposed TLIHC such that the DC output voltage and AC output voltage are regulated to their

respective reference values (V_{DC}^* and V_{AC}^*). For controlling the DC output voltage, a type-3 controller is used and for controlling the AC output voltage, a cascaded type control structure is used. In the AC cascaded control structure, the inner part is the inner current control loop and the outer part is outer voltage control loop.

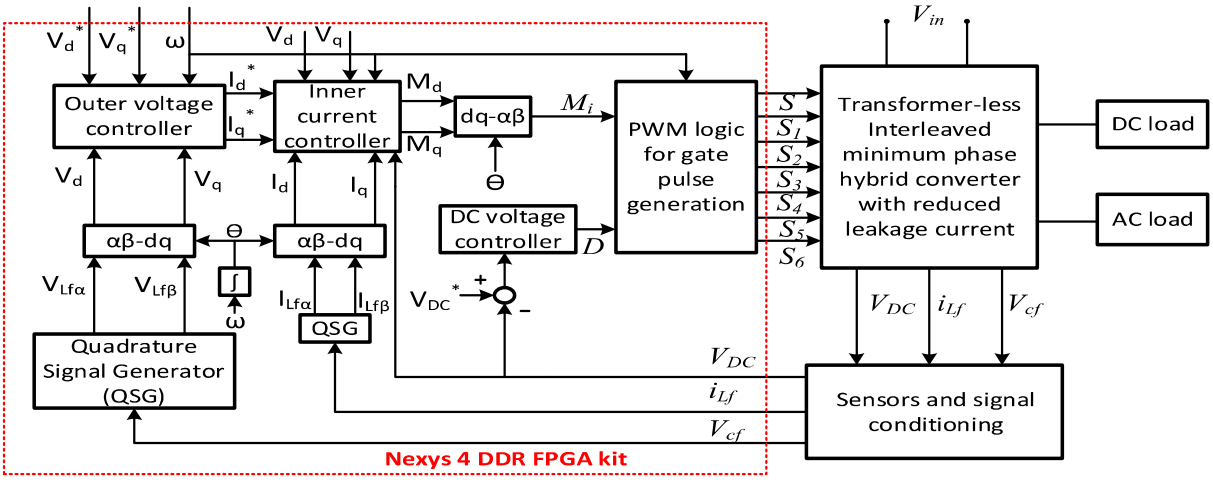


Fig. 4.1 Block diagram of overall control structure of the proposed TLIHC.

In case of the TLIHC, the AC reference voltage V_{AC}^* is directly given in $d-q$ domain (V_d^*, V_q^* and frequency ω). The quadrature signal generator (QSG) consists of a quadrature signal generation block and a phase control loop to calibrate the quadrature signals in real-time similar to Clark's transformation. The outputs of the controller block are non-shoot through duty ratio (D) and modulation index (M_i) which are given to the PWM block of the TLIHC. Finally, the gate control signals (S, S_1, S_2, S_3, S_4, S_5 and S_6) are generated.

4.3 DC Output Close Loop Control

DC side of the proposed TLIHC is basically a modified boost converter, where two magnetically coupled coils (L_1 and L_2) and one DC link capacitor (C) are considered for the DC part. The DC link capacitor further boosts the DC output voltage level, so that the DC gain of TLIHC is higher than that of the conventional boost converter. The DC side small-signal average transfer function ($\frac{\tilde{v}_{DC}(s)}{\tilde{d}(s)}$) of the state variable for the proposed TLIHC is discussed in chapter 3 (in section 3.3.2).

For the design parameters selected from Table 4.1, the plant transfer function of the system in numerical form is given as

$$\frac{\tilde{v}_{DC}(s)}{\tilde{d}(s)} = \frac{(5.768*10^{-5})s^3 + 2.368s^2 + 114.7s + 1.67*10^6}{(1.396*10^{-8})s^4 + (1.446*10^{-6})s^3 + (1.59*10^{-2})s^2 + (0.1465)s + 1080} \quad (4.1)$$

Table 4.1 Design parameters of TLIHC

Parameters	Values
V_{in}	170 V
C_o	400 µF
C	340 µF
L_1	2.82 mH
L_2	2.04 mH
M	1.48 mH
R_{DC}	700 Ω
R_{AC}	45 Ω

From chapter 3 (Fig. 3.9), it can be noticed that the proposed TLIHC has no right half-plane zero (RHPZ) and the minimum phase property is achieved for the operating condition $0.61 < D \leq 0.8$. Also, the proposed TLIHC is a boost derived type hybrid converter. Due to non-minimum phase behaviour of the boost converter, controllers such as PI and PID do not exhibit good performance with load variations and parametric uncertainties. On the other hand, from [113], it can be observed that the optimized type-3 controllers exhibit better closed-loop performance, higher bandwidth and better phase margin. Because of these reasons, a type-3 controller is used to control the DC output voltage of TLIHC.

The DC output of the proposed TLIHC is regulated by the duty ratio (D), where the switch-on duration of switch (S) decides the value of D. The overall schematic of the DC side controller is shown in Fig. 4.2. From the figure, it can be observed that a comparator compares the actual sensed DC output voltage (V_{act}) with the DC reference voltage (V_{ref}). Then the compared error signal is given to the controller. Finally, after comparing the controller output with the carrier signal (V_{tr}(t)),

the control signal of the switch (S) is obtained. On the basis of the charging and discharging modes of passive components, the proposed TLIHC can be operated in two states: i) non-shoot state (when S is ON) and ii) shoot-through state (when S is OFF). The switching signal S controls the DC output voltage of TLIHC.

The schematic of Type-3 controller is shown in Fig. 4.3 and the transfer function of the controller is obtained as

$$C(S) = \frac{V_c(S)}{V_i(S)} = \frac{R_1 + R_3}{C_2 R_1 R_3} \times \frac{\left(S + \frac{1}{R_2 C_1}\right)\left[\left(S + \frac{1}{C_3(R_1 + R_3)}\right)\right]}{S\left(S + \frac{C_1 + C_2}{R_2 C_1 C_2}\right)\left(S + \frac{1}{C_3 R_1}\right)} \tag{4.2}$$

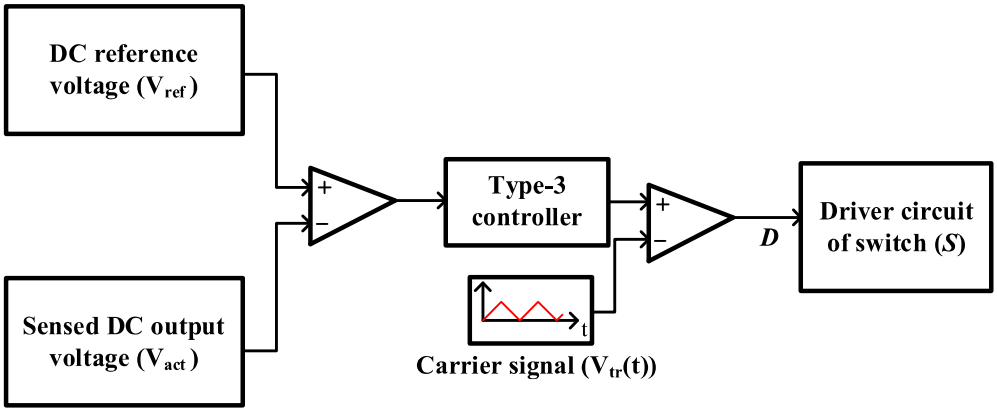


Fig. 4.2 Overall schematic of DC side controller.

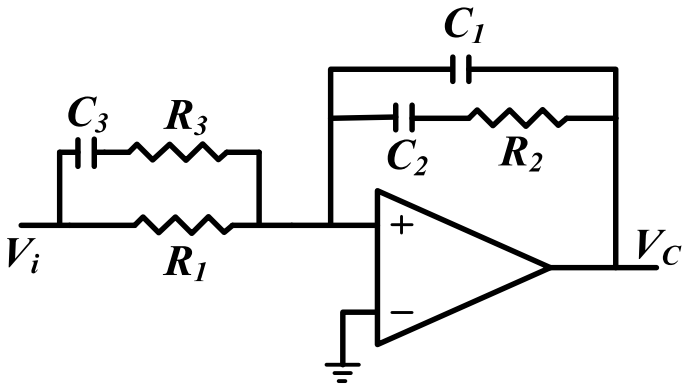


Fig. 4.3 Schematic of Type-3 controller.

Table 4.2 Zero and pole locations of Type-3 controller

Zeros		Poles	
f_{z1}	$\frac{1}{2\pi(R_2C_1)}$	f_{p1}	0 (at origin)
f_{z2}	$\frac{1}{2\pi C_3(R_1 + R_3)}$	f_{p2}	$\frac{C_1 + C_2}{2\pi(R_2C_1C_2)}$
		f_{p3}	$\frac{1}{2\pi(R_1C_3)}$

The locations of zeros and poles of Type-3 controller are given in Table 4.2. It can be observed that the Type-3 controller has two zeros and three poles among which one pole is located at origin. Also, from the pole-zero locations, it can be concluded that the phase of the controller reaches 180^0 at some frequencies. So, the compensated TLIHC can maintain a reasonable phase margin. Fig. 4.4 shows the bode plot of uncompensated and compensated system for the DC output. It can be observed from the bode plot that the gain margin (GM) and phase margin (PM) of the compensated system are 18 dB and 46^0 respectively.

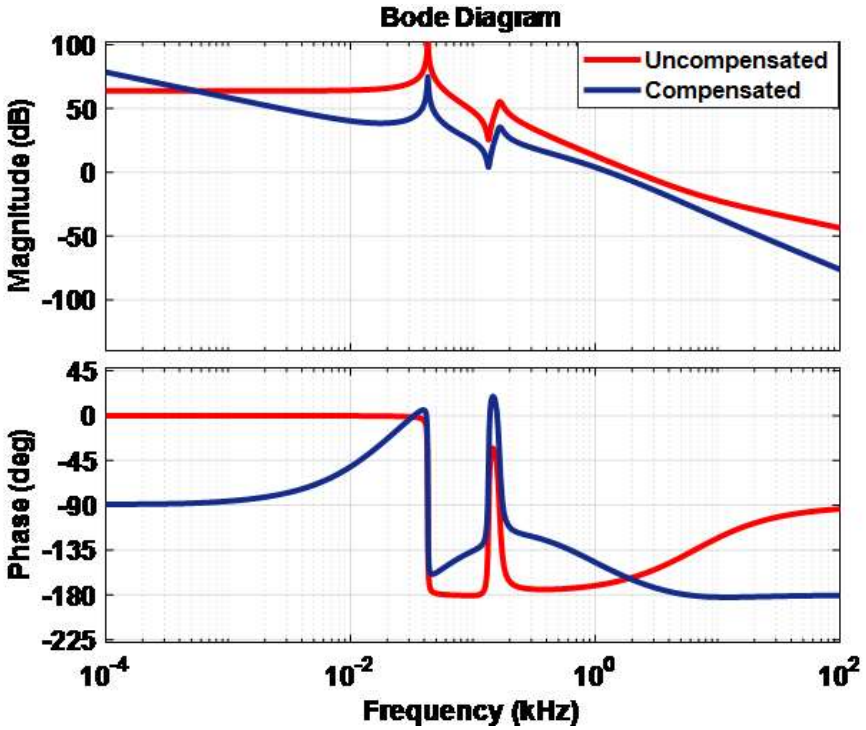
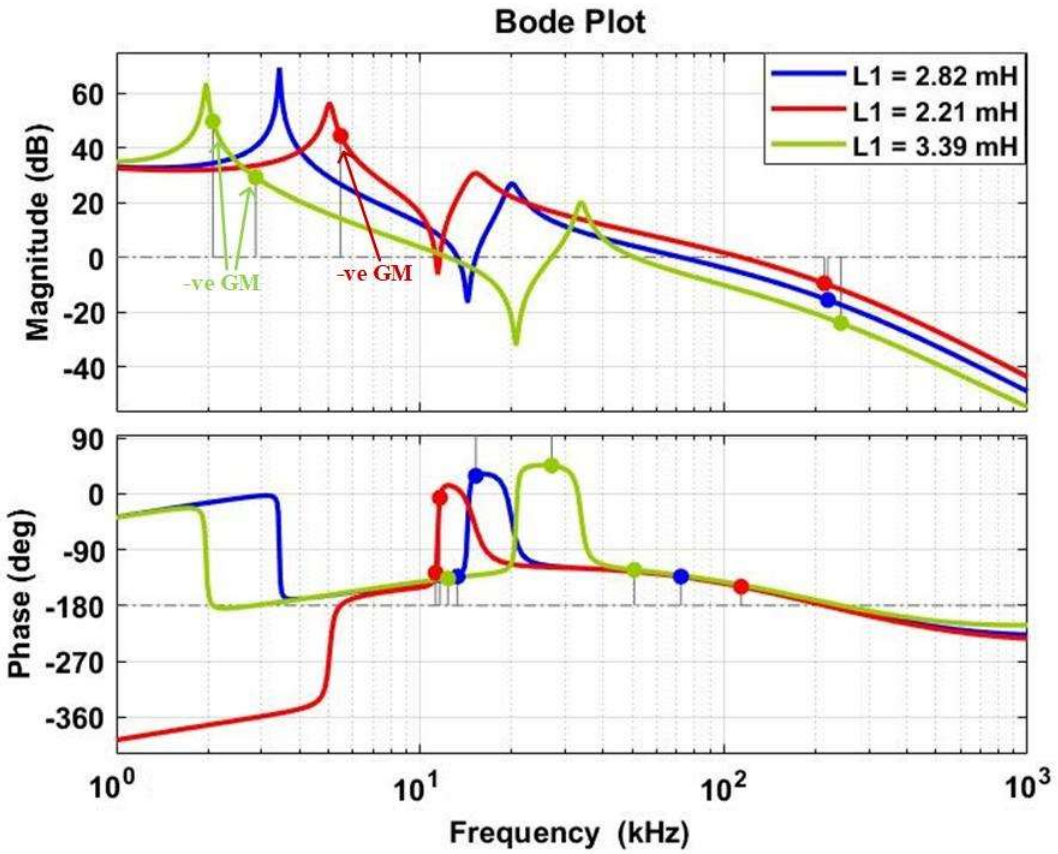


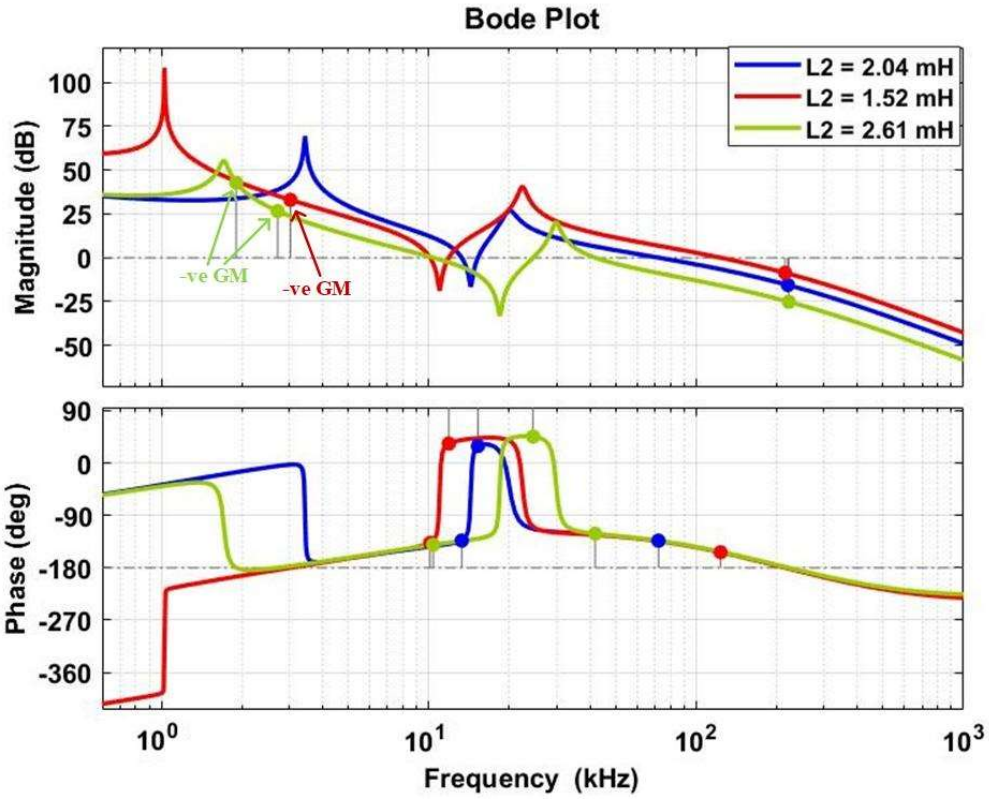
Fig. 4.4 Compensated and uncompensated bode plot for DC output voltage.

4.3.1 Performance of DC Side Controller

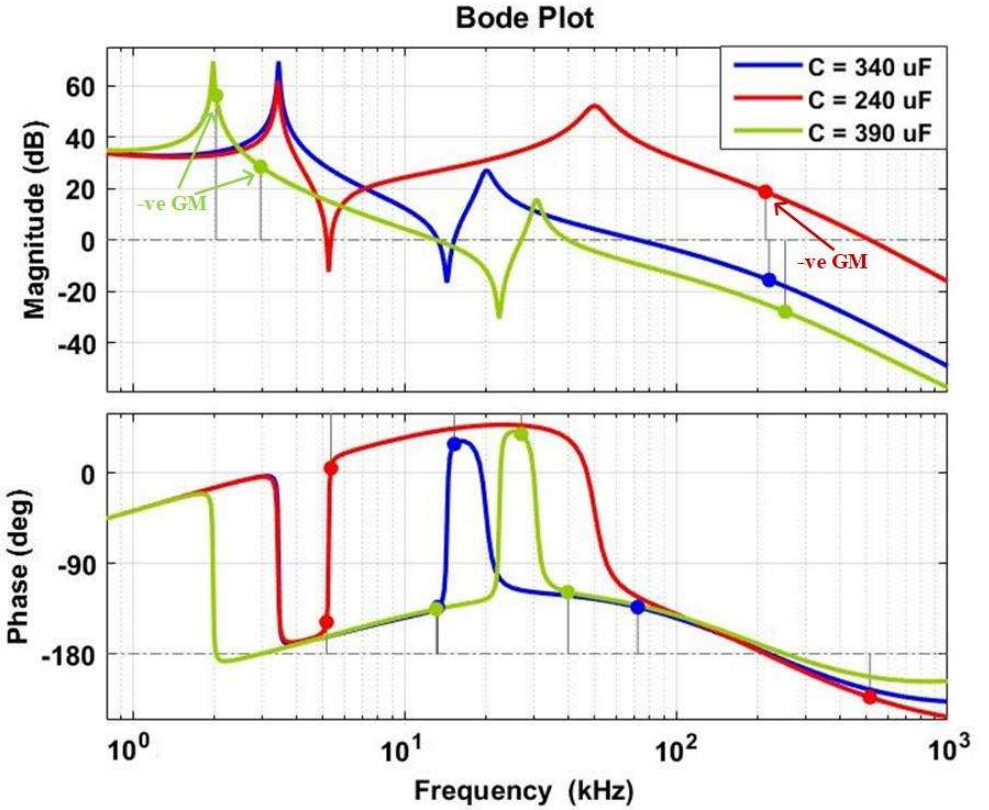
To check the robustness of the controller, the performance of the controller has been verified by changing various passive parameters (inductor and capacitor) of the proposed TLIHC. However, the passive parameters are calculated according to the charging and the discharging slope of the ripple content and the variation in its percentage. In chapter 3, the circuit diagram of the proposed TLIHC is shown in Fig. 3.1, wherein the designed values of the passive parameters L_1, L_2 and C are 2.82 mH, 2.04 mH and 340 µF respectively. Also, the inductor currents ripple percentage ($x_{L1}\%$ and $x_{L2}\%$) is selected as ≤ 10 % and the capacitor voltage ripple percentage ($x_C\%$) is selected as ≤ 5 %. Fig. 4.5 shows the compensated bode plot for the DC output by varying various passive parameters of the proposed TLIHC. In order to verify the robustness of the controller, variations in L_1, L_2 and C are done for both higher and lower values from their designed values. Fig. 4.5 (a) and (b) show the compensated bode plot, varying the passive parameter L_1 and L_2. Similarly, Fig. 4.5 (c) shows the compensated bode plot, varying the passive parameter C. Fig. 4.5 (d) shows the compensated bode plot varying the passive parameters L_1, L_2 and C simultaneously.



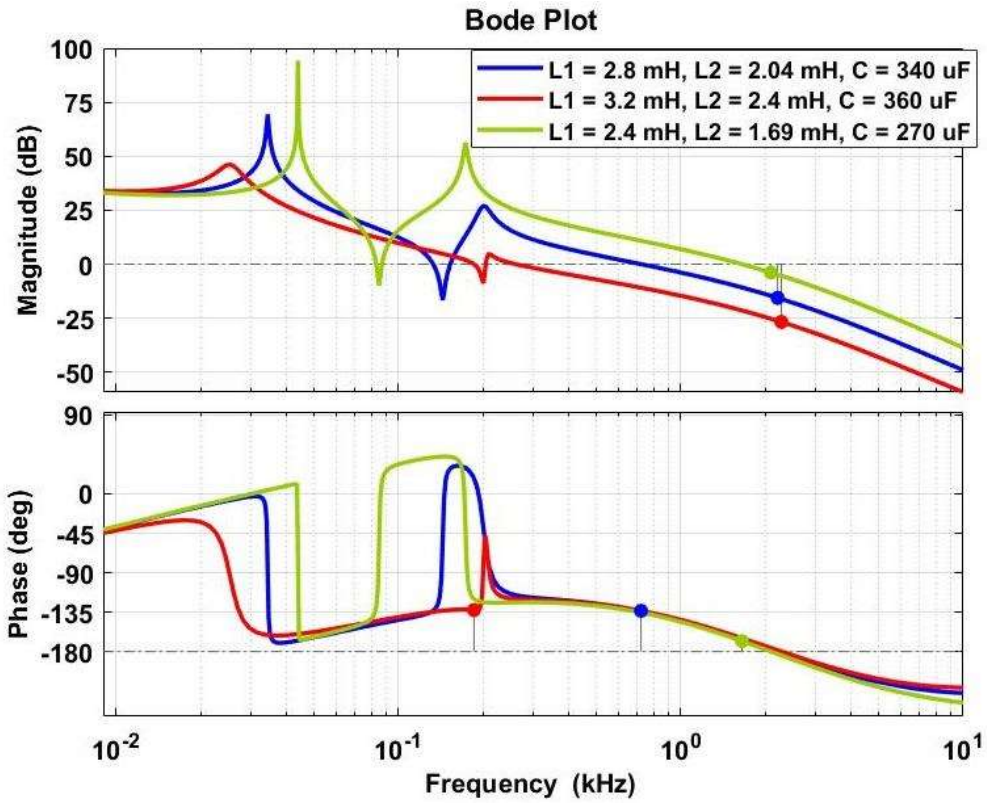
(a)


Bode Plot
L2 = 2.04 mH
L2 = 1.52 mH
L2 = 2.61 mH
Magnitude (dB)
100
75
50
25
0
-25
-50
-ve GM
-ve GM
Phase (deg)
90
0
-90
-180
-270
-360
10^0
10^1
10^2
10^3
Frequency (kHz)

(b)


Bode Plot
C = 340 uF
C = 240 uF
C = 390 uF
Magnitude (dB)
60
40
20
0
-20
-40
-ve GM
-ve GM
Phase (deg)
0
-90
-180
10^0
10^1
10^2
10^3
Frequency (kHz)

(c)



(d)

Fig. 4.5 Compensated bode plot of the proposed TLIHC varying (a) L_1, (b) L_2, (c) C and (d) L_1, L_2 and C simultaneously.

From Fig. 4.5 (a), it can be observed that the system sustains stability up to $\pm$ 20 % variation of L_1 (2.256 mH $\leq L_1 \leq$ 3.384 mH) from the designed value. The instability appears in the system as the gain margin (GM) is negative beyond this range. Similarly, up to $\pm$ 20 % variation in the designed value of L_2 (1.62 mH $\leq L_2 \leq$ 2.45 mH), the system remains in stable condition and becomes unstable beyond this, which is observed in Fig. 4.5 (b). However, from Fig. 4.5 (c), it can be observed that the system operates in stable region from 23 % lower to 10 % higher values compared to the designed value of C (262 µF $\leq C \leq$ 375 µF). Beyond this range, the system behaviour is unstable due to negative GM. From Fig. 4.5 (d), it can be observed that for simultaneous variation of all the passive parameters up to the above-mentioned limits, the system is stable as both GM and phase margin (PM) are positive. As the transfer function ($\frac{\tilde{v}_{DC}(s)}{\tilde{d}(s)}$) depends on the passive parameter values of L_1, L_2 and C, when these parameter values are changed, the transfer function is also changed accordingly. The controller is designed in such a manner that it

produces a stable output, when the variation in those passive parameter values is small as observed in Fig. 4.5. Hence, it can be concluded that the controller is robust enough to tolerate $\pm$ 20 % variation in the designed value of L_1 and L_2, and 23 % lower to 10 % higher variation of the designed value of C.

4.4 AC Output Close Loop Control

A synchronous reference frame-based control algorithm is used to regulate the AC output of the proposed TLIHC similar to single-phase voltage source inverter [61] and [62]. A type-2 controller is used in the outer voltage control loop of the AC controller, whereas a proportional controller is used in the inner current control loop.

4.4.1 Synchronous Reference Frame Control Strategy

In synchronous reference frame control strategy, a time-invariant direct-quadrature rotating frame model of inverter output is considered to make the controller design simpler. In this technique, the AC output voltage and current signals are controlled in the DC domain, which leads to a better performance as compared to controlling the sinusoidal signals using other controlling techniques. Further, in this strategy an orthogonal rotating reference frame axes ($d-q$ axes), which rotates at synchronous speed are considered. The inverter output voltage and current signals are sensed by using appropriate sensors in terms of α- signal (or β- signal) in the stationary reference frame. This α- signal is used to generate the β- signal (or vice-versa) by using QSG and these two signals correspond to the $\alpha\beta$- axes (orthogonal to each other). Then, the AC domain signals ($\alpha\beta$ signals) are converted into time-invariant DC domain signals ($dq-$ signals) and subsequently passed to the controller. Therefore firstly, two orthogonal axes (rotating reference frame) are considered, and then the projection of sinusoidal signals (time-variant) on the $d-q$ axes are taken to make it time-invariant. The axes are considered to be rotating at the rate of ω rad/sec such that the projection of these sinusoidal signals on $d-q$ axes are time-invariant. These $\alpha\beta$ signals are the time varying orthogonal sinusoidal signals.

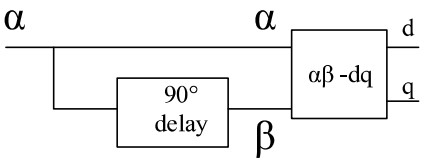


Fig. 4.6 Quadrature signal generation and $\alpha\beta - dq$ transformation.

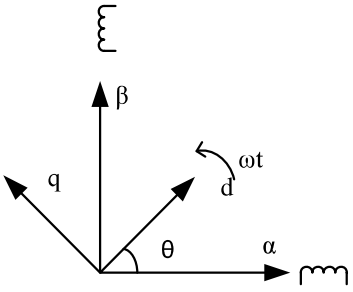


Fig. 4.7 Reference frame model in space frame.

For $\alpha\beta - dq$ transformation, β components are generated by delaying α components by 90^0. Fig 4.6 shows the QSG block and $\alpha\beta - dq$ transformation block. Fig 4.7 shows reference frame in space for the transformation.

To convert $\alpha\beta - dq$ components and $dq - \alpha\beta$ components, the following transformation matrices are used

$$\begin{bmatrix} X_d \\ X_q \end{bmatrix} = \begin{bmatrix} Cos\ \omega t & Sin\ \omega t \\ -Sin\ \omega t & Cos\ \omega t \end{bmatrix} \begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} \tag{4.3}$$

$$\begin{bmatrix} X_d \\ X_q \end{bmatrix} = [T] \begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} \tag{4.4}$$

$$\begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} = [T]^{-1} \begin{bmatrix} X_d \\ X_q \end{bmatrix} \tag{4.5}$$

where $[T] = \begin{bmatrix} Cos\ \omega t & Sin\ \omega t \\ -Sin\ \omega t & Cos\ \omega t \end{bmatrix}$

4.4.2 D-Q Modelling of AC Side of TLIHC

For controlling the AC output voltage, AC output voltage and filter inductor current are sensed. As these two quantities are time variant quantities, using $\alpha\beta - dq$ transformation, the sensed AC voltage and filter inductor current are made DC time invariant quantities in $d - q$ domain without using any matrix transformation. Hence, for easier control and reducing the complexity of the calculations, $\alpha\beta - dq$ transformation is used. The different controllers like PI and PID controllers offer effective and reliable steady state control solutions, when the controlled quantities are DC in nature. However, if the input quantities applied to these feedback controllers are periodic or sinusoidal in nature, the integrator term of the controller typically fails to introduce a finite gain. Thus, for controlling AC voltage of the proposed TLIHC, $\alpha\beta - dq$ transformation has been used in this work.

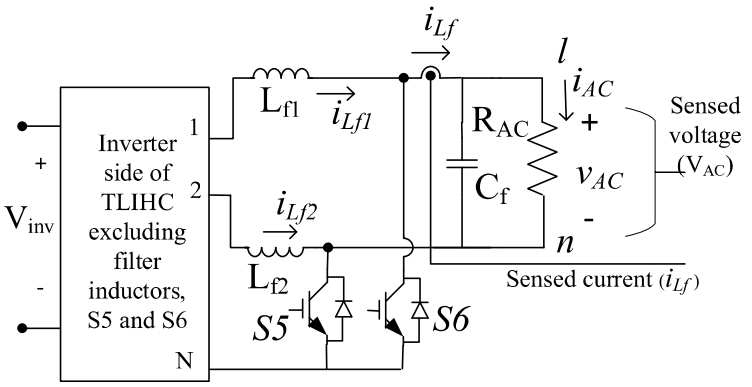


Fig. 4.8 AC side sensed voltage and current signals.

Fig 4.8 shows AC side sensed inductor current (i_{Lf}) and AC output voltage (V_{AC}). During the positive half cycle of the AC output voltage, i_{Lf} represents the current through the filter inductor L_{f1} and during the negative half cycle it represents the current through the inductor L_{f2}. Similarly, the sensed AC voltage is the voltage across the filter capacitor (C_f). Fig 4.9 represents circuit diagram of the proposed TLIHC referred to the AC output filter. The filter inductor (L_f) represents L_{f1} during the positive half cycle and L_{f2} during the negative half cycle of the AC output voltage. As in case of the proposed TLIHC, unipolar sinusoidal pulse width modulation (SPWM) technique is used. Three levels of inverter output voltage $V_{inv} = \delta(t)V_{dc}$ are obtained prior to the AC filter parameters, which are V_{dc}, 0 and -V_{dc}. The controlled switches of TLIHC are operated at high

switching frequency, except for switches S_5 and S_6. During the entire switching cycle, V_{inv} can be calculated as follows:

$$V_{inv} = \frac{1}{T_{sw}} \int_{t-T_{sw}}^{t} \delta(t) V_{dc} d\tau \tag{4.6}$$

where $\delta(t)$ is modulated by M_i and it is given as

$$\delta(t) = \begin{cases} 1, \text{during the power and zero states of positive half cycle} \\ 0, \text{ during the shoot} - \text{through state} \\ -1, \text{during the power and zero states of negative half cycle} \end{cases} \tag{4.7}$$

From expression (4.3), V_{inv} can be written as

$$V_{inv} = M_i V_{dc} \tag{4.8}$$

where $V_{dc} = \frac{V_{in}}{D}$

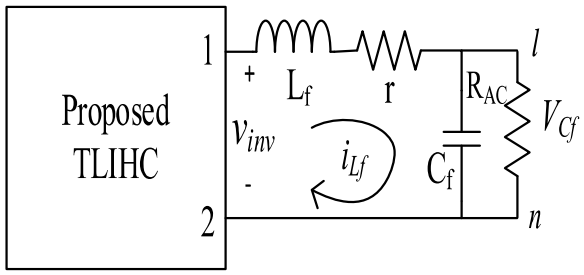


Fig. 4.9 Proposed TLIHC referred to AC output filter.

By applying KVL in Fig. 4.8

$$M_i V_{dc} = L_f \frac{di_{Lf}}{dt} + r i_{Lf} + V_{Cf} \tag{4.9}$$

$$\frac{di_{Lf}}{dt} = -\frac{r}{L_f} i_{Lf} - \frac{V_{Cf}}{L_f} + \frac{M_i}{L_f} V_{dc} \tag{4.10}$$

By applying KCL in Fig. 4.7

$$C_f \frac{dV_{Cf}}{dt} = i_{Lf} - \frac{V_{Cf}}{R_{AC}} \tag{4.11}$$

The expression given in (4.10) can be written in $\alpha\beta$ matrix form as follows:

$$\frac{d}{dt}\begin{bmatrix} i_{Lf\alpha} \\ i_{Lf\beta} \end{bmatrix} = -\frac{r}{L_f}\begin{bmatrix} i_{Lf\alpha} \\ i_{Lf\beta} \end{bmatrix} - \frac{1}{L_f}\begin{bmatrix} V_{Cf\alpha} \\ V_{Cf\beta} \end{bmatrix} + \frac{V_{dc}}{L_f}\begin{bmatrix} M_{i\alpha} \\ M_{i\beta} \end{bmatrix} \tag{4.12}$$

After applying $\alpha\beta - dq$ transformation, (4.12) can be written as

$$\frac{d}{dt}[T]^{-1}\begin{bmatrix} i_{Lfd} \\ i_{Lfq} \end{bmatrix} = -\frac{r}{L_f}[T]^{-1}\begin{bmatrix} i_{Lfd} \\ i_{Lfq} \end{bmatrix} - \frac{1}{L_f}[T]^{-1}\begin{bmatrix} V_{Cfd} \\ V_{Cfq} \end{bmatrix} + \frac{V_{dc}}{L_f}[T]^{-1}\begin{bmatrix} M_{id} \\ M_{iq} \end{bmatrix} \tag{4.13}$$

Differentiating the left-hand side of (4.13), the simplified expression is written as

$$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}\frac{d}{dt}\begin{bmatrix} i_{Lfd} \\ i_{Lfq} \end{bmatrix} = \begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix}\begin{bmatrix} i_{Lfd} \\ i_{Lfq} \end{bmatrix} - \frac{r}{L_f}\begin{bmatrix} i_{Lfd} \\ i_{Lfq} \end{bmatrix} - \frac{1}{L_f}\begin{bmatrix} V_{Cfd} \\ V_{Cfq} \end{bmatrix} + \frac{V_{dc}}{L_f}\begin{bmatrix} M_{id} \\ M_{iq} \end{bmatrix} \tag{4.14}$$

In state space form (4.14) can be written as

$$\frac{d}{dt}\begin{bmatrix} i_{Lfd} \\ i_{Lfq} \end{bmatrix} = \begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix}\begin{bmatrix} i_{Lfd} \\ i_{Lfq} \end{bmatrix} - \frac{r}{L_f}\begin{bmatrix} i_{Lfd} \\ i_{Lfq} \end{bmatrix} - \frac{1}{L_f}\begin{bmatrix} V_{Cfd} \\ V_{Cfq} \end{bmatrix} + \frac{V_{dc}}{L_f}\begin{bmatrix} M_{id} \\ M_{iq} \end{bmatrix} \tag{4.15}$$

Taking Laplace transform of (4.15)

$$sI_{Lfd}(s) = \omega I_{Lfq}(s) - \frac{r}{L_f}I_{Lfd}(s) - \frac{V_{Cfd}}{L_f} + M_d\frac{V_{dc}}{L_f} \tag{4.16}$$

$$sI_{Lfq}(s) = -\omega I_{Lfd}(s) - \frac{r}{L_f}I_{Lfq}(s) - \frac{V_{Cfq}}{L_f} + M_q\frac{V_{dc}}{L_f} \tag{4.17}$$

Expressing given in (4.11) can be written in $\alpha\beta$ matrix form as follows

$$\frac{d}{dt}\begin{bmatrix} V_{Cf\alpha} \\ V_{Cf\beta} \end{bmatrix} = \frac{1}{C_f}\begin{bmatrix} i_{Lf\alpha} \\ i_{Lf\beta} \end{bmatrix} - \frac{1}{C_f R_{AC}}\begin{bmatrix} V_{Cf\alpha} \\ V_{Cf\beta} \end{bmatrix} \tag{4.18}$$

After transformation and differentiation, the Laplace transformation of (4.18) can be written as follows

$$sV_{Cfd}(s) = \frac{1}{C_f}I_{Lfd}(s) + \omega V_{Cfq}(s) - \frac{1}{C_f R_{AC}}V_{Cfd}(s) \tag{4.19}$$

$$sV_{Cfq}(s) = \frac{1}{C_f}I_{Lfq}(s) - \omega V_{Cfd}(s) - \frac{1}{C_f R_{AC}}V_{Cfq}(s) \tag{4.20}$$

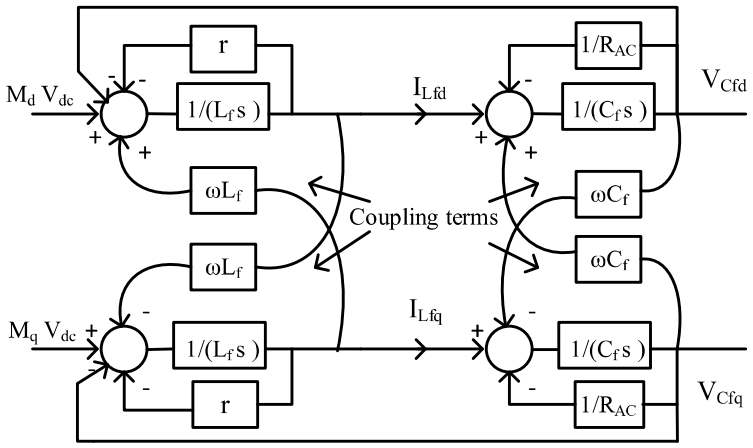


Fig. 4.10 Signal flow graph of mathematical model of AC output side of the proposed TLIHC.

The expressions given in (4.16), (4.17), (4.19) and (4.20) represent the mathematical model of AC output side of the proposed TLIHC. Fig 4.10 shows the signal flow graph of the mathematical model of the AC output side of the proposed TLIHC.

From the signal flow graph of the mathematical model of the AC output side of the proposed TLIHC, it can be observed that there are two coupling terms ωL_f and ωC_f. While designing the controller for the proposed TLIHC, the coupled terms are decoupled by adding or subtracting the required terms. After decoupling, the transfer function of the inner current control loop can be expressed as $\frac{1}{r+sL_f}$. As, the value of r is very small, the inner current loop transfer function is approximated to $\frac{1}{sL_f}$. So, a simple proportional controller can be used for the inner current control loop. The outer voltage control loop is designed based on the transfer function $\frac{R_{AC}}{1+sR_{AC}C_f}$. Generally, the output voltage controller of inverter is designed at very light load condition. A type-2 controller is used for the outer voltage control loop of the proposed TLIHC. The schematic of the overall control structure of AC output side of TLIHC is shown in Fig. 4.11, where two $\alpha\beta - dq$ and one $dq - \alpha\beta$ transformation matrix is used. The $\alpha\beta - dq$ transformation matrix is used to convert the sensed time variant AC output voltage and current quantities into their time-invariant synchronous reference frame quantities. The $dq - \alpha\beta$ transformation matrix is used to convert the controlled time-invariant form of reference signal $V_m(t)$ into its time variant one. The simplified

control structure of AC output side of the proposed TLIHC is shown in Fig. 4.12. The design parameters for the AC output side of TLIHC is given in Table 4.3.

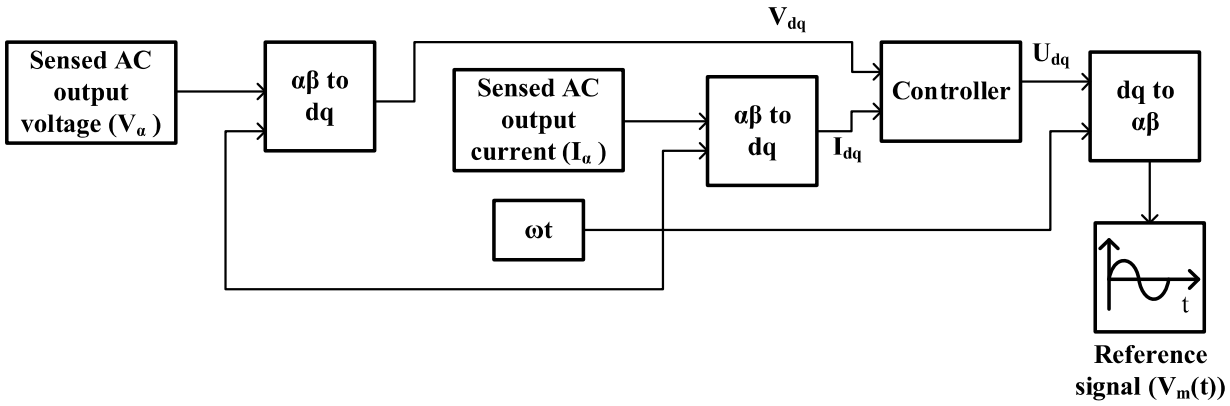


Fig. 4.11 Schematic of overall control structure of AC output side of TLIHC.

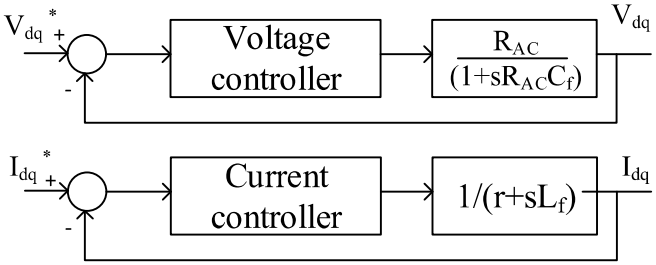


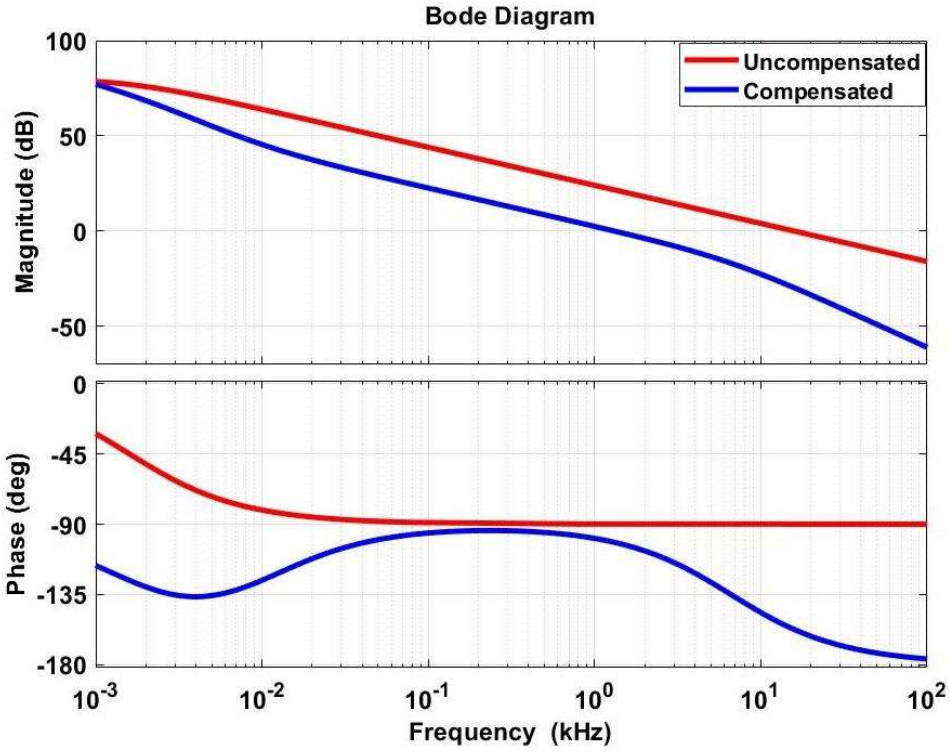
Fig. 4.12 Simplified control structure of AC output side of TLIHC.

Table 4.3 Design parameters for AC output side of the proposed TLIHC

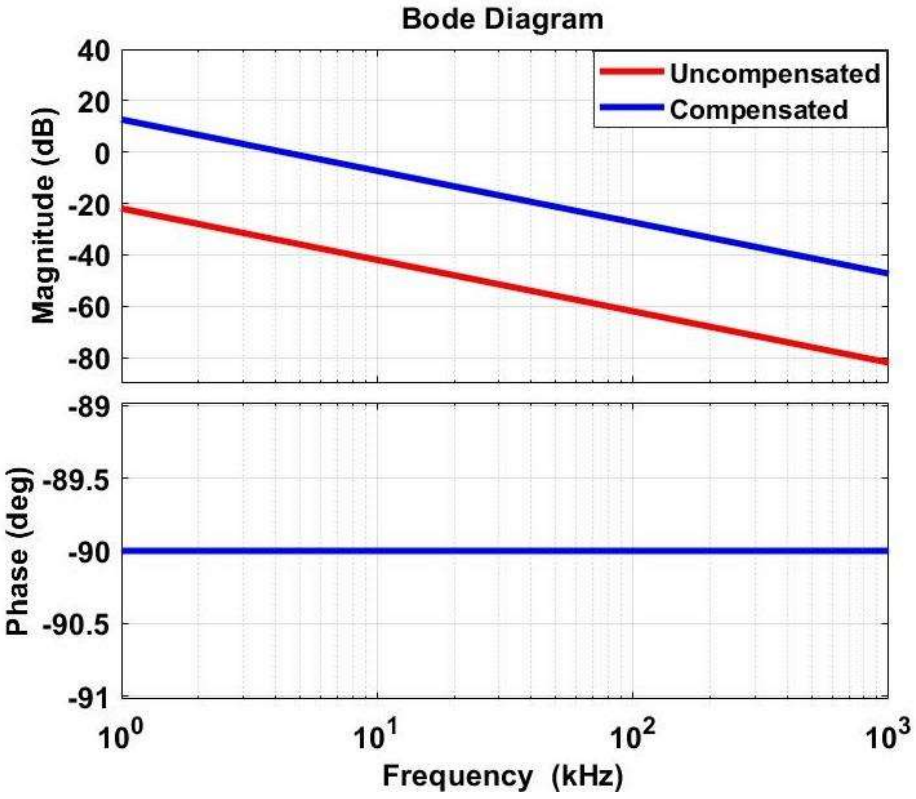
Parameters	Values
L_{f1}	2 mH
L_{f2}	2 mH
C_f	5 μF
R_{AC}	50 Ω

4.4.3 Performance of AC Side Controller

The AC output waveforms of the proposed TLIHC are similar to that of conventional voltage source inverter (VSI). Therefore, the filter design is also similar to those of VSIs ($L_f = L_{f1} + L_{f2}$). As the developed topology is a symmetrical filter-based topology, the filter inductor is split into two equal parts ($L_{f1} = L_{f2} = \frac{L_f}{2}$). Fig. 4.13 (a) and (b) shows the uncompensated and compensated bode plot of the AC outer voltage and inner current loops. It can be observed from Fig. 4.13 that the compensated outer voltage loop has a phase margin of 74^0 and bandwidth of 1.2 kHz. The compensated inner current loop has a phase margin of 90^0 and bandwidth of 4.1 kHz. Further, it can be observed that the inner current loop is much faster than the outer voltage loop. So, during AC load change conditions, the AC load current is settled to a steady state value quickly. In addition, as the DC output controller is faster than the AC output controller, the DC output voltage is settled to a steady state value without disturbing the AC output voltage during load change conditions.



(a)



(b)

Fig. 4.13 Compensated and uncompensated Bode plot for **(a)** AC voltage control loop and **(b)** AC current control.

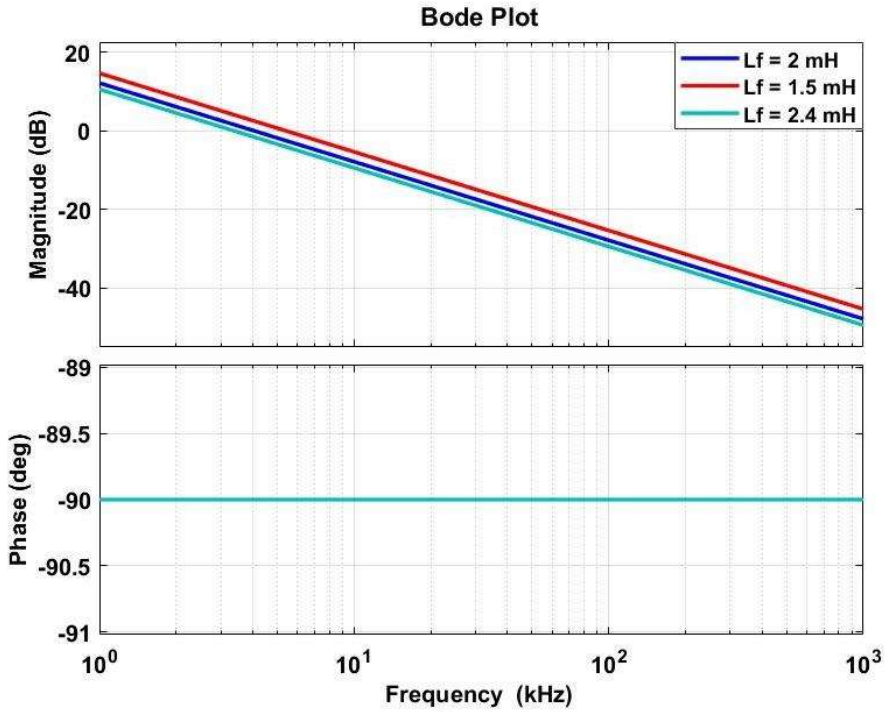


Fig. 4.14 Compensated Bode plot of AC current control loop varying AC filter inductor.

The compensated bode plot for the inner current control loop by varying the AC filter inductance value is shown in Fig. 4.14. As the filter inductor internal resistance (r) is very small, the inner current controller is designed on the transfer function $\frac{1}{sL_f}$, which results into constant phase margin (PM) of 90^0, irrespective of the type of AC filter inductance (symmetrical/unsymmetrical filter inductance) used in the proposed TLIHC. From Fig. 4.14, it can be observed that the bandwidth changes in each half cycle of the AC output voltage, if unequal (unsymmetrical filter inductance) filter inductors are used. If two different values of filter inductors are used, the bandwidth of the inner current control loop is different for positive and negative half cycles of the AC output voltage. As, the bandwidth is the band of frequencies to which the system can respond satisfactorily, the distortion in AC output voltage is more for half cycles with lower bandwidth as compared to the higher bandwidth half cycles. Further, the other important point for the closed-loop operation of TLIHC is that the inner current loop should always give faster response than the outer voltage loop. So, the chances of instability are more, if the bandwidth of the inner current control loop is not sufficiently large compared to the outer voltage control loop.

4.5 Verification of Dynamic Response of TLIHC

The dynamic response of the proposed TLIHC is verified through simulation and the cross-regulation behaviour of TLIHC is verified through experimentation. The various operating parameters of TLIHC and their attributes for simulation and experimental studies are given in Table 4.4.

Table 4.4 List of Parameters and Attributes for Dynamic Response of TLIHC

Parameters	Attributes
L_1	2.82 mH
L_2	2.04 mH
C	360 µF
C_0	400 µF
R_{DC}	700 Ω
R_{AC}	45 Ω

4.5.1 Simulation Results of TLIHC

The simulation studies of the proposed TLIHC for the dynamic response are carried out using MATLAB/SIMULINK. The DC output voltage for step-down in duty ratio is shown in Fig. 4.15 (a). From Fig. 4.15 (a), it can be observed that the DC output voltage has been stepped down at 1.68 sec and settles at 930 V within 0.2 sec, which verifies the fast dynamic response of the controller during step-down operation of D. Also, it can be noticed from Fig. 4.15 (a) that the proposed TLIHC has no transient overshoot and ringing, when D is decreased. Fig. 4.15 (b) shows the AC output voltage and current of TLIHC during the step-down condition of D from 0.78 to 0.76.

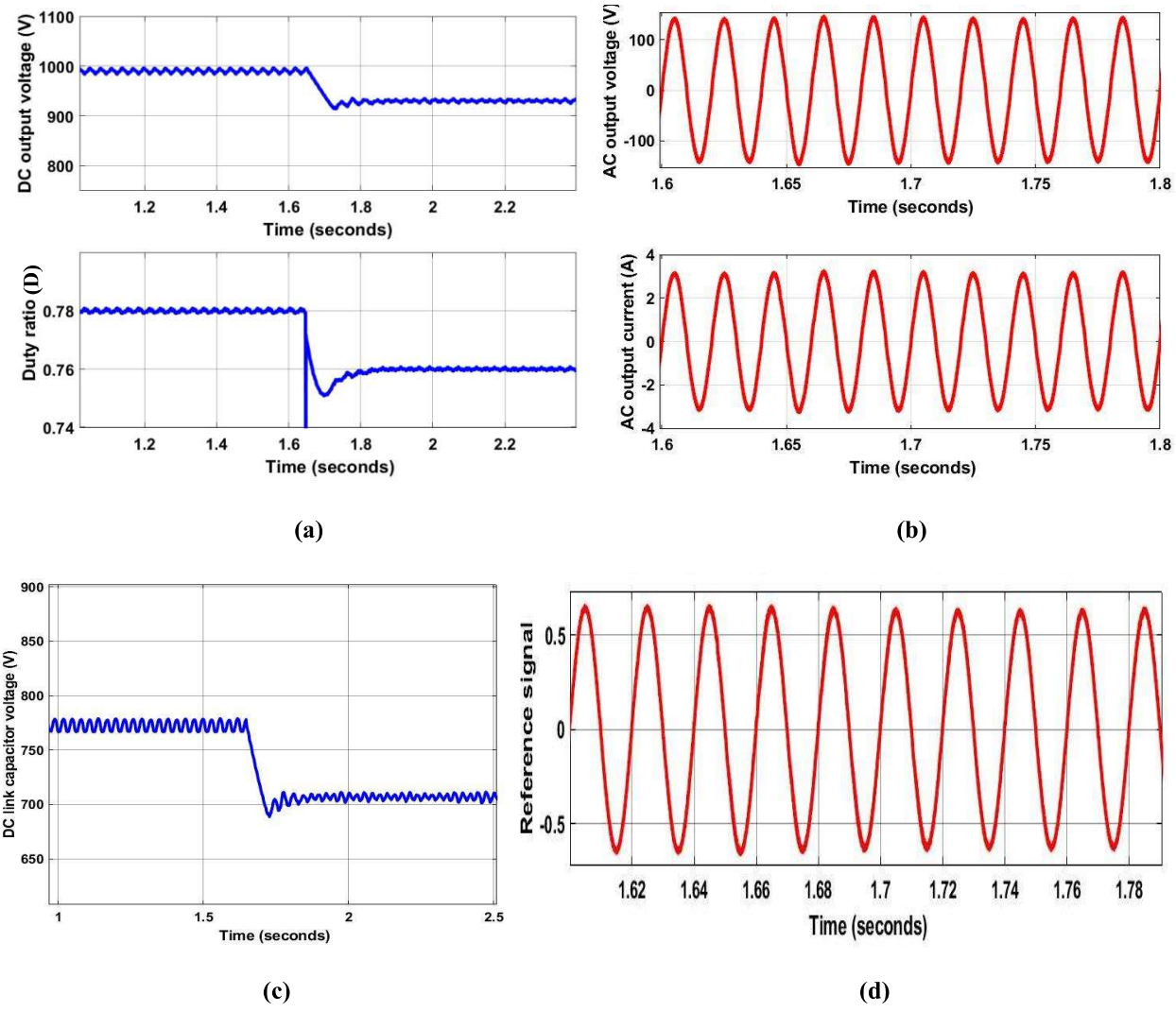
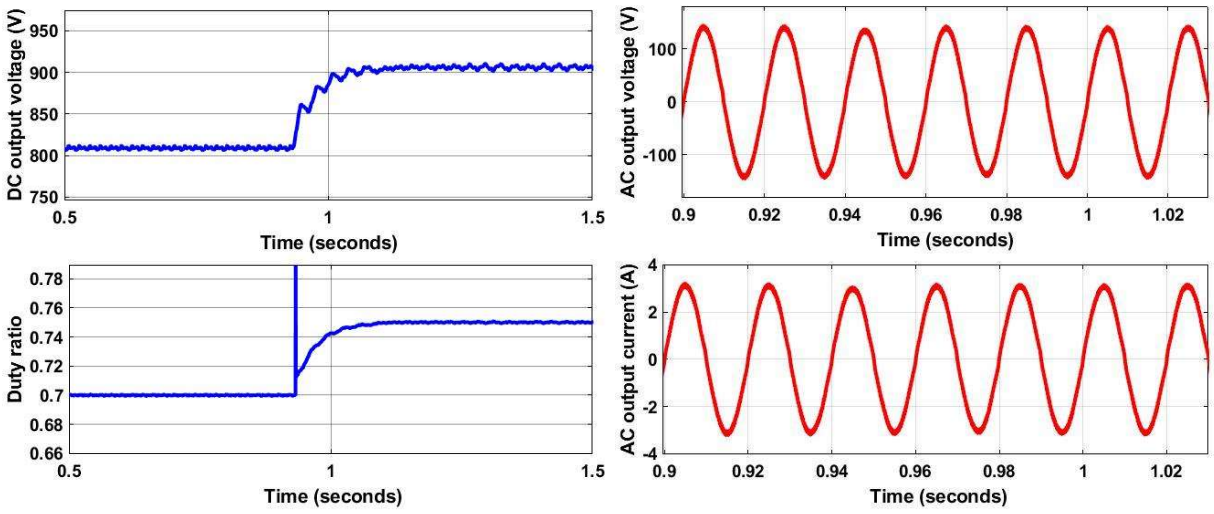
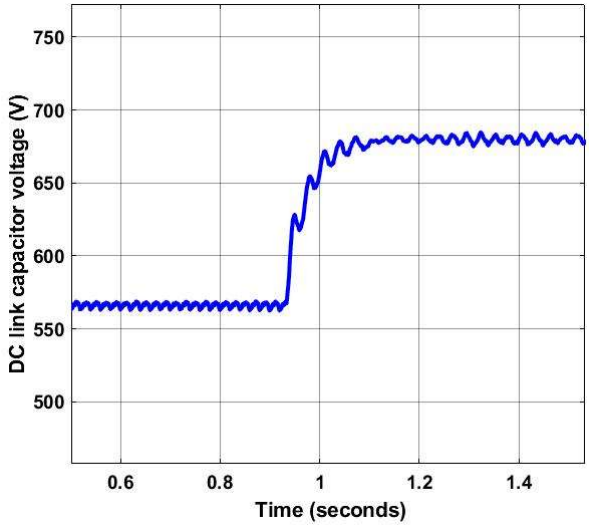


Fig. 4.15 Response to step-down in duty ratio. **(a)** DC output voltage with respect to change in duty ratio, **(b)** AC output voltage and current, **(c)** DC link voltage and **(d)** Reference signal for SPWM implementation.

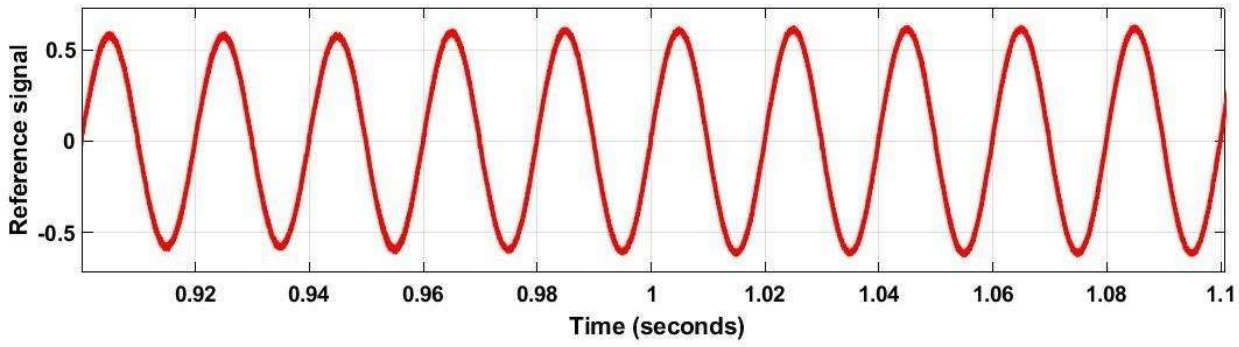
It can be observed from Fig 4.15 (b) that the AC output voltage does not show any fluctuation due to stepping down of DC output voltage, which leads to a regulated AC output voltage of the proposed TLIHC. Fig. 4.15 (c) shows the DC link voltage variation due to sudden change in D. It can be observed from Fig. 4.15 (c) that the DC link voltage has been step down at 1.68 sec and settles down to 709 V within 0.2 sec. Fig. 4.15 (d) shows the reference signal for the generation of switching pulses of the inverter side switches of TLIHC. As, the inverter input voltage ($V_{inv} = \frac{V_{in}}{D}$) is increased due to decrease in D, the modulation index (M_i) of TLIHC is slightly decreased to make the AC output voltage same. From Fig. 4.15 (d), it can be noticed that the reference signal is slightly decreased due to increase in D or DC reference voltage in case of the proposed TLIHC.



(a) **(b)**



(c)



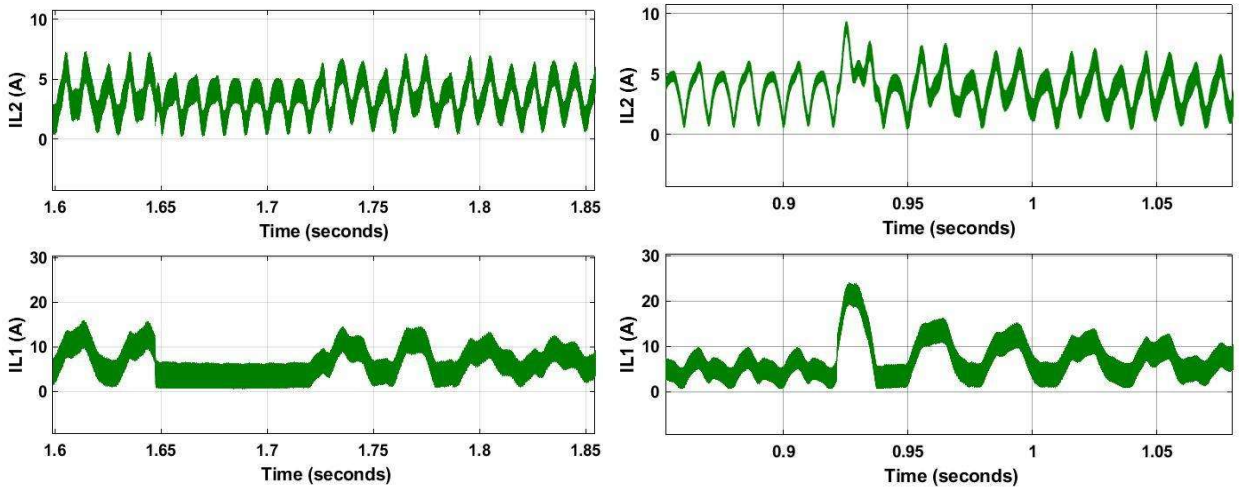
(d)

Fig. 4.16 Response to step-up in duty ratio. **(a)** DC output voltage with respect to change in duty ratio, **(b)** AC output voltage and current, **(c)** DC link voltage and **(d)** Reference signal for SPWM implementation.

The DC output voltage with respect to the step-up in D is shown in Fig. 4.16 (a). From Fig. 4.16 (a), it can be observed that the DC output voltage is stepped up at 0.92 sec and settles at 907 V within 0.3 sec, which verifies fast dynamic response of the controller during step-up operation of D. Also, it can be noticed from Fig. 4.16 (a) that the proposed TLIHC has no transient undershoot and ringing, when the D is increased. Fig. 4.16 (b) shows the AC output voltage and current of TLIHC during the step-up condition of D from 0.7 to 0.75. It can be observed from Fig 4.16 (b) that the AC output voltage has very little fluctuation in its peak magnitude due to stepping up of DC output voltage, which leads to a regulated AC output voltage of the proposed TLIHC. Fig. 4.16 (c) shows the DC link voltage variation due to sudden change in D. It can be observed from Fig. 4.16 (c) that the DC link voltage has been stepped up at 0.92 sec and settles at 680 V within 0.3 sec. Fig. 4.16 (d) shows the reference signal for the generation of switching pulses of the inverter side switches of TLIHC. It is observed that the reference signal is slightly increased during the sudden change in D or DC reference voltage. As the inverter input voltage $V_{inv} = \frac{V_{in}}{D}$ is decreased due to increase in D, the M_i of TLIHC is slightly increased to make the AC output voltage same.

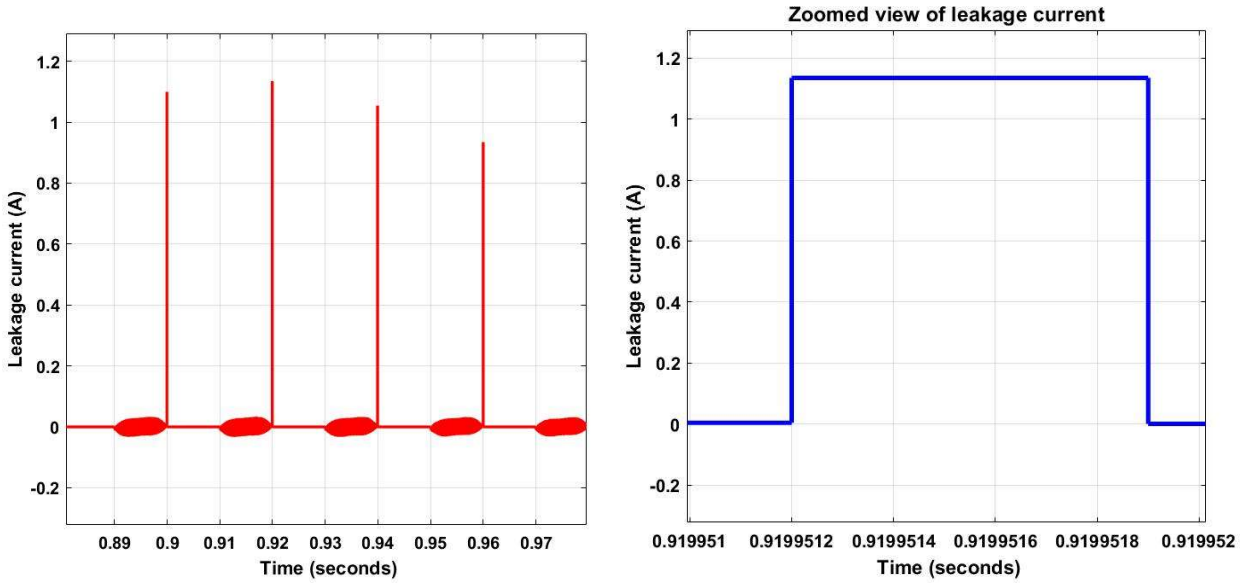
Fig. 4.17 shows the magnetically coupled inductor currents I_{L1} and I_{L2} during the sudden change in D or DC reference voltage. Fig. 4.17 (a) shows the magnetically coupled inductor currents during the step-down condition of D. Fig. 4.17 (b) shows the behaviour of I_{L1} and I_{L2} for the step-up condition of D. It is observed from Fig. 4.17 that both the currents decrease during the step-down condition of D and increase during the step-up condition of D. It is also observed that the

current I_{L1} is more affected than I_{L2} during the transition period, both in step-down and step-up conditions of D.



(a) **(b)**

Fig. 4.17 Input side magnetically coupled inductor currents (I_{L1} and I_{L2}). **(a)** Response to step-down in duty ratio and **(b)** Response to step-up in duty ratio.



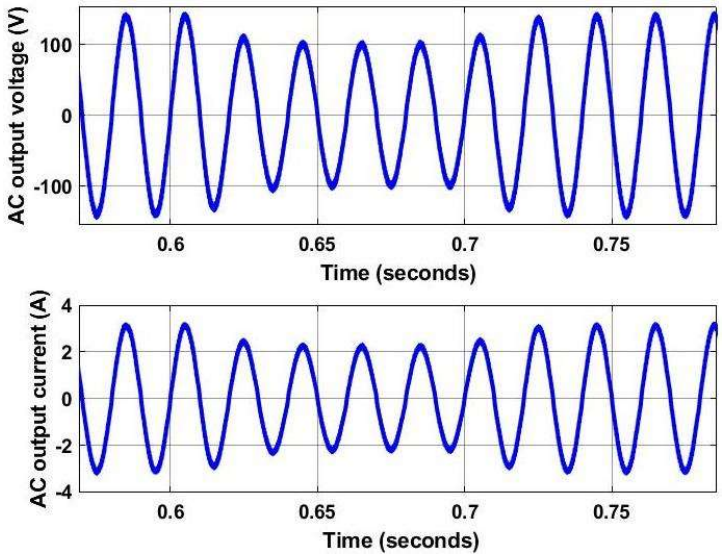
(a) **(b)**

Fig. 4.18 Leakage current profile of TLIHC. **(a)** Leakage current during the close loop operation and **(b)** Zoomed view of leakage current at the peak magnitude instant.

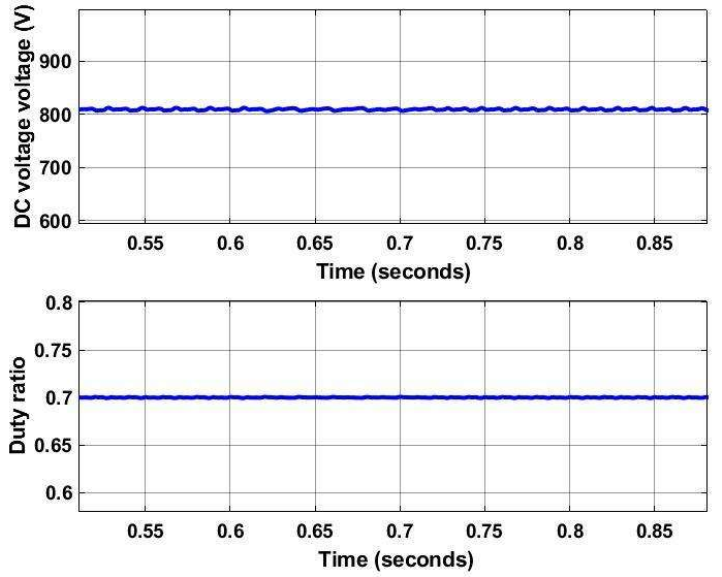
Fig 4.18 (a) shows the leakage current profile of the proposed TLIHC during the close loop operation. From the leakage current profile, it can be observed that the average value of the leakage

current is below 50 mA. Fig 4.18 (b) shows the zoomed view of leakage current at the peak magnitude instant. From Fig. 4.18 (b), it can be observed that the duration of peak magnitude leakage current is well below the safety standards (300 mA of leakage current for ≥ 0.3 sec).

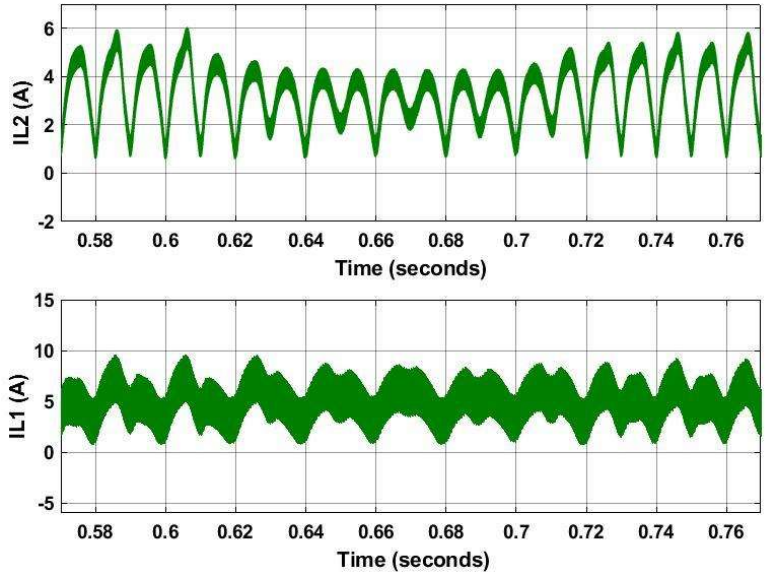
Fig. 4.19 shows the close loop performance of TLIHC for change in AC reference voltage. In Fig. 4.19 (a), the AC output voltage has been stepped down from 140 V (peak) to 100 V (peak) at 0.612 sec and then again stepped up to 140 V (peak) at 0.7 sec. From Fig 4.19 (a) it can be observed that the AC output voltage and current maintain smooth transition during the step-up and step-down operation with fast dynamic response and low settling time.



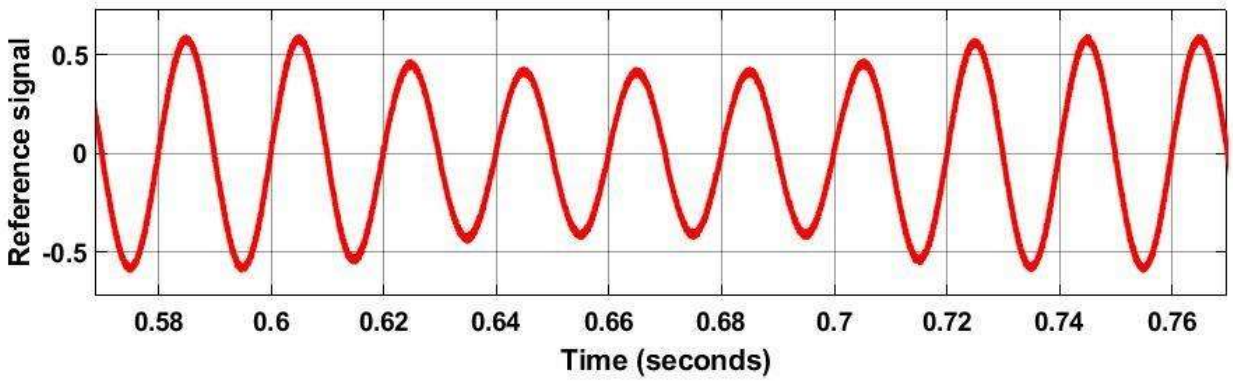
(a)



(b)



(c)



(d)

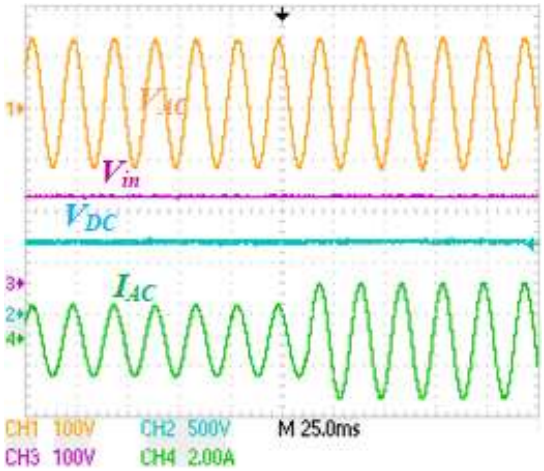
Fig. 4.19 Step-down and step-up of AC output voltage of TLIHC. **(a)** AC output voltage and current profile, **(b)** DC output voltage and duty ratio, **(c)** Input side magnetically coupled inductor currents and **(d)** Reference signal for SPWM technique implementation.

Fig. 4.19 (b) shows the DC output voltage and duty ratio of the proposed TLIHC during both step-down and step-up operation of AC output voltage. As the DC gain of TLIHC is depend on D and during the entire step-down as well as step-up operation of AC output voltage D is constant, the DC output voltage remains unchanged during the operation. Fig. 4.19 (c) shows the input side inductor currents (I_{L1} and I_{L2}) during the step-down and step-up operation of AC output voltage. It can be observed from the figure that the inductor currents slightly decrease during the step-down operation and increase during the step-up operation. Fig. 4.19 (d) shows the reference signal for implementation of SPWM technique in the proposed TLIHC. It can be observed that the reference

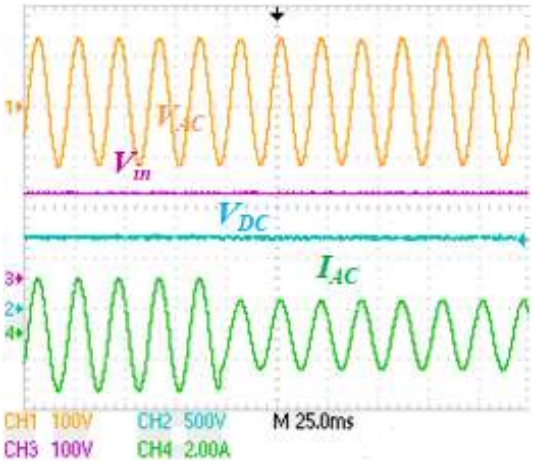
follows the AC output voltage paten for the smooth operation of TLIHC during the step-down and step-up operation of AC output voltage.

4.5.2 Experimental Verification of Cross Regulation Behaviour

The DC output of the proposed TLIHC can be controlled independently using the control parameters D, whereas the AC output can be controlled mainly by using the control parameter M_i. Fig. 4.20 shows the dynamic response of the proposed TLIHC during a step change in loads in case of either outputs (DC and AC). The AC controller is subjected to step increase in the load of 50% as shown in Fig. 4.20 (a). From the Fig. 4.20 (a), it can be observed that the AC current settles to a steady state value instantly, whereas the DC voltage and AC voltage are constant regardless of AC load current. The similar kind of response can be achieved, even when the AC controller is subject to a step decrease in load current of 50% as observed from Fig. 4.20 (b). This concludes that the controller is able to stabilize in both types of load variations and also it is able to cross-regulate among different quantities. Further, the DC voltage controller is subjected to step increase in the load of 50% as shown in Fig. 4.20 (c). It can be observed from Fig. 4.20 (c) that the DC voltage as well as the current settles to their steady state value within 2.5 ms, whereas the AC output voltage and current are undisturbed. Similarly, for 50% step-down loading, the DC output voltage settles within 2 ms, whereas the AC output voltage is undisturbed as observed from Fig. 4.20 (d). This feature depicts the superior cross-regulation behaviour of DC and AC voltages in the case of the proposed TLIHC.



(a)



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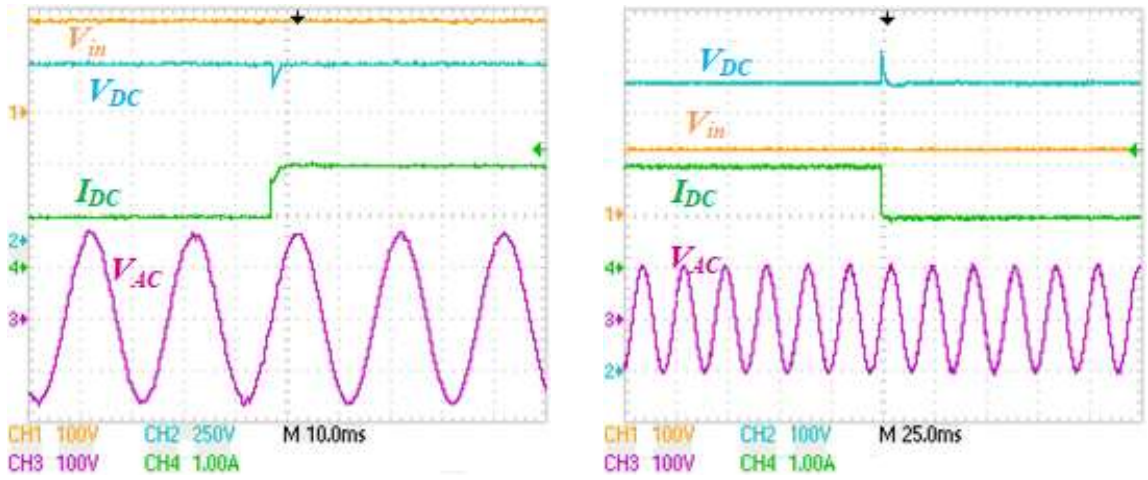
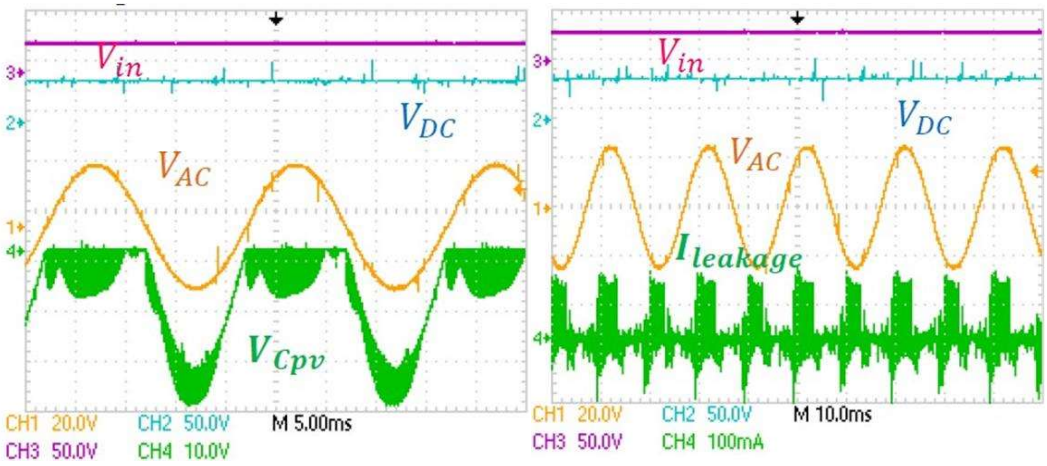


(c) **(d)**

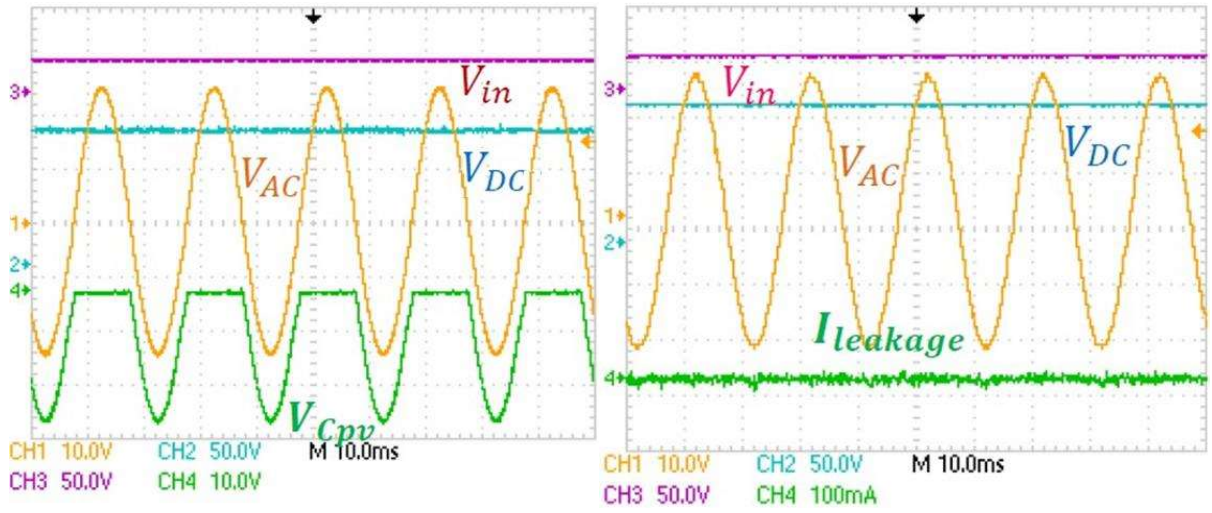
Fig. 4.20 Dynamic response of the proposed TLIHC **(a)** 50% step-up in AC load, **(b)** 50% step-down in AC load, **(c)** 50% step-up in DC load and **(d)** 50% step-down in DC load.

4.5.3 Leakage Current Comparison

For the leakage current comparison, between the proposed TLIHC and other conventional hybrid converters, a boost derived hybrid converter (BDHC) is considered. Fig. 4.21 shows the experimental results of the proposed TLIHC and the BDHC. It can be observed from Fig. 4.21 (a) that BDHC has pulsating (high frequency) common mode voltage (V_{Cpv}) across C_{PV}, which results in high leakage current, as shown in Fig. 4.21 (b). It can be noticed from Fig. 4.21 (c) that the proposed TLIHC has no high frequency components in V_{Cpv}, which results in low leakage current as shown in Fig. 4.21 (d). Thus, the proposed TLIHC has reduced leakage current as compared to BDHC.



(a) **(b)**



(c) **(d)**

Fig. 4.21 Experimental results of **(a)** V_{Cpv}, V_{in}, V_{DC}, and V_{AC} in the BDHC, **(b)** $I_{leakage}$, V_{in}, V_{DC}, and V_{AC} in the BDHC, **(c)** V_{Cpv}, V_{in}, V_{DC}, and V_{AC} in the proposed TLIHC and **(d)** $I_{leakage}$, V_{in}, V_{DC}, and V_{AC} in the proposed TLIHC.

4.6 Summary

In this chapter, the controller behaviour and dynamic response of TLIHC has been verified to check the robustness and performance of the controller. The performance of the designed controller has been verified by changing various passive parameters (inductor and capacitor) of the proposed TLIHC. Detailed mathematical modelling of AC side controller of TLIHC in terms of $d-q$ synchronous rotating frame control strategy has been discussed. The close-loop simulation and experimental verifications has been carried out for validating the performance of the proposed TLIHC. All the circuit operating features of TLIHC such as wide operating range of D and M_i simultaneously, minimum phase behaviour, well-regulated AC and DC outputs and minimization of common mode leakage current well below the safety limit have also been verified for the closed-loop operation. Further for dynamic load conditions, the cross-regulation behaviour of TLIHC has been verified. Additionally, a comparison between the proposed TLIHC and BDHC in terms of common mode leakage current and voltage across the PV panel to ground parasitic capacitance has been observed through experimental results.