# CHAPTER-1

## Introduction

## 1.1 Thesis Abstract

As the world progresses toward next-generation computing, achieving faster data processing and higher integration density while maintaining power efficiency remains challenging. Device scaling has been utilized in the complementary metal-oxide-semiconductor (CMOS) technology to improve performance, such as dynamic power dissipation, chip area, and delay. However, further miniaturization of devices introduces short-channel effects, resulting in substantial static leakage power. Consequently, researchers are seeking innovative alternatives to conventional CMOS technology that can overcome these scaling limitations to enhance computational performance.

Spintronics is an emerging field in modern memory and computing technology that utilizes the spin of electrons and their associated magnetic moments to store information. Unlike conventional CMOS technology, which relies on the charge of electrons that depreciates due to static leakage current. Spintronics involves the magnetization state to represent binary data that can be retained almost indefinitely without a continuous power supply in spintronics-based circuits and memory, offering non-volatility. Furthermore, the magnetization state can be switched in the low energy budget through the spin transfer torque (STT) switching mechanism. Due to these advancements, the researchers have started to focus on the development of a spintronics device such as magnetic tunnel junction (MTJ) based computing architectures, which offer negligible static leakage, non-volatility, faster data processing, and higher integration density.

This thesis work pursues two main objectives: device modeling and logic circuit design for spin-based computing. Firstly, we developed a SPICE compatible STT-MTJ compact model, accurately capturing both tunnel magnetoresistance (TMR) and tunnel

magnetocapacitance (TMC) phenomena, which are essential for simulating next-generation spin-based devices and circuits. Further, we also develop an advanced micromagnetic simulation framework based on the non-equilibrium Green's function (NEGF) formalism to analyze the STT switching behaviour in MTJ devices. Secondly, we designed a novel STT-MTJ-based non-volatile latch with an auto-write termination (AWT) circuit, which eliminates redundant writing of the MTJ and stops the write operation once it is complete. This design enhances reliability, reduces area, and minimizes power dissipation. The simulations presented in this thesis were conducted using NGSPICE, HSPICE, Magic IC Layout, and OOMMF simulation tools. The thesis is organized into five chapters as follows:

***Chapter 1*** introduces the spintronics device, specifically the MTJ, highlighting its advantages in next-generation memory and computing technology. This chapter includes details on the remarkable properties of the MTJ device and explains its basic physics, including key properties such as MTJ structure, magnetic anisotropy, TMR, TMC, and STT switching techniques. Additionally, the chapter reviews the literature on device modeling and logic circuits, including compact modeling of MTJs, micromagnetic simulation frameworks that analyze the STT switching behaviour in MTJ devices, and hybrid CMOS/MTJ circuits such as non-volatile latches, flip-flops, and AWT circuits. At the end of the chapter, a brief summary is presented to support the formation of the problem statement for the thesis work.

In the next chapter, ***Chapter 2***, we address the limitations of existing compact MTJ models that emulate the TMR effect and magnetization dynamics but lack the TMC effect. This chapter introduces a SPICE-based STT-MTJ compact model that incorporates both TMR and TMC effects. The voltage-induced TMC effect is modeled using a combination of the Debye-Fröhlich model, Zhang-sigmoid theory, parabolic barrier approximation, and

spin-dependent drift-diffusion model, which accurately emulates magnetocapacitance behaviour of MTJ device across different frequencies. The proposed model is validated through HSPICE simulations, showing good agreement with experimental data.

***Chapter 3*** presents an advanced micromagnetic simulation framework utilizing the NEGF formalism for modeling STT-MTJ devices. This simulation framework combines the TCL-based NEGF model for spin transport with the micromagnetic simulations for magnetization dynamics, enabling comprehensive analyses of the STT switching behaviour in MTJs.

In the next chapter, ***Chapter 4***, we propose an STT-MTJ-based non-volatile latch with an AWT feature. This latch has a simple structure, improved stability, higher speed, and seamless integration with CMOS logic styles. It eliminates the need for an additional write driver circuit, resulting in a smaller footprint during MTJ writing. Consequently, the proposed latch consumes less power compared to previous designs, using fewer transistors for write operations and logic implementation. The AWT circuit continuously monitors the write operation, prevents redundant MTJ writing, and removes excessive write current flow, thereby saving power.

In ***Chapter 5***, the thesis is concluded while highlighting the significant contributions and a summary of the results achieved in this research work. This chapter also contains the future scope of the thesis work.

## 1.2 Introduction

Spintronics is an emerging field in modern memory and computing technology that utilizes the spin of electrons and allied magnetic moments to store information. The conventional CMOS technology relies on the charge stored in capacitive nodes that depreciates due to static leakage current [1], [2], [3], [4], [5], [6], [7], [8], [9], [10]. Modern spin-based devices

and memories depend on the Giant magnetoresistance (GMR) effect discovered by Albert Fert and Peter Grünberg in 1988 [11], [12], for which they were awarded the Nobel Prize in Physics in 2007. The GMR effect is observed in two ferromagnetic (FM) layers separated by a non-magnetic (NM) layer, demonstrating a significant difference in resistance between parallel (P) and antiparallel (AP) magnetization alignments of FM layers. The overall resistance in P alignment is relatively lower than that in AP alignment, and such a device is commonly known as a spin valve [13]. The discovery of GMR has greatly gleaned interest in magnetoresistive-based memory, *i.e.*, magnetoresistive random access memory (MRAM). Early MRAMs were based on magnetic field-assisted switching, which faced scaling issues due to the need for a long-range Oersted field to alter the magnetization of the FM layer. In the year 1996, J. C. Slonczewski theoretically predicted the spin transfer torque (STT) switching to alter the magnetization of the FL [14], [15], a significant step in spintronics that was later experimentally confirmed as an efficient technique over magnetic field-based switching of magnetization of FM layer. Nowadays, STT-MRAMs are seen as promising candidates for memory and computing applications due to their additional CMOS properties like zero standby power and non-volatility. They also offer high density through the three-dimensional (3D) integration of magnetic tunnel junctions (MTJs) with CMOS technology [16]. MTJs have evolved as an advancement over the spin-valve devices wherein the non-magnetic (NM) layer is an insulator. STT-MRAM stored logic data as a resistance state determined by the magnetization alignment of FM in the MTJs. Recent advancements in MTJs have led to the development of high-quality epitaxial CoFeB/MgO/CoFeB stacked structures switched by STT [17], [18], [19], [20], [21], [22]. Ongoing research focuses on enhancing energy efficiency through material [23] and process [24] innovations. MTJs have also demonstrated

potential in applications beyond memory, such as oscillators [25], [26], [27], [28] and neuromorphic computing [29], [30], [31], highlighting their worth for future computing technologies. Therefore, this chapter introduces the work carried out in this thesis. Starting with basic concepts and device physics, it moves towards advanced applications of STT-MTJ and provides an outlook of cutting-edge technology.

This chapter aims to enlighten readers about STT-based MTJ devices, compact modeling, circuits, and memory. It is organized as follows: section 1.3 provides the background and motivation for the research. Section 1.4 offers a brief discussion on magnetization, spin polarization, and spin filtering. Section 1.5 discusses the structure and working principles of the MTJs. In Section 1.6, STT magnetization switching techniques used to flip the magnetization alignment of the FL in MTJs are discussed. Section 1.7 gives an overview of the MTJ device modeling. Hybrid CMOS/MTJ-based logic-in-memory (LiM) circuits are covered in Section 1.8. finally, Section 1.9 addresses the problem statement of the thesis.

## 1.3 Background and Basic Concepts of Spintronics

In conventional electronics, the charge of the electrons is utilized to store and process analog and digital information. In contrast, spintronics leverages the quantum mechanical spin of an electron. The spin of an electron generates a magnetic moment opposite to its spin angular momentum, making each electron as a tiny magnet with an associated magnetic moment, as illustrated in **Figure 1.1**. The relationship between the magnetic moment and angular momentum is given by:

$$\vec{\mu} = -\frac{g_e \mu_B}{\hbar}\vec{L} = \gamma\vec{L} \qquad 1.1$$

For electrons, the direction of magnetic moment is opposite to the spin angular momentum

[32]. Both quantities are vector quantities, typically represented with an arrow. The factor "$-\frac{g_e \mu_B}{\hbar}$" is known as the gyromagnetic ratio ($\gamma$) for an electron. Here, $\mu_B$ represents the Bohr's magneton, and $g_e$ is the electron g-factor, which is a constant with a value of '2' for electrons.

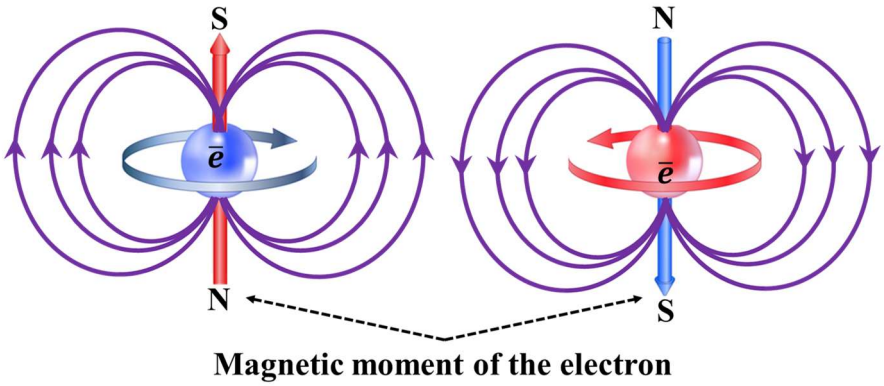



**Figure 1.1** Spin magnetic moment of an electron

The concept of modern magnetic memories, such as MRAM, originates from the discovery of the Giant Magnetoresistance (GMR) effect, which revolutionized the field of spintronics and nanoscale data storage. GMR was observed in a layered structure known as a spin valve [13], which consists of a non-magnetic (NM) layer sandwiched between two ferromagnetic (FM) layers, as shown in **Figure 1.2**. It was found that when the magnetization states of the FM layers are anti-parallel (AP), the structure exhibits a higher resistance compared to when the magnetization states are parallel (P). Quantitatively, GMR is defined as the normalized difference in the total resistance of the P and AP state of the spin valve structure. It is mathematically represented as:

$$GMR = \frac{R_{AP} - R_P}{R_P} \times 100\% \qquad 1.2$$

where $R_P$ represents the low resistance when the magnetization states are parallel, and $R_{AP}$ represents the high resistance when the magnetization states are anti-parallel. To store data

in GMR devices, the magnetization of one FM layer, known as the pinned layer (PL), is kept fixed by providing it with high magnetic coercivity. In contrast, the second FM layer, referred to as the free layer (FL), has low magnetic coercivity, enabling its magnetization to switch freely.

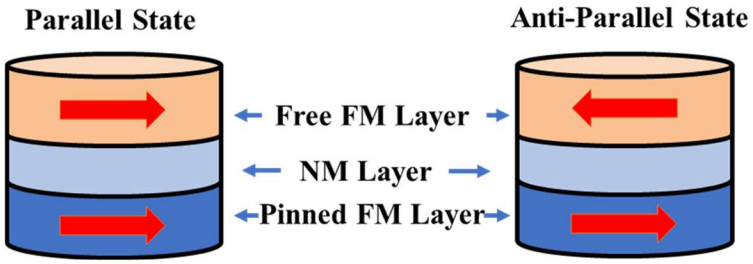



**Figure 1.2** Magnetization states of a GMR spin valve device (a) P states (b) AP states.

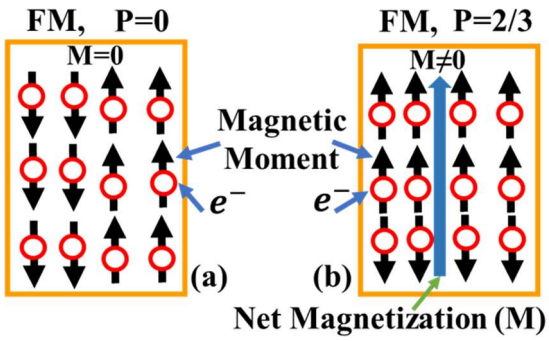
The GMR effect was a relatively weak phenomenon that encouraged to the development of an advanced device known as the magnetic tunnel junction (MTJ). In MTJs, a similar resistance change with respect to the magnetization of FM layers was observed, termed as tunnel magnetoresistance (TMR) [33]. This development resulted in the invention of magnetoresistive random access memories (MRAMs) [34], which store data as the resistance state of an MTJ. MTJ devices have grown over the years to become a much more energy-efficient alternative due to the electrical control of magnetization of the MTJ through spin-polarized current. This innovation has enabled the development of fast and low-power memories using STT switching [14], known as STT-MRAM. Further advancements in MRAM technology have been driven by other switching techniques such as spin Hall effect (SHE) [35], [36], SHE-assisted STT [37], [38], spin-orbit torque (SOT) [39], [40], [41] and voltage-controlled magnetic anisotropy (VCMA) [42], which offer even higher speed and low power that enhance the potential of MRAMs in modern memories and logic-in-memory (LiM) computing applications.

## 1.4 Magnetization, Spin Polarization, and Spin Filtering

In FM materials, inherent spin polarization exists at equilibrium because of the unpaired electrons in the d-subshell. These unpaired electrons contribute to individual magnetic moments, as depicted in **Figure 1.3**. The vector sum of these individual magnetic moments produces a total resultant magnetic moment. The magnetization of an FM layer is defined as the net magnetic moment of these bound orbital electrons per unit volume.

$$\vec{M} = \frac{\left(\sum_{i=1}^{N} \vec{\mu_i}\right)}{Volume} \qquad 1.3$$

where $\vec{\mu_i}$ represents the individual magnetic moments of bounded electrons and $N$ is the total number of orbital electrons.




(a) (b)

**Figure 1.3** (a) Net magnetization (M) and inherent spin polarization (P) in the FM material, (a) M=0 and P=0, and (b) M≠0 and P≠0.

The bound electrons interact with free electrons through magnetic moment exchange. In this process, the spin magnetic moment of the free electrons is polarized in the direction of the bulk magnetization; this phenomenon is known as spin filtering, shown in **Figure 1.4**. This can be compared to a filter that selectively allows either up-spin or down-spin electrons, rejecting the opposite spin orientation. As a result, the electron population predominantly consists of either up-spin or down-spin electrons. **Figure 1.4** further explains the concept of

majority (up-spin) and minority (down-spin) spins and the spin filtering mechanism. The current generated in this process is known as spin-polarized current, and its strength ($I_S$) is defined as follows:

$$I_S = I_\uparrow - I_\downarrow = PI_C \tag{1.4}$$

where, $I_{\uparrow(\downarrow)}$ represents the current due to up(down)-spin electrons, $I_C$ is the charge current through the FM material, and $P$ represents the spin polarization factor of the FM. When $I_\downarrow = I_\uparrow$, $P = 0$, This shows the characteristics of an NM material that lacks a dominant spin orientation.

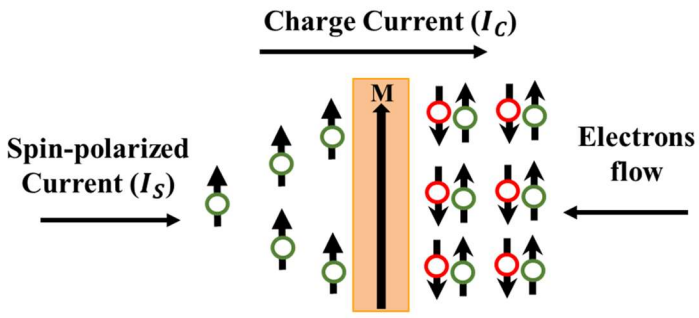



**Figure 1.4** Illustration of spin filtering mechanism

In terms of energy band diagrams, the generation of a net magnetic moment in FM materials arises from the unequal distribution of up-spin and down-spin electrons near the Fermi energy level [43]. The inherent spin polarization (P) of FM materials is defined as follows:

$$P = \frac{N_\uparrow - N_\downarrow}{N_\uparrow + N_\downarrow} \tag{1.5}$$

Here, $N_\uparrow$ and $N_\downarrow$ denote the number of up-spin and down-spin electrons at the Fermi energy, respectively. **Figure 1.5(a)** illustrates the energy versus density of states (DOS) curve for a typical FM material. At equilibrium, there are more up-spin electrons near the Fermi energy compared to down-spin electrons. Since electrons near the Fermi energy are primarily responsible for current conduction in electronic devices, the majority spin electrons will

contribute more to current conduction than the minority spin electrons when a potential is applied. In NM materials, the concentrations of up-spin and down-spin electrons at the Fermi energy level are equal, as shown in **Figure 1.5(b)**. It means that when a charge current passes through an NM material, it generates equal concentrations of up-spin and down-spin electrons, *i.e.*, $N_{\uparrow} = N_{\downarrow}$, $P_N = 0$.

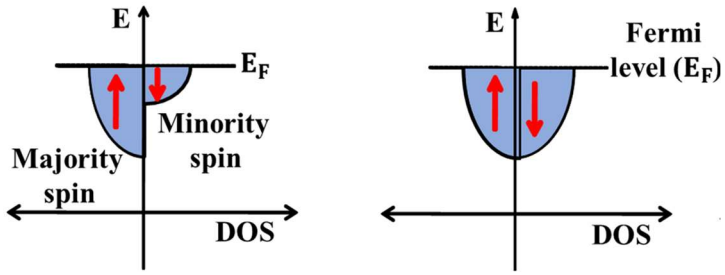



**Figure 1.5** Energy band structure (Energy vs DOS) of (a) FM (b) NM.

## 1.5 MTJ Structure and Working Principle

An MTJ is a multilayered structure with a thin insulating layer, known as the tunnel barrier (TB), positioned between two FM layers. One of these FM layers, referred to as the pinned layer (PL), has a fixed magnetic orientation, which is stabilized by a synthetic antiferromagnetic (SAF) layer positioned beneath it. The other FM layer, called the free layer (FL), can switch its magnetic orientation to either P or AP with respect to the PL. The magnetic orientation of the FL can be changed by applying an external magnetic field or a suitable switching technique. When the magnetization orientation of the FL is parallel with the PL, the device exhibits low resistance, termed parallel resistance ($R_P$). Conversely, when the magnetization orientation of the FL is antiparallel to the PL, the device shows high resistance, termed antiparallel resistance ($R_{AP}$). Based on the magnetic anisotropy direction, MTJ is classified into in-plane MTJ (iMTJ) and perpendicular MTJ (pMTJ), as illustrated in **Figure 1.6(a)** and

**Figure 1.6(b)**, respectively. **Figure 1.6(c)** depicts the typical R-H curve of the pMTJ [34], showing the two stable resistance states: low resistance ($R_P$) and high resistance ($R_{AP}$) due to the TMR effect. In this context, $R_P$ represents the stored logic '1', while $R_{AP}$ represents the stored logic '0'. The energy band diagram of the pMTJ is presented in **Figure 1.6(d)** [30], showing the energy barrier ($E_b$) that separates the P and AP states, and its height determines the stability of these states [44]. The resistance variation between these states can be quantified by the TMR ratio using equation 1.6 [44].

$$TMR = \frac{R_{AP}-R_P}{R_P} \times 100\% \qquad 1.6$$

Here, $R_{AP}$ and $R_P$ represent the resistances in the AP and P states, respectively. The TMR ratio of an MTJ is influenced by its shape, size, thickness, and the materials used in the tunnel barrier, etc. Achieving a high TMR is crucial for sensing the MTJ state in hybrid CMOS/MTJ circuits and non-volatile memories.

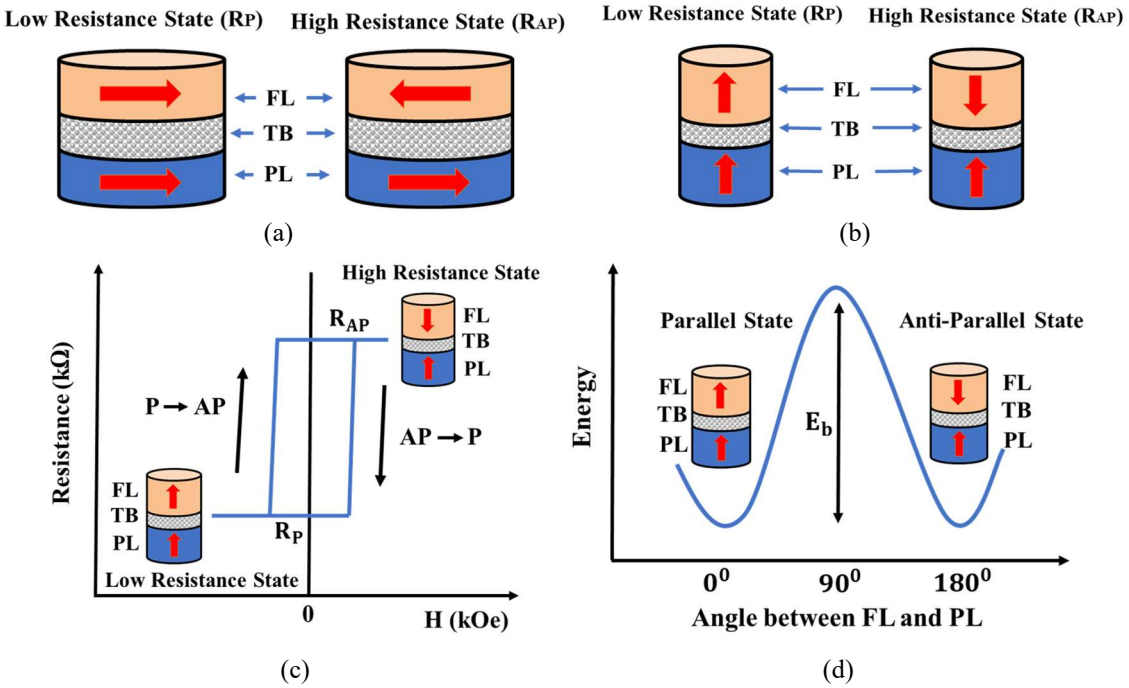



**Figure 1.6** Illustration of (a) iMTJ, (b) pMTJ, (c) R-H curve of pMTJ, (d) Energy band diagram for pMTJ.

### 1.5.1. Magnetic Anisotropy in Thin Film MTJ Devices

The performance of the spintronics device and system is influenced by the sensitive properties of thin film FL. A key property of magnetic materials is their easy axis, or anisotropy direction [45], which represents the direction of minimum energy. The magnetization direction in the magnetic materials is determined by magnetic anisotropy (MA), which provides an easy axis along which the magnetization can easily be aligned. It is classified into two types based on the alignment of the easy axis, *i.e.*, in-plane magnetic anisotropy (IMA) and perpendicular-plane magnetic anisotropy (PMA). In the case of IMA, the easy axis of the magnetic material is parallel to its plane, resulting in-plane MTJ (iMTJ). On the other hand, PMA tries to align the magnetization perpendicular to the plane of the magnetic material, resulting in perpendicular MTJ (pMTJ). PMA is further classified based on its origin: interfacial PMA (iPMA) that occurs in materials like CoFeB when the thickness of FL is below a critical thickness ($t_C$), while crystalline PMA (cPMA) is found in materials such as CoPt and FePd due to their high crystalline anisotropy [46], [47]. Further, the easy and hard axes in the thin film FL can be distinguished using hysteresis loops of the magnetic material. When a magnetizing field (H) is applied along the easy axis (at 0 or 180 degrees), the material achieves saturation magnetization with relative ease. Conversely, a much higher magnetic field (H) is needed to approach saturation magnetization along the direction perpendicular to the easy axis, known as the hard axis, as shown in **Figure 1.7** [48].

The shape and the material to design the MTJ for the memory or hybrid CMOS/MTJ circuits must ensure that it can maintain its magnetization state for several years. MA is crucial for creating hysteresis in the FL layer and should be high enough for long-term data retention. However, since the magnetization of FL needs to switch to '0' and '1' states during

write operation, the anisotropy should not be excessively high to allow for efficient magnetization switching.

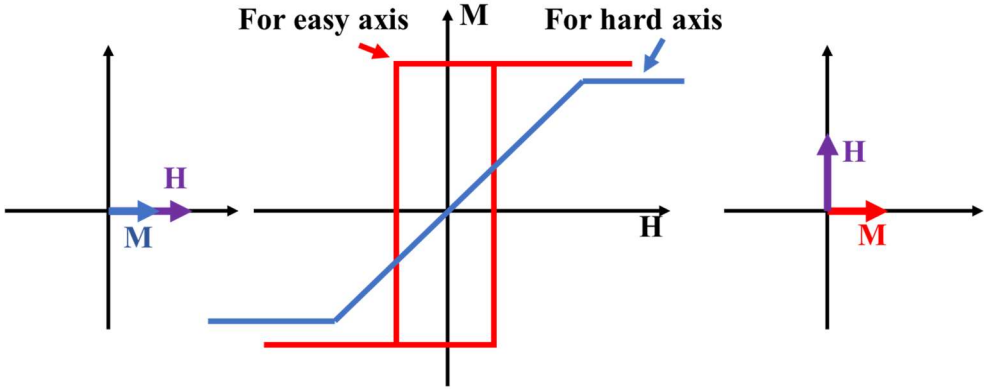



**Figure 1.7** Hysteresis loops along the hard and easy axis for a thin FL layer

Mathematically, the effective magnetic anisotropy field is expressed as [49]:

$$H_{eff} = \frac{2K_{eff}}{M_S} \tag{1.7}$$

$$K_{eff} = 2\pi(N_{dy} - N_{dx})M_s^2 + K_b + \frac{K_i}{t_{FL}} - 2\pi N_{dz}M_s^2 \tag{1.8}$$

where, $M_S$ represents the saturation magnetization, $K_i$ is the interfacial anisotropy density, $K_b$ is the bulk anisotropy density related to bulk PMA devices, $t_{FL}$ is the thickness of the FL, and $K_{eff}$ is the effective magnetic anisotropy energy density, which is the sum of the IMA and PMA energy densities. The magnetization of the FL layer is in-plane when $K_{eff} < 0$ and perpendicular-plane when $K_{eff} > 0$, depending on $t_{FL}$ and the shape-dependent demagnetization coefficients ($N_d$), as illustrated in **Figure 1.8**. To achieve interfacial PMA in the FL, $t_{FL}$ should be less than the critical thickness ($t_C$) *i.e.*, $t_{FL} < t_C$ as shown in **Figure 1.9**. The critical thickness ($t_C$) for the FL layer is expressed as

$$t_c = -\frac{2K_i}{K_b - \frac{1}{2}\mu_0 M_S^2} \tag{1.9}$$

In recent years, pMTJs have garnered significant interest from researchers due to their low

power switching and high scalability. Experimental results by Ikeda *et al.* [17] demonstrate that a stronger PMA is achieved with a thinner FL.

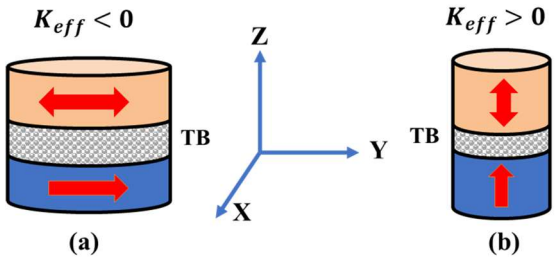



**Figure 1.8** MTJ structures based on magnetic anisotropy (a) In-plane MTJ and (b) perpendicular-plane MTJ

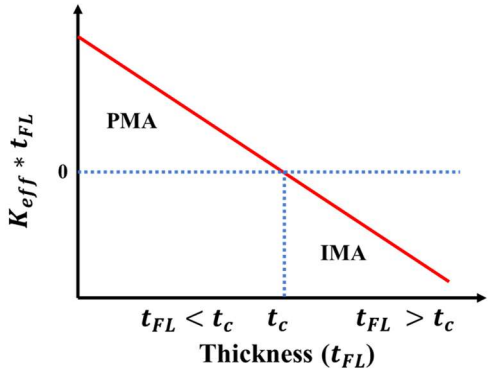



**Figure 1.9** Change in magnetic anisotropy with the thickness of the FL layer

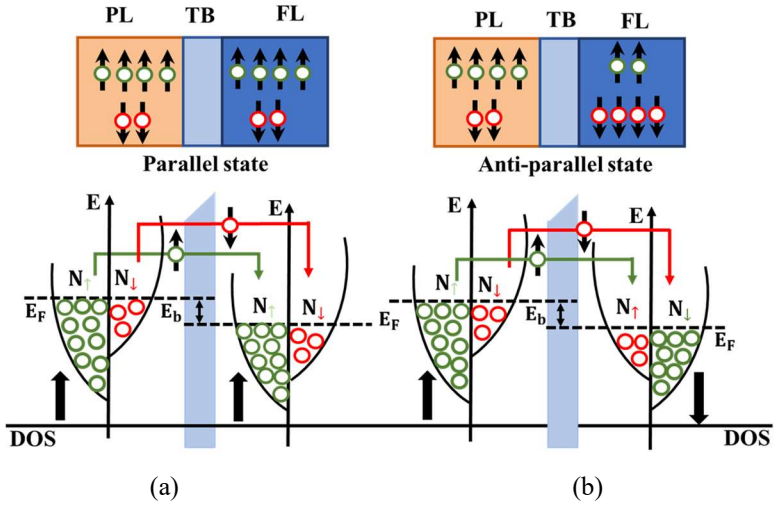



**Figure 1.10** Schematic representation of TMR effect in MTJ [17]. (a) Tunneling of electrons in P state from PL to FL layer (b) Tunneling of electrons in AP state from PL to FL layer.

### 1.5.2. Tunnel magnetoresistance effect in MTJ devices

The tunneling magnetoresistance (TMR) ratio is defined similarly to GMR, which is

measured by the difference in resistance between the P and AP magnetic states in MTJs. TMR arises from the tunneling of electrons through an insulating TB between the PL and the FL. During this process, electrons with specific spin orientations tunnel through the barrier if there are available states with the same spin orientations on the other side. The conductance is proportional to the product of the Fermi level density of states (DOS) of both FM layers. The expression for the conductance in the parallel state ($G_P$) and conductance in the anti-parallel state ($G_{AP}$) is given by [50]:

$$G_P \propto N_P^{\uparrow}.N_F^{\uparrow} + N_P^{\downarrow}.N_F^{\downarrow} \quad 1.10$$

$$G_{AP} \propto N_P^{\uparrow}.N_F^{\downarrow} + N_P^{\downarrow}.N_F^{\uparrow} \quad 1.11$$

Here, $N_P^{\uparrow}(N_P^{\downarrow})$ and $N_F^{\uparrow}(N_F^{\downarrow})$ is the number of DOS for up-spin (down-spin) electrons in the pinned and free layer of the FM materials in the MTJ. In the P state, as shown in **Figure 1.10(a)**, the majority up-spin electrons ($N_P^{\uparrow}$) and the minority down-spin electrons ($N_P^{\downarrow}$) of the PL can easily tunnel through the TB to the FL layer with majority up-spin ($N_F^{\uparrow}$) and minority down-spin ($N_F^{\downarrow}$) electrons, respectively. This results in high conductance or low resistance. In contrast, in the AP state shown in **Figure 1.10(b)**, the majority of up-spin electrons ($N_P^{\uparrow}$) and minority down-spin electrons ($N_P^{\downarrow}$) of the PL tunnel through the TB with difficulty in filling the same spin orientations minority up-spin ($N_F^{\uparrow}$) and majority down-spin ($N_F^{\downarrow}$) electrons of the FL layer, lead to the low conductance or large resistance. Therefore, in the P state, electrons encounter low resistance ($R_P$) compared to the resistance ($R_{AP}$) in the AP state. This illustrates that the TMR effect is strongly dependent on spin polarization. TMR quantifies the difference between $R_P$ and $R_{AP}$. The conductance of the parallel and antiparallel configurations can be expressed as $G_P = 1/R_P$ and $G_{AP} = 1/R_{AP}$. The TMR can be

written as

$$TMR = \frac{G_P - G_{AP}}{G_{AP}} = \frac{R_{AP} - R_P}{R_P} \quad 1.12$$

The $R_P$ and $R_{AP}$ can be expressed in terms of spin polarization of FM layers as [44],

$$R_P = R_o \times \frac{2}{1 + P_P.P_F},\ R_{AP} = R_o \times \frac{2}{1 - P_P P_F} \quad 1.13$$

where $P_F$ and $P_P$ represent the spin polarization of both free and pinned layers, which can be calculated using equation 1.5. $R_0$ represents the factor of resistance), which depends on the various parameters of the MTJ, such as the area of the free layer, bias voltage, and temperature. Furthermore, the TMR can be expressed using equation 1.13 according to Jullière's model [33], [44],

$$TMR = \frac{2P_P P_F}{1 - P_P P_F} \times 100\% \quad 1.14$$

The tunneling of electrons between FM layers was first reported by Jullière in 1975 using a Fe/Ge/Co multilayer structure [33]. Due to experimental limitations, this discovery received little attention, and there was no significant high TMR values reported for the next 20 years. The TMR was first observed at room temperature by Moodera *et al.* and Miyazaki *et al*. using an AlOx barrier in 1995 [51], [52]. This breakthrough paved the way for the development of non-volatile memories and hybrid CMOS/MTJ circuits [53], [54].

### 1.5.3. Tunnel magnetocapacitance effect in MTJ devices

MTJs are promising for non-volatile memory and logic circuits in computing due to their significant TMR ratio at room temperature. However, maintaining TMR robustness against bias voltage is crucial for high magnetic sensitivity in MTJs [55], [56], [57]. It is well-known that TMR decreases with increasing bias voltage, reducing its sensitivity [58], [59]. This decline is attributed to hot-electron properties in the AP state of the two FM layers [58]. For

instance, MTJs with $Co_{70}Fe_{30}$ FM layers exhibit zero-bias TMR values of 377 % in MgO-based and 89 % in AlO-based MTJs, which drop to 75 % and 20 %, respectively, at a bias voltage of 0.5 V [60]. Improvements in bias-reduced TMR have been reported for MTJs with minimal lattice mismatch between the FM and insulating layers [61], [62], [63], [64], [65], [66]. Fully epitaxial Fe/MgO/GaOx/Fe MTJs show a zero-bias TMR of 92 %, with the half-bias voltage $V_{1/2}$ (the bias voltage at which the TMR is halved), increasing to 0.5 V, as shown in **Figure 1.11** [61]. Additionally, Fe/spinel $MgAl_2O_4$/Fe MTJs demonstrate a TMR of 117 % near zero bias and a large $V_{1/2}$ range of 1.0 to 1.3 V [62], [63], [64], [65]. Further advancements reveal a TMR of 240 % near zero bias, maintaining 180 % at 0.5 V in $MgAl_2O_4$-based MTJs [66]. Despite these improvements, bias voltage consistently reduces TMR, presenting an essential challenge in MTJ applications. Therefore, researchers are exploring alternative characteristics of MTJs that exhibit strong robustness against bias voltage.

To find alternatives to TMR in MTJs that are robust against bias voltage, researchers have extensively studied AC spin transport in MTJs. These studies, both theoretical and experimental [67], [68], [69], [70], [71], [72], [73], focus on the interesting spin phenomena exhibited by MTJs. These phenomena include frequency-dependent spin transport and spin capacitance, and potential applications in high-speed storage devices and high-frequency elements. One of the most attractive AC spin transport properties is tunneling magnetocapacitance (TMC), which complements TMR. TMC is actively investigated for its unique characteristics, such as high magnetic sensitivity, thermal stability, and robustness against bias voltage [69], [70], [71], [74], [75], [76], [77], [78].

First explored in $Co/Al_2O_3/Co$ MTJs in 2002 by H. Kaiju *et al*. [69], TMC has been found to depend on frequency, showing values as large as TMR at high frequencies. In the TMC

effect, capacitance is higher for the P state ($C_P$) of the MTJ rather than for the AP state ($C_{AP}$), *i.e.* $C_P > C_{AP}$. This behaviour is explained by the spin-injection accumulation model, where a large amount of charge accumulates at the interface between the FM layer and TB layer for the P state due to high conductance, while a small amount of charge accumulates for the AP state due to low conductance.

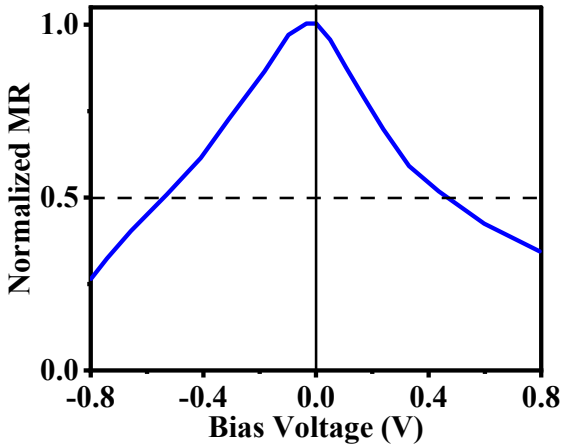



**Figure 1.11** Normalized MR with bias voltage at room temperature, reproduced from [61]

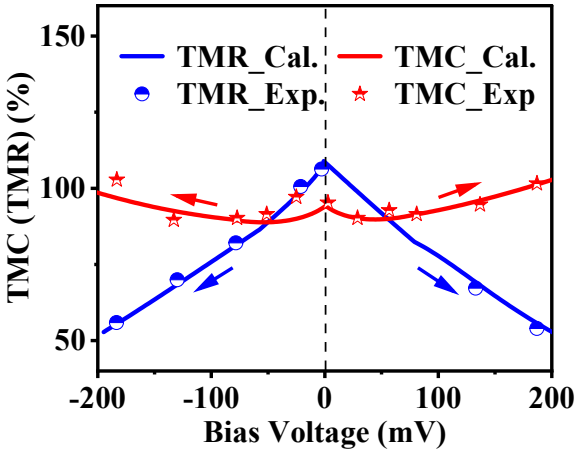



**Figure 1.12** Bias voltage dependence of TMC and TMR ratios, reproduced from [75]

The TMC ratio is defined as:

$$TMC = \frac{C_P - C_{AP}}{C_{AP}} \times 100\ \% \qquad 1.15$$

where, $C_{P(AP)}$ is the capacitance of the P (AP) state in MTJs. TMC can surpass TMR at

specific frequencies, which is effectively explained by the Debye-Fröhlich (DF) model. For instance, the maximum TMC in MgO-based MTJs has been reported to reach 155 %, compared to a TMR of 100 %. In this case, the DF model predicts that TMC could potentially achieve 1000 % [71]. Unlike TMR, TMC has been shown to be temperature-independent due to the presence of spin capacitance [74]. Moreover, TMC is more robust against biasing than TMR, with $V_{1/2}$ for TMC being nearly twice that of TMR in MgO-based MTJs [70]. Interestingly, a study in the literature [75] indicates that TMC slightly increases from 98 % to 102 % with biasing, while TMR decreases from 100 % to 50 %, as shown in **Figure 1.12**. Recent research also shows that TMC increases with bias voltage, in contrast to the general decrease observed in TMR. For example, a significant TMC ratio of 332 % has been observed at room temperature in MgO-based (001)-textured MTJs [76]. Further enhancements, surpassing 450 % at a low bias of 75 mV, have been achieved using epitaxial MTJs with a $MgAl_2O_4$(001) barrier [77], [78]. This substantial value of TMC is attributed to the highly effective tunneling spin polarization that results from excellent lattice matching at the FM and barrier interface. The DF model, incorporating the Zhang-sigmoid formula, parabolic barrier approximation, and spin-dependent drift-diffusion model, suggests that a TMC ratio of up to 1500 % could be achieved in MTJs with a spin polarization of 90 %. These findings motivate the researchers to develop new applications based on large TMC effects, such as multi-value memories, spin logic devices, magnetic sensors, and neuromorphic computing.

## 1.6 Magnetization switching techniques: Spin transfer torque switching

The magnetization state of the MTJ can be altered from P to AP or vice versa by switching the magnetization alignment of the FL, a process known as writing/storing data in the MTJ. Several techniques exist for achieving this, including field-induced magnetic switching

(FIMS), spin transfer torque (STT), spin-Hall effect (SHE), voltage-controlled magnetic anisotropy (VCMA), and spin-orbital torque (SOT). Among these, STT has gained the most widespread use due to its commercial viability.

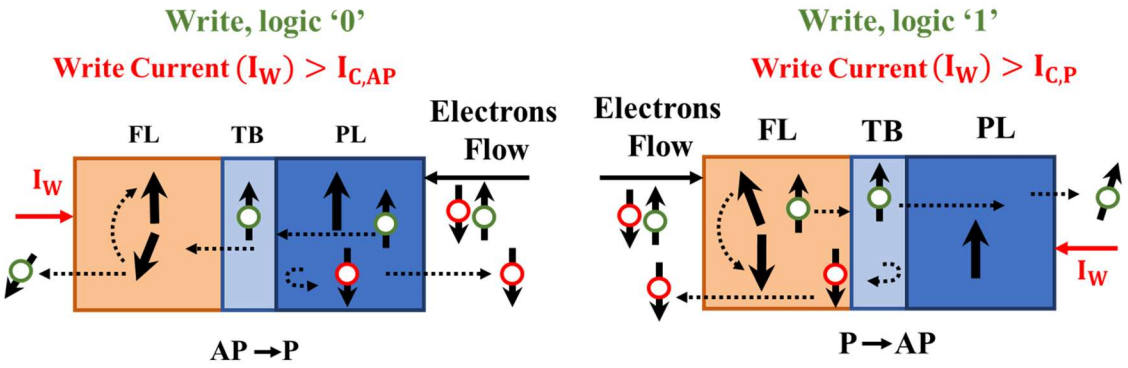



**Figure 1.13** Schematic representation of the STT switching (a) During the switching from AP to P states, when the current $I_W > I_{C,AP}$ flows from the FL to the PL, and the changes in the resistance to $R_P$ (b) Conversely, during the switching from P to AP states, when the current $I_W > I_{C,P}$ flows from the PL to the FL, and the changes in the resistance to $R_{AP}$.

Spin transfer torque was theoretically predicted independently by Slonczewski [14] and Berger [15] in 1996. It was later observed experimentally in 2004 in a low-resistance CoFeB/$Al_2O_3$/CoFeB MTJ structure [79]. STT switching is a current-induced magnetization switching (CIMS) approach, demonstrating significant improvements in speed and power dissipation compared to conventional field-induced switching. In the STT switching, a spin-polarized current is employed in the MTJ device to change the magnetic orientation of the FL. The magnetization of MTJ can also be switched from the AP state to the P state or vice versa by passing a write current ($I_W$) which exceeds the critical current ($I_C$) [80], [81], [82]. In the case of AP to P switching, the current $I_W$ flows from the FL to the PL, electrons move from the PL to the FL are spin-polarized in the direction of PL, as shown in **Figure 1.13(a)**. The majority of up-spin electrons (shown using ↑) tunnel through the barrier, maintaining

their polarization, and reach the FL, where they transfer their spin angular momentum, causing the magnetization of FL to align with the PL by applying a large STT, resulting in the magnetization state to switch from AP to P, when the $I_W > I_{C,AP}$. Whereas, minority down-spin electrons (shown using ↓ ) are reflected back from the interface of the barrier and exert insufficient torque that is unable to alter the magnetization of the PL layer. The synthetic antiferromagnetic (SAF) layer, known as the exchange layer, is used below the PL in pMTJ stack in order to increase the coercivity of PL. Conversely, when the current $I_W$ flows from the PL to the FL, electrons moving from the FL to the PL are spin-polarized in the direction of magnetization of FL, as shown in **Figure 1.13(b)**. The majority of up-spin polarized electrons tunnel through the barrier without affecting the magnetization of the PL due to its high coercivity. However, the down-spin electrons, which are comparatively small in number (minority spin) are reflected back and exert sufficient torque on the magnetization of relatively soft magnetic FL that alters the magnetization from P to AP when $I_W > I_{C,P}$. It has been observed that switching from P to AP requires approximately 50-75 % more write current than switching from AP to P, indicating that $I_{C,P} > I_{C,AP}$. This asymmetry in switching conditions is due to different spin polarization efficiency factors for the P and AP states, which depend on the spin polarization and the angle between the magnetization direction of FL and PL. The average critical current density, $J_{c0} = (|J_{C,AP}| + |J_{C,P}|)/2$, where $J_{C,AP}$ and $J_{C,P}$ are the critical current densities for switching the AP to P and P to AP states, respectively, is reported [83] to be $2.2 \times 10^6$ A/cm$^2$ for MgO-based MTJs, which is one-third of that in AlOx-based MTJs. While, in the dual-barrier MgO-based MTJ structure, it is reduced to $1.1 \times 10^6$ A/cm$^2$ [83].

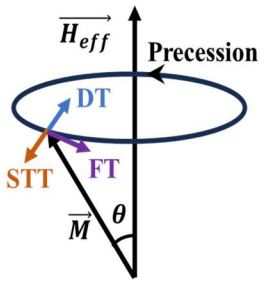



**Figure 1.14** Schematic representation of the Landau-Lifshitz-Gilbert-Slonczewski (LLGS) equation, including field-like torque (FT), Gilbert's damping torque (DT), and STT. In this diagram, FLT arises from the effective magnetic field ($\vec{H}_{eff}$), and DT is directly opposed to STT.

Several studies have been conducted on magnetization dynamics induced by STT [84], [85], [86], [87]. The magnetization dynamics of both iMTJ and pMTJ under the influence of an effective magnetic field ($\vec{H}_{eff}$) are represented by the Landau-Lifshitz-Gilbert-Slonczewski (LLGS) equation as follows

$$\frac{\partial \vec{M}}{\partial t} = \alpha\left(\vec{M} \times \frac{\partial \vec{M}}{\partial t}\right) - \mu_0\gamma\left(\vec{M} \times \vec{H}_{eff}\right) - \frac{\gamma\hbar JP}{2et_{FL}M_s}\left(\vec{M} \times \left(\vec{M} \times \overrightarrow{M_p}\right)\right) \quad 1.16$$

where, $\vec{M}$ represents the normalized magnetization vector (unit vector), defined as $\vec{M} = \vec{m}/M_s$, where $\vec{m}$ is the magnetization vector, and $M_s$ is the saturation magnetization. Here, the first term describes the precession of the magnetization vector ($\vec{M}$) of FL around the effective magnetic field ($\vec{H}_{eff}$ ). It is always perpendicular to both $\vec{M}$ and $\vec{H}_{eff}$. Here, γ is the gyromagnetic ratio, $\mu_0$ is the magnetic permeability of the free space, and the term $\gamma_0 = \mu_0\gamma$, which is equivalent to $2.211\times10^5\, mA^{-1}sec^{-1}$ for a free electron. The effective magnetic field is the sum of various fields,

$$H_{eff} = H_{ext} + H_{ma} + H_{dem} + H_{th} \quad 1.17$$

In this context, $H_{ext}$ represents the applied external magnetic field, $H_{ma}$ denotes the magnetization anisotropy arising from to crystal structure, $H_{dem}$ is the demagnetization field, and $H_{th}$ is the field due to stochastic thermal noise. The second term in the LLGS equation

(equation 1.16) is the damping term, which decreases the precession angle ($\theta$) and aligns the magnetization with $H_{eff}$. Here, α is the damping constant, which dictates the rate of energy dissipation. The third term of the LLG equation represents the STT term. The direction and magnitude of this STT term relative to the damping term are influenced by the direction of the current density ($J$), as shown in **Figure 1.14**.

## 1.7 An Overview of MTJ Device Modeling

Magnetic Tunnel Junction (MTJ) device modeling can be categorized into two primary types based on their features and implementation methods: compact modeling and micromagnetic modeling, as shown in **Figure 1.15**. Compact MTJ models are based on the macrospin approximation, offering a balance between accuracy and computational efficiency. These models are particularly well-suited for the design of complex hybrid CMOS/MTJ circuits and systems due to their low computational demands. In contrast, micromagnetic models provide a more detailed representation of the magnetization dynamics within an MTJ, but they come with a high computational cost, making them less practical for circuit design applications [88].

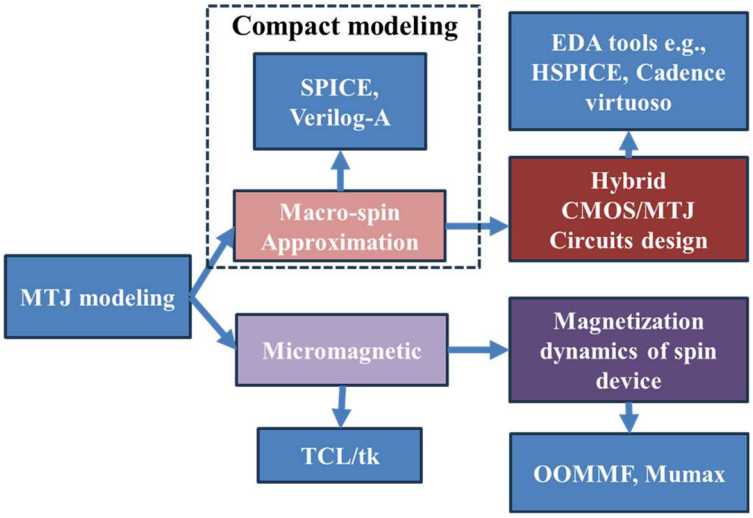



**Figure 1.15** Classification of MTJ device modeling

### 1.7.1. Compact modeling of the MTJ device

To validate functionality and ensure efficient design, it is essential to simulate hybrid MTJ/CMOS circuits and systems accurately, for evaluating their performance prior to fabrication. This necessitates the development of a compact MTJ model that accurately captures both the magnetic and electrical characteristics of MTJs. **Figure 1.16** illustrates a general flow chart for developing such a compact model. By focusing on the fundamental characteristics and operational principles of MTJ devices, these compact models facilitate the optimization and scalability of advanced electronic applications.

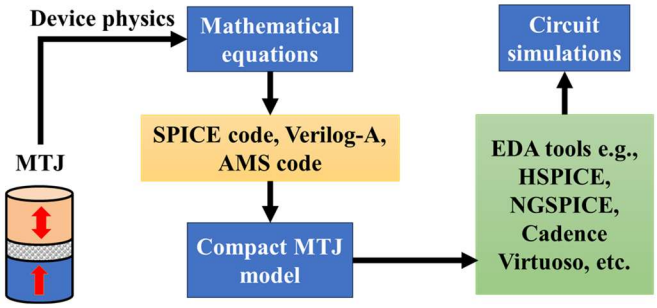



**Figure 1.16** Flow chart of the compact modeling of MTJ device

Compact MTJ models are typically implemented using the Simulation Program with Integrated Circuits Emphasis (SPICE), Verilog-A, and VHDL-AMS (Analog and Mixed-Signal) language [89], [90]. These models are preferred for designing complex hybrid CMOS/MTJ circuits and systems due to their low computational requirements and compatibility with simulation tools like Hewlett Simulation Program with Integrated Circuits Emphasis (HSPICE), NGSPICE, and Cadence. Various compact models were developed after the development of the HSPICE-based compact model for spin-valves by Bas and Black [91]; the first universal macrospin model for GMR was introduced in 2000 that effectively captures the nonlinear and hysteresis characteristics of GMR [92]. In 2005, the first HSPICE-based macrospin model for the MTJ was introduced by Lee *et al*. [93]. This model is realized as a five-terminal

subcircuit that reproduces the characteristics of an MTJ, including hysteresis and asteroid curves with thermal variation and resistance versus bias voltage (R-V) characteristics. The macrospin model of the MTJ for STT switching is present in the literature [94], which uses the SPICE subcircuit for all DC and transient characteristics of the MTJ, including the hysteresis, variation of resistance with bias voltage, and critical switching current with the critical switching time. This model was designed to work over a wide range of operating conditions. To show the effectiveness of this model, an MTJ-based non-volatile D flip-flop is designed and simulated. Georgios D. Panagopoulos *et al*. presented a physics-based compact model for MTJ that is implemented using the SPICE-inbuilt voltage-dependent current source and capacitance subcircuit [95]. This model is more user-friendly due to the flexibility in changing the physical device dimensions, such as the thickness of the oxide barrier layer and material anisotropy. Jongyeon Kim *et al*. introduced a technology-agnostic MTJ SPICE model with user-defined dimensions for scalability studies of both iMTJ and pMTJ in STT-MRAM applications [96]. The simulation framework for this model employs SPICE subcircuits to capture various aspects of MTJ physics, as illustrated in **Figure 1.17**. This model has been validated with experimental results and accurately reproduces realistic MTJ characteristics.

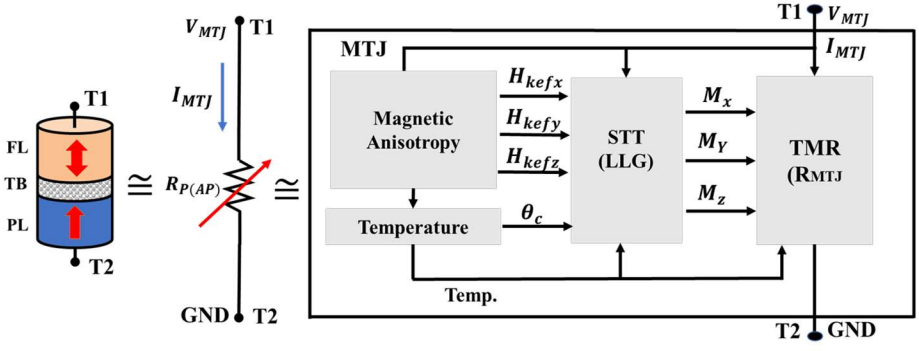



**Figure 1.17** Simulation framework of the compact MTJ model [96]

Although HSPICE is an industry-standard simulator, models based on Verilog-A and VHDL-AMS languages offer greater flexibility, higher readability, improved modularity, and ease of update. Additionally, these models integrate more seamlessly with any CMOS PDK (process design kits) in the Cadence tool compared to SPICE-based models. Many MTJ models have been developed over time based on these concepts. For instance, literature [97] presents a VHDL-AMS-based MTJ model created using the S-W model, and it is noted as one of the first compact model to incorporate the vectorial aspect of the magnetic field. Similarly, a continuous-time 3D model was developed in the literature [98]. Later, in literature [99], a Verilog-A-based dynamic STT-MTJ model was developed, which includes the thermal effects and switching probability. In literature [100], the authors present a static macro model of a CoFeB/MgO/CoFeB MTJ structure developed using Verilog-A language, which is implemented on the Cadence Virtuoso platform with the Spectre simulator. This model incorporates various experimental parameters to enhance simulation accuracy. The functionality and behaviour of the MTJ model are verified through DC and transient simulations.

Despite the excellent potential of STT-MTJs, their performance is hindered by significant reliability issues such as process variations, temperature effects, stochastic switching, and dielectric breakdown due to self-heating, which can cause functional errors in hybrid CMOS/MTJ circuits [101]. Wang *et al*. proposed a compact MTJ model incorporating the phenomena of dielectric breakdown of the MgO barrier and STT stochastic behaviour, integrating technical variations and temperature evaluations [102]. However, this model did not account for the effect of current pulse width on dielectric breakdown. In 2015, they introduced an updated SPICE compact model that considered temperature variation and its impact on performance [103]. In hybrid CMOS/MTJ designs, the resistance of the MTJ should

match the resistance of the transistor on which it is fabricated. To achieve lower resistance, the thickness of the MgO tunnel barrier should be reduced, while still being capable of withstanding the high current required for the STT mechanism, which generates significant potential across the MTJ [104]. Several experiments have been conducted to understand this behaviour [105], [106], [107]. Therefore, a timely and comprehensive MTJ model is essential, incorporating field and voltage dependence, ramped voltage breakdown, time to failure, temperature effects, area scaling, and variations tolerant to design reliable hybrid circuits.

### 1.7.2. Micromagnetic Modeling of the MTJ Device

Widely used CAD tools for micromagnetic simulations are OOMMF [108] and Mumax3 [109], which are useful in the context of STT-based devices with uniform magnetization. These micromagnetic simulators are also capable of dealing with non-uniform magnetization, like vortex and domain wall, which are beyond the scope of this thesis. These simulators have computer aided solvers that also facilitate defining a micromagnetic problem in terms of geometry and material parameters. Micromagnetic simulations involve the numerical solution of the LLG equation while considering the magnetic body consisting of several magnetic domains. In order to perform these simulations, the atomic spins are grouped into small cells/grids. However, these cells/grids cannot be larger than the characteristic exchange length [110]. In a micromagnetic model, the effective field is the superposition of the external or Zeeman's field and the intrinsic fields. The material and geometry-dependent intrinsic fields consist of crystalline anisotropy, demagnetization, and exchange field. In micromagnetic simulations, the LLGS equation is solved by using the finite-difference methods in terms of time and space. The solution of the LLG equation is done using numerical methods which involve complex computation. The computational time generally depends on the

geometry, cell/domain size, and complexity of the problem.

The rising demand for fast and more energy-efficient memory solutions and STT-MRAM has emerged as potential choices for next-generation non-volatile memory [111]. Therefore, a detailed investigation of the spin transport and magnetization dynamic in MTJs is crucial for realizing their maximum potential in revolutionizing memory storage and computing capabilities [29], [112]. The MTJ devices have a complex architecture that needs to be analyzed in a micromagnetic simulation, which has the closest existing solvers that aid the simulation of magnetization dynamics in MTJ devices. Existing micromagnetic simulation frameworks and compact models compatible with SPICE for MTJs examine magnetization dynamics while considering that the current density does not depend on position and time during the magnetization switching. However, during the switching process, spin configurations vary from point to point, which leads to a change in the resistance of the MTJ. Consequently, the current density flowing through the MTJ structure experiences variations rather than constant, particularly in the case of high TMR MTJs [113]. Further, S. Fiorentini *et al*. reported that current density can vary by a factor of three in modern MTJs, where the TMR is greater than 200 % [114]. Moreover, C. Y. You *et al.* [115], [116] focused on advancing an OOMMF extension for a more flexible micromagnetic simulation, illustrating the TMR-dependent switching process with non-uniform current density (NUCD). However, they do not offer an appropriate spin transport module for an accurate picture of STT-MTJ devices. Datta *et al.* [117] reported a non-equilibrium green function (NEGF) based quantum transport simulation model for MTJ. They came up with a novel method for calculating the conductance of MTJ devices along with the spin torque. Also, their coupled model allows us to estimate experimental switching voltage for the AP to P and P to AP switching employing various MTJ

devices and material parameters related to the ferromagnet and dielectric. However, the framework does not have the capability to incorporate the magnetization dynamics of the MTJ FL. Furthermore, the spin transport NEGF formalism does not account for the NUCD effect, which has a significant impact on magnetization dynamics and the switching behaviour of MTJ devices. The micromagnetic simulation tools, such as OOMMF [108] and Mumax3 [109], are considered standard for capturing the magnetization dynamics or switching behaviour of MTJ. Herein, OOMMF extensions [118], which have been proposed by different research groups from academia and industry, facilitate the modeling of magnetization dynamics. However, they do not offer an appropriate spin transport module for an accurate picture of MTJ devices. Hence, the MTJ design is handled using a mixed-mode simulation framework consisting of magnetization dynamics [95], [117], [119], and the spin transport model based on NEGF formalism is considered separately. Further, Jullière's model [33] for spin transport and monodomain approximation for magnetization dynamics are used in compact models [120], [121], [122], [123], [124], [125], [126], [127], [128] compatible with SPICE.

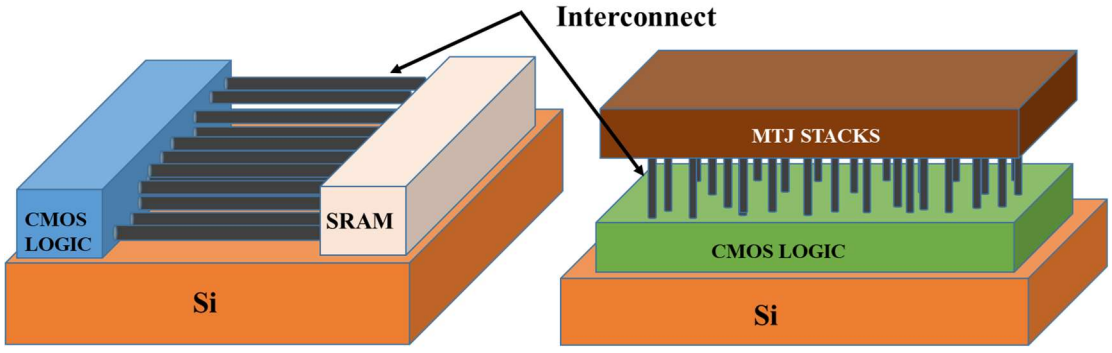



**Figure 1.18** (a) Conventional Von-Neumann architecture, showing the separate placement of logic and memory blocks on the silicon layer. (b) Modern logic-in-memory (LiM) architecture, with MTJs stacked over the CMOS logic.

## 1.8 Hybrid CMOS/MTJ-based Logic-in-Memory Computing Circuits

Among various spintronic devices, MTJ devices stand out for their commercial viability due to their superior properties. As a result, researchers have paid more attention to the design and development of hybrid CMOS/MTJ circuits. In these hybrid circuits, STT switching-based MTJs are utilized for their significant advantage of nonvolatility, allowing data storage for long periods even without power.

The Von-Neumann architecture, separates CMOS logic and memory blocks, connecting them with interconnects/high-speed buses (**Figure 1.18 (a)**). This separation limits the data transfer rate between these blocks, requires a large area, and leads to significant static power dissipation in logic blocks due to deep sub-micron CMOS scaling. Additionally, interconnects used for signals and clocks consume considerable power. The concept of logic-in-memory (LiM) was first proposed by Kautz in 1969 [129]. LiM architecture addresses these issues by placing the memory block on top of the CMOS logic (**Figure 1.18 (b)**). Incorporating MTJ devices in the LiM architecture provides nonvolatility, allowing the power to be completely switched off for unused or idle blocks, resulting in almost zero static power dissipation in standby mode. Another significant advantage is the ease of integrating or three-dimensional (3D) integration of MTJs on top of CMOS, which reduces latency, improves integration density, and enhances data transfer speed between memory and logic blocks. Efforts are also being made to develop novel spintronic-based reconfigurable logic-memory devices [130], [131], [132], [133]. For instance, in 2017, Luo *et al*. proposed an innovative multilayer magnetic device, Ta/CoFeB/MgO, combining logic and memory operations using both the anomalous Hall effect and negative differential resistance phenomenon to perform various reconfigurable logic operations. This combination has overcome the limitations of

conventional architecture [133], [134], [135], [136], [137]. Further, emerging unconventional spintronics paradigms are reservoir computing, probabilistic computing, and mem-computing [138].

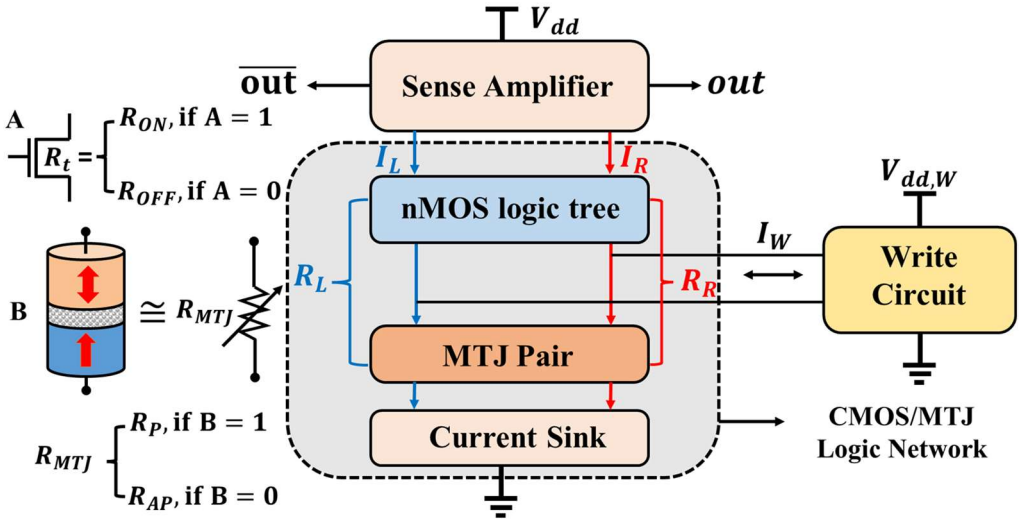



**Figure 1.19** Modern logic-in-memory (LiM) architecture for developing hybrid CMOS/MTJ circuits.

The diagram (**Figure 1.19**) illustrates the integration of MTJs with CMOS technology to design a hybrid circuit capable of both logic computation and data storage within the LiM architecture [139], [140]. Here, the nMOS logic tree block is responsible for designing logic functions using nMOS transistors, while the MTJ pair block is used for both logic operations and data storage in MTJs. A writing circuit block provides sufficient $I_W$ to write data into the MTJs. $R_L$ and $R_R$ represent the total resistance due to the nMOS transistor and the MTJs in the left and right branches, respectively. In this diagram, $A$ and $B$ are assumed to be two logical inputs of the function. Three main components of the LiM architecture are:

### 1.8.1. Read/Sense circuit

A sense amplifier is employed to read or access the data stored in the pair of MTJs or the output of the logic function implemented in the CMOS/MTJ logic network. Typically, the pair of MTJs is in opposite states, either P or AP. The reading of data from the MTJs pair is

feasible due to the differing resistance values of the P and AP states.

Various sense amplifiers (SA) have been reported in the literature, including dynamic current-mode sense amplifiers [141], and pre-charge sense amplifiers (PCSA) [142], [143] SRAM-based sense amplifiers [144]. These current-mode sense amplifiers measure the current difference between two branches where the MTJ pair is connected. A higher current difference between the branches is essential for reliable and accurate reading. The current in the left branch ($I_L$) and the right branch ($I_R$) depends on the total equivalent resistance of the nMOS logic trees and the MTJs in each path. Since the resistance difference in the MTJs is directly related to the TMR ratio, a higher TMR is crucial for the reliable read operation of hybrid CMOS/MTJ circuits. This inherent property of the MTJs facilitates the integration of MTJs with current-mode sense amplifiers [145], which read/access the MTJ state and amplify the output to represent the correct logic state. The PCSA-based sense amplifier has become popular and widely used in developing hybrid CMOS/MTJ circuits due to its high sensing speed of approximately 200 ps, sensing reliability of around $10^5$, sensing speed of about 124 ps/bit, and power consumption of approximately 1 fJ/bit, as determined through simulations using a 90 nm STMicroelectronics design kit [142]. Various modifications have been proposed in the literature to enhance PCSA performance, including enhancements for sensing reliability [146], separate-PCSA (SPCSA) for lower power and higher speed [147], and reliability-enhanced PCSA (REPCSA) for a larger sensing margin [148].

### 1.8.2. Write/Store circuit

It is used to write binary data into a pair of MTJs. Each pair of MTJs is required to store a single bit of data, which can later be read by different types of SA, as mentioned previously. Various write circuits based on the MTJ switching mechanism have been designed to

store/write binary data into an MTJ pair.

In the PCSA-based sensing/reading circuit, a pair of MTJs are always in opposite states, either P and AP state or vice versa. Consequently, both MTJs must be switched to the opposite state when reconfiguring the input data. To achieve the writing operation using the STT switching mechanism, the bidirectional writing current ($I_W$) generated by an nMOS and pMOS transistors of the write circuit must be greater than the critical current ($I_C$), which is less than 50 µA for 28 nm technology [149]. Based on the requirement for bidirectional write current in STT switching, four-transistor (4T) and six-transistor (6T) writing circuits (seen in **Figure 1.20**) have been reported in the literature [149], [150]. While 6T write circuits generate higher write current and less write delay because of the dependency of STT switching on the magnitude of write current. The following paragraphs will provide detailed working of the two write circuits and their control mechanism.

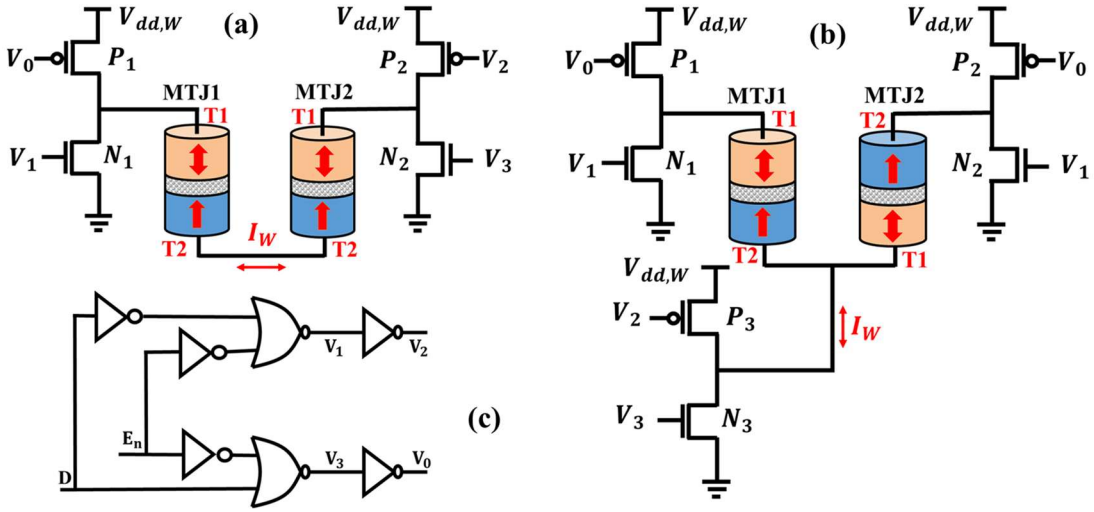



**Figure 1.20** Schematic representation of (a) Four transistors (4T) write-core circuits (b) Six transistors (6T) write-core circuits (c) write-enable circuit for control of the direction of current based on the input data (D) [150].

In the 4T write-core circuit depicted in **Figure 1.20(a)**, four transistors labeled $P_1$, $P_2$, $N_1$, and $N_2$ are utilized for writing to the MTJ pair. In this configuration, the terminal $T_1$ of MTJ1

is connected to the terminal $T_2$ of MTJ2. The transistors ($P_1$, $P_2$, $N_1$ and $N_2$) are controlled by intermediate signals $V_0$, $V_1$, $V_2$, and $V_3$, which are generated by the write-enable circuit shown in **Figure 1.20(c)**. During the write operation, transistors $P_1$ and $N_2$ are ON, while $P_2$ and $N_1$ are OFF, or vice versa, for flowing current in the opposite direction. Similarly, the 6T write-core circuit, shown in **Figure 1.20(b)**, employs six transistors named $P_1$, $P_2$, $P_3$, $N_1$, $N_2$, and $N_3$ for writing to the MTJ pair. In this configuration, the terminal $T_2$ of MTJ1 is connected to the terminal $T_1$ of MTJ2. During the writing operation, transistors $P_1$, $P_2$, and $N_3$ are turned ON, while $N_1$, $N_2$, and $P_3$ are turned OFF, or vice versa, for flowing current in the opposite direction. The transistors ($P_1$, $P_2$, $P_3$, $N_1$, $N_2$, and $N_3$) are also controlled by intermediate signals $V_0$, $V_1$, $V_2$, and $V_3$ from the same write-enable circuit used for the 4T write circuit. These intermediate signals are generated by the write-enable circuit to control the bidirectional write current by turning ON the corresponding transistors. The write-enable circuit consists of three NOT and two NOR logic gates, as shown in **Figure 1.20(c)**. A control signal ($E_n$) and input data signal ($D$) determine the direction of the write current ($I_W$) during the write operation. To enable the write operation, the $E_n$ should be logic '1'. **Table 1.1** shows various control signals generated during the write operation required to achieve the corresponding MTJs magnetization state.

**Table 1.1** Control Signals Corresponding to the MTJ State for the Write Circuit

| **Control inputs** | | **Intermediate signals** | | | | **MTJs state** | |
|---|---|---|---|---|---|---|---|
| **En** | **D** | **V0** | **V1** | **V2** | **V3** | **MTJ1** | **MTJ2** |
| 0 | X | 1 | 0 | 1 | 0 | X | X |
| 1 | 0 | 0 | 0 | 1 | 1 | AP | P |
| 1 | 1 | 1 | 1 | 0 | 0 | P | AP |

* X represents the don't care.

All hybrid CMOS/MTJ circuits experience significant writing delays, which restrict their ability to function at higher clock frequencies. However, the 6T write circuit generates a

larger write current, thereby reducing write delay, at the cost of increased chip area. To reduce the write delay, the following circuit design perspective can be considered,

- Increase in the power supply of the writing circuit ($V_{dd,w}$) increases the write current ($I_W$), which reduces the write delay. However, this also increases power dissipation since power is proportional to the $V_{dd,w}^2$. Consequently, the $V_{dd,w}$ of the write circuit is always kept higher than the power supply of the SA ($V_{dd}$) (refer to **Figure 1.19**).
- The write current can also be increased by increasing the transistor width of write circuits since the magnitude of the write current is directly proportional to the aspect ratio of the MOS transistors [151]. Hence, it also incurs an area overhead.
- To ensure reliable writing and reduce writing failures, the control signal ($E_n$) must enable greater than the switching time for the MTJ pair, which is typically much greater than the average write time, almost five times the average switching time, leading to significant energy wastage and a slowdown in the writing process. Hence, an additional circuit is needed to stop the write operation once data is written in the MTJ.

These conventional write circuits incorporate a write-core circuit to generate bidirectional current, and a write enable signal to initiate the write operation, as illustrated in **Figure 1.20**. However, this approach results in inefficient use of space due to the extensive use of transistors in the design. Additionally, in the conventional write circuit, current continues to flow for a long duration even after the MTJ state has switched, leading to significant energy wastage and a slowdown in the writing process. Consequently, energy wastage stands out as a major challenge in conventional writing methods. One prominent solution to address these

issues is to incorporate the auto-write termination (AWT), which promptly halts current flow upon detecting MTJ switching, albeit at the expense of increased circuit area. Both LiM implementations and non-volatile computations involve MTJs and their corresponding write circuits, which traditionally suffer from energy wastage due to continuous current flow even after the MTJ state has switched. This is exacerbated by the stochastic nature of STT-based MTJ switching, which requires writing times to be significantly longer than the average to ensure reliability. This AWT approach, while potentially increasing the circuit area due to additional components, effectively reduces energy wastage and enhances writing efficiency. Various techniques have been proposed in the literature [152], [153], [154] to mitigate the write energy wastage and minimize the write delay by implementing a self-terminated write mechanism. For example, in an article [152], an auto-write termination circuit was introduced for a non-volatile latch. However, a self-write-terminated driver proposed in another study [154] has a high transistor count due to its write-enable circuit that employs a MUX in the write completion detector circuit, resulting in a larger area and higher power requirements. Thus, considering the challenges mentioned above of the existing write circuits, this thesis focuses on area-efficient auto-write-termination circuits for STT-MTJ-based logic circuit implementation.

### 1.8.3. CMOS/MTJ Logic network

It is crucial for implementing logic functions, leveraging a combination of the nMOS logic tree and MTJ pair blocks. Input variables are applied to the gate terminal of nMOS transistors, and some are stored in the MTJ pair. Herein, the MTJs are used for both logic implementation and long-term data storage even when power is off due to their inherent non-volatility and distinct resistance states (P and AP). On the other hand, the nMOS transistors are

used only for logic implementation. The nMOS transistor is turned ON for logic '1' and offers an ON resistance ($R_{on}$) in the range of kilo-ohm (KΩ), while turned OFF for logic '0' and offers an OFF resistance ($R_{off}$) in the range of mega-ohm (MΩ). Whereas, the resistance of P and AP states of the MTJ ($R_P$) and ($R_{AP}$), which depends on TMR, is represented as logic '1' and logic '0', respectively. For effective logic implementation, $R_{on} < R_P$ and $R_{off} > R_{AP}$. The outputs of the logic implementation $out$ and $\overline{out}$ provide the true and complementary values based on the current in the right ($I_R$) and left ($I_L$) paths, respectively. This current value depends on the total resistance offered by the left ($R_L$) and right ($R_R$) paths. If the current $I_R$ is less than $I_L$, the output ($\overline{out}$) is quickly pulled down to logic '0' due to relatively fast discharging, while $out$ is set to logic '1'. Conversely, when $I_R$ is greater than $I_L$, the output ($out$) is quickly pulled down to logic '0' through relativity fast discharging and $\overline{out}$ is set to logic '1'.

Various hybrid CMOS/MTJ circuits are implemented, such as Boolean logic gate [155], [156], magnetic lookup table [157], magnetic flip flops [158], [159], [160], [161] magnetic full adder [139], [140], [149], [162], [163] and magnetic arithmetic logic unit (ALU) [164], [165], etc. Due to the inherent characteristics of the MTJ, various other applications are also developed for next-generation computing [166], [167], [168]. The hybrid circuits discussed in the literature are either partially non-volatile [169], with the logic tree implemented using a combination of nMOS transistors and MTJs, or fully non-volatile [170], with the logic tree realized exclusively using MTJs. Fully non-volatile logic implementations are more power-efficient. Therefore, to turn the partially non-volatile logic implementations into fully non-volatile logic implementations, logic inputs applied to the nMOS transistors must be stored in the non-volatile memory. For this, non-volatile (NV)-latches are important entities in both

LiM and NV computing architectures. Different NV latches have been proposed in recent years envisaged to fulfill the requirements of LiM and NV computing architectures. The latch proposed in [171] is based on the separated latch and sensing circuit (SLS) structure that can consume a large area and energy due to separated sensing and writing circuits. Also, high sensing delay can be caused by the sensing operation being performed in two stages. The latch proposed in [172] requires the use of a separate write circuit, which also increases area and energy consumption. While the latch in [173] has an inbuilt read and write circuit, however, using the same path for reading and writing of the MTJ can increase read disturbance. Furthermore, existing latches do not have a write energy-saving mechanism, and their design is not suitable for integrating with an auto-write termination (AWT) technique, therefore, a large amount of energy can be wasted during the write operation.

## 1.9 Problem Definition

This thesis focuses on device modeling and logic circuit design for spin-based computing based on an extensive literature survey done in this chapter. The section 1.5 highlights the existence and significance of TMC in MTJ structures for next-generation applications. It is crucial to implement a compact model that accurately captures both TMR and TMC effects. Section 1.7 outlines the limitations of existing simulation frameworks and tools in simultaneously incorporating spin transport and magnetization dynamics using the physical and material parameters of FM and NM materials. To address this gap, the development of an advanced micromagnetic simulation framework enabled by the Non-Equilibrium Green's Function (NEGF) formulation for modeling STT-MTJ devices is necessary. Further literature survey in section 1.8 discusses the hybrid CMOS/MTJ-based LiM architecture. The stochastic nature of MTJ switching, influenced by thermal fluctuations, causes significant variability in

the time required for writing into STT-MTJs, leading to the waste of writing energy. This variability necessitates the development of auto-write terminate (AWT) circuits to stop the write operation upon completion. Implementing fully non-volatile logic circuits using the LiM architecture also requires a non-volatile latch with a simplified architecture, better stability, higher speed, smaller footprint, lower power consumption, and ease of integration with CMOS logic styles. Based on the literature review, the problems identified and addressed in this thesis are organized into separate chapters as follows:

(i) ***Chapter 2*** deals with SPICE-compatible compact modeling STT-MTJ that accurately captures both TMR and TMC effects. In which, we address the limitations of previous MTJ models that emulate TMR and magnetic switching behaviour but lack the TMC effect. This thesis introduces a SPICE-based STT-MTJ framework incorporating both TMR and TMC effects. The voltage-induced TMC effect is modeled using a combination of the Debye-Fröhlich model, Zhang-sigmoid theory, parabolic barrier approximation, and spin-dependent drift-diffusion model, which accurately emulates magnetocapacitance behaviour with respect to frequency in MTJ device. The proposed model is validated through HSPICE simulations, showing good agreement with experimental data.

(ii) ***Chapter 3*** deals with an advanced micromagnetic simulation framework based on the NEGF formalism to analyze the STT switching behaviour in MTJ devices. This simulation framework combines the TCL-based NEGF model for spin transport with the micromagnetic simulations for magnetization dynamics, enabling comprehensive analyses of the STT switching behaviour in MTJs.

(iii) ***Chapter 4*** deals with an area-efficient auto-write-terminate circuit for NV latch and logic-in-memory applications. In which, we propose an STT-MTJ-based non-volatile

latch with an AWT feature. This latch has a simple structure, improved stability, higher speed, and seamless integration with CMOS logic styles. It eliminates the need for an additional write driver circuit, resulting in a smaller footprint during MTJ writing. Consequently, the proposed latch consumes less power compared to previous designs, using fewer transistors for write operations and logic implementation. The AWT circuit continuously monitors the write operation, prevents redundant MTJ writing, and removes excessive write current flow, thereby saving power.