Chapter 5

Expandable Input Impedance Sourced Isolated DC-DC Resonant Converter

5.1 Introduction

For a solar PV system, the MPPT algorithm varies the control variable of the front-end converter to harness solar power efficiently. However, the output remains uncontrolled and needs to be regulated for further utilization and thereby requiring an additional power converter. Also, to meet the voltage requirements of the utility side, a high-gain converter is often required to boost the low voltage output of solar PV. Although using the transformer's voltage gain flexibility, high voltage gain can be achieved, the DHABRC operates as a step-down converter and provides soft-switching effectively around unity gain. Since the expandable network allows us to operate with different voltage range depending upon the number of cells, a number of possibilities can be explored using the expandable configuration at the input. This chapter discusses an expandable input impedance-sourced isolated resonant converter (EIISIRC), where an expandable impedance network is added at the input side of the earlier proposed isolated resonant converter to feed the solar power to DC microgrid or to the household appliances like solar heater or cooker. This chapter explains the converter's circuital operation and mathematical modeling. Based on the analysis, the converter is designed to operate with soft-switching. The proposed converter's 500 W laboratory prototype is developed and tested to verify the mathematical modeling and the achieved soft-switching operation.

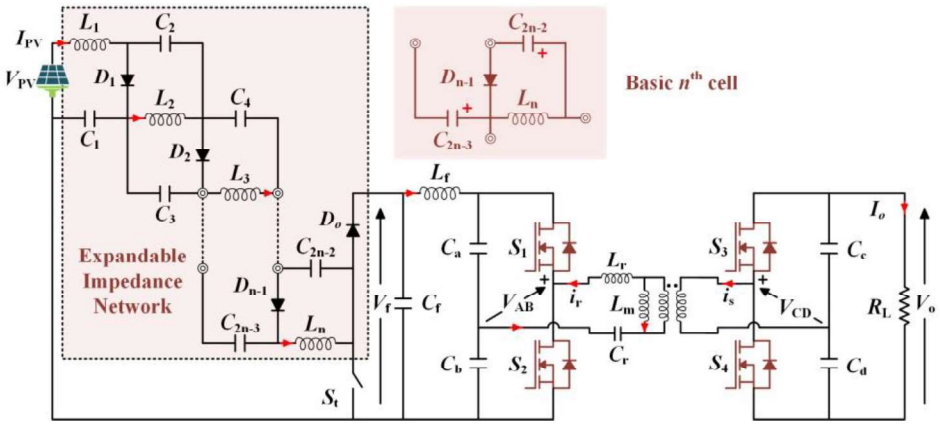


Fig. 5.1 Diagram of Expandable input impedance-sourced isolated resonant converter.

5.2 Proposed Converter

Fig. 5.1 illustrates the circuit diagram of the proposed Expandable input impedance sourced isolated resonant converter (EIISIRC). The operation of the converter can be described as follows:

5.3 Expandable input impedance-sourced network (EIIS)

The expandable input impedance sourced network is constructed using an L_nC_{2n-2} network consisting of n cells. Each cell incorporates two capacitors, one inductor, and one diode, as shown in Fig. 5.1. Notably, the voltage gain of the network is determined by the expression $1/(1-nD)$, where D denotes the duty ratio. The component counts for the network are as follows:

No. of Inductors = n

No. of Capacitor = ($2n$-2)

No. of Diodes = n-1

No. of Active Switches = 1

To comprehensively study the performance of the proposed converter, the case of n = 3 is investigated. This corresponds to an L_3C_4 network comprising three inductors (L_1 - $L3$), four capacitors (C_1 - C_4), three diodes (D_1 - D_o), and one active switch (S_t), as depicted in Fig. 5.2. The converter's operation is characterized by two states based on the switching of the S_t: DT_s and (1- D).T_s, where T_s represents the switching cycle period.

5.3.1 DTs Switching State

The active switch S_t is ON for DT_s during this state, as illustrated in Fig. 5.2 (a). This results in all diodes being reverse-biased. Notably, the inductor current (I_{L1} - I_{L3}) increases while the capacitor voltages (V_{C1} – V_{C4}) are simultaneously discharged. Additionally, the filtering capacitor, C_f, discharges to supply the load. The waveforms corresponding to this state are presented in Fig. 5.3. The inductor voltages for this state can be given as

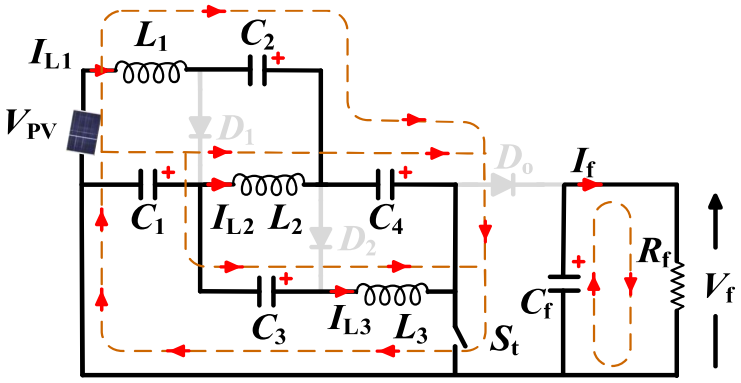
$$V_{L1} = V_{PV} + V_{C2} + V_{C4} \tag{5.1}$$

$$V_{L2} = V_{C1} + V_{C4} \tag{5.2}$$

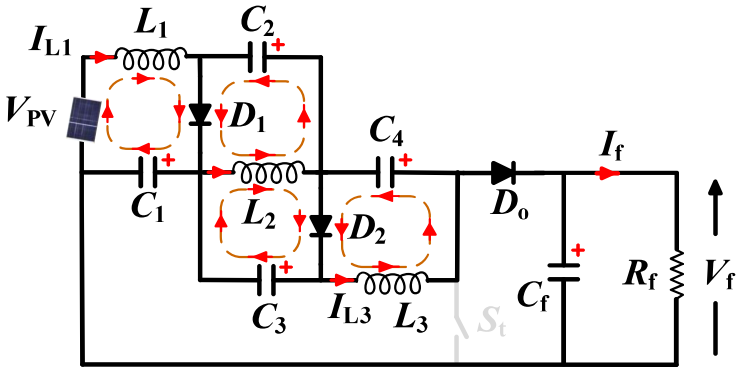
$$V_{L3} = V_{C1} + V_{C3} \tag{5.3}$$

The capacitor currents for this state can be given as

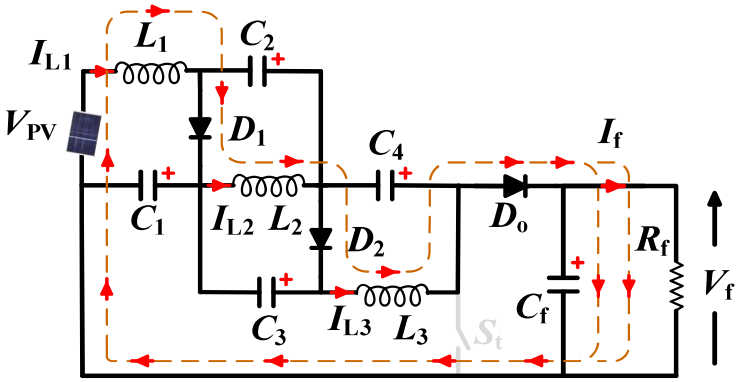
$$I_{C1} = I_{L2} + I_{L3} \tag{5.4}$$



(a)



(b)



(c)

Fig. 5.2 Operating modes of proposed EIIS network (a) DTs switching instant; (b) TBuffer instant; (c) (1-D)Ts switching instant.

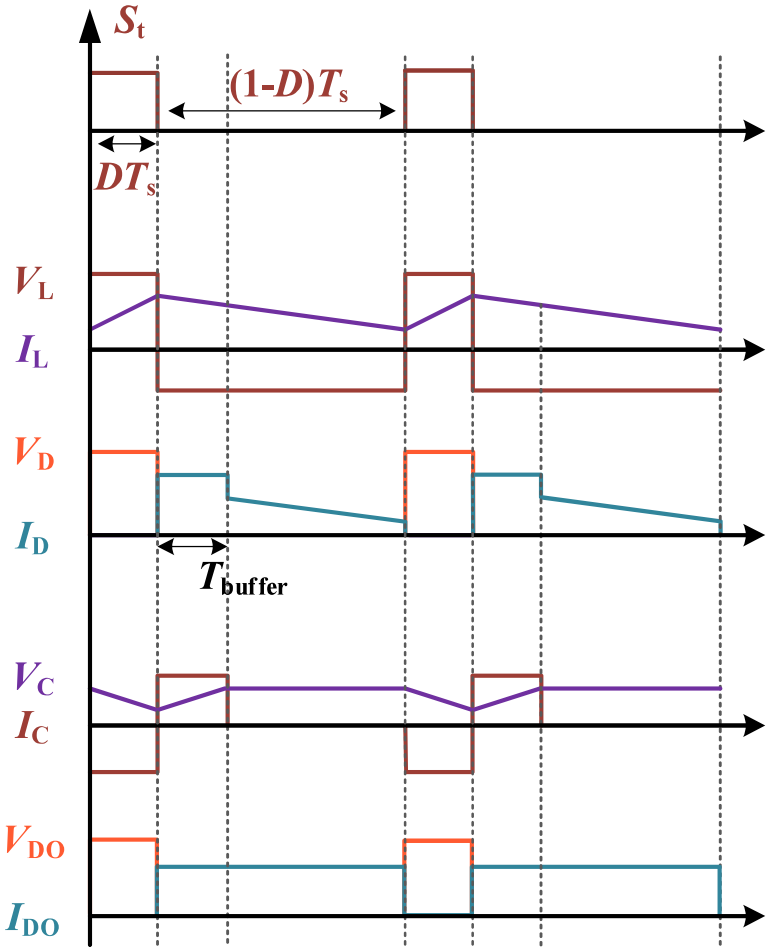


Fig. 5.3 Operating waveform of proposed EIIS network.

$$I_{C2} = -(I_{L2} + I_{L3}) \tag{5.5}$$

$$I_{C3} = -I_{L3} \tag{5.6}$$

$$I_{C4} = -(I_{L1} + I_{L3}) \tag{5.7}$$

$$I_{Cf} = -I_f \tag{5.8}$$

5.3.2 (1-D)T_s Switching State

Upon turning OFF switch S_t, all diodes become forward-biased. A brief buffer time (T_{Buffer}) ensures that the high inductor current recharges the previously discharged capacitors rapidly. Due to the short duration of this buffer time, it is typically neglected in the analysis (Fig. 5.2

(b)). Subsequently, all inductors supply the load and recharge the discharged capacitors, as illustrated in Fig. 5.2 (c). The waveforms corresponding to this operating interval are presented in Fig. 5.3.

The inductor voltages for this state can be given as

$$V_{L1} = V_{PV} - V_{C1} \tag{5.9}$$

$$V_{L2} = -V_{C2} = -V_{C3} \tag{5.10}$$

$$V_{L3} = V_{C4} \tag{5.11}$$

The capacitor currents for this state can be given as

$$I_{C1} = I_{D1} + I_{D2} - (I_{L2} + I_{L3}) \tag{5.12}$$

$$I_{C2} = I_{D1} - I_{L1} \tag{5.13}$$

$$I_{C3} = I_{D2} - I_{L3} \tag{5.14}$$

$$I_{C4} = I_{D1} + I_{D2} - (I_{L1} + I_{L2}) \tag{5.15}$$

$$I_{Cf} = (I_{L1} + I_{L2} + I_{L3}) - (I_{D1} + I_{D2}) - I_f \tag{5.16}$$

The voltage across the capacitors within the network is determined by applying the principle of volt-second balance over a single time period (T_s). This analysis considers the DT_s and (1-D)T_s intervals to derive the steady-state equations. The steady-state values are as follows:

$$V_{C1} = \frac{1-2D}{1-3D} V_{PV} \tag{5.17}$$

$$V_{C2} = V_{C3} = V_{C4} = \frac{D}{1-3D} V_{PV} \tag{5.18}$$

The voltage (peak) across C_f can be given as follows.

$$V_f = V_{C1} + V_{C3} + V_{C4} = \frac{1}{1-3D} V_{PV} \tag{5.19}$$

Therefore, the voltage gain 'A' for the impedance network can be given as.

$$A = \frac{V_f}{V_{PV}} = \frac{1}{1-3D} \tag{5.20}$$

The maximum blocking voltage across the diodes and switch S_t can be given as

$$V_{D1} = V_{D2} = V_{Do} = \frac{1}{1-3D} V_{PV} \tag{5.21}$$

$$V_{st} = \frac{1}{1-3D} V_{PV} \tag{5.22}$$

Similarly, by current second balance across the capacitors (C_1, C_2, C_3, and C_4), the steady-state current can be given by:

$$I_{L1} = I_{L2} = I_{L3} = I_{PV} \tag{5.23}$$

By applying the power balance across the input and output terminals, the input current can be given as:

$$I_{PV} = \frac{I_f}{1-3D} \tag{5.24}$$

Since the EIIS network can be extended to *n*-cells, the equations for *n*-cells are as follows.

$$V_{C1} = \frac{1-(n-1)D}{1-nD} V_{PV} \tag{5.25}$$

$$V_{C2} = V_{C3} = \text{.....} = V_{C(2n-2)} = \frac{D}{1-nD} V_{PV} \tag{5.26}$$

Similarly, the voltage gain can be given as (5.27).

$$A = \frac{V_f}{V_{PV}} = \frac{1}{1-nD} \tag{5.27}$$

$$V_{D1} = V_{D2} = \text{.....} = V_{D(n-1)} = \frac{1}{1-nD} V_{PV} \tag{5.28}$$

$$V_f = \frac{1}{1-nD} V_{PV} \tag{5.29}$$

The critical boundary condition for inductor current can be given as (5.30).

$$I_L = \frac{\Delta I_L}{2} \tag{5.30}$$

From (5.30), the value of inductance under the boundary condition can be calculated as:

$$L_{kr} = \frac{D(1-D)(1-3D)}{2I_{PV}} V_f T_s \tag{5.31}$$

Thus, the critical inductor time constant (T_{kr}) is defined as:

$$T_{kr} = D(1-D)(1-3D) = \frac{2L_{kr}}{RT_s} \tag{5.32}$$

Equations governing the critical inductance (L_{kr}) and inductor time constant (T_{kr}) for n-cells can be given as:

$$L_{kr} = \frac{D(1-D)(1-nD)}{2I_{PV}} V_f T_s \tag{5.33}$$

$$T_{kr} = D(1-D)(1-nD) = \frac{2L_{kr}}{RT_s} \tag{5.34}$$

For different values of n, the CCM-DCM region, T_{CR}, and D are expressed in Fig. 5.4.

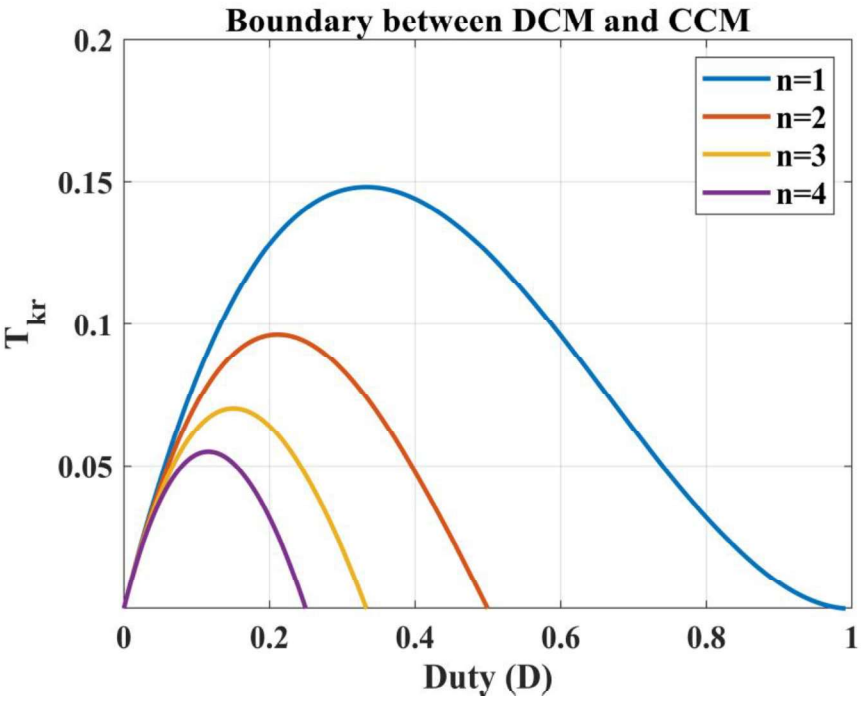


Fig. 5.4 Boundary condition between CCM and DCM.

5.4 Expandable Input Impedance Sourced Isolated Resonant Converter

The operation of the expandable input impedance sourced isolated resonant converter, featuring an expandable impedance network and an isolated resonant converter, can be understood by considering three distinct operating intervals as follows-

5.4.1 Interval I: ($T_0 - T_1$)

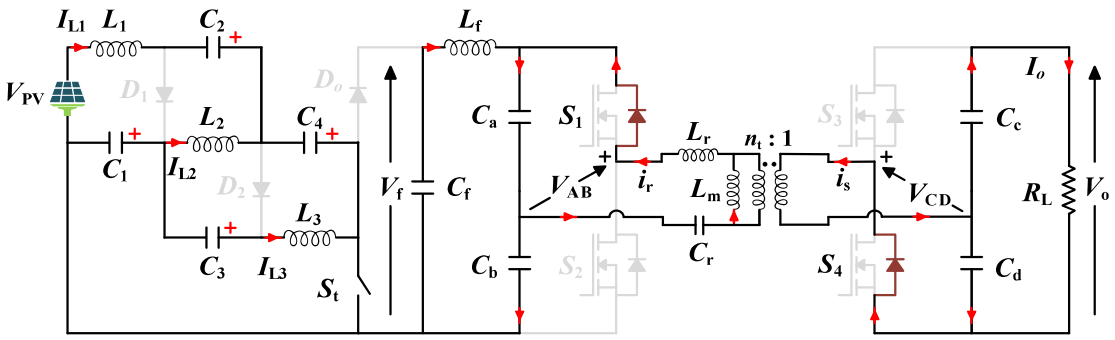
Interval I begins when S_t receives the gate signal for the duration of the DT_s, creating a positive voltage across the inductors. As a result, the inductors of the EIIS network start to store energy. Moreover, S_1 receives the gating signal $V_{GS1,}$ making the V_{AB} positive. Switch S_4 is already in on-state, making V_{CD} negative. The resonant tank releases its energy toward the source, and the body-diode of S_1 conducts. Since voltage $-V_{CD}$ appears across the L_m, current "i_m" reduces continuously. On the secondary side, the current "i_s" will enter through the dot end of the high-frequency transformer (HFT) as "i_r" > "i_m" and the current flow through the body diode of switch S_4, as shown in Fig. 5.5 (a). The resonant capacitor voltage increases sinusoidally, lagging "i_r" by 90^o as shown in Fig. 5.6. As the resonant tank releases energy, the current "i_r" decreases until it equals "i_m", causing "i_s" to increase from zero towards positive. This reversal occurs at $\omega_s t = \beta$ when S_4 conducts, as shown in Fig. 5.5 (b). From $\omega_s t = \alpha$, the tank circuit starts to store energy, and current "i_r" increases from zero towards positive. As the current "i_r" reverses its direction, S_1 will conduct as shown in Fig. 5.5 (c). Since the body diodes of the active switches (S_1 and S_4) conduct before the switch, the switches are turning on with ZVS.

5.4.2 Interval II: ($T_1 - T_2$)

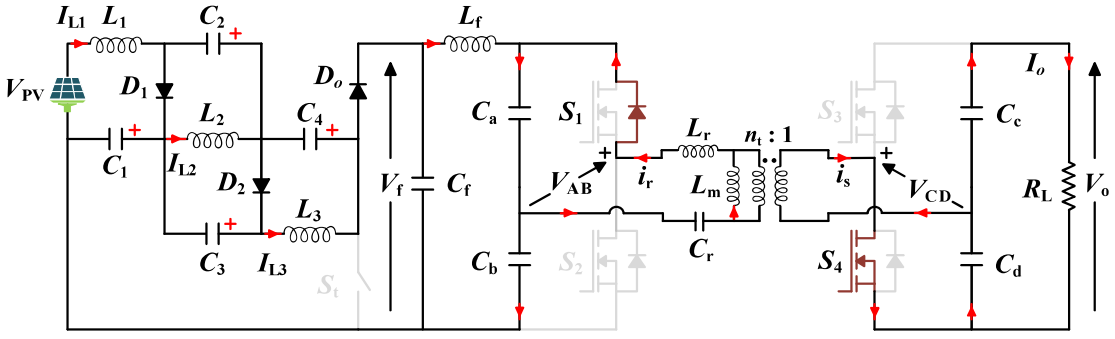
Interval II begins when S_t stops receiving gating signals, causing the inductors of the EIIS network to discharge during the remaining intervals. The rest of the converter's operation is similar to that in Interval I.

5.4.3 Interval III: ($T_2 - T_3$)

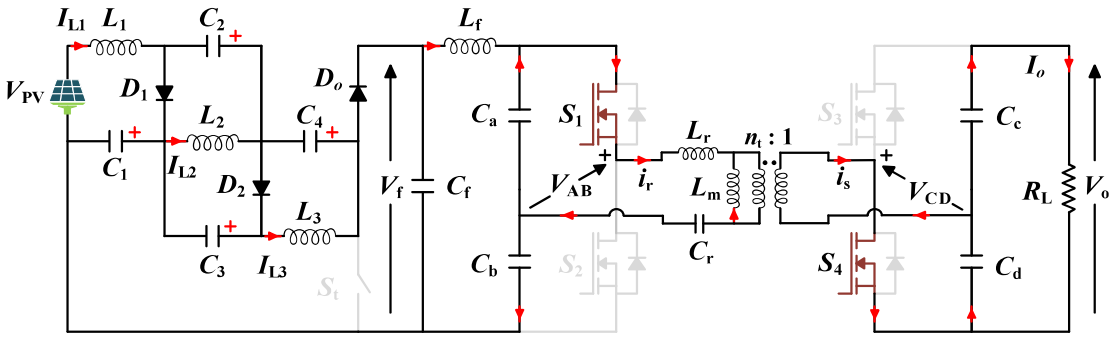
Interval III begins when the gating signal V_{GS4} is removed from S_4 and V_{GS3} is given to S_3, making the bridge voltage "V_{CD}" positive. Due to the given direction of the "i_s", the body diode of S_3 will carry the current, as shown in Fig. 5.5 (d) and Fig. 5.6. Since the switching is symmetrical after half of the cycle, the rest of the operation for intervals IV and V can be explained similarly.



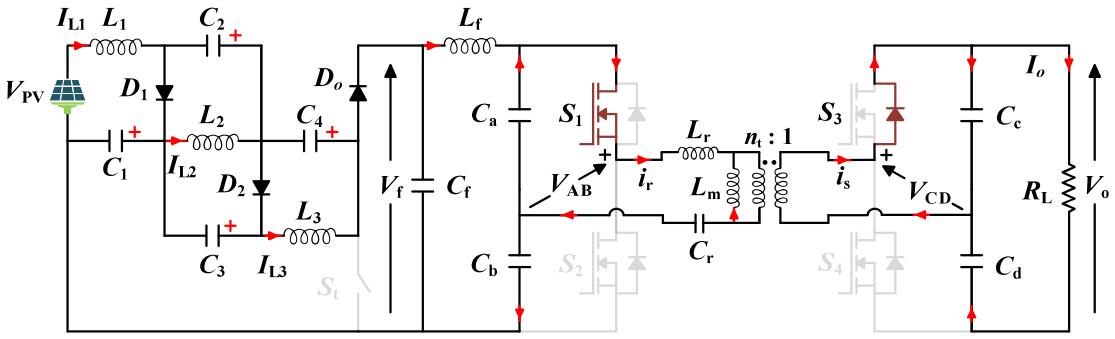
(a)



(b)



(c)



(d)

Fig. 5.5 Equivalent circuit diagram of the EIISIRC in (a)-(d) Interval-I to Interval-V.

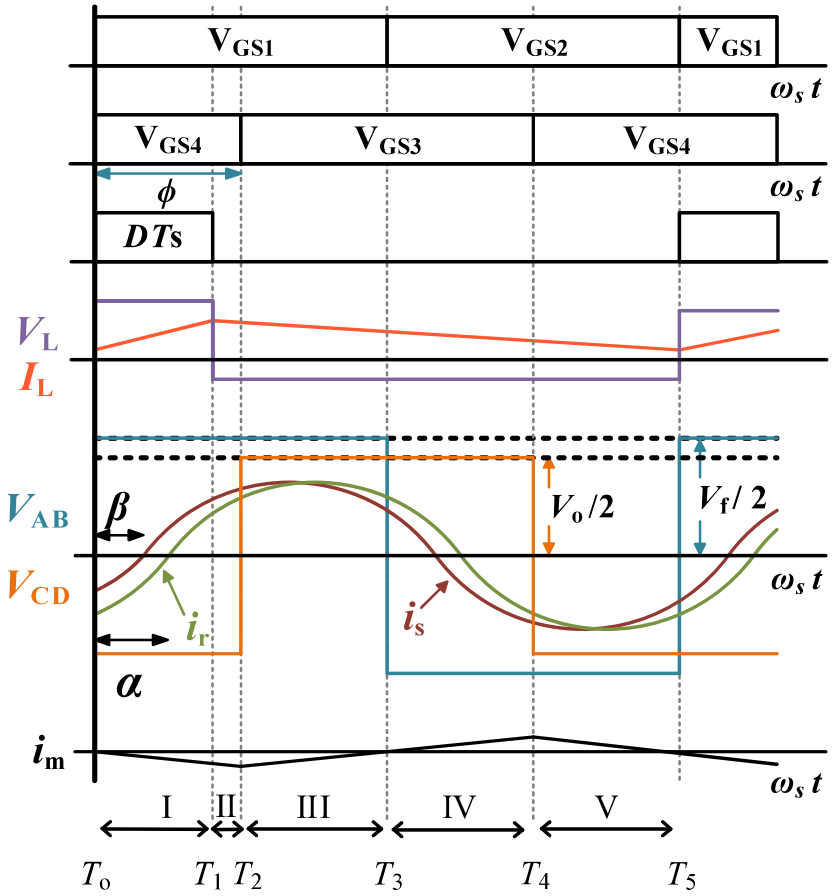


Fig. 5.6 Waveforms of the EIISIRC in steady-state condition.

5.5 PSO Algorithm for PSC

Particle swarm optimization is a swarm foraging-inspired computational technique discovered by Russell Eberhart and James Kennedy in 1995. The development of the PSO involves basic vector operation, leading to a fast-converging algorithm. In PSO, the particles are denoted as a candidate solution and represented as a position (x_i) and velocity vector (v_i).

These particles learn and update using their experience and experience of the swarm. Every candidate has a best position (P_{bi}) based on their experience. Similarly, there is a global best of the whole swarm (G_b). The position and velocity updates as per the mathematical equation given as:

$$v_i^{k+1} = wv_i^k + c_1r_1(P_{bi}^k - x_i^k) + c_2r_2(G_b^k - x_i^k) \tag{5.35}$$

$$x_i^{k+1} = x_i^k + v_i^{k+1} \tag{5.36}$$

For i = 1, 2, 3…. p (No. of particles).

Where k denotes the iterations and v_i^{k+1} and v_i^k is the velocity of particle i at iteration k+1 and k, x_i^{k+1} and x_i^k is the position of particle i at iteration k+1 and k, w is the inertia coefficient of particle, c_1 and c_2 are constant weighting factor, r_1 and r_2 are the random numbers (chosen between 0 and 1). c_1 and c_2 are cognitive and social learning coefficient that tries to move the particle towards personal and global best, respectively.

The step-by-step operation for the PSO-based MPPT algorithm used for the proposed converter is shown in Algorithm 1.

Algorithm 1 PSO-based Maximum Power Point Tracking

Input: Input Voltage and input current.

Initialization: Swarm size (p), position vectors (x_i), velocity vectors (v_i), inertia constant (ω), weighting factors (c_1 and c_2), and random numbers (r_1, and $r_2 \in (0,1)$).

Global Optimization

1: For each particle's given sampling time, input voltage and input current are sensed, and power is calculated.
2: The power value (Personal best P_b) is updated for each swarm only if the current value of power is greater than the previous value; otherwise, it remains the same.
3: At the end of each iteration, the personal best of each particle is compared with the previous global best (G_b), and G_b is updated only if it is lesser than the current personal best value of any swarm.
4: Based on steps 2 and 3, update each particle's position and velocity vectors using (21) and (22).
5: Repeat steps 1 to 4 until the algorithm is converged and global peak power is achieved.

Output: Based on the value of the G_b, Generate the duty cycle "D".

5.6 Design of the Converter

To ease the design calculation, the base parameters selected for the proposed converter are as follows-

$$V_B = V_f \ , \ Z_B = \sqrt{\frac{L_r}{C_r}} \ , \text{and } \omega_B = \omega_r \tag{5.37}$$

Here, V_B, Z_B, and ω_B denote the base voltage, base impedance, and base angular frequency in rad/sec. Using the above-mentioned base parameters, the resonant tank components can be normalized in per-unit values as follows-

$$X_{Lr,pu} = F \ , \ X_{Cr,pu} = 1/F \ , \ X_{Lm,pu} = F/K \tag{5.38}$$

For a given switching frequency (ω_s) and resonant frequency (ω_r), the normalized switching frequency (F) can be given as:

$$F = \frac{\omega_s}{\omega_r} \tag{5.39}$$

5.6.1 Modeling of the IRC

The resonant converter is analyzed using the fundamental harmonics approximation (FHA) technique. Under this technique, the resonant parameters are presented in the form of their fundamental switching frequency as the resonant tank acts like a band-pass filter. The bridge voltages V_{AB} and V_{CD} can be expressed as (5.40) and (5.41).

$$V_{AB} = \begin{cases} \frac{V_{PV}}{2} & 0 \le t < \frac{T_s}{2} \\ -\frac{V_{PV}}{2} & \frac{T_s}{2} \le t < T_s \end{cases} \tag{5.40}$$

$$V_{CD} = \begin{cases} \frac{V_o}{2} & \frac{\phi T_s}{2\pi} \le t < \frac{\phi T_s}{2\pi} + \frac{T_s}{2} \\ -\frac{V_o}{2} & 0 \le t < \frac{\phi T_s}{2\pi} \ , \ \frac{\phi T_s}{2\pi} + \frac{T_s}{2} \le t < T_s \end{cases} \tag{5.41}$$

The fundamental primary currents i_r can be calculated using the superposition principle in the equivalent circuit as (5.42).

$$i_{r,pu}(t) = i_{rp} \sin\left(\omega_s t - \alpha\right) \tag{5.42}$$

where $i_{rp} = \left(\frac{2\sqrt{1 + \lambda^2 - 2\lambda \cos\phi}}{\pi\left(F - 1/F\right)} \right)$

and $\alpha = \tan^{-1}\left(\left(\frac{\csc\phi}{\lambda} \right) - \cot\phi \right)$ (5.43)

'α' is the angle by which the current i_r lags behind V_{AB}.

Similarly, the fundamental secondary current can be derived as follows.

$$i'_{s,pu}(t) = i_{sp}\sin(\omega_s t - \beta) \tag{5.44}$$

where $i_{sp} = 2\dfrac{\sqrt{1+(\lambda X)^2 - 2\lambda X\cos\phi}}{\pi(F-1/F)}$

$$X = \left(\frac{F-1/F}{(F-1/F)\,||\,(F/K)}\right)$$

$$\beta = \tan^{-1}\left(\frac{(F/K)\csc\phi}{\lambda(F-1/F+F/K)} - \cot\phi\right) \tag{5.45}$$

'β' is the angle by which current i_s lags V_{AB}. The current i_s leads ahead bridge voltage V_{CD} by an angle 'θ' given as follows.

$$\theta = \phi - \beta = \tan^{-1}(\lambda X\csc\phi - \cot\phi) \tag{5.46}$$

The quality factor 'Q' can be given as follows.

$$Q = \pi^2 P Z_B / 2N^2 V_B^2 \tag{5.47}$$

5.6.2 Calculation of Voltage Gain and Power

The voltage gain can be calculated as (5.48).

$$\lambda = \frac{Z'_{ac,pu}\,||\,(F/K)}{(F-1/F)+Z'_{ac,pu}\,||\,(F/K)} = f(\theta) \tag{5.48}$$

Since the phase-shift angle is the controlling parameter for the power through the IDC. Using (5.46) and (5.48), voltage gain can be further modified as:

$$\lambda = \frac{\sin\phi}{Q(F-1/F)} \tag{5.49}$$

From (5.49), it can be seen that the converter gain depends upon the 'Q', 'F', and 'ϕ'. However, the L_m does not affect converter gain.

5.6.3 Soft-Switching Realization

The primary side active switches operate with ZVS when the i_r is inductive or $\alpha>0$. So, from (5.43), it must satisfy the condition that

$$\lambda < \sec\phi \tag{5.50}$$

As the minimum value of 'sec ϕ' is 1, primary active switches will operate with ZVS only when the $\lambda < 1$. The soft-switching operation of the primary bridge switches is independent of L_m. The active switches carry the secondary current in the opposite direction for the secondary side. So, for the secondary side active switches, ZVS can be observed when i_s leads V_{CD}, which means $\theta > 0$. From (5.45), it gives the condition as (5.51).

$$\lambda > \cos\phi / X \tag{5.51}$$

So, the secondary side switches will operate with ZVS only when $F > 1$.

5.7 Design of the Proposed Topology

In this section, a 500 W prototype will be designed for an input voltage of 60 V to provide an output voltage of 120 V (assuming the DC link voltage of 120 V ± 2.5 % ripple factor). The proposed topology will be able to harness solar power for a voltage range of 50 to 70 V. Based on the rating, the parameters of the proposed topology can be derived as follows.

5.7.1 Normalized Switching Frequency (F)

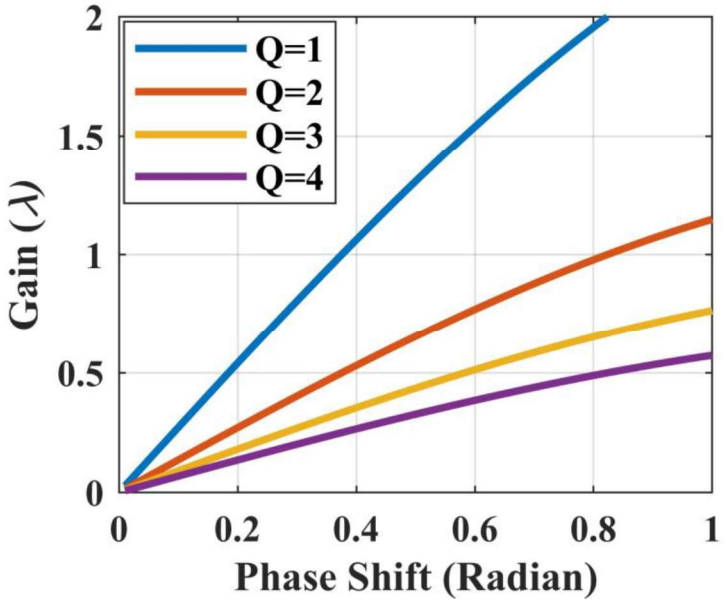
A precisely chosen normalized switching frequency can help operate the converter with soft switching. Further, the conduction losses can be minimized by optimizing the resonant currents, which are the function of the F. Considering soft-switching and losses for a fixed frequency switching of the converter, $F = 1.2$ is used for an optimal operation.

5.7.2 Gain (λ), turns ratio (n_t), and Inductance Ratio (K)

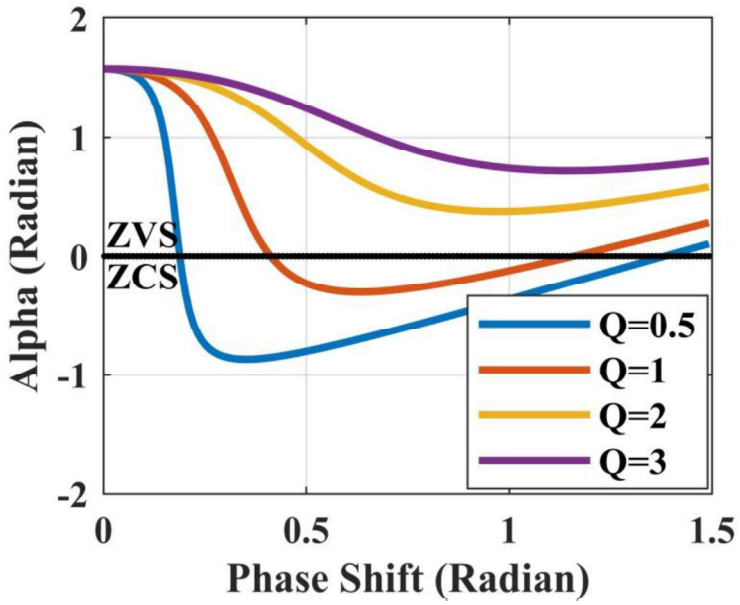
From the modeling shown earlier, it can be concluded that to operate the converter with ZVS, the gain must be $\lambda \leq 1$. So, the λ_{max} should be unity. The turns ratio 'n_t' can be increased further to obtain a higher DC link voltage per the requirement. Now, with known limits of converter gain, the turn ratio can be given as (5.52).

$$n_t = \frac{V_f \lambda_{max}}{V_{o\,max}} \tag{5.52}$$

Similarly, using (5.52), the minimum converter gain (for V_{DC} = 120 V-2.5 %) and corresponding inductance ratio can be calculated using (5.51) from the no-load condition as K = 0.1678.



(a)



(b)

Fig. 5.7 Effect of the quality factor on the variation of (a) Converter gain (λ) and (b) Angle alpha presenting ZVS range with phase shift angle (Radian).

5.7.3 Quality Factor

The quality factor plays a key role in deciding the size of the resonating components and the current through them. For a resonant converter, the size of the reactive component is

proportional to the quality factor. So, a small value of a quality factor is expected. In Fig. 5.7 (a), the converter gain vs. phase-shift angle curve is shown. It can be seen from the curve that for a low value of the quality factor, the converter gain increases rapidly, which is undesirable. To operate the converter with ZVS, the primary current angle (alpha) vs phase shift angle curve is drawn and shown in Fig. 5.7 (b). It can be observed from Fig. 5.7 (b) that when the quality factor is less than 2, the zero-voltage switching will be lost.

As the quality factor can't be a large value and for less than 2, zero voltage switching operation is lost, so an optimum value of 2 is selected for the operation of the proposed converter.

5.7.4 Resonant Components

Now, as the critical parameters are decided, the tank parameters can be determined as follows.

$$L_r = \frac{FZ_b}{2\pi F_s},\ C_r = \frac{F}{2\pi Z_b F_s},\ \text{and}\ L_m = \frac{L_r}{K} \tag{5.53}$$

5.7.5 Design of the EIIS Network Inductors

For n = 3 stages, since the current through each inductor remains constant, the inductors are designed by considering the ripple factor (%RF). The specific design for this case is as follows:

$$L_1 = L_2 = L_3 = \frac{D(1-D)V_{PV}}{f_s(1-3D)(\%RF)I_{L1}} \tag{5.54}$$

Similarly, the inductor for n stage EIIS can be calculated by

$$L_1 = L_2 = \ldots\ldots = L_n = \frac{D(1-D)V_{PV}}{f_s(1-nD)(\%RF)I_{L1}} \tag{5.55}$$

5.7.6 Design of Film Capacitors of the EIIS Network

The current carrying capacity per unit capacitance property for the required voltage rating is considered to replace the electrolytic capacitor with the film capacitor. The film capacitor has an RMS current rating of 1 A/μF. The film capacitors must carefully determine the minimum capacitance required for the given system. The minimum capacitance (C_k) value needed to

handle the rms value of capacitor current (I_{cap}) at a switching frequency (f_s), while maintaining a required voltage ripple factor (%RF) for capacitor voltage C_k and can be expressed as:

$$\left(C_k\right)_{\min} = \frac{I_{cap}}{2\pi f_s (\%RF) V_{ck}} \tag{5.56}$$

Where, k = 0, 1, 2……(2n-2).

5.7.7 Design of Film Capacitors (FC) of IRC

The FCs (C_a and C_b) take part in the resonance operation and are responsible for generating square signals across the bridge voltages. To eliminate the noise on the input side, the input FCs are calculated for a 2% ripple in V_{PV} as follows.

$$C_a = C_b = \frac{\left[I_{PV}\left(\pi - \phi\right) - i_{rp}\left(\cos\alpha + \cos\left(\phi - \alpha\right)\right)\right]}{\omega_s \Delta V_{Ca}} \tag{5.57}$$

Further, it is also desirable that C_a and C_b be equal and too large than the resonance capacitance C_r to avoid resonating interference. So,

$$C_a = C_b \simeq 100\, C_r \tag{5.58}$$

Based on the above constraints in (5.57) - (5.58), C_a and C_b of equal value 20 μF are selected.

Similarly, assuming the output current is ripple-free, the current via C_c and C_d when the switch S_3 is turned off will be equal to the output current for a duration of half the switching cycle. The ripple voltage of the C_c and C_d can be calculated as:

$$\Delta V_{C_c} = \Delta V_{C_d} \approx \frac{1}{C_c}\int_0^{T_s/2} I_o dt$$

$$C_c = C_d = \frac{I_o}{2\omega_s \Delta V_{C_c}} \tag{5.59}$$

From (5.59), the C_c and C_d are chosen to be approximately 20 µF.

Based on the given design calculation, the film capacitors are chosen from the MKP1848H series [155] and compared with the electrolytic capacitor series [156]. It is evident that the film capacitors are 10 times more compact than the electrolytic capacitor for the same voltage and current per unit capacitance rating.

Table 5.1 Comparative analysis

Parameters	[97]	[98]	[99]	[100]	[101]	[102]	[103]	[104]	[105]	[117]	EIISRIC
Switches	4	2	4	4	4	4	5	8	5	4	5
Diodes	4	3	3	3	4	7	6	0	2	4	3
Inductors	1	2	2	2	1	3	2	2	0	1	5
Capacitors	3(EC)	7 (EC)	4(EC)	4(EC)	3(EC)	3(EC)	3(EC)	3(EC)	4(EC)	4(EC)	10(FC)
Transformer	1	1	1	1	1	1	1	1	2	1	1
Voltage Gain	$\frac{2n_t}{(1-2D)}$	$\frac{n_t}{(1-2D)}$	$\frac{2}{n(1-2D)}$	$\frac{n_t}{(1-2D)}$	$\frac{2n_t}{(1-2D)}$	$\frac{n_t}{4(1-D)^2}$	$\frac{n_t}{2(1-D)}$	$\frac{n_t}{(1-2D)}$	$\frac{2n_t}{(1-2D)}$	n_t	$\frac{M}{(1-nD)}$
Soft Switching	Yes	yes	No	yes	No	No	No	No	Yes	Yes	Yes
Peak Efficiency	95.5%	NA	95%	89.06%	98.7%	95.9%	94.6%	NA	95%	95.8%	96.05%
Solar PV Integration	No	No	No	No	No	No	No	No	Yes	Yes	Yes
Algorithm	×	×	×	×	×	×	×	×	ST-MPPT	P&O	PSO
Time to reach GMPP	×	×	×	×	×	×	×	×	3s	×	0.72s

Table 5.1 compares the proposed topology with existing Topologies. [97]-[105], [117] uses vulnerable electrolytic capacitors which affects the overall life span of converter. In [97]-[104], presents an impedance based isolated DC-DC converter. However, these topologies have not been verified for the Solar PV integration. The topology presented in [101] achieves the highest efficiency; however, it lacks soft-switching capability, which increases stress on the components. Additionally, [101] employs less reliable electrolytic capacitors and does not validate its compatibility with solar PV systems, as it does not implement any MPPT algorithm for single- or multi-peak PV curves. Although [102] exhibits higher voltage gain characteristics, its topology lacks expandability, and the switches are not soft-switched, resulting in increased stress on components. Additionally, [102] has not been validated for PV integration. Only [105] and [117] incorporate solar PV integration, with [105] utilizing a grid-tied inverter and quasi-Z-source series resonant DC-DC converter that employs Shade Tolerant MPPT (ST-MPPT) to track global maxima under partial shading conditions, but requiring two transformers. In contrast, the proposed topology uses just one transformer and Particle Swarm

Optimization (PSO), which is simpler and faster than ST-MPPT. Similarly, [117] integrates solar PV but depends solely on the transformer turn ratio for voltage gain, limiting its suitability for wide input voltage variations, and employs the slow P&O algorithm, effective only for single-peak PV characteristics. The proposed converter achieves a peak experimental efficiency of 96.05%, which is comparable to other topologies. Thus, the proposed converter provides a more suitable and efficient solution for solar PV applications over a wide input voltage range, with improved reliability and longevity due to its use of film capacitors.

5.8 Experimental Verification

For experimental validation, a 500 W laboratory prototype of the EIISIRC is developed and tested for steady-state conditions, soft switching, uniform irradiance conditions (UIC), and partial shading conditions (PSCs). The photograph of the experimental prototype is shown in Fig. 5.8. The design parameters used in the experimental setup and PSO algorithm are shown in Table 5.2. Chroma's 62100H-600S solar PV emulator is used to emulate the PV curve, while the algorithm is implemented using a TI's microcontroller TMS320F28335 experimental kit.

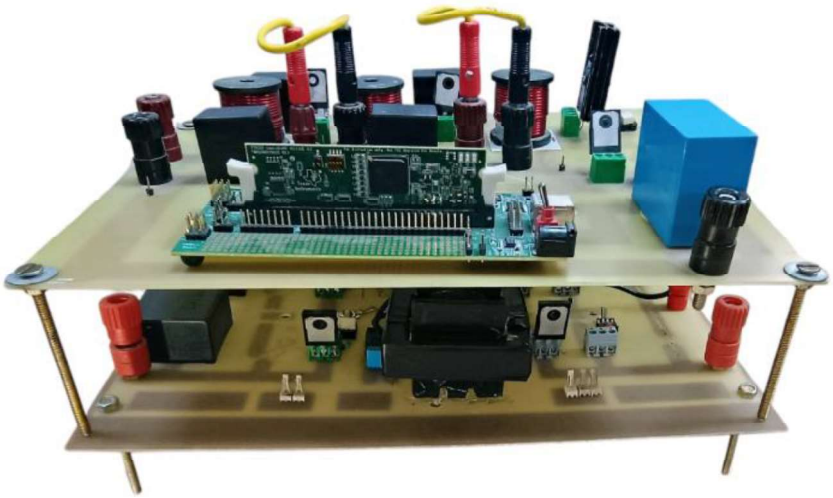


Fig. 5.8 Photograph of experimental Setup of EIISIRC.

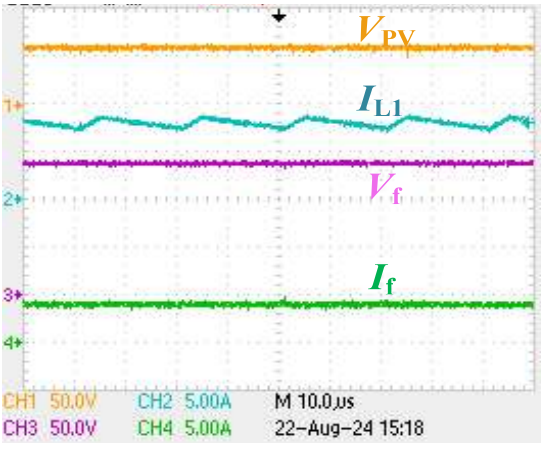
5.8.1 Steady State Results for Proposed Expandable Input Impedance Sourced Isolated Resonant Converter

Fig. 5.9 illustrates the performance of the EIISIRC system. In Fig. 5.9 (a), with an input PV voltage of 60 V and an inductor current (I_{L1}) of 8.33 A, the system achieves an output of 140

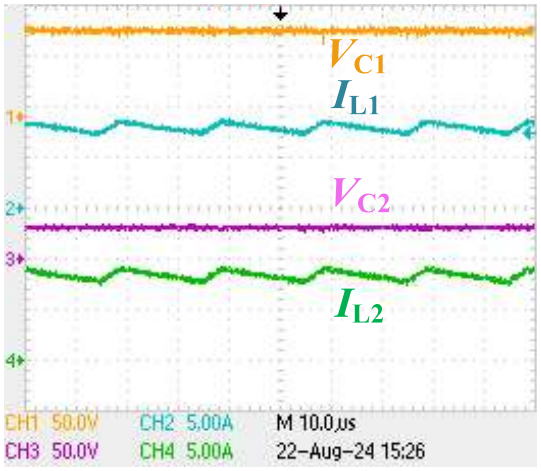
V and 3.4 A. Fig. 5.9 (b) displays the current and voltage stresses within the impedance network, showing V_{C1} at 86 V and V_{C2} at 26 V. Fig. 5.9 (c) depicts the voltage stress across the diodes, with V_{D1} and V_{D2} both at 120 V, along with the inductor current. Lastly, Fig. 5.9 (d) demonstrates the high gain capability of the EIIS network, where an input voltage of 60 V and a duty cycle of $D = 0.28$ enable the EIIS network to boost the input voltage up to 390 V.

Table 5.2 Design parameters of EIISIRC and PSO

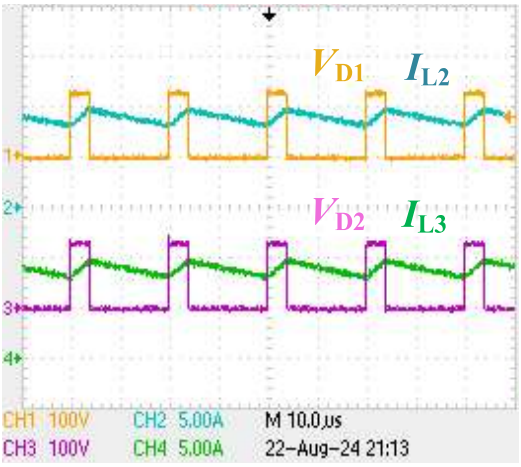
Parameters	**Value**	**Parameters**	**Value**
Input PV Voltage (V_{PV})	60 V	Particles	3
Output Voltage (V_o)	120 V	w	0.4
Output Power (P_o)	500 W	c_1	1.45
Switching Frequency (f_s)	50 kHz	c_2	1.63
Resonant inductor (L_r)	60.68 µH	r_1 and r_2	(0,1)
Parallel inductor (L_m)	292 µH	n_t	28:25
Resonant capacitor (C_r)	240.43 nF	C_a-C_d	20 µF
Inductors (L_1, L_2, and L_3)	560 µH	C_2-C_4	15 µF
C_1	20 µF	C_f	25 µF



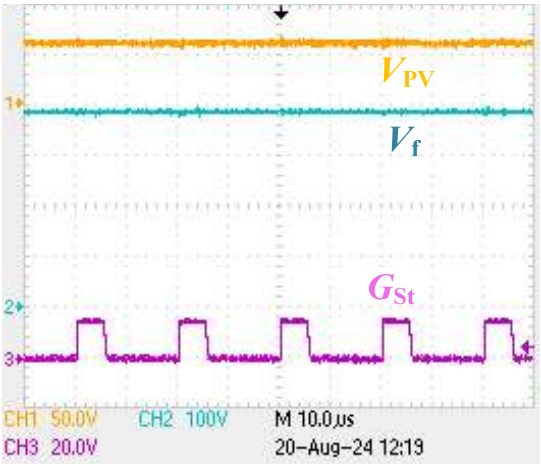
(a)



(b)

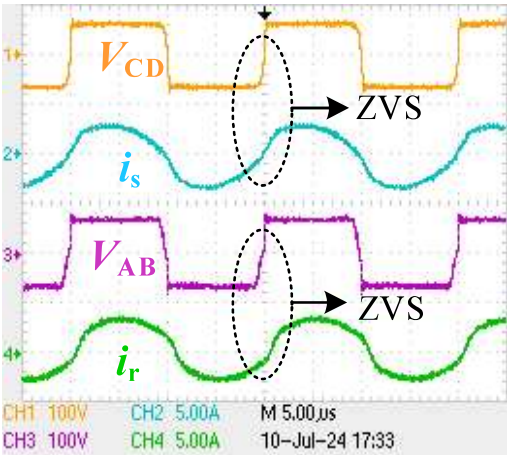


(c)

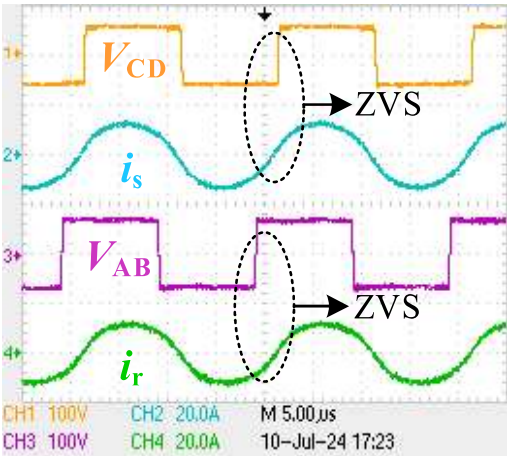


(d)

Fig. 5.9 Steady-state results of EIISIRC (a) Input and output characteristics. (b) Charging and discharging of capacitor voltage and inductor current of EIIS network (c) Voltage stress across diodes and inductor current of EIIS network. (d) The high gain capability of the EIIS network.



(a)



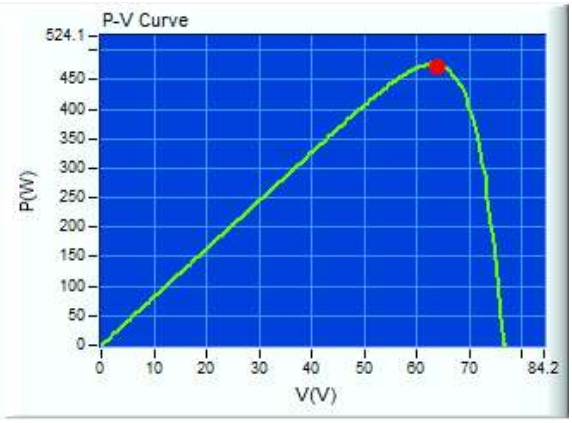
(b)

Fig. 5.10 Soft-switching results (a) at 20% loading (b) at 100% loading showing the bridge voltage (V_{AB} and V_{CD}) and their corresponding bridge currents (i_r and i_s), respectively.

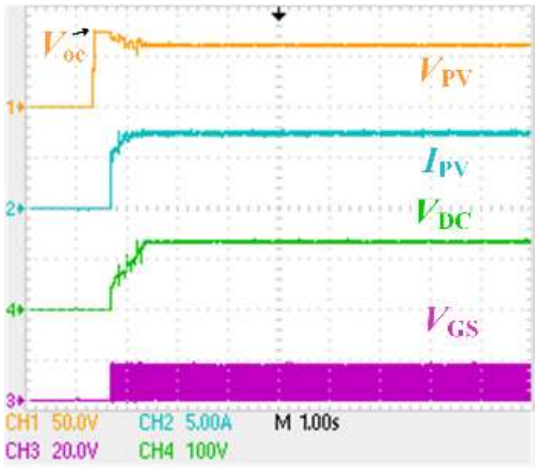
5.8.2 Experimental Results for Soft-switching

To exemplify the soft-switching operation of the IRC, experimental results for steady-state conditions are shown for 20% and 100% loading in Fig. 5.10. For the primary and secondary bridge switches, ZVS operation can be observed when the current in the active switch's lags behind their gating signal since the direct measurement of the switch current is not possible and requires to break the circuit. So, the soft-switching results (ZVS operation) are presented using the bridge voltage and corresponding bridge current. Also, it is worth noticing that the i_s will lead V_{CD} (instead of lagging for ZVS operation) as the current in secondary side switches are in opposite directions to the current i_s. In Fig. 5.10 (a)-(b), the IRC is operated to provide

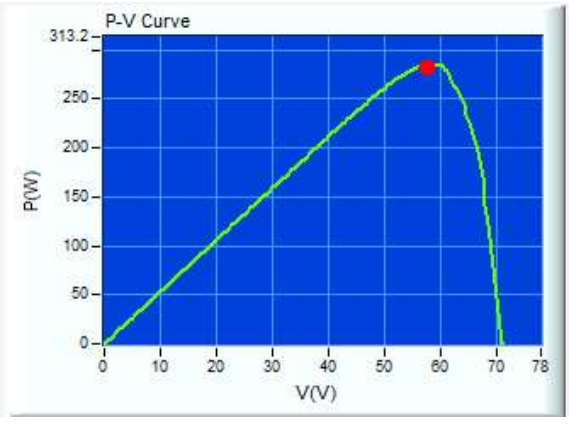
120 V (120 V ± 2.5 %) output at 500 W and 100 W. It can be observed from the experimental results that the active switches are turning on with ZVS.



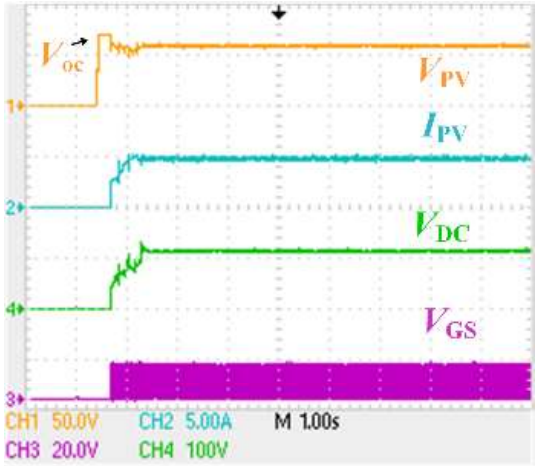
(a)



(b)



(c)



(d)

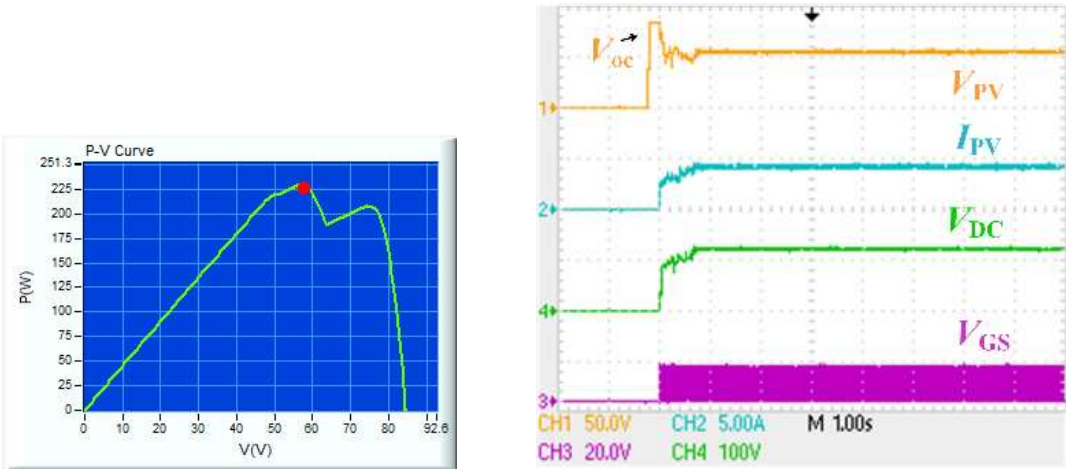
Fig. 5.11 Experimental results under UIC showing PV curves, their corresponding input voltage, input current, and output voltage with the gate signal VGS1 for (a) PVC-1, (b) Tracking results, (c) PVC-2, and (d) Tracking results.

5.8.3 Results Under Uniform Irradiance Conditions

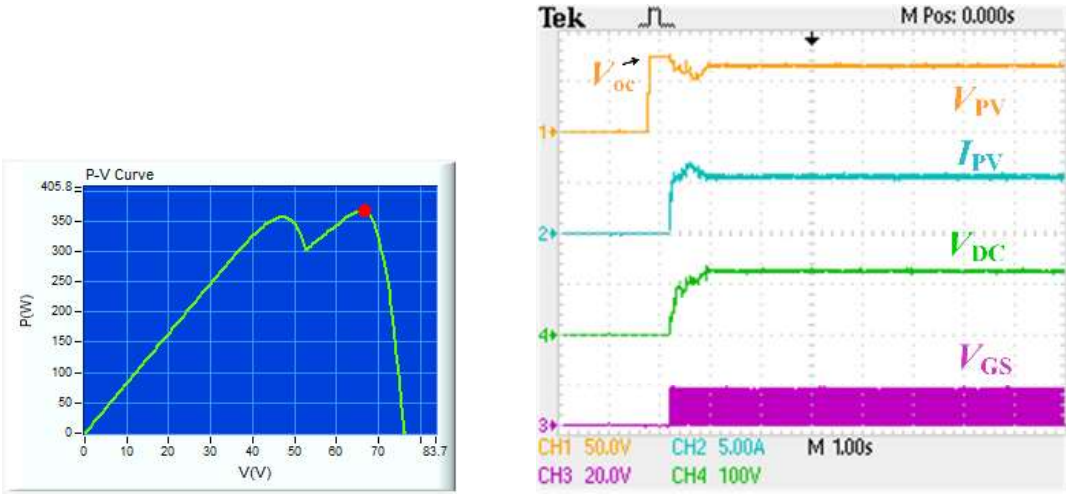
To exemplify the efficacy of the PSO algorithm, two PV curves (PVC-1 and PVC-2) are emulated using the PV emulator to test the uniform irradiance conditions. PVC-1 operates at a peak power of 476.4 W at 62.7 V with open circuit voltage (V_{oc}) at 76.5 V, as shown in Fig. 5.11 (a). The algorithm takes approximately 0.72 s to detect the global peak power point for PVC-1, as shown in Fig. 5.11 (b). PVC-2 operates at a peak power of 284.8 W at 58 V with V_{oc} of 70.9 V, as shown in Fig. 5.11 (c). The algorithm takes approximately 0.64 s to detect the peak power point, as shown in Fig. 5.11 (d) for PVC-2.

5.8.4 Results Under Partial Shading Conditions and Dynamic Irradiance Conditions

For testing the PSCs, three PV curves (PSC-1 to PSC-3) are emulated using the solar PV emulator. PVC-1 operates at a global maximum power (GMP) of 228.5 W at 55.7 V with V_{oc} of 84.2 V, as shown in Fig. 5.12 (a). The local maximum power (LMP) can be observed at 207.6 W at 74.32 V. The algorithm takes approximately 0.76 s to detect the GMP point, as shown in Fig. 5.12 (a). PSC-2 operates at a GMP of 368.9 W at 66.5 V with V_{oc} of 76 V, as shown in Fig. 5.12 (b). The LMP can be observed at 356.1 W at 47.51 V. The algorithm takes 0.72 s to detect the GMP point, as shown in Fig. 5.12 (b).



(a)

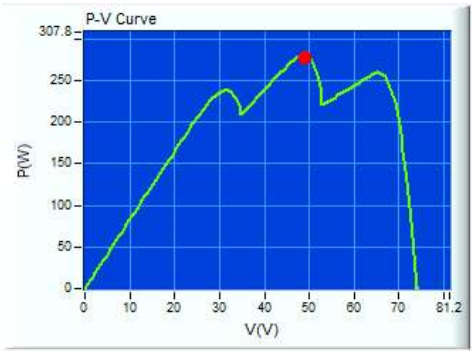


(b)

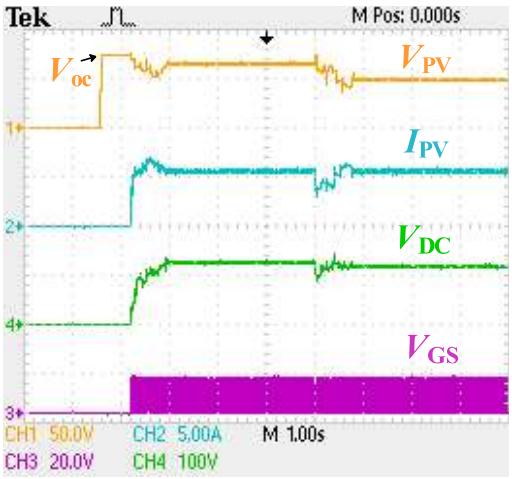
Fig. 5.12 Experimental results for PSCs showing PV curves along with the corresponding experimental results, illustrate the input voltage, input current, and output voltage with the gate signal V_{GS1} for (a) PSC-1 and (b) PSC-2.

For dynamic irradiance behavior, the shading pattern is changed from PSC-2 to PSC-3 and PSC-3 to PSC-1. PSC-3 has a GMP of 279.8 W at 48.9 V with a V_{oc} of 73.9 V, as shown in Fig. 5.13 (a). The experimental results corresponding to the dynamic change in irradiance are shown in Fig. 5.13 (b)-(c). When PSC-2 is applied, the duty varies to detect the GMP, and it takes approximately 6-8 iterations to reach GMP. When a change in irradiance is sensed due to a change in shading pattern, the duty cycle varies to search for the new global peak power again. The algorithm repeats the process till the convergence is achieved. A similar process can be observed when the shading pattern is changed from PSC-3 to PSC-1. It can be concluded

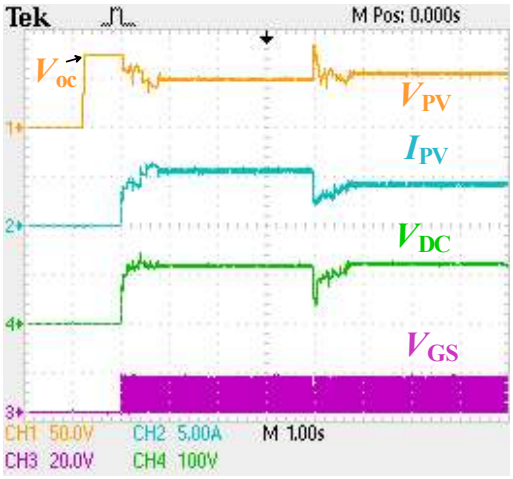
from the experimental results of the UIC and PSC tests that the algorithm tracks the peak power with no oscillation in steady-state waveforms.



(a)



(b)

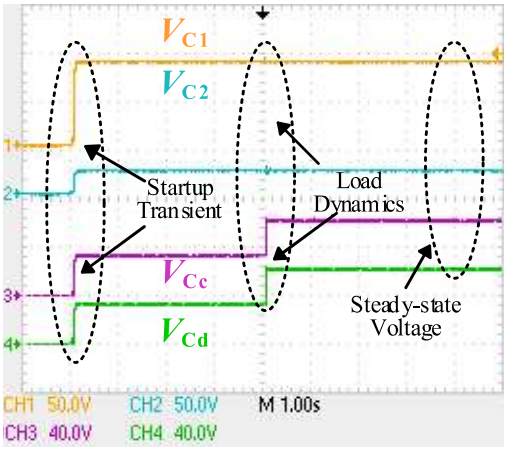


(c)

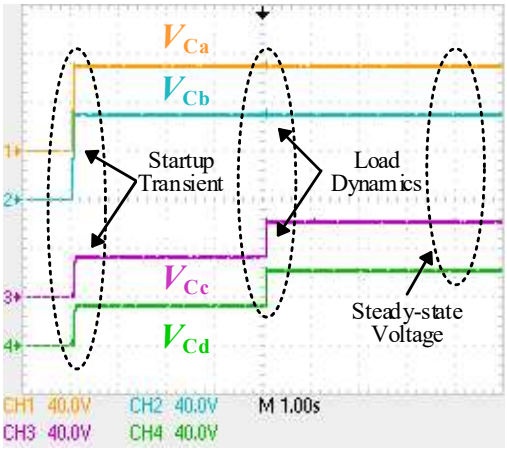
Fig. 5.13 Experimental results showing dynamic irradiance (a) PSC-3. (b) Change in shading patterns from PSC-2 to PSC-3 (c) Change in shading patterns from PSC-3 to PSC-1 showing input voltage, input current, and output voltage with gate signals V_{GS1}.

5.8.5 Verification of Film Capacitor Usage

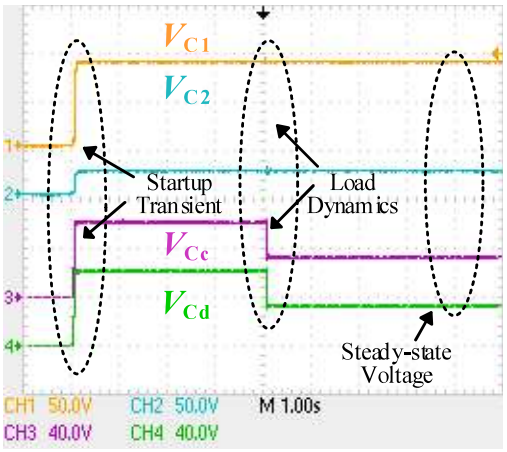
Fig. 5.14 highlights the performance of film capacitors in the proposed EIISIRC, comparing them to traditional electrolytic capacitors. FCs exhibit superior performance such as reliability, lifespan, size, and power density. To further validate the practicality of using FCs, voltage measurements were recorded across the capacitors under various conditions, including startup transients, load dynamics, and steady-state operations, as shown in Fig. 5.14 (a)-(d). Fig. 5.14 (a) illustrates the performance of the film capacitor when there is a sudden load increase of 50%. Here, Fig. 5.14 (a) represents the effect of the load change on the DC-link capacitors (C_c and C_d) along with the capacitors of the EIIS network (C_1 and C_2). On the other hand, Fig. 5.14 (b) represents the effect of the load change on the DC-link capacitors (C_a and C_b) along with the capacitors of the IRC (C_c and C_d). Similarly, Fig. 5.14 (c) and 5.14 (d) represent the performance of the film capacitor when there is a sudden load increase of 50%.



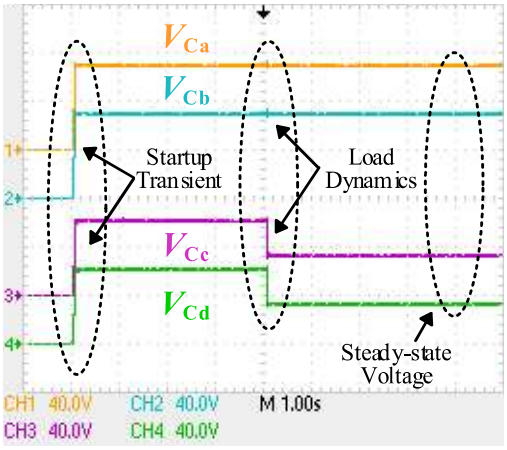
(a)



(b)



(c)



(d)

Fig. 5.14 Film capacitor voltages during startup transients, load dynamics, and steady-state conditions (a) V_{C1}-V_{C2} and V_{Cc}-V_{Cd} voltage for 50% step load increase (b) V_{Ca}-V_{Cd} voltage for 50% step load increase (c) V_{C1}-V_{C2} and V_{Cc}-V_{Cd} voltage for 50% step load decrease and (d) V_{Ca}-V_{Cd} voltage for 50% step load decrease.

From Fig. 5.14, it is evident that the FC voltages remain stable and free from oscillations under dynamic load changes. The various tests and experimental results confirm the feasibility of using FCs for the EIISIRC.

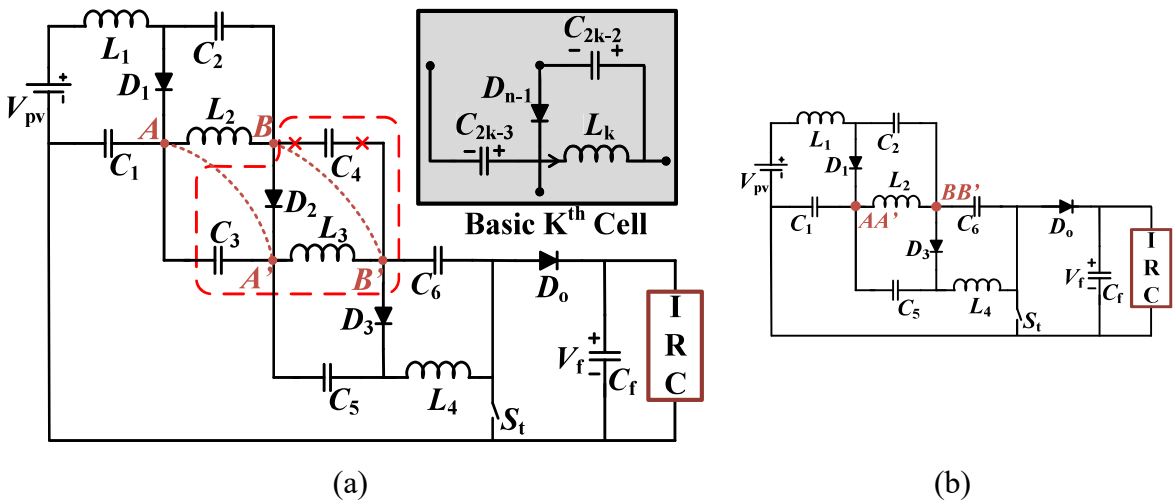
5.9 Design Flexibility with the EIIS and Integration with Grid System

As mentioned earlier, to match the voltages with existing utility levels, a high gain DC-DC converter or an impedance network is often incorporated at the input stage. It can be seen from the proposed configuration; the input impedance network efficiently steps up the low PV input voltage to the required voltage level depending upon the number of cells. As the number

of cells changes, the voltage gain changes accordingly as shown in (5.29). Now, if we need to feed solar power to a low-voltage or high-voltage DC/AC microgrid, the cell structure can be managed accordingly to get the desired voltage level. Now, since the MPPT algorithm is applied to the expandable network and hence its output varies depending upon the duty ratio and input voltage, an extra converter is further needed to feed the solar power to the DC grid at a DC voltage level. So, considering the safety feature, the proposed isolation resonant converter is added at the output of the expandable impedance network.

Furthermore, impedance networks inherently protect against shoot-through faults or short circuits caused by misfiring, enhancing the system's resilience against electromagnetic interference (EMI). So, the expandable design enables us to attain different voltage gain characteristics with the introduction of cells at each stage. Beside these advantages, if any element of n-cell network gets damaged (suppose C_4 gets damaged), then the damaged cell can be removed (by short circuiting the terminals of previous cell with cell next to faulty cell as shown in Fig. 5.15 (a)) and operated as n-1 cell enabling the uninterrupted operation for the proposed configuration as shown in Fig. 5.15 (b).

Now, as far as the AC grid integration is considered, the impedance network (EIIS) can be adapted for getting high gain at the DC link which can be further cascaded with the inverter system. The isolated resonant converter can be used as an intermediate DC-DC converter for a battery storage system for charging the battery using the solar power or AC grid under the absence of the solar power under closed loop control system. However, if the combined EIISIRC converter is adapted with inverter cascaded structure, it would be a costly system hence not preferable for AC grid system.



(a) (b)

Fig. 5.15 Expandable network (a) With fault (b) Without fault in C_4

5.10 Conclusion

This chapter presents an expandable input impedance-sourced isolated resonant converter (EIISIRC) designed for optimal performance under partial shading conditions (PSCs) using particle swarm optimization (PSO). The converter's expandable impedance network enables scalable voltage gain, where each added cell modifies the gain by a factor of $1/(1-nD)$. The proposed design utilizes an isolated resonant converter (IRC) for galvanic isolation, optimized for zero voltage switching via the first harmonics approximation (FHA) technique. Employing film capacitors for voltage smoothing improves the converter's reliability, lifespan, and compactness. This concept is validated by integrating the converter with a solar photovoltaic (PV) system using a particle swarm optimization (PSO)-based maximum power point tracking (MPPT) algorithm. This integration effectively tracks the global peak power within 0.72 seconds under multi-peak PV characteristics induced by partial shading conditions (PSCs). A comparative analysis with existing topologies demonstrates the unique advantages of the proposed EIISIRC, notably its use of film capacitors and the PSO algorithm for rapid peak power tracking. The converter's integrability is further validated through a 500 W experimental prototype tested under steady-state, uniform irradiance, and partial shading conditions.