Chapter 3

Effect of Gate Oxide Stacking on the Electrical Performance Characteristics of Source Pocket Engineered GaSb/Si Heterojunction Vertical TFETs

3.1 Introduction

The literature review carried out in Chapter-1 shows that the lateral/vertical gate-oxide stacking based TFETs as shown in Fig. 1.16 of Chapter-1 have superior performance characteristics in the form of higher drive current, steeper SS and smaller ambipolar conduction over the conventional homogeneous gate-oxide based TFETs [70],[99],[112],[127],[132],[142]. The use of the lateral/vertical gate oxide stacking in the TFETs enhances their drive current without affecting the OFF-state leakage current [51],[70],[118],[122]. Both the lateral and vertical gate-oxide stacking based heterogeneous gate-oxide structures influence the overall electric field and intrinsic gate capacitances and hence the RF performance parameters of the TFETs. The results of Chapter-2 also show that the source pocket engineering improves the performance of GaSb/Si heterojunction VTFETs. In view of the above, the present chapter is devoted to analyze the effect of gate oxide stacking (lateral/vertical) on the performance of source pocket engineered (SPE) GaSb/Si heterojunction (HJ) VTFETs (SPE GaSb/Si HJ VTFETs). The device-level performance of the proposed SPE GaSb HJ VTFETs has been investigated by using the commercially available SILVACO ATLAS^{TM} device simulator software. The layout of the present chapter is given as follows:

Section 3.2 deals with simulation methodology for the presented VTFETs in the same

manner as discussed in Chapter 2. The Section 3.3 presents results and discussions regarding the effects of different gate oxide stacking on device level performance of the presented VTFETs where the electrical performance characteristics such as drain current, SS, I_{ON}/I_{OFF} ratio, transconductance (g_m), output conductance (g_d), intrinsic gate to drain capacitance (C_{gd}), intrinsic gate to source capacitance (C_{gs}), cut-off frequency (f_T), gain bandwidth product (GBP), transconductance generation factor (TGF), and transconductance frequency product (TFP) have been analyzed. Finally, Sec. 3.4 includes the summary and conclusion of the present chapter.

3.2 Proposed Structures and TCAD Simulation Details

The proposed TFET structure with associated device parameters used for the TCAD simulation study are discussed. Possible fabrication feasibility and simulation methodology are also discussed in this section.

3.2.1 Proposed Device Structures

Fig 3.1 shows source pocket engineered (SPE) GaSb/Si heterojunction (HJ) vertical TFET (VTFET): (a) without any gate oxide stacking (SPE GaSb/Si HJ VTFET), (b) with vertical gate oxide stacking structure (SPE GaSb/Si HJ VTFET with VS), and (c) with lateral gate oxide stacking structure (SPE GaSb/Si HJ VTFET with LS) presented for the TCAD simulation in this study and their cross-sectional views are depicted in Fig. 3.1 (d), (e), and (f) respectively. The models used to simulate the presented VTFETs are same as discussed in Chapter-2. The models are non-local band-to-band tunneling (BTBT) model (to include local variation in the energy band for better accuracy); Shockley-Read-Hall model (to include the carrier generation-recombination phenomenon); band gap-narrowing model (to incorporate the heavy doping effects on

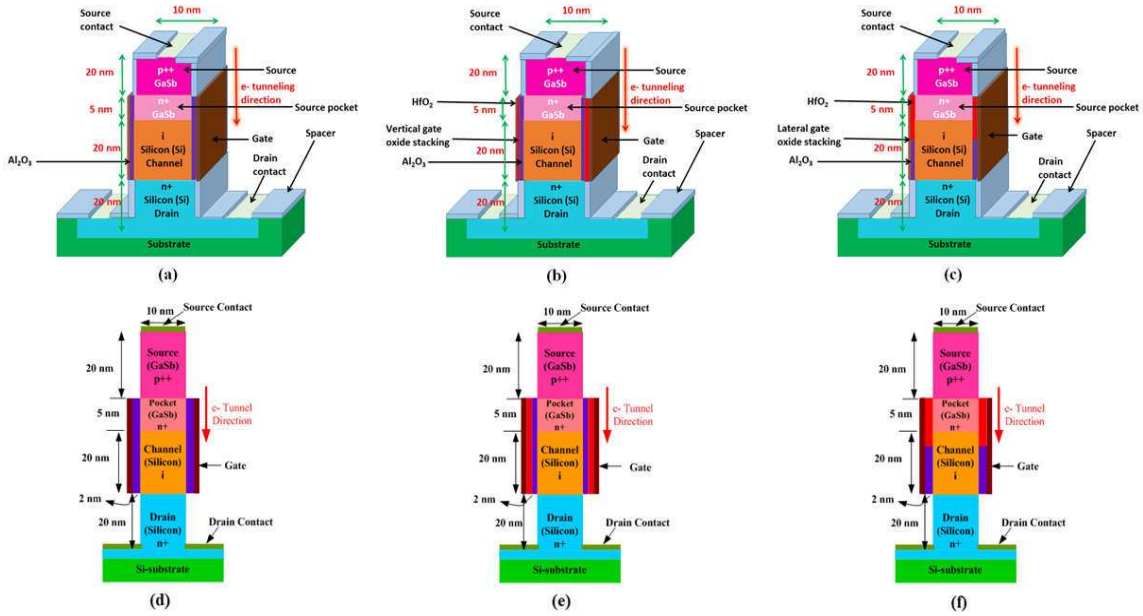

Fig. 3.1: Schematic representation of source pocket engineered GaSb/Si heterojunction vertical TFET without gate oxide stacking (SPE GaSb/Si HJ VTFET), (b) with vertical gate oxide stacking (SPE GaSb/Si HJ VTFET with VS), and (c) with lateral gate oxide stacking (SPE GaSb/Si HJ VTFET with LS); Cross sectional view of (d) SPE GaSb/Si HJ VTFET (e) SPE GaSb/Si HJ VTFET with VS and, (f) SPE GaSb/Si HJ VTFET with LS.

the bandgap of source, drain and pocket regions); field-dependent mobility model (to consider field dependent carrier velocity); Auger recombination model (to include non-radiative recombination processes), and the Fermi-Dirac statistics (for carrier distribution in various regions of the device). Uniform doping concentrations in various regions of the device are assumed. A donor doping concentration (N_D) of $5x10^{18}$ /cm^3 is considered for the drain region to reduce ambipolar effect in the TFET as discussed in Chapter-2 [59]. The important point to remember is that SPE GaSb/Si HJ VTFET is the same device which is considered in Chapter-2 with Al_2O_3 (green color as shown in Fig. 3.1) as only gate oxide having a thickness of 2 nm with dielectric constant of 9.3. In

TABLE 3.1

DEVICE DESIGN PARAMETERS OF THE SOURCE POCKET ENGINEERED GASB/SI HETEROJUNCTION VERTICAL TFETS WITH AND WITHOUT GATE OXIDE STACKING

Parameters	**SPE GaSb/Si HJ VTFET**	**SPE GaSb/Si HJ VTFETs with VS/LS**
Source region doping (N_A)	2×10^{19} cm^{-3}	2×10^{19} cm^{-3}
Pocket region doping (N_D)	7×10^{18} cm^{-3}	7×10^{18} cm^{-3}
Channel region doping (N_A)	5×10^{16} cm^{-3}	5×10^{16} cm^{-3}
Drain region doping (N_D)	5×10^{18} cm^{-3}	5×10^{18} cm^{-3}
Channel thickness (t_{Si})	10 nm	10 nm
Work function of gate material (Φ_m)	4.2 eV	4.2 eV
Gate dielectric constant of Al_2O_3 (ε)	9.3	9.3
Gate dielectric constant of HfO_2 (ε)	-	25
Gate region length (L_G)	25 nm	25 nm
Source region length (L_S)	20 nm	20 nm
Drain region length (L_D)	20 nm	20 nm
Tunnel mass of hole in GaSb (m_{htGaSb})	$0.4m_o$	$0.4m_o$
Tunnel mass of electron in GaSb (m_{etGaSb})	$0.0410m_o$	$0.0410m_o$
Tunnel mass of hole in silicon (m_{htSi})	$0.24m_o$	$0.24m_o$
Tunnel mass of electron in silicon (m_{etSi})	$0.20m_o$	$0.20m_o$
Pocket length (GaSb)	5 nm	5 nm
Lattice constant of GaSb	6.09 ^{0}A	6.09 ^{0}A
Lattice constant of Si	5.43 ^{0}A	5.43 ^{0}A
Bandgap energy GaSb	0.70 eV	0.70 eV
Bandgap energy Si	1.12 eV	1.12 eV
Electron affinity GaSb	4.06 eV	4.06 eV
Electron affinity Si	4.05 eV	4.05 eV

case of SPE GaSb/Si HJ VTFET with VS, Al_2O_3 and HfO_2 (purple color as shown in Fig. 3.1 with dielectric constant 25) of 1 nm thickness each are vertically stacked to form total gate oxide thickness of 2 nm [127,[132]. On the other hand, Al_2O_3 and HfO_2 of 2 nm thickness each are laterally stacked to form the resultant heterogeneous gate oxide thickness of 2 nm in the SPE GaSb/Si HJ VTFET with LS [70],[92],[112]. Other models related to simulation are same as that of the models considered in Chapter-2. Optimized device design parameters of the presented VTFETs are listed in Table-3.1.

Recently researchers have grown Al_2O_3 and HfO_2 directly on silicon substrate. Therefore, effective oxide thickness (EOT) formula used is given below. Using the formula written below calculations of EOT for both vertical stacking and lateral stacked VTFETs were carried out. The thickness of the dielectric layer has been depicted in Fig. 3.1. For vertical stacking Al_2O_3 and HfO_2 have been taken of 1 nm each and for lateral stacking, Al_2O_3 and HfO_2 of 2 nm each laterally placed to each other. EOT for lateral stacked VTFET is found to be 1.42 nm and EOT for the lateral stacked VTFET at source side consisting of HfO_2 dielectric is found to be 0.84 nm using the Eq. (3.1).

$$EOT = t_{HfO2} \; X \; \frac{k_{Al2O3}}{k_{HfO2}} + t_{Al2O3} \tag{3.1}$$

Where t_{HfO2} – thickness of HfO_2, t_{Al2O3} – thickness of Al_2O_3, k_{HfO2} – dielectric constant of HfO_2 (22), k_{Al2O3} – dielectric constant of Al_2O_3 (9.3).

3.2.2 Possible Fabrication Steps of the Proposed TFETs Structures

The fabrication process flow depicted in Fig. 3.2 and Fig. 3.3 is similar as described in Chapter-2. The n^+ drain and *i*-Si channel region may be successly grown on a clean Si substrate by the MBE or LPCVD method as discussed in Chapter-2. GaSb layers for the

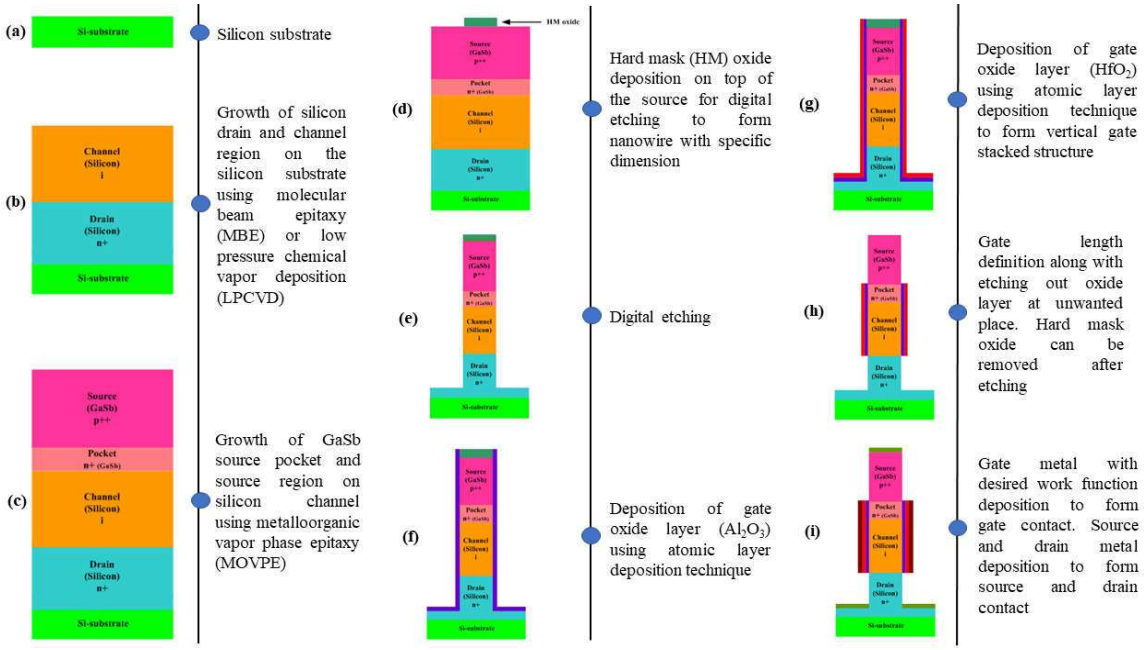

Fig. 3.2: Fabrication steps of GaSb/Si heterojunction vertical TFET with source pocket with vertical gate oxide stacked structure (SPE GaSb/Si HJ VTFET with VS) in 2D view (a) Starting with a silicon (Si) substrate, (b) growth of silicon in drain and channel region on the silicon substrate using molecular beam epitaxy (MBE) or low-pressure chemical vapor deposition (LPCVD), (c) growth of GaSb source pocket and source region on silicon channel using metalloorganic vapor phase epitaxy (MOVPE), (d) Hard mask (HM) oxide deposition on top of the source for digital etching to form width of the vertical TFET with specific dimension, (e) digital etching, (f) deposition of gate oxide layer (Al_2O_3) using atomic layer deposition (ALD) technique, (g) deposition of gate oxide layer (HfO_2) using atomic layer deposition technique to form vertical gate stacked structure, (h) gate length definition along with etching out oxide layer at unwanted place. Hard mask oxide can be removed after etching, (i) gate metal with desired work function deposition to form gate contact. Source and drain metal deposition to form source and drain contact.

source pocket and source region can then be grown on the channel layer using MOVPE method. Oxide hard mask (HM) is deposited on the top of the source layer to define vertical TFET width followed by the igital etching out of the rest portion to form the

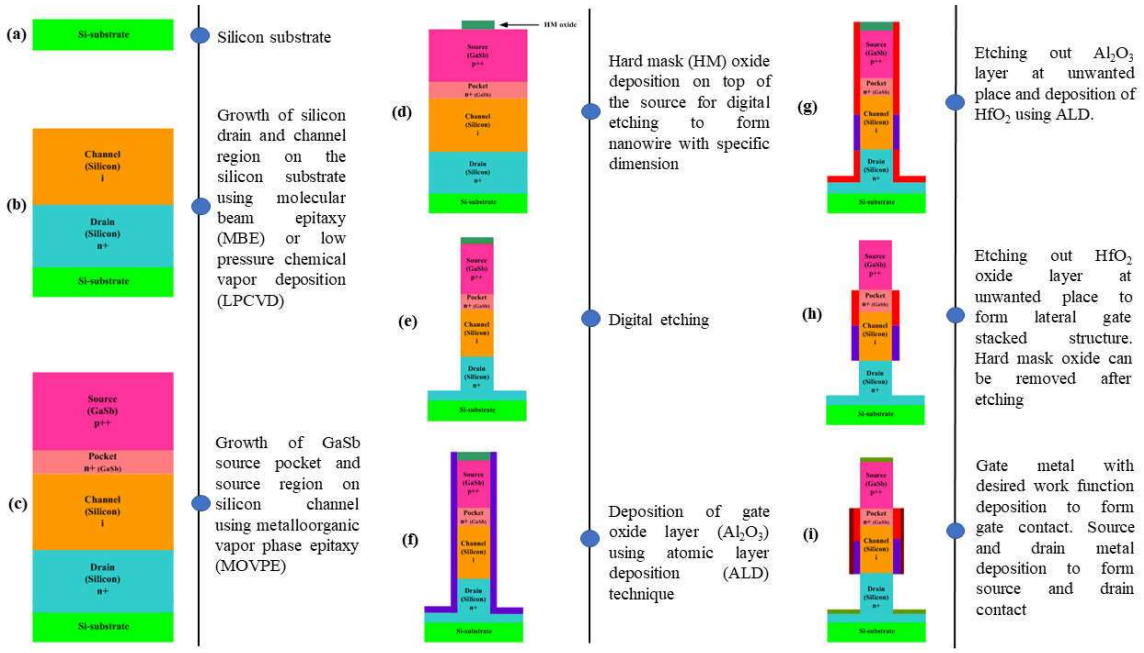

Fig. 3.3: Fabrication steps of GaSb/Si heterojunction vertical TFET with source pocket with lateral gate oxide stacked structure (SPE GaSb/Si HJ VTFET with LS) in 2D view (a) Starting with a silicon (Si) substrate, (b) growth of silicon in drain and channel region on the silicon substrate using molecular beam epitaxy (MBE) or low-pressure chemical vapor deposition (LPCVD), (c) growth of GaSb source pocket and source region on silicon channel using metalloorganic vapor phase epitaxy (MOVPE), (d) Hard mask (HM) oxide deposition on top of the source for digital etching to form width of the vertical TFET with specific dimension, (e) digital etching, (f) deposition of gate oxide layer (Al_2O_3) using atomic layer deposition (ALD) technique, (g) deposition of gate oxide layer (HfO_2) using atomic layer deposition technique to form lateral gate stacked structure, (h) etching out HfO_2 oxide layer at unwanted place to form lateral gate stacked structure. Hard mask oxide can be removed after etching, (i) gate metal with desired work function deposition to form gate contact. Source and drain metal deposition to form source and drain contact.

desired vertical double gate structure. The Al_2O_3 layer followed by HfO_2 layer can be deposited using ALD method to form lateral or vertical gate stacking structures. Oxide layer from the unwanted area can be removed by selective etching technique. The hard

mask can be removed after gate length defination. The gate electrode metal of required work function is then deposited for the gate contact. Ti/Au or Ni/Au can be deposited by sputtering methods for the drain and source contacts of the device.

3.2.3 Simulation Methodology

The proposed VTFET structure is simulated using SILVACO ATLAS^{TM} TCAD tool following same methodogy as described in Sec 2.2 of the previous chapter. Therefore, various models used in the TCAD tool for simulating the proposed structure are briefly discussed in the following.

The non-local band-to-band tunneling model (BBT.NONLOCAL) is used for including the local variation in the energy band and electric field in the tunneling path for improving the tunneling accuracy. The tunnelling area has been defined by using QTX.MESH and QTY.MESH models while the tunnelling direction is defined by QTUNN.DIR model as discussed in the last chapter. The non-local coupling model BBT.NLDERIVS is used to remove the convergence related issues. Effective masses of the electrons and holes are defined by ME.TUNNEL and MH.TUNNEL models respectively. The Fermi-Dirac statistic is defined through FERMI model for carrier concentration while the concentration-dependent Shockley-Read-Hall model CONSRH is used to define the carrier the generation-recombination process in the device as discussed in Sec 2.2. The AUGER model is used in the TCAD to include the effect of the Auger recombination phenomenon in the device. The Lombardi Mobility model (CVT) is used for the field-dependent mobility of the carriers in the semiconductors of the proposed device. The band gap narrowing model BGN is considered to include the effect of heavy doping in the source, drain and pocket regions of the device. The effects

traps at the source/channel heterojunction interface are included in the TCAD tools through the non-local trap assisted models TAT.NLDEPTH and TAT.RELEI. The pocket thickness of 5 nm is the same as considerd in Chapter-2.

3.3 Results and Discussion

This section analyses electrical performance parameters such as drain current, output current, SS, I_{ON}/I_{OFF} ratio, transconductance (g_m), output conductance (g_d), intrinsic gate to drain capacitance (C_{gd}), intrinsic gate to source capacitance (C_{gs}), cut-off frequency (f_T), gain bandwidth product (GBP), transconductance generation factor (TGF), and transconductance frequency product (TFP) for SPE GaSb/Si HJ VTFET, SPE GaSb/Si HJ VTFET with VS, and SPE GaSb/Si HJ VTFET with LS.

3.3.1 DC Performance analysis

Fig. 3.4(a) shows the surface potential whereas Fig. 3.4(b) shows the electric field distribution of the presented VTFETs. Surface potential is found to be maximum for the SPE GaSb/Si HJ VTFET with LS followed by SPE GaSb/Si HJ VTFET with VS. Minimum value of surface potential can be observed for the device with homogeneous gate dielectric or with any gate stacking based SPE GaSb/Si HJ VTFET. The reason for higher surface potential for the gate stacked TFETs is due to greater amount of induction in charge by the gate at the heterojunction formed between GaSb and Si with the presence of high-*k* gate oxide. Electric field is also found to be following the same trend as of surface potential because it is directly proportional to electric field and found maximum for SPE GaSb/Si HJ VTFET with LS and minimum for SPE GaSb/Si HJ VTFET. The reason for the higher electric field and surface potential for the SPE GaSb/Si HJ VTFET with LS than SPE GaSb/Si HJ VTFET with VS can be attributed to

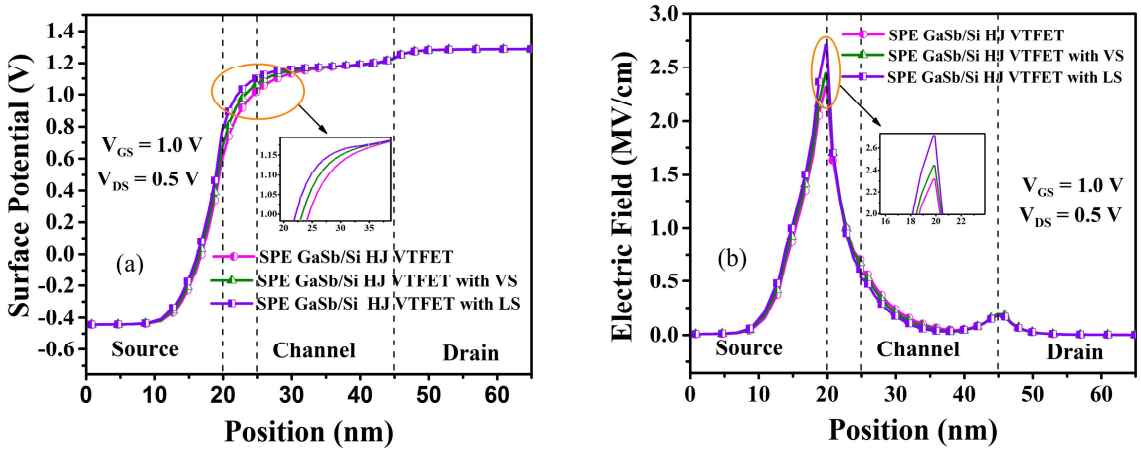

Fig. 3.4: Comparison of (a) surface potential and (b) electric field in ON-State for SPE GaSb/Si HJ VTFET, SPE GaSb/Si HJ VTFET with VS, and SPE GaSb/Si HJ VTFET with LS.

direct influence of the high-*k* present above the channel in the SPE GaSb/Si HJ VTFET with LS. In case of SPE GaSb/Si HJ VTFET with VS, the vertical stacking where high-*k* is placed over the low-k is somehow reducing the charge induction mechanism compared to SPE GaSb/Si HJ VTFET with LS.

The energy band diagram of the presented TFETs in OFF-state and ON-state is shown in Fig. 3.5(a) and (b) respectively. TFET is said to be in OFF-state when no voltage is applied across gate to source terminal and at this state misalignment between the conduction band of the channel and the valence band of source does not allow the electrons to tunnel through the source-channel junction as shown in Fig. 3.5(a). Fig. 3.5(b) shows energy band distribution in ON-state where a positive gate voltage is applied for the creation of tunneling path so that electrons can tunnel from source side to channel region. This is due to lowering of conduction band of the channel which in turn makes a proper alignment between the conduction band of the channel and the

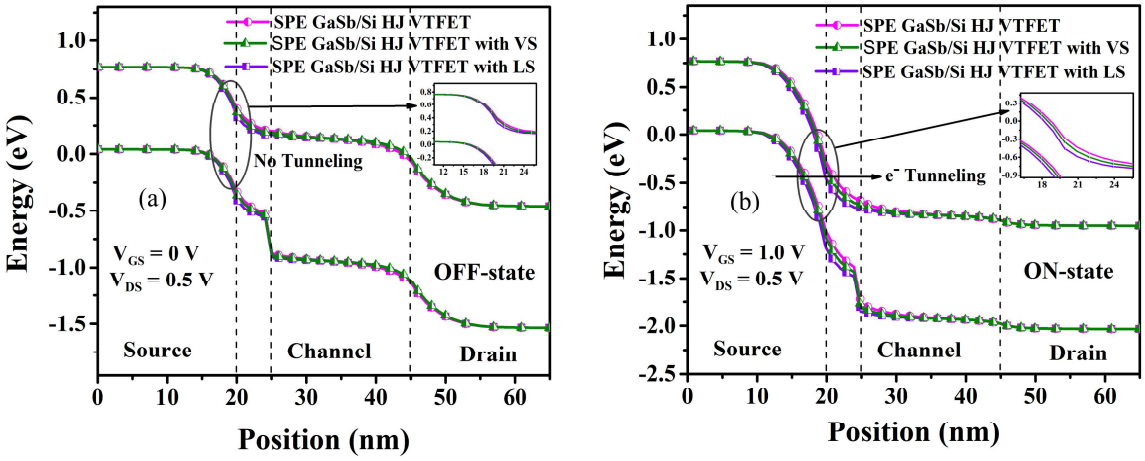

Fig. 3.5: Comparison of energy band distribution in (a) OFF-state, and (b) ON-state for SPE GaSb/Si HJ VTFET, SPE GaSb/Si HJ VTFET with VS, and SPE GaSb/Si HJ VTFET with LS.

valence band of source. In the same figure it can be observed that the tunneling width of SPE GaSb/Si HJ VTFET with LS is comparatively lower than SPE GaSb/Si HJ VTFET with VS and SPE GaSb/Si HJ VTFET which leads to higher carrier tunneling in SPE GaSb/Si HJ VTFET with LS than other two presented VTFETs. The reason for the lower tunneling width is because of the higher electric field at the source-channel junction for the GaSb/Si HJ VTFET with LS than the other two VTFETs.

The transfer (log scale (left axis) and linear scale (right axis)) and output characteristics of the presented VTFETs have been shown in Fig. 3.6(a) and (b) respectively. The transfer characteristics is obtained with respect to gate voltage (V_{GS}) from 0 to 1V keeping drain voltage (V_{DS}) constant at 0.5 V whereas the output characteristics is obtained with respect to V_{DS} (0 to 1 V) for a constant V_{GS} of 0.5. Maximum ON-current of 2.15×10^{-5} A/µm is shown by SPE GaSb/Si HJ VTFET with LS followed by SPE GaSb/Si HJ VTFET with VS (2.125×10^{-5} A/µm) and SPE GaSb/Si HJ VTFET (2.068×10^{-5} A/µm). The reason for the higher ON-current in SPE GaSb/Si HJ VTFET

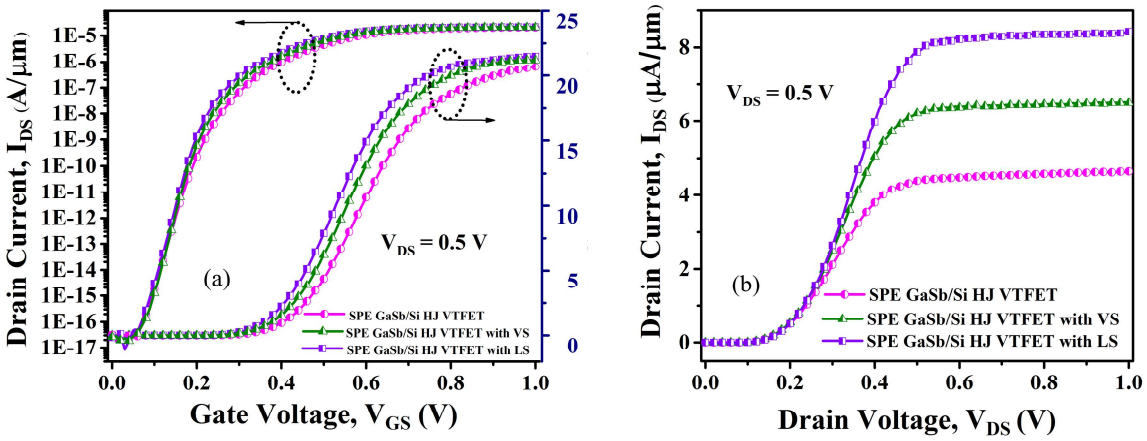

Fig. 3.6: Comparison of (a) transfer characteristics, and (b) output characteristics for SPE GaSb/Si HJ VTFET, SPE GaSb/Si HJ VTFET with VS, and SPE GaSb/Si HJ VTFET with LS.

with LS can be attributed to higher tunneling rate of carriers due to lower tunneling width in the SPE GaSb/Si HJ VTFET with LS than SPE GaSb/Si HJ VTFET with VS and SPE GaSb/Si HJ VTFET. Similarly, output characteristics is following the same trend like transfer characteristics where SPE GaSb/Si HJ VTFET with LS is shown to have maximum current followed by SPE GaSb/Si HJ VTFET with VS and SPE GaSb/Si HJ VTFET respectively.

Fig. 3.7(a) shows the sub-threshold swing (SS) variation whereas Fig. 3.7(b) shows the I_{ON}/I_{OFF} ratio for all the presented tunnel FETs i.e., SPE GaSb/Si HJ VTFET with LS, SPE GaSb/Si HJ VTFET with VS and SPE GaSb/Si HJ VTFET. From Fig. 3.7(a) we can see that the device with lateral gate oxide stacking i.e SPE GaSb/Si HJ VTFET with LS is having lowest SS (22 mV/dec) compared to other two VTFETs under study. Similarly, from Fig. 3.7(b) it can be depicted that the SPE GaSb/Si HJ VTFET with LS is showing highest I_{ON}/I_{OFF} ratio compared to SPE GaSb/Si HJ VTFET with VS and SPE GaSb/Si HJ VTFET. From this DC performance analysis, it can be concluded that

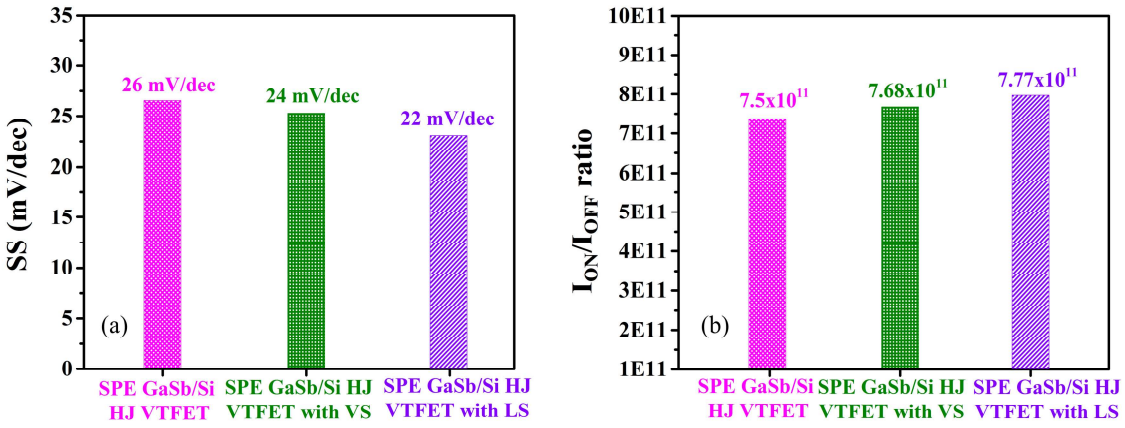

Fig. 3.7: Comparison of (a) average sub-threshold swing (SS), and (b) I_{ON}/I_{OFF} ratio for SPE GaSb/Si HJ VTFET, SPE GaSb/Si HJ VTFET with VS, and SPE GaSb/Si HJ VTFET with LS.

the source pocket engineered GaSb/Si vertical TFET with lateral gate oxide stacking (SPE GaSb/Si HJ VTFET with LS) showing superiority in performance than the other two presented structures i.e. source pocket engineered GaSb/Si vertical tunnel FET with vertical gate oxide stacking (SPE GaSb/Si HJ VTFET with VS) and source pocket engineered GaSb/Si vertical tunnel FET without any gate oxide stacking or homogeneous gate dielectric (SPE GaSb/Si HJ VTFET). The main reason for the same is attributed to enhancement in electric field at source channel junction by the use of high-*k* material nearer to the source end for the SPE GaSb/Si HJ VTFET with LS. Moreover, the device with gate stacking structure (SPE GaSb/Si HJ VTFET with LS and SPE GaSb/Si HJ VTFET with VS) is showing improvement in performance than the device without any gate oxide stacking (SPE GaSb/Si HJ VTFET).

3.3.2 RF Performance analysis

Now we will discuss some RF performance characteristics of all the VTFETs under study to analyze the impact of gate oxide stacking on RF performances.

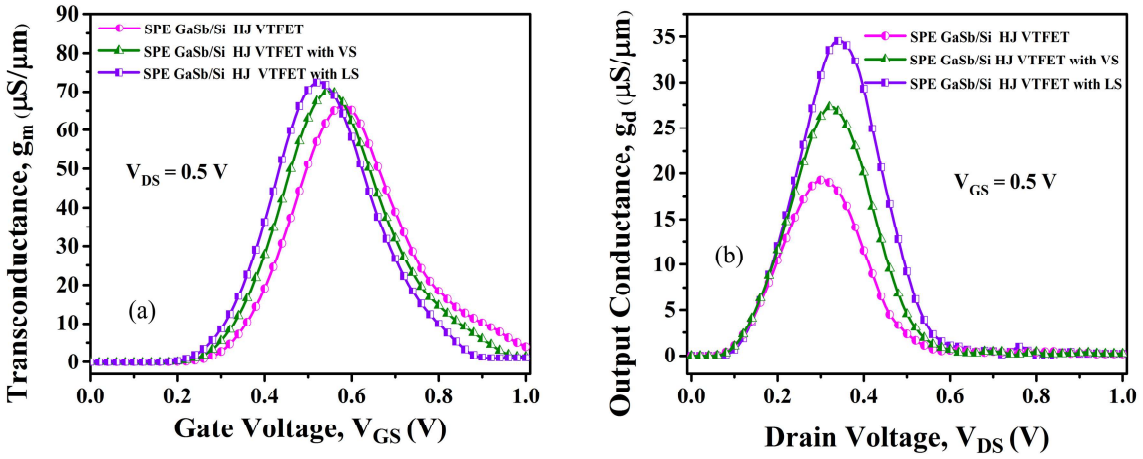

Fig. 3.8: Comparison of (a) transconductance characteristics (g_m), and (b) output conductance characteristics (g_d) for SPE GaSb/Si HJ VTFET, SPE GaSb/Si HJ VTFET with VS, and SPE GaSb/Si HJ VTFET with LS.

Transconductance (g_m) comparison plot of all the presented structures is illustrated in Fig. 3.8(a) while output conductance (g_d) comparison plot is depicted in Fig. 3.8(b). The information which can be gathered from Fig. 3.8(a) that g_m of SPE GaSb/Si HJ VTFET with LS is having highest value followed by SPE GaSb/Si HJ VTFET with VS and SPE GaSb/Si HJ VTFET. This reason for the same can be attributed to higher drain current for the former device compared to other two devices. It is always preferred to have larger value of g_m for efficient conversion of gate voltage to drain current. Therefore, SPE GaSb/Si HJ VTFET with LS with highest value of g_m is more suitable for circuit level applications. This is due to higher ON-current in SPE GaSb/Si HJ VTFET with LS than the other two presented VTFETs. Fig. 3.8(b) shows comparative plot of output conductance characteristics (g_d) of the VTFETs presented for study. It is observed from the same figure that the device SPE GaSb/Si HJ VTFET with LS is found to have larger value of g_d than SPE GaSb/Si HJ VTFET with VS and SPE GaSb/Si HJ VTFET. Thus, SPE GaSb/Si HJ VTFET with LS is having better g_d is more capable of converting drain voltage to drain current than the other two presented VTFETs. The reason for the larger

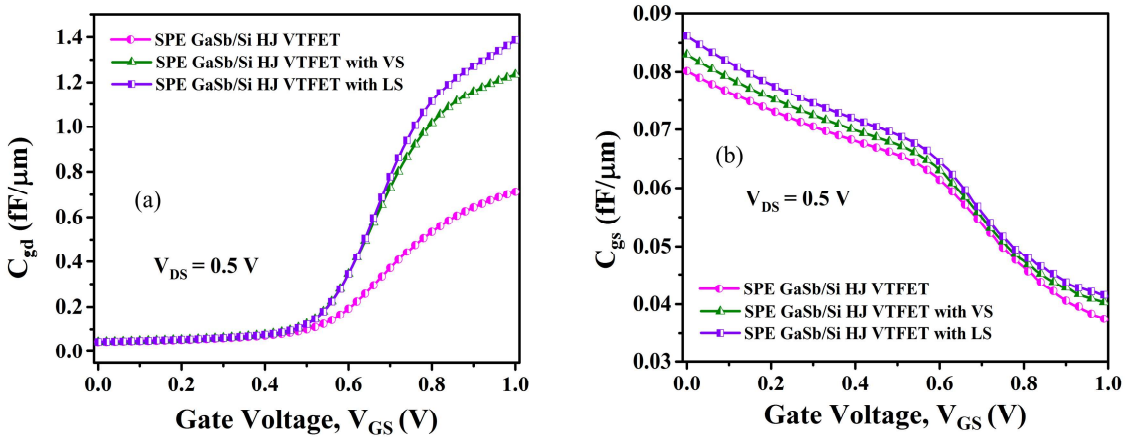

Fig. 3.9: Comparative plot of (a) intrinsic gate-drain capacitance (C_{gd}) (b) intrinsic gate-source capacitance (C_{gs}) for SPE GaSb/Si HJ VTFET, SPE GaSb/Si HJ VTFET with VS, and SPE GaSb/Si HJ VTFET with LS.

value of g_d in SPE GaSb/Si HJ VTFET with LS is attributed to larger value of output current in the said VTFET compared to the other two presented VTFETs as shown in Fig. 3.6(b).

Intrinsic gate capacitances are important RF parameters which influence the overall performance of any TFET. As discussed in Chapter-2 that TFET is mainly having two parasitic/Miller capacitances, namely, intrinsic gate to drain capacitance (C_{gd}) and intrinsic gate to source capacitance (C_{gs}) where C_{gd} is is much higher than C_{gs} [71]. Comparative plot of the C_{gd} is shown in Fig. 3.9(a) whereas comparative plot of the C_{gs} is shown in Fig. 3.9(b) for the VTFETs presented for study. SPE GaSb/Si HJ VTFET with LS and SPE GaSb/Si HJ VTFET with VS are shown to have higher value of C_{gd} and C_{gs} because of the use of gate oxide stacking which increases intrinsic gate capacitances. The reason for the higher intrinsic gate capacitance in lateral/vertical gate stacked VTFETs is due to presence of gate oxide with high-*k* value which enhances the permittivity so as intrinsic capacitances.

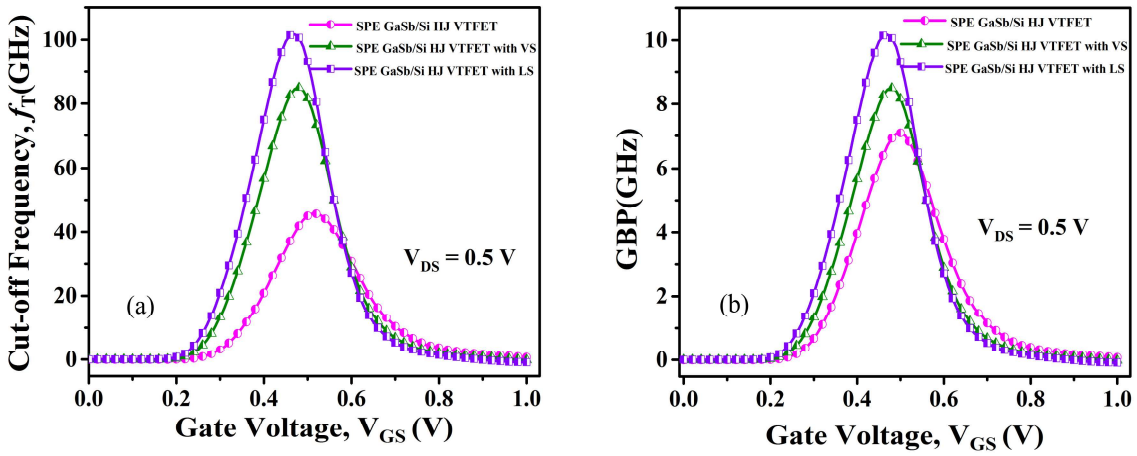

Fig. 3.10: Comparative plot of (a) cut-off frequency (f_T), and (b) GBP for SPE GaSb/Si HJ VTFET, SPE GaSb/Si HJ VTFET with VS, and SPE GaSb/Si HJ VTFET with LS.

Cut-off frequency (f_T) and gain bandwidth product (GBP) are also essential parameters for RF performance investigation of the TFET. The mathematical expression has been already discussed in Chapter-2. Fig. 3.10(a) compares the f_T for all the devices i.e., SPE GaSb/Si HJ VTFET, SPE GaSb/Si HJ VTFET with VS, and SPE GaSb/Si HJ VTFET with LS under study. The cut-off frequency (f_T) increases initially with the gate-source voltage for all the three VTFETs presented for study but after reaching a specific value it starts to decrease because of mobility degradation at higher gate bias [135]. The device SPE GaSb/Si HJ VTFET with LS possesses the highest value of f_T (101 GHz) followed by SPE GaSb/Si HJ VTFET with VS (84 GHz) and SPE GaSb/Si HJ VTFET (46 GHz). As cut-off frequency is g_m dependent, SPE GaSb/Si HJ VTFET with LS is shown to have the highest cut-off frequency due to its significantly higher value of g_m compared to other two VTFETs structures. Gain-bandwidth product (GBP) is also an important RF figure of merit. The region of operation with constant gain of a TFET is conveyed from GBP. Fig. 3.10(b) shows the GBPs of all the presented VTFET. It can

be concluded from the values of GBP that incorporating the gate oxide stacking improves the GBP value. The SPE GaSb/Si HJ VTFET with LS has the highest value followed by SPE GaSb/Si HJ VTFET with VS and SPE GaSb/Si HJ VTFET. Improved value of transconductance of SPE GaSb/Si HJ VTFET with LS and SPE GaSb/Si HJ VTFET with VS are the primary reasons for higher value of GBP in gate oxide stacking based VTFETs compared to the VTFET without having any gate oxide stacking.

In the context of circuit-level applications of any TFET, faster operation with efficient in terms of energy saving are much needed. TFETs are considered as an alternative to MOSFET because of higher value of transconductance generation factor (TGF) of former device compared to the later one. This property of TFET got rid of significant amount of power savings compared to MOSFET. In this view, the study of TGF is very much needed for applications TFET in circuit-level. The mathematical expression for calculation of this parameter is given in Eq. (2.5) of Chapter-2. Comparison of TGF is shown in Fig. 3.11(a) from which it can be noted that SPE GaSb/Si HJ VTFET with LS and SPE GaSb/Si HJ VTFET with VS have higher TGF than SPE GaSb/Si HJ VTFET because of higher value of transconductance and ON-current in stacked gate oxide-based VTFET. This implies that device with vertical and lateral gate oxide stacking is better in terms of fast and energy efficient operation than the device without having any gate oxide stacking. The transconductance frequency product (TFP) is also an important RF parameter of TFETs. The mathematical expression for calculation of this parameter is given in Eq. (2.6) of Chapter-2. TFP increases linearly with g_m. As g_m starts to decrease, TFP also decreases after attaining a maximum value. TFP of all the presented tunnel FETs is elucidated in Fig. 3.11(b). It can be summarized from the aforesaid

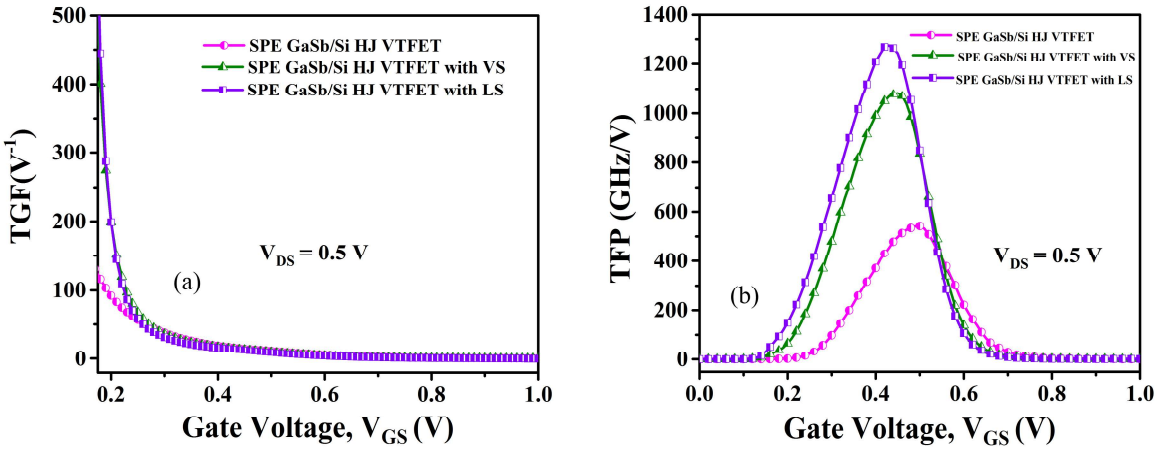

Fig. 3.11: Comparative plot of (a) TGF, and (b) TFP for SPE GaSb/Si HJ VTFET, SPE GaSb/Si HJ VTFET with VS, and SPE GaSb/Si HJ VTFET with LS.

figure that SPE GaSb/Si HJ VTFET with LS has higher TFP than that of SPE GaSb/Si HJ VTFET with VS and SPE GaSb/Si HJ VTFET due to higher value of f_T and TGF for the SPE GaSb/Si HJ VTFET with LS. TFET with higher TFP are always preferred to have faster circuit-level performance. In addition, the TFET with higher TFP shows better linearity. In the view of this discussion, it can be concluded that SPE GaSb/Si HJ VTFET with LS will show better linearity because of its higher value of TFP than SPE GaSb/Si HJ VTFET with VS and SPE GaSb/Si HJ VTFET.

Table-3.2 lists the RF performance parameters of all the presented tunnel FETs i.e., SPE GaSb/Si HJ VTFET, SPE GaSb/Si HJ VTFET with VS, and SPE GaSb/Si HJ VTFET with LS. The proposed source pocket engineered GaSb/Si vertical tunnel FET with lateral gate oxide stack (SPE GaSb/Si HJ VTFET with LS) shows better performance over source pocket engineered GaSb/Si vertical tunnel FET with vertical gate oxide stack (SPE GaSb/Si HJ VTFET with VS) and source pocket engineered GaSb/Si vertical tunnel FET without any gate oxide stacking or homogeneous gate oxide (SPE GaSb/Si HJ VTFET).

TABLE 3.2

DIFFERENT ANALOG/RF PERFORMANCE PARAMETERS COMPARISON OF THE PRESENTED GASB/SI VERTICAL TFETS WITH LATERAL, VERTICAL AND HOMOGENEOUS GATE OXIDE STACKING

Parameters	**SPE GaSb/Si HJ VTFET**	**SPE GaSb/Si HJ VTFET with VS**	**SPE GaSb/Si HJ VTFET with LS**
g_m (μS/μm)	66	70	72
g_d (μS/μm)	19	27	34
C_{gd} (fF/μm)	0.895	1.23	1.34
C_{gs} (fF/μm)	0.037	0.0393	0.0395
f_T (GHz)	46	84	101
GBP(GHz)	7	8.5	10
TGF (V^{-1})	140	490	500
TFP (GHz)	550	1082	1270

3.4 Conclusion

In this chapter, electrical performance characteristics evaluation of source pocket engineered GaSb/Si vertical tunnel FET has been made considering the effects of different types of gate oxide stacking i.e., lateral and vertical gate oxide stacking. Extensive TCAD based simulation results show that source pocket engineered GaSb/Si vertical tunnel FET with lateral gate oxide stacking (SPE GaSb/Si HJ VTFET with LS) is showing better device level performance in terms of higher ON-current, higher I_{ON}/I_{OFF} ratio, lower SS, higher g_m, g_d, f_T, GBP, TGF, and TFP over source pocket engineered GaSb/Si vertical tunnel FET with vertical gate oxide stacking (SPE GaSb/Si

HJ VTFET with VS) and source pocket engineered GaSb/Si vertical tunnel FET without any gate oxide stacking (SPE GaSb/Si HJ VTFET). However, SPE GaSb/Si HJ VTFET with LS has higher intrinsic gate capacitances over SPE GaSb/Si HJ VTFET with VS and SPE GaSb/Si HJ VTFET can degrade its circuit-level performance. Keeping these things in mind, the next chapter (Chapter-4) has been devoted to evaluate the circuit-level performance of all the three presented VTFETs where a static random-access memory (SRAM) based on TFET has been analyzed.