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An Inductor-Less, Discontinuous Current Source Gate Driver for SiC Devices

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ABSTRACT EMI has remained a limiting factor in driving the SiC MOSFETs to its maximum potential and achieving a trade-off between EMI and switching losses is a major challenge for the designers. In this paper, an inductor-less, discontinuous current source gate driver (DCSD) is proposed. Exclusion of inductor results in a compact footprint and easy integration in IC form. The absence of predriver for proposed DCSD reduces the complexity of the driver, making it easier to control and implement. In addition, very low propagation delay is attained with the proposed DCSD which allows SiC MOSFETs to switch at higher switching frequencies with low losses. The proposed DCSD is compared with a commercially available reference gate driver for SiC MOSFET, and the results are analyzed and validated with hardware prototype. A better trade-off between switching losses and EMI is obtained with the proposed driver, where during turn-off, a 65% reduction in dV_{ds}/dt and 45% reduction in dI_d/dt is achieved at the cost of 33% increase in the total switching loss.

INDEX TERMS SiC MOSFET, gate driver, cascode current mirror, propagation delay, EMI.

I. INTRODUCTION

Emergence of Silicon Carbide (SiC) based devices are an advancement in device industry. The material property of Silicon Carbide (SiC) breaks many boundaries set by Silicon (Si) such as breakdown field, electron saturated drift velocity, thermal conductivity and electron velocity, making it a potential replacement for Si IGBT in many high power applications [1]–[3]. SiC MOSFETs material property and capability to operate at high temperature and high frequencies, reduces the thermal and filtering requirement to a large extent and hence makes it an ideal choice for high power dense solutions [4]–[6]. The high voltage and current transition during high frequency switching of SiC MOSFET in presence of parasitic inductance increases the oscillations and overshoot in switching waveforms [7], [8], thereby making the SiC based power converters prone to Electromagnetic interference (EMI) thus challenges the protection and reliability of the power converter. Operating the device at lower switching rate reduces the EMI effect, but increases the switching losses. Trade-off between the switching losses and EMI through gate driver is essential to extract the maximum potential of SiC MOSFET.

Gate driving topologies for high frequency applications are categorized as voltage driven, current driven and resonant driven [9]–[12]. The most common topology is voltage driven where a voltage source in series with a resistance is used to charge the gate capacitance. It is simple technique and is implemented in numerous applications. The series resistance determines the switching speed of the connected device. Power loss and no scope for energy recovery make the voltage driven topologies less suitable for high frequency operation. In Current driven, a constant current source in series with a resistance is used to charge the gate capacitance. Creating a stable current source is major hurdle in the implementation of current driven topology. Possibility of gate energy recovery during turn-off makes resonant driven as an encouraging solution for gate driving at higher frequency. The quality factor Q of the L-C tank in resonant topology limits the energy recovery and increases the design complexity at high frequency.

Current source gate driver (CSD) works on the principle of charging the gate capacitance through inductor current connected along with a series resistance. Higher gate current

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ensures faster switching and hence low switching losses. Depending on the nature of current through inductor, two types of CSDs are reported in literature namely Continuous current source drivers (CCSDs) [13]–[15] and discontinuous current source drivers (DCSDs) [16]–[21]. Bigger size of the inductor required to maintain continuous current through inductor in continuous CSDs, not only increases the driver losses but also makes the driver bulky. In order to tackle these two major limitations, discontinuous CSD came into picture. It decreases the driver loss and also reduces the size of inductor at the cost of complex controller. Presence of inductor in gate driver mainly brings the following limitations:

1) Large inductance (in case of continuous CSDs) leads to low power dense driver solution.
2) High driver losses (in case of continuous CSDs) due to continuous current in the driver circuit.
3) Complex control (in case of discontinuous CSDs) to achieve discontinuous inductor current.
4) Slow switching transitions leading to more switching losses.

Comparison of continuous CSD and discontinuous CSD is reported in [22]. DCSD comes with advantages over CSD such as, inductor size in DCSDs is much smaller as compared to the inductor in CCSDs, lesser gate drive losses is obtained with DCSDs, DCSD offers superior performance during step change in duty cycle and peak gate current in DCSD is independent of duty cycle and switching frequency. Discontinuous current source driver proposed in [16]–[21] overcomes the limitations of CSDs. However, it still faces challenges in the form of:

1) Presence of inductor makes driver circuit difficult to integrate in IC form
2) Requirement of predrivers for the switches present in gate driver circuit increases the complexity of the overall driver circuit
3) Propagation delay introduced due to the driver circuit

This paper focuses on designing an inductor-less discontinuous current source gate driver to reduce the driver loss and overcome aforementioned limitations. Compared to its Si counterpart, SiC MOSFET of similar rating has low input capacitance thereby requires less charge to be injected and taken out of the gate terminal for successful switching. This result in high switching transition leading to EMI effect. Gate driver for SiC MOSFET needs to provide a trade-off between switching losses and EMI [23], [24]. To drive the SiC MOSFET, CREE has recently offered a commercial gate driver CRD-001 [25]. In this solution the IXYS based voltage source driver - IXD609 [26] is used. This made the authors to compare the proposed gate driver with IXD609 as reference gate driver (RGD). This paper proposes an inductor-less discontinuous current source gate driver with trade-off solution between EMI and overall losses. A cascode current mirror based circuit is proposed to drive the gate of SiC MOSFET. As compared to other DCSDs, the proposed gate driver has following advantages: a) Inductor-less current source operation, b) Elimination of predrivers requirement and c) Reduction of propagation delay. Similar to other CSDs, the proposed circuit shows high immunity to Cdv/dt, preventing spurious turn-on of SiC MOSFET.

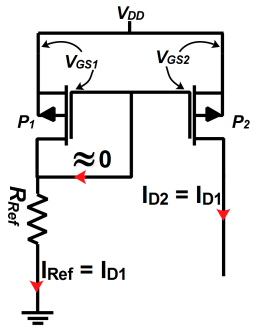

FIGURE 1. Simple current mirror.

The paper is structured as follows: proposed gate driver is introduced and explained in section II. Implementation of switching test rig is discussed in section III. Performance analysis of proposed driver for SiC MOSFET is presented with experimental results in section IV. Comparative performance analysis of proposed driver with reference gate driver is presented in Section V. Advantages of proposed driver is presented in Section VI. Finally, the conclusion of the presented work is discussed in Section VII followed by references.

II. PROPOSED GATE DRIVER

Current mirror as shown in Fig.1 is one of the building blocks in analog circuits. As the name designates, current mirror reflects the input current at the output. Property of low input resistance and large output impedance makes the output of current source constant. The principle of operation for current mirror is, current flowing through drains of two identical MOSFETs are equal, when equipotential gate source applied across both the MOSFETs. Primary applications of a current mirror are: biasing of circuits, current amplifier, current mode signal processing and active loads. NMOS based current mirror act as a current sink whereas PMOS based current mirror acts as a current source. Basic current mirror is shown in Fig.1. Drain and gate terminals of PMOS P_1 are shorted results in self-biased configuration (also known as the diode connected configuration) where PMOS P_1 operates in saturation mode and holds the condition:

$$V_{DS} > V_{GS} - V_{TH} \tag{1}$$

I_{REF} flowing through P_1 creates V_{GS} across P_1 and same V_{GS} is created across P_2

$$V_{GS1} = V_{GS2} \tag{2}$$

Since P_1 is self biased, hence it operates in saturation mode. Reference current I_{REF} can be written as [27], [28]:

$$I_{REF} = I_{D1} = \left(\frac{\mu_n C_{ox}}{2}\right)_1 (V_{GS1} - V_{TH1})^2 \tag{3}$$

where, μ_n is charge-carrier effective mobility, C_{ox} is the gate oxide capacitance per unit area. For drain current of P_2 to be independent of the drain-to-source voltage, it should operate in saturation mode. The drain current I_{D2} of P_2 is then:

$$I_{D2} = \left(\frac{\mu_n C_{ox}}{2}\right)_2 (V_{GS2} - V_{TH2})^2 \tag{4}$$

Dependence of drain current on drain-to-source voltage is very crucial for many application taking stability into consideration. Drain current of P_1 and P_2, can be written as:

$$\left.\begin{aligned} I_{D1} &= \left(\frac{\mu_n C_{ox}}{2}\right)_1 (V_{GS1} - V_{TH1})^2 (1 + \lambda_1 V_{DS1}) \\ I_{D2} &= \left(\frac{\mu_n C_{ox}}{2}\right)_2 (V_{GS2} - V_{TH2})^2 (1 + \lambda_2 V_{DS2}) \end{aligned}\right\} \tag{5}$$

where λ is the channel length modulation constant

For MOSFETs of similar rating and from same manufacturer, μ_n, C_{ox} and λ are same since these three factors depend on the material and build quality. Therefore for identical transistors:

$$\left.\begin{aligned} \left(\frac{\mu_n C_{ox}}{2}\right)_1 &= \left(\frac{\mu_n C_{ox}}{2}\right)_2 \\ V_{TH1} &= V_{TH2} \\ \lambda_1 &= \lambda_2 \end{aligned}\right\} \tag{6}$$

Therefore form equation (2),(5) and (6):

$$I_{REF} = I_{D1} = I_{D2} \tag{7}$$

This relationship holds good for transistors with similar aspect ratio or width-to-length ratio. Else the relation will become:

$$I_{D2} = \frac{(W/L)_2}{(W/L)_1} I_{REF} \tag{8}$$

where, W is the gate width and L is the gate length. (W/L) ratio of both the identical MOSFETs from same manufacturer are same as it depends on the packaging and manufacturing precision. For equal (W/L) ratio, equation (8) becomes:

$$I_{REF} = I_{D2} \tag{9}$$

Hence equation (9) concludes the mirroring action in P_2, as the current flowing through it is equal to the reference current. The current flowing through P_2 can be utilized as a current source in the proposed gate driver. Current mirrors can be broadly classified as : (i) Simple current mirror, (ii) Wilson current mirror, (iii) Cascode current mirror as shown in Fig.2. Simple current mirror is least complex but has poor current gain accuracy and least output impendence. Wilson current mirror is moderately complex and also has poor current gain accuracy but is having more output impedance as compared to simple current mirror. Cascode current mirror is most complex among the three types of mirrors, but is having highest current gain accuracy along with large output impedance [28], [29]. One of the major

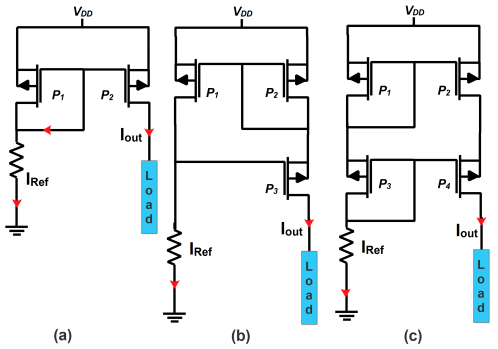

FIGURE 2. Different types of current mirror: (a) simple current mirror; (b) Wilson current mirror; and (c) cascode current mirror.

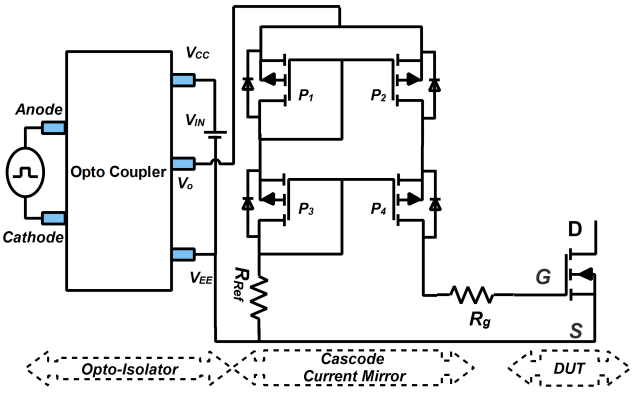

FIGURE 3. Proposed mirror gate driver.

challenges in operation of mirror circuit at higher rating or V_{ds}, is the channel length modulation (λ) and to overcome this, cascode arrangement of mirror is a good solution [29]. This makes the authors to choose cascode arrangement for designing the driver circuit. The basic idea of using a current mirror circuit in gate driver is derived from [30], where NMOS based Wilson current mirror is used as current sink in controlling Normally-on SiC JFET. However, SiC MOSFET is a normally off device and the gate driver is expected to act both as source and sink. The proposed mirror gate driver (MGD) is shown in Fig.3, where a PMOS based cascode current mirror operating as current source is used to charge the input capacitance of SiC MOSFET. A current mirror circuit works on the principle of mirroring the current drawn by the reference resistance into the parallel branch where load is connected. In cascode current mirror as shown in Fig.3, for same (W/L) ratio of all the four PMOS, the current drawn by R_{Ref} is equal to the current flowing into the R_g. The gate of the SiC MOSFET connected through gate resistance R_g is acting as the load for the cascode mirror. In a cascode current mirror, four similar PMOS (P_1, P_2, P_3 and P_4) are connected as shown in Fig.3, all the PMOS transistors are operating in self biased mode. The self-biased PMOS eliminates the requirement of predrivers for the operation of CSDs hence reducing the complexity of the driver to a great extent. An optocoupler is used prior to

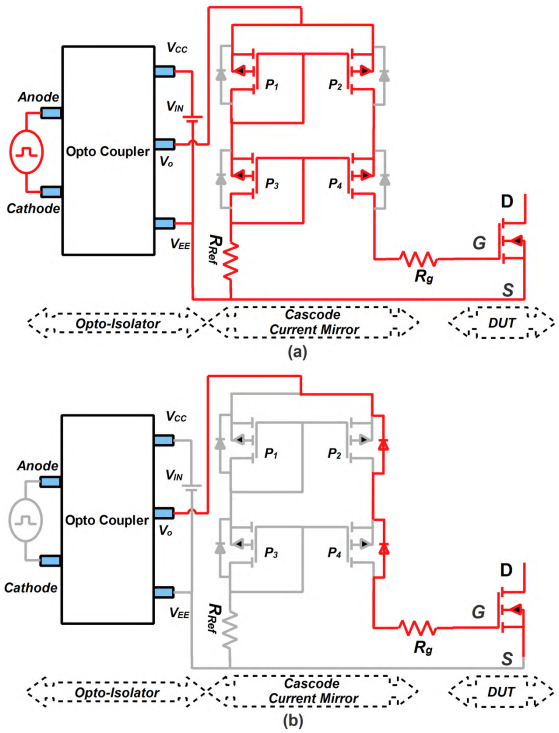

FIGURE 4. Modes of proposed MGD. (a) Turn-on. (b) Turn-off.

driver, to provide isolation between the control circuit and power circuit. Output of optocoupler acts as the input to the mirror and will operate till the control signal is present at the input of the opto-isolator hence making the current source a discontinuous type. This discontinuous property of mirror reduces the driver losses to a substantial amount. The prime motives of this proposed driving technique for SiC MOSFET are:

1) To provide inductor-less current source gate driving solution.
2) Discontinuous current source operation.
3) Eliminating the need of predrivers for CSD operation.
4) Obtaining minimal propagation delay.

Proposed MGD operates in two modes, turn-on mode and turn-off mode as shown in Fig.4. During turn-on mode shown in Fig.4(a), P_1 and P_3 connected in self biased configuration will create a mirror action in P_2 and P_4. Hence reference current I_{Ref} drawn by R_{Ref} through P_1 and P_3 is equal to the mirrored current flowing in R_g through P_2 and P_4. Mirrored current is pushed into the gate of device under test (DUT) to turn it on. This turn-on mode will operate as long as pulsed input voltage from optocoupler's output is applied across the cascode current mirror, which is available until control pulse is applied across the anode and cathode terminal of the optocoupler. Input voltage supply to the optocoupler is supplied by the V_{IN}. During turn-off mode, since control pulse at optocoupler is absent, optocoupler will not generate output voltage across the mirror, thereby mirror action will not take place. So no current is injected into the gate of the DUT. Therefore turn-off process of DUT starts, where input capacitances of the DUT starts discharging through gate terminal. The gate current coming out of the gate terminal of DUT during its turn-off transition, passes through the R_g and body diode of P_2 and P_4 enters into the optocoupler, where it is grounded as shown in Fig.4(b). Performance analysis of the proposed MGD and comparison with the state-of art is explained in the following sections.

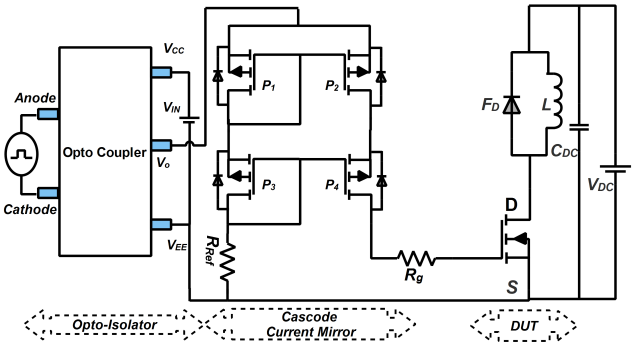

FIGURE 5. Circuit to test the potential of proposed mirror gate driver.

TABLE 1. Proposed gate driver components.

Components	*Description*
PMOS	TJ8S06M3L
Opto-isolator	HCPL-3120
$R_{reference}$	PWR263S-35-10R0F

III. IMPLEMENTATION OF SWITCHING TEST RIG

An inductive test rig circuit shown in Fig.5, where a switch is tested for severe switching conditions and simultaneously the proposed mirror gate driver is evaluated. Cascode current mirror is developed as per the design consideration discussed in previous section. Table 1 shows the hardware components used for developing the proposed mirror gate driver. For mirror action, four PMOS are selected having similar rating and from the same manufacturer, apart from this utmost care is also taken to keep the PMOSs at equidistance from each other by keeping the traces of almost equal length among the four PMOS. The description of inductive test rig circuit utilized to test the dynamic behavior of the DUT driven with the proposed mirror gate driver is shown in Table 2. SiC MOSFET is taken as DUT and the performance of proposed mirror gate driver is observed and analyzed. Waveforms of gate-source voltage (V_{gs}), gate current (I_g), drain-source voltage (V_{ds}) and drain current (I_d) of SiC MOSFET are recorded at various operating conditions and further analysis is done. A stray inductance in gate path exits in a PCB layout, which depends on the trace length between the driver output terminal and gate terminal of DUT. Lesser the trace length, less will be the gate stray inductance. This stray inductance slows the charging of gate capacitance, hence making longer duration of turn-on process resulting in higher turn-on losses. While designing the PCB layout of the inductive test circuit, utmost

TABLE 2. Inductive test rig circuit component parameters.

Components	*Description*
DUT (SiC MOSFET)	C2M0160120D (1.2kV, 17.7A)
Inductor	PCV-2- 104-10L (100μ H 10.1A)
Freewheeling diode (SiC Schottky Diode)	SCS215AEC (650V 15A)
DC Link capacitor	ALS30A102KF500 (1000μ F 500V)

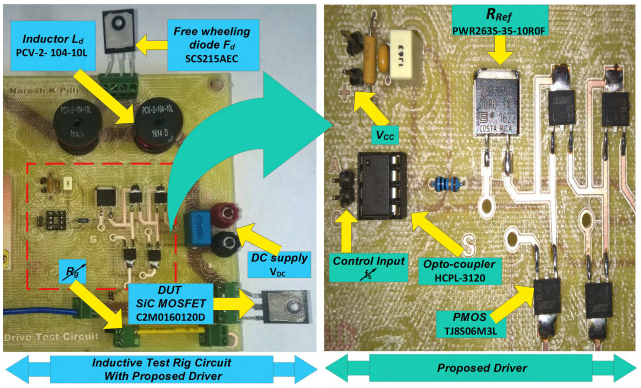

FIGURE 6. Laboratory prototype of inductive test rig circuit with proposed mirror gate driver.

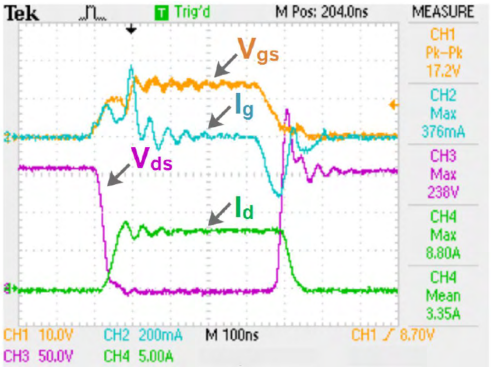

FIGURE 7. Switching waveforms of SiC MOSFET with $R_g = 5\Omega$ and $f_s = 50$ KHz; top: Gate voltage V_{gs} generated (10 V/div, 100 ns/div), second: Gate current I_g (200 mA/div), third: Voltage applied across SiC MOSFET V_{ds} (50 V/div), bottom: Drain current I_d through SiC MOSFET (5 A/div).

care was taken to reduce the distance between the driver output and the gate terminal of DUT to minimize the effect of stray inductance in gate path. Fig. 6, shows the hardware prototype of the proposed work. Fig. 7, shows the waveforms of V_{gs}, I_g, V_{ds} and I_d for SiC MOSFET driven by the proposed mirror gate driver at $f_s = 50$ KHz, 1% duty ratio and $R_g = 5\Omega$.

Tests were performed at four different switching frequencies (50 KHz, 30 KHz, 20 KHz, 10 KHz) and with four different gate resistances (10 Ω, 5 Ω, 3.3 Ω, 0 Ω). Various experimental observations were made which is discussed in the next section.

IV. RESULT ANALYSIS

Nature of drain current (I_d) and drain-source voltage (V_{ds}) of a device during the switching transition gives the insight of the switching losses and electromagnetic interference (EMI) of the device. These transitions in I_d and V_{ds} are primarily controlled by gate driver. Speed of switch transition depends on how quickly the charges are pushed into or taken out of the gate terminal to charge or discharge the input capacitance of the device. Quick transition also leads to oscillations in I_d and V_{ds}. The R_g provides impedance to the gate charging and discharging circuit. To test the potential of proposed mirror gate driver, waveforms of I_d and V_{ds} for SiC MOSFET, driven at four different switching frequency and gate resistance, were recorded. Using these data various performance parameters are extracted.

A. SWITCHING TRANSITION

Switching transitions in I_d and V_{ds} is primarily controlled by gate driver. To test the potential of proposed mirror gate driver, waveforms of I_d and V_{ds} for SiC MOSFET, driven at four different switching frequency and gate resistance, were recorded. Using these data various performance parameters are extracted.

1) Turn-on transition: The turn-on loss of a device is governed by time taken to switch the device from off-state to on- state. The quicker the transition, lesser is the losses, hence slope of drain current I_d and drain-source voltage V_{ds} of a device during turn-on transition decides the turn-on loss of the device. To analyze the impact of proposed mirror gate driver on turn-on losses, test was performed at two different operating conditions, (i) switching the device at constant $f_s = 50$ KHz and variable R_g, (ii) switching the device with $R_g = 5\Omega$ and variable f_s. As R_g increases, the slope of I_d and V_{ds} increases at constant $f_s = 50$ KHz as shown in Fig.8(a) and Fig. 8(c). The slope of I_d and V_{ds} decreases with the increase in f_s at constant $R_g = 5\Omega$ as shown in Fig. 8(b) and Fig. 8(d). This is due to increased impedance offered by the stray elements in the path of gate driver circuit. The larger slopes leads to higher turn-on losses.
2) Turn-off transition: Slope of I_d and V_{ds} during turn-off depicts the turn-off losses of the device. Steeper the slope, smaller the losses, but EMI increases with steeper slope. Due to parasitic inductance in SiC MOSFET, voltage overshoot in V_{ds} during turn-off transition increases with steeper slope, challenging the reliability and protection of the converter. Effect of proposed mirror gate driver on turn-off losses and V_{ds} overshoot studied under two operating conditions, (i) switching the device at constant $f_s = 50$ KHz and variable R_g, (ii) switching the device with $R_g = 5\Omega$ and variable f_s. The slope of I_d and V_{ds} increases with the increase in R_g at constant $f_s = 50$ KHz as shown in Fig.9(a) and Fig.9(c). The slope of I_d and V_{ds} decreases with the increase in f_s at constant $R_g = 5\Omega$ as shown in Fig.9(b) and Fig.9(d). Turn-off losses increases with the increase in slope. At constant $f_s = 50$ KHz, the voltage overshoot of V_{ds} decreases with the increase in R_g. Similarly, with fixed $R_g = 5\Omega$, V_{ds} overshoot increases with the increase in switching frequency f_s.

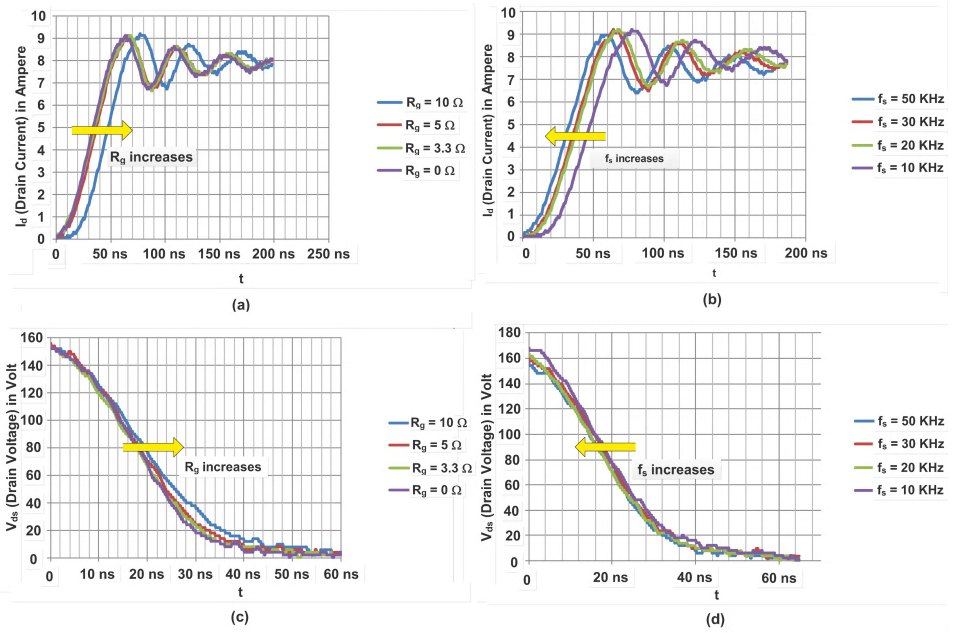

FIGURE 8. Turn-on switching waveforms of SiC MOSFET driven by proposed mirror gate driver (a) drain current of SiC MOSFET driven at 50 KHz and variable R_g, (b) drain current of SiC MOSFET driven with $R_g = 5\Omega$ and variable f_s, (c) drain-source voltage of SiC MOSFET driven at 50 KHz and variable R_g, (d) drain-source voltage of SiC MOSFET with $R_g = 5\Omega$ and variable f_s.

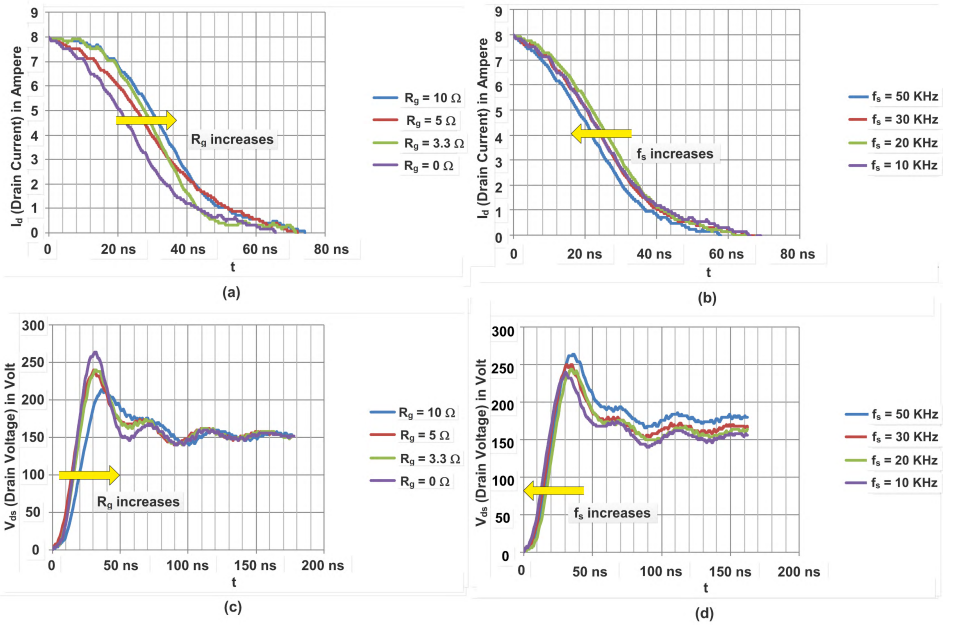

FIGURE 9. Turn-off switching waveforms of SiC MOSFET driven by proposed mirror gate driver (a) drain current of SiC MOSFET driven at 50 KHz and variable R_g, (b) drain current of SiC MOSFET driven with $R_g = 5\Omega$ and variable f_s, (c) drain-source voltage of SiC MOSFET driven at 50 KHz and variable R_g, (d) drain-source voltage of SiC MOSFET with $R_g = 5\Omega$ and variable f_s.

B. ENERGY LOSS

Fig.10, shows the variation of energy losses under two different operating conditions. From Fig.10(a), it is observed that with $R_g = 5\Omega$, both turn-on and turn-off losses decreases with the increase in switching frequency. At switching frequency of 50 KHz, the turn-on and turn-off loss increases with the increase in gate resistance R_g as shown in Fig.10(b). Total losses (E total) shown in Fig.10, include the combined form of turn-on and turn-off losses.

C. VOLTAGE OVERSHOOT(ΔV_{DS})

V_{ds} overshoot decreases with the increase in R_g as shown in Fig.11, since the impedance to discharge path of the gate charge is increased. On the other hand, the energy losses

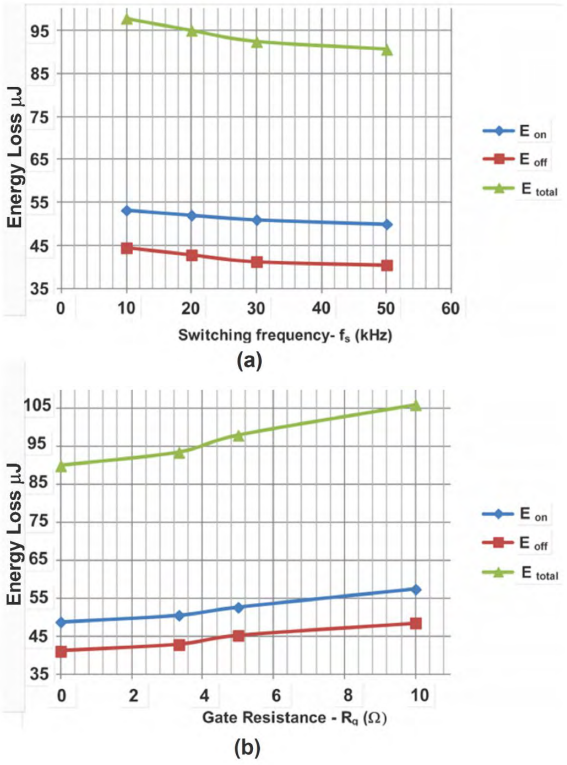

FIGURE 10. Switching energy loss of SiC MOSFET (a) $R_g = 5\Omega$ and variable f_s, (b) $f_s = 50$ KHz and variable R_g.

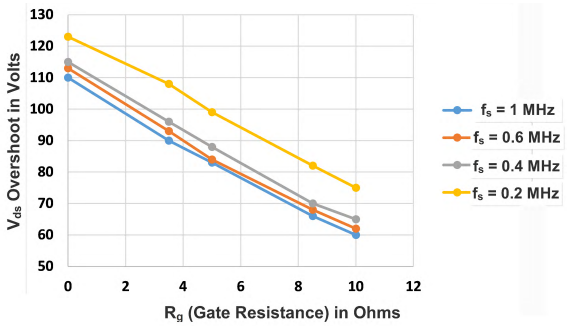

FIGURE 11. Variation in V_{ds} overshoot with change in R_g and at different f_s.

increase with R_g, hence a trade-off between switching losses and voltage overshoot is necessary.

V. COMPARISON WITH REFERENCE GATE DRIVER

A reference gate driver (RGD) IXD609 [26] used in buffer stage of commercial gate driver CRD-001 [25] by CREE, exclusively designed to drive SiC MOSFET, is taken into consideration for comparative analysis. Switching waveforms of SiC MOSFET driven with proposed mirror gate driver and reference gate driver are shown in Fig. 12(a) and Fig.12(b), respectively. Large V_{ds} overshoot (ΔV_{ds}) is observed with RGD as compared to the proposed MGD. There is 55% reduction in ΔV_{ds} using the proposed mirror gate driver.

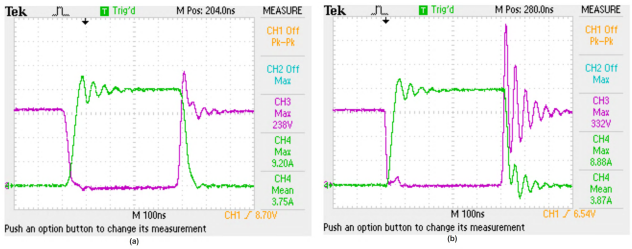

FIGURE 12. Switching waveforms of SiC MOSFET with $R_g = 5\Omega$ and $f_s = 50$ kHz (a) driven by proposed mirror gate driver and (b) driven by reference gate driver.

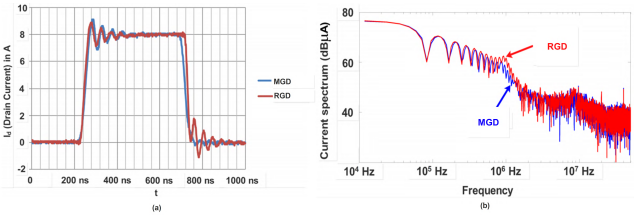

FIGURE 13. (a) Comparison of measured I_d shown in Fig. 11, and (b) its calculated Spectral envelopes.

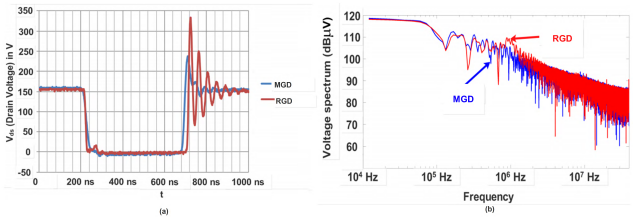

FIGURE 14. (a) Comparison of measured V_{ds} shown in Fig. 11, and (b) its calculated Spectral envelopes.

To compare the dynamic operation and analyze the behavior of both the drivers during one complete switching cycle, waveforms of I_d and V_{ds} for both the drivers are plotted on the same reference using the measured data. Measured data of voltage and current are trapezoidal waveforms, FFT of these waveforms produce the spectrum of switching waveform [31], [32]. Furthermore its spectrum behavior is also drawn using time-domain data, as shown in Fig.13 and Fig.14. Spectral content at high frequency plays an important role in EMI generation. The losses and high frequency spectrum follow inverse relationship. For both the drivers, Fig.13(a) and Fig.13(b) shows the drain current profile of SiC MOSFET, in time domain and frequency domain respectively. From 1MHz to 50MHz, proposed mirror gate driver shows 5-7dB EMI reduction as compared to voltage gate driver. Similarly the time and frequency waveforms of V_{ds} for both the drivers are shown in Fig.14(a) and Fig.14(b), respectively. A reduction of 20dB is observed in proposed mirror gate driver compared with reference gate driver at 1MHz. From 1MHz to 50MHz, proposed mirror gate driver shows 5-10dB EMI reduction as compared with the voltage gate driver.

From Fig.13(a) and Fig.14(a), it is observed that the difference in behavior of both the driving condition is more promi-

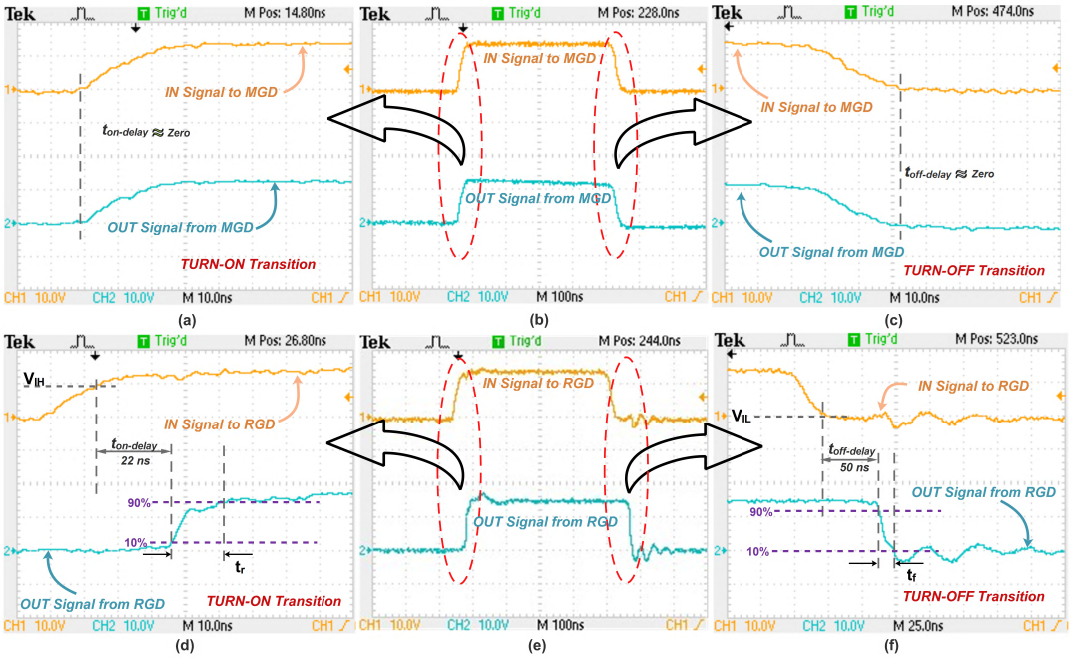

FIGURE 15. Switching transients for proposed MGD, (a) Turn-on transient with MGD (b) Complete switching cycle with MGD (c) Turn-off transient with MGD(d) Turn-on transient with RGD (e) Complete switching cycle with RGD (f) Turn-off transient with RGD.

nent during the turn-off transition, the current and voltage overshoots are less for proposed MGD compared to the RGD.

A. PROPAGATION DELAY

While choosing a gate driver for specific application, parameters such as rise time (t_r), fall time (t_f), turn-on delay ($t_{on-delay}$) and turn-off delay ($t_{off-delay}$) plays an important role. The t_r and t_f mainly decides the switching losses, whereas the $t_{on-delay}$ and $t_{off-delay}$ limits the loop response and transient response. Timing diagram during turn-on and turn-off transition provides the information of the parameters t_r, t_f, $t_{on-delay}$ and $t_{off-delay}$. Fig.15 shows the timing diagram of proposed MGD alongside RGD. IN signal is the input to the driver from an opto-isolator and OUT is the driver output given to the gate terminal of a switch. In Fig.15, channel 1 shows the IN signal and channel 2 shows the OUT signal. The timing diagram for proposed MGD during turn-on and turn-off transient are shown in Fig.15(a) and Fig.15(c) respectively. The rise time t_r and fall time t_f are 21.6ns and 25.6ns respectively. The $t_{on-delay}$ and $t_{off-delay}$ resulting in propagation delay of the driver is found to be close to zero. Marginal propagation delay enhances the loop response. The timing diagram for RGD during turn-on and turn-off transient are shown in Fig.15(d) and Fig.15(f), respectively. The rise time t_r and fall time t_f are 14ns and 10ns, respectively. The $t_{on-delay}$ and $t_{off-delay}$ resulting in propagation delay of the driver is found to be 22ns and 50ns respectively.

Comparison of timing parameters for both the drivers is done under similar operating condition. In both the cases i.e. MGD and RGD, propagation delay measured from Fig.15 during turn-on and turn-off transient does not include the propagation delay incurred due to opto-coupler. All four parameters t_r, t_f, $t_{on-delay}$ and $t_{off-delay}$, compared and summarized in Table 3 are solely due to the MGD and RGD excluding the opto-coupler stage. Rise time and fall time for reference gate driver is less compared with proposed mirror gate driver, resulting in quick transition from ON to OFF and vice-versa. Quick transients enhances the EMI effect, low EMI is attained with proposed mirror gate driver at the cost of higher switching losses due to the comparatively sluggish switching transients. A large difference in propagation delay is observed from Table 3, with propagation delay close to zero is found in case of proposed mirror gate driver. Substantial propagation delay found in RGD is introduced by Schmitt trigger and anti-cross conducting circuitry consisting of logic gates (AND,NAND and INVERTER) [33]. Transition rate issues present in the CMOS circuit of RGD is overcome by the inclusion of Schmitt trigger [34]. Hence for proper operation of RGD circuit, the circuit components responsible for introduction of propagation delay is unavoidable. In proposed MGD due to the cacscode mirror configuration, problem of cross conduction and transition rate issues are not present, hence resulting in negligible propagation delay. In DCSDs topologies [16]–[21], phase-leg arrangements of NMOS are

TABLE 3. Comparison of output gate pulse.

Gate Driver	(t_r) *in ns*	(t_f) *in ns*	($t_{on-delay}$) *in ns*	($t_{off-delay}$) *in ns*
RGD	14	10	22	50
MGD	21.6	25.6	$\simeq zero$	$\simeq zero$

TABLE 4. Topological comparison between proposed MGD and other gate driving circuits in the literature.

Gate Driver	*Output current*	*No.of Inductors*	*No.of control switches*	*Propagation delay*
Proposed MGD	Discontinuous	0	0	Negligible
Proposed in [13]	Continuous	1	2	Present
Proposed in [14]	Continuous	1	4	Present
Proposed in [15]	Continuous	1	4	Present
Proposed in [16]	Discontinuous	1	4	Present
Proposed in [17]	Discontinuous	2	4	Present
Proposed in [19]	Discontinuous	1	4	Present
Proposed in [20]	Discontinuous	2	4	Present
Proposed in [21]	Discontinuous	2	2	Present

present. To avoid shoot-through in these phase-leg arrangements, dead time is enforced between the complimentary signals applied to high side and low side switches. Dead time is limited due to propagation delay. Proposed gate driver does not consists of half-bridge or full-bridge configurations, and there is no-requirement of dead time for its operation. Hence the propagation delay achieved by the proposed gate driver is close to zero.

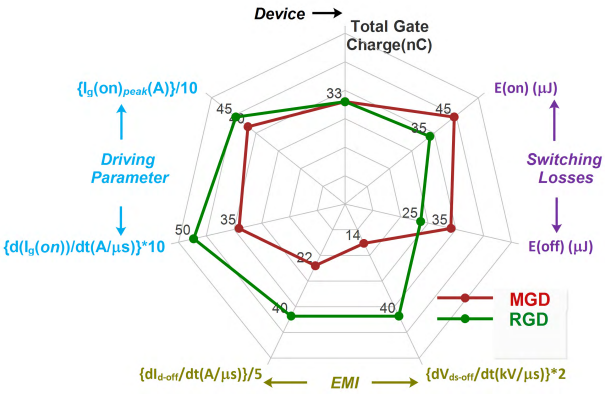

FIGURE 16. Comparative analysis of proposed mirror gate driver with reference gate driver.

The comparative study is summarized in Fig.16, drawn with the measured data shown in Fig.12. The EMI factors chosen for comparison are during turn-off case since the difference is more prominent during turn-off. For SiC MOSFET driven with both the drivers on same inductive test rig circuit under similar operating conditions. Peak gate current and rate of gate current are observed as the driving parameters which results in different switching losses and EMI effect. In the proposed mirror gate driver, the peak gate current is 11% less than that of reference gate driver peak gate current. In addition the rate of gate current rise is 30% less as compared to reference gate driver. With the aforementioned change in the driving condition, taking RGD as the reference, following conclusion is drawn from the comparative analysis shown in Fig.16:

1) Turn-on loss is increased by 28%.
2) Turn-off loss is increased by 40%.
3) Total switching losses are increased by 33%.
4) dV_{ds}/dt is significantly reduced by 65%.
5) dI_d/dt is substantially reduced by 45%.

The above observations conclude that for an increase of 33% of total switching losses, dV_{ds}/dt is reduced by 65% and there is reduction of 45% in dI_d/dt. Hence a productive trade-off is achieved with the proposed mirror gate driver circuit.

VI. ADVANTAGES OF THE PROPOSED MGD

Discontinuous current source drivers (DCSDs)is introduced to overcome the limitations of continuous current source drivers (CCSDs). Comparison of DCSD and CCSD is explained in [22]. Proposed MGD has following advantages over previous DCSDs [16]–[21]:

1) *Inductor-less operation:* Previous DCSDs proposed in [16]–[21] consists of inductor, proposed MGD doesn't require inductor for its operation. Therefore power density of proposed MGD is more and is easier to integrate in IC form.
2) *Absence of control switches:* Previous DCSDs proposed in [16]–[20] employ four control switches and DCSD proposed in [21] employs two control switches but proposed MGD doesn't require control switch. Therefore reduces the complexity of the circuit and also reduces the overall size of gate driver circuit.
3) *Negligible propagation delay:* Proposed MGD achieves negligible propagation delay. Therefore making it suitable for driving synchronous converter to increases the loop response due to negligible propagation delay.
4) *C(dv/dt) immunity:* Similar to other current source drivers, in proposed MGD, SiC MOSFET is either clamped to zero or to V_{cc}. Hence making the power MOSFET immune to spurious turn-on due to high *C(dv/dt)*.

Depending on the operation, different types of driver circuit consists of different types of components, such as inductor, capacitor, resistor and switches. Inductor occupies significant space. Switches require a separate predrivers for its operation, thereby increasing the complexity of operation. Presence of bridge circuits in the circuit enforces introduction propagation delay in the form of dead time. Hence a gate

driver consisting of different types of components and its number, provides the information about the performance and complexity of the driver. Topological comparison between proposed MGD and gate driver circuits mentioned in the literature are summarized in Table 4. Nature of output current in gate driver proposed in [17], [20], and [21] is continuous in nature making the driver more lossy compared to other drivers. Gate driver circuits proposed in [17], [20], and [21] consists of more number of inductor, hence making these drivers much bulky and less power density. Gate driver circuit proposed in [15] and [20] consists of most number of total components as compared to other circuits, hence are more complex. Gate driver circuit proposed in [14]–[17], [19], and [20] require four predrivers for its operation, making these drivers more complex to control and implement. Half-bridge or full-bridge configuration is present in all the gate drivers proposed in [13]–[17], [19]–[21]. Hence dead time operation required in these circuits will result in propagation delay of the overall gate driver circuit. Absence of inductor in the proposed MGD, results in much compact size and easier to integrate in an IC form. In proposed MGD, operation of switches in self-biased mode and nature of cascode mirror operation, doesn't demands additional predriver circuits. Hence the complexity of the circuit is reduced and overall efficiency of the circuit is improved.

VII. CONCLUSION

In this paper, an inductor-less discontinuous current source gate driver is presented. Absence of inductor makes this current source gate driver more compact and light weight. However absence of inductor and capacitors in the proposed MGD, make it unable to recover gate energy. Discontinuous current property reduces the driver losses. PMOS based cascode current mirror as current source is considered to drive the device. Self-biased operation of PMOS in cascode mirror eliminates the requirement of predrivers for its operation hence making the proposed mirror gate driver simple. Proposed mirror gate driver is validated using hardware prototype and a detailed performance analysis for driving SiC MOSFET is performed. Comparative analysis of proposed mirror gate driver and IXYS driver is performed under similar operating condition. A significant reduction of 55% in voltage overshoot during turn-off is obtained with proposed mirror gate driver. Minimal propagation delay is achieved with the proposed mirror gate driver making it suitable for high frequency switching of SiC MOSFETs. A better trade-off between switching losses and EMI is obtained with the proposed mirror gate driver, where during turn-off, 65% of reduction in dV_{ds}/dt and 45% of reduction in dI_d/dt is achieved at the cost of 33% increase in total switching loss. Hence the proposed mirror gate driver provides immunity to the EMI for the power device.

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