Performance Investigation of Back Gated SiO_2/HfO_2 Stacked Gate Oxide Ge/Si Heterojunction STFET

4.1 Introduction

As we have discussed in chapter-2, VSG-HJ STFET increases the drive current, I_{ON}/I_{OFF} ratio and thermal insulation along with decrease in leakage current. In chapter-3 it was noticed that dual material gate engineering along with horizontal gate staking increased the reliability in STFETs. These improvements in trapped charges reliability was done at the cost of increased fabrication complexity. Therefore where trapped charges reliability is not required we can go for VSG-HJ-STFET as proposed in chapter-2. Further from chapter-1, it is seen that the tunnel Field Effect Transistors (TFETs) are gated reverse-biased p-i-n diodes which can achieve sub-60 mV/dec subthreshold swing by the principle of the band to band tunneling [41]-[46]. TFETs turn on at a low operating voltage [44]. This can be achieved in two ways, by modulating the tunnel barrier by changing the gate voltage and using the density of states switching. Low OFF-state current and subthreshold swing (*SS*) provides TFETs the commercial potential to be superior to MOSFETs [44]. However, the low ON-state current in TFETs is a matter of concern. Moreover, TFETs show the unique property of ambipolarity which is the conduction of current at both high negative and high positive gate voltages. Ambipolar conduction makes the TFET vulnerable in complementary-FET circuit applications thus limiting its utility in digital circuits [184]-[185].

In order to improve the performance of TFETs, VSG-HJ STFET was proposed in chapter-2. Increase in drive current is essential for circuit applications. Therefore in this chapter we propose a Back Gated VSG-HJ STFET called (BG-HJ-STFET) to further

increase the drive current. After a thorough simulation analysis, we observed that the DC/RF and linearity analysis performance of the BG-HJ-STFET has improved. TFETs with back gate shows improved BTBT rate, leading to the enhanced on-current [131], [186]-[187]. However, the ambipolar current of BG-HJ-TFET is also increased since the BTBT rate improvement is activated in the ambipolar state as well [131], [188].

The following is the structure of this chapter: The device's schematic structure and parameters are specified in section 4.2. Section 4.3 provides fabrication steps, section 4.4 discusses simulation setup and model calibrations, section 4.5 contain results and analysis, and section 4.6 concludes the work.

4.2 Device Under Study

4.2.1 Schematic Structure of the Device

Figures 4.1 (a) and (b) depict the proposed device architecture without and with the back gate respectively. To make the reader more convincing, the nomenclatures for the presented TFETs are given as follows: The homojunction TFET without any back gate (single gate) is abbreviated as SG-STFET; similarly, heterojunction TFET without any back gate (single gate) is abbreviated as SG-HJ-STFET. In the case of back gated TFETs having homojunction and heterojunction are named BG-STFET and BG-HJ-STFET respectively. The optimized device parameters used for device-level performance analysis are listed in table 4.1.

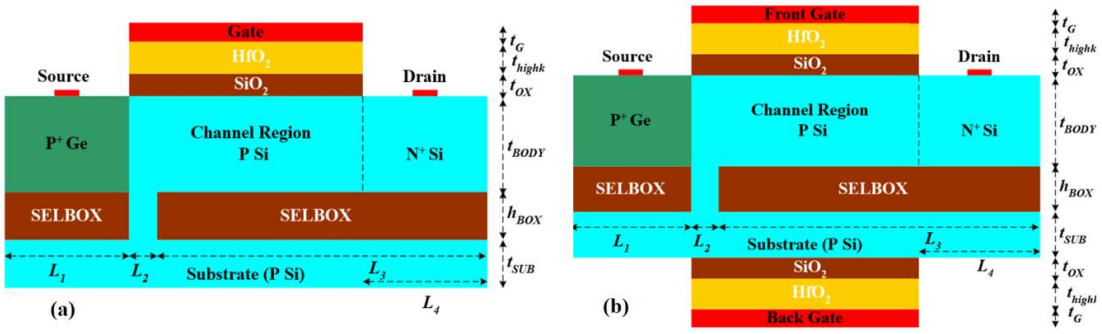

Figure 4.1 2-D schematic structures of (a) SG-HJ-STFET, and (b) BG-HJ-STFET.

4.2.2 Possible Fabrication Steps

The fabrication feasibility of BG-HJ-STFET is given below and other presented TFETs are assumed to have the same process flow [109], [189]-[190].

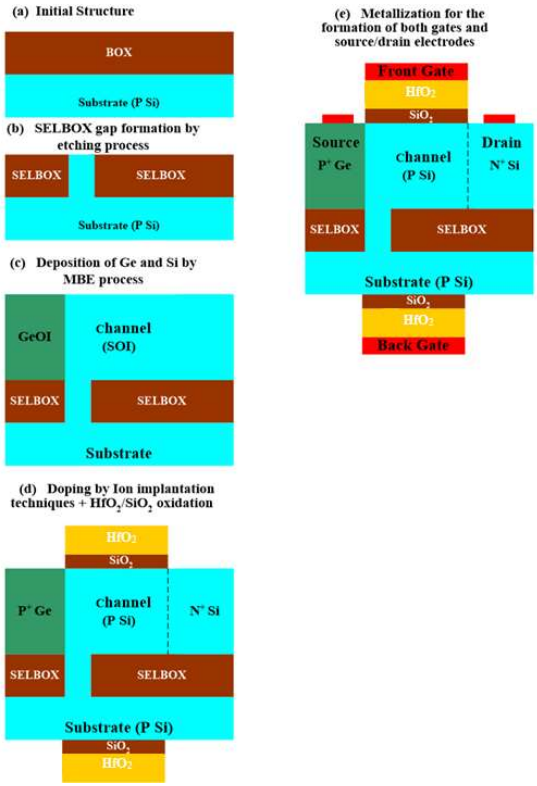

Figure 4.2 Fabrication Steps of BG-HJ-STFET.

- A clean silicon substrate is considered where oxidation is done to form an SOI structure.
- A small gap is created in the SOI structure to form a SELBOX structure.
- MBE Epitaxial process is used for the growth of the drain, channel, and source (Ge) region.
- P^+ and N^+ impurity implantation in source and drain regions.
- Gate dielectric formation using atomic layer deposition (ALD) process form vertical stack SiO_2/HfO_2 structure followed by metallization, as shown in Figure 4.2.

Table 4.1 Device Parameters for the simulation.

Parameters	**SG- HJ-STFET**	**BG-HJ-STFET**
Source doping concentration (N_S)	1×10^{19} cm^{-3}	1×10^{19}cm^{-3}
Channel doping concentration (N_{ch})	1×10^{16} cm^{-3}	1×10^{16} cm^{-3}
Drain doping concentration (N_D)	5×10^{18} cm^{-3}	5×10^{18} cm^{-3}
The thickness of the channel (t_{Si})	15 nm	15 nm
The thickness of SiO_2 gate oxide (t_{ox})	1 nm	1 nm
The thickness of High-k gate oxide (t_{ox})	2 nm	2 nm
Effective Oxide Thickness (EOT)	1.312 nm	1.312 nm
Gate length (L_G)	40 nm	40 nm
Source length (L_S)	30 nm	30 nm
Left side SELBOX Length (L_1)	31 nm	31 nm
Drain length (L_4)	30 nm	30 nm
Right side SELBOX Length (L_3)	67 nm	67 nm
Thickness of buried oxide (BOX) (t_{BOX})	10 nm	10 nm
Length of SELBOX gap (L_2)	2 nm	2 nm
Hole tunnel mass in silicon (m_{htSi})	0.24m_o	0.24m_o
Hole tunnel mass in germanium (m_{htGe})	0.044m_o	0.044m_o
Electron tunnel mass in silicon (m_{etSi})	0.20m_o	0.20m_o
Electron tunnel mass in germanium (m_{etGe})	0.082m_o	0.044m_o
Lattice constant of Ge	5.656 ^{0}A	5.656 ^{0}A
Lattice constant of Si	5.429 ^{0}A	5.429 ^{0}A
Bandgap energy Ge	0.70 eV	0.70 eV
Bandgap energy Si	1.12 eV	1.12 eV
Electron affinity Ge	4.01 eV	4.01 eV
Electron affinity Si	4.05 eV	4.05 eV
Front Gate Metal Work Function (eV), ψ_{sf}	4.1 eV	4.1 eV
Back Gate Work Function (eV), ψ_{sb}	4.1 eV	4.1 eV

4.2.3 Simulation Setup and Models Approval

SILVACO ATLAS TCAD tool is used for the simulation of all the aforementioned structures [157]. We have already described models in Chapter 1, including the nonlocal band-to-band tunneling (BTBT) model, the Shockley-Read-Hall model (SRH), the AUGER recombination model, and the mobility model based on concentration (CONMOB), and the mobility model based on electric field (FLDMOB).

To assure the validity of the aforesaid models, we have calibrated our used models with previously reported experimental work [158]. To do so, we have considered TFET of the same dimension as reported in the experimental work. Figure 4.3 demonstrates the comparative plot between experimental work and simulation results including our used models. The outcome acquired is close to prior reported experimental work [158], which approves the models included during the simulation process.

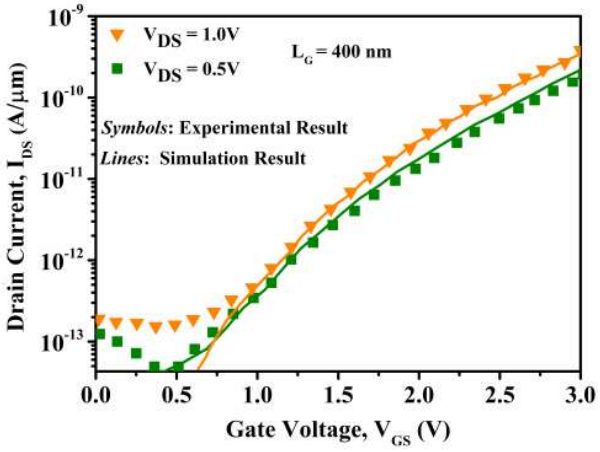

Figure 4.3 Calibration of the ATLAS TCAD models: comparison of simulation data with the experimental result as reported [158].

4.3 Results and Discussion

This section is devoted to analyzing the DC, analog/RF, and linearity characteristics of the proposed back gated heterojunction TFET on SELBOX substrate i.e., BG-HJ-STFET.

The merits of the proposed TFET have been established by comparing the simulation results of the proposed device with the other three TFETs presented for study.

4.3.1 DC Performance Analysis

In this section, we have done a comparative DC performance analysis of all the presented structures for study i.e., SG-STFET, SG-HJ-STFET, BG-STFET, and BG-HJ-STFET. DC performance analysis comprises a study of transfer characteristics, surface potential, energy band diagram, and electric field. Figure 4.4 depicts the transfer characteristics in the logarithm scale for all the devices under study. Here, BG-HJ-STFET provides the highest I_{ON} current compared to other TFETs. Heterojunction-based TFETs are providing higher ON-state current than homojunction (Si) based TFETs. This is because of low band gap material like Ge present at the source region to form Ge/Si heterojunction which in turn enhances tunneling of carriers from source to channel increase [46], [72], [74]-[75], [82]. I_{ON} and I_{OFF} current exhibited by BG-HJ-STFET are 2.74322×10^{-5} A/μm and 2.029×10^{-16} A/μm respectively. In addition, I_{ON}/I_{OFF} ratio and sub-threshold swing (SS) are found to be the best for the proposed TFET i.e., BG-HJ-STFET. DC parameters for all the presented TFETs are listed in table 4.2.

Figure 4.5 (a) shows the plots of surface potential w.r.t the device length for all the aforementioned devices. It is evident from the figure that the surface potential of the proposed BG-HJ-STFET is having a higher value compared to other TFETs. This is again due to the use of both heterojunction and back gate which increases the overall surface potential of the proposed TFET. Figure 4.5 (b) demonstrates the electric field in the ON-state for all presented TFETs. The electric field is found to be maximum for the BG-HJ-STFET compared to other devices. The reason for the same can be attributed to the presence of heterojunction along with the back gate which in turn increases the electric field. Figures 4.6 (a) and (b) show the energy band diagram in OFF-state and ON-state,

respectively. In ON-state, the application of gate voltage makes the band alignment in such a way that there will be tunneling of electrons from the valence band of the source to the conduction band of the channel region whereas in OFF-state due to misalignment between the valence band of the source to the conduction band of the channel no such tunneling of electrons is possible.

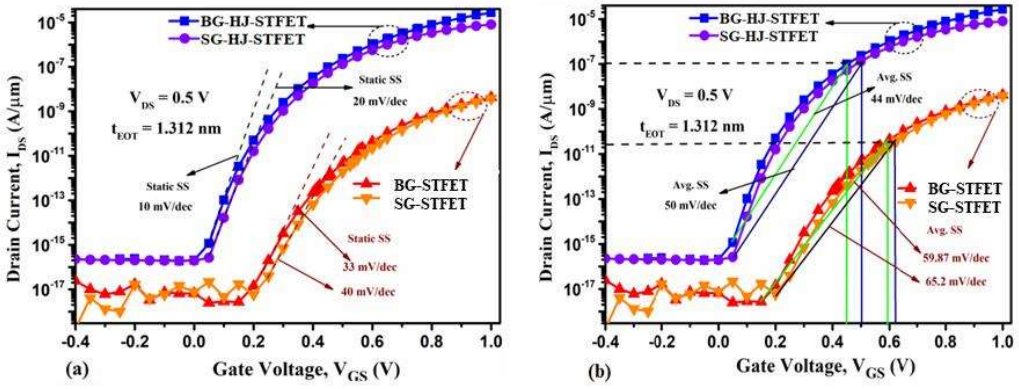

Figure 4.4 Comparative plots of logarithmic drain current versus gate voltage of BG–HJ- STFET, (BG-STFET) and SG-HJ-STFET (SG-STFET) with the analysis of (a) Static Subthreshold swing (SS) and (b) Average subthreshold swing (SS).

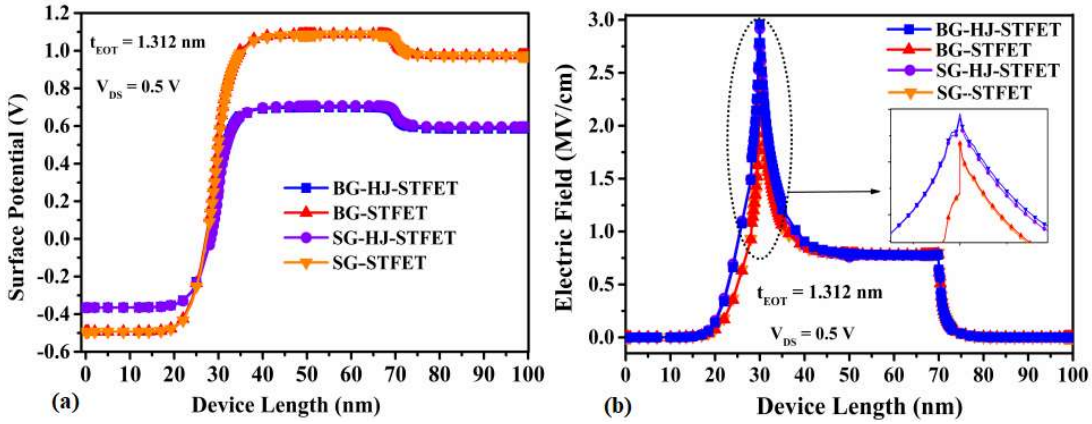

Figure 4.5 Comparative plots of (a) surface potential, and (b) electric field at on-state for all the presented TFETs.

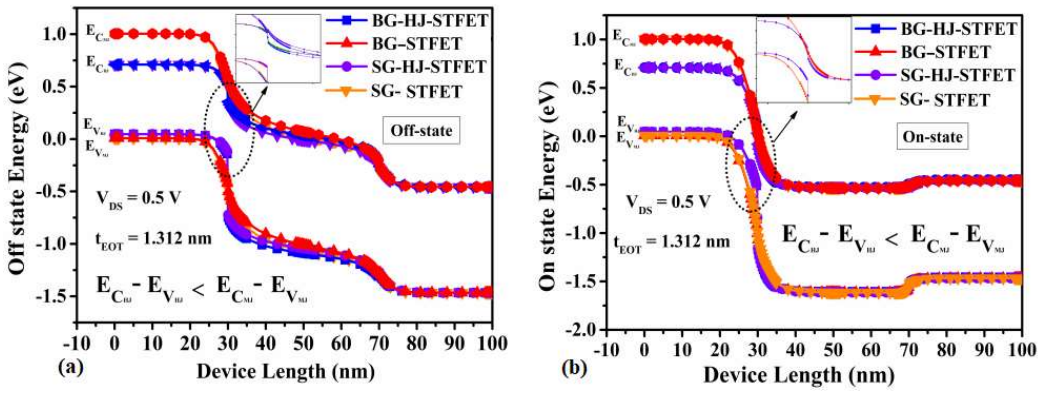

Figure 4.6 Comparative plots of (a) OFF-state energy band diagram, and (b) ON-state energy band diagram for all the presented TFETs.

Table 4.2 Performance **c**omparative table among all the studied TFETs.

Parameters /units	**BG-HJ-STFET**	**BG-STFET**	**SG-HJ STFET**	**SG-STFET**
I_{ON}/I_{OFF}	1.35×10^{11}	6.2×10^{8}	4.1×10^{10}	5.0×10^{8}
Static SS (mV/dec)	10	33	20	40
Average SS (mV/dec)	44	59.9	50	65.2
Threshold voltage (V_t), (V)	0.45	0.80	0.5	0.82

4.3.2 RF Performance Analysis

Semiconductor enterprises need low-power devices without a decrease in switching speed. Today's IC industry faces a big challenge to maintain high operating frequency without an added increase in power supply [191]. Therefore, RF performance investigations of the presented structure i.e., SG-STFET, SG-HJ-STFET, BG-STFET, and BG-HJ-STFET are highly needed to make them operate at higher frequency with low supply voltage. In this regard, RF parameters like transconductance (g_m), the gate to drain capacitance (C_{gd}), cut-off frequency (f_T), and transit time (τ) are explored here. To decide the efficiency of the device, transconductance (g_m) is a significant parameter that

demonstrates the capacity of the device to reflect drain current against gate voltage and it is given by Eqn: 4.1[179]:

$$g_m = \frac{dI_D}{dV_{GS}} \tag{4.1}$$

$$\tau = \frac{1}{2\pi f_T} \tag{4.2}$$

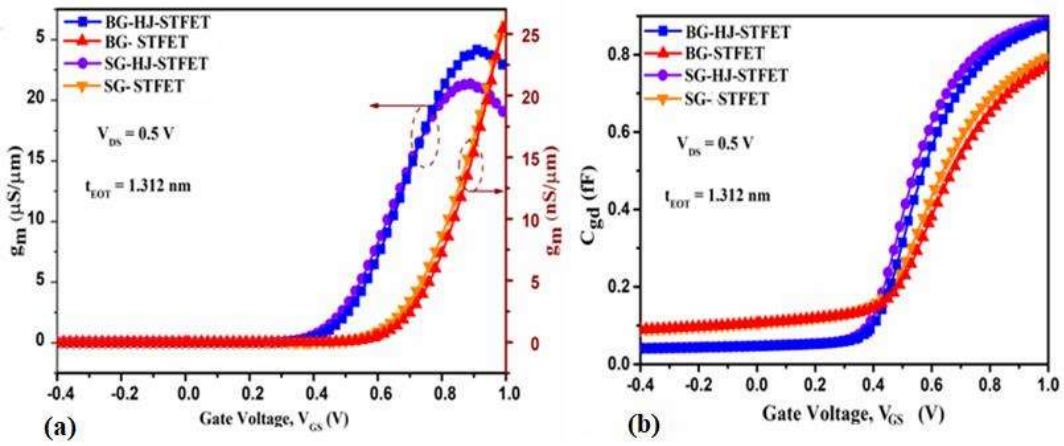

Figure 4.7 Comparative plots of (a) transconductance (g_m), and (b) intrinsic gate to drain capacitance (C_{gd}), for all the presented TFETs.

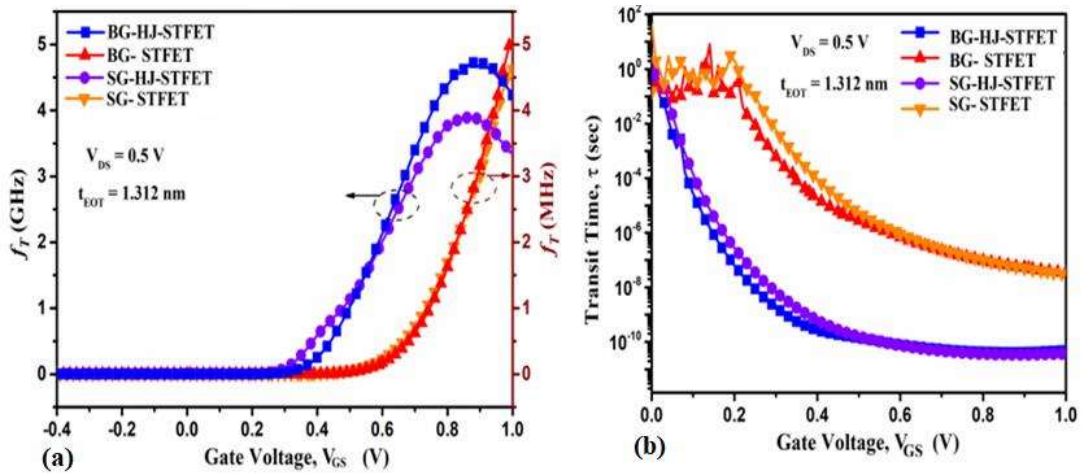

Figure 4.8 Comparative plots of (a) cut-off frequency (f_T), and (d) transit time (τ) for all the presented TFETs.

The g_m plots for all of the reported TFETs vs. V_{GS} are shown in Figure 4.7 (a). It can be seen from this plot that the BG-HJ-STFET has greater g_m values than other structures

with a maximum value of 24 μS/μm. After attaining a peak g_m subsequently starts to diminish for higher values of V_{GS} because of mobility saturation of carriers [191]. The effect of parasitic capacitance on high-frequency parameters is found to be very significant. Keeping this in mind, the study of parasitic capacitance is extremely needed for all the TFETs under study. In TFET, gate-to-drain intrinsic capacitance (C_{gd}) is the important intrinsic parasitic capacitance compared to the gate-to-source intrinsic capacitance (C_{gs}) [26]. In Figure 4.7 (b), it can be observed that C_{gd} is higher for heterojunction-based TFETs compared to homojunction (Si) based TFETs. Another essential RF parameter is the cut-off frequency (f_T) which plays an important role in deciding the device's performance at high frequency. Figure 4.8 (a) demonstrates the f_T versus V_{GS} plots where f_T increases with an increase in V_{GS} and reaches a maximum value of 4.5 GHz for the proposed BG-HJ-STFET. Transit time (τ) is another important parameter for analog/RF performance examination which estimates the time required by carriers to travel from source to drain region. Consequently, it determines how quickly the device can work for digital applications, and the expression for the same is given in Eqn: 4.2. Figure 4.8 (b) demonstrates the transit time plot for all the TFETs under study and the curve itself approves that the transit time required by the carriers for the proposed device is very low having a value of 0.5 ns. It signifies that the proposed device can work faster compared to other TFETs presented for study. From all these RF performance analyses it is clear that the proposed BG-HJ-STFET is better than the other structures and can be used for high-frequency applications.

4.3.3 Linearity Performance Analysis

For high-frequency applications, we need linear devices with lower harmonic signal distortion. In today's technology, most devices are operated in the GHz range. Therefore,

linearity study is very much essential to have distortionless communication systems is also considered linear devices. As transconductance (g_m) varies with V_{GS}, linearity figures of merits (FoMs) are investigated in terms of the second and third derivative of drain current vs. V_{GS} (gm_2 and gm_3), second-order voltage intercept point (VIP2), third-order voltage intercept point (VIP3), third-order intermodulation distortion (IMD3), IIP3 and 1-dB compression point. These parameters can be mathematically expressed as [192].

$$g_{m2} = \frac{\partial^2 I_D}{\partial V^2_{GS}} \tag{4.3}$$

$$g_{m3} = \frac{\partial^3 I_D}{\partial V^3_{GS}} \tag{4.4}$$

$$VIP2 = 4X \frac{gm1}{gm2} \tag{4.5}$$

$$VIP3 = \sqrt{24X\left(\frac{gm1}{gm3}\right)} \tag{4.6}$$

$$IIP3 = \frac{2}{3}X\left(\frac{gm1}{gm3\ X\ R_S}\right) \tag{4.7}$$

$$IMD3 = \left[\frac{9}{2}X\,(VIP3)^3\ X\ g_{m3}\right]^2 X\ Rs \tag{4.8}$$

$$1-dBcompressionpoint = 0.22\sqrt{\frac{g_m}{g_{m3}}} \tag{4.9}$$

where R_s = 50 Ω.

The g_{m2} and g_{m3} are the elementary parameters that may be affected during high-frequency operation and cause distortion which prompts non-linearity. Figure 4.9 (a) shows the variation of g_{m2} vs. V_{GS} where the maxima of g_{m2} at the minimum conduction point give the rejection of the odd harmonics with maximum conversion gain.

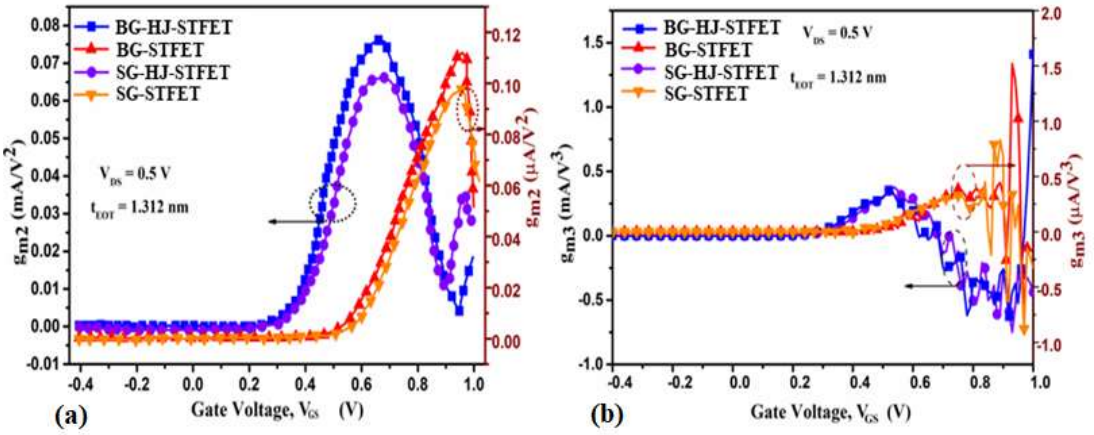

Figure 4.9 Comparative plots of (a) g_{m2} and (b) g_{m3} versus gate voltage at V_{DS} = 0.5 V.

Figure 4.9 (b) shows plots of g_{m3}, which provides zero crossover points and zero crossover points (ZCP) is the sign of the best appropriate DC biasing point. ZCP indicates exceptionally low distortion in device execution [193]. It can be concluded from the same figure that the higher-order derivative of transconductance for the proposed BG-HJ-STFET is better than all other TFETs presented for study. Figure 4.10 (a) shows the ZCP of all the TFETs where the proposed BG-HJ-STFET is found to have a minimum value of ZCP. This proves the linearity of the proposed device. 1-dB compression point is another linearity parameter, defined as the input power at which gain drops by 1-dB. It should be as high as possible to have better linearity. Figure 4.10 (b) shows the 1-dB compression point of all the TFETs under study. Here it can be depicted that the proposed BG-HJ-STFET shows to have a higher value of 1-dB compression point.

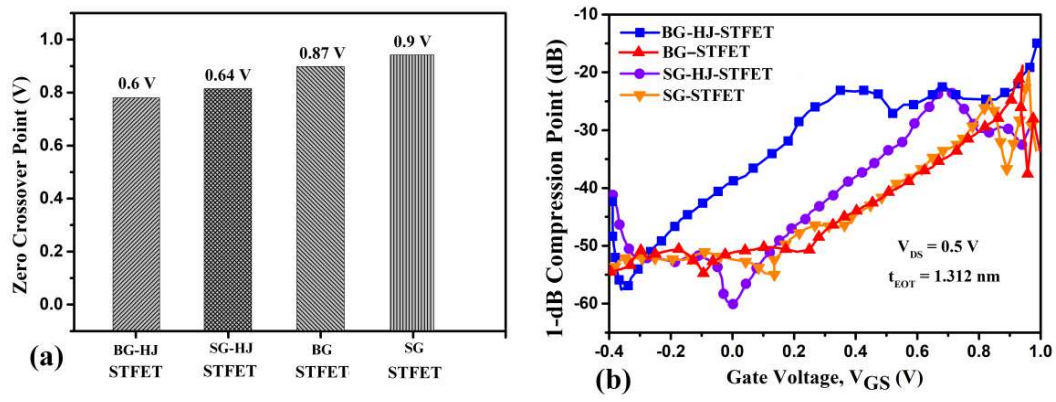

Figure 4.10 Comparative plot of (a) zero crossover point and (b) 1-dB compression point of all the TFETs presented for study.

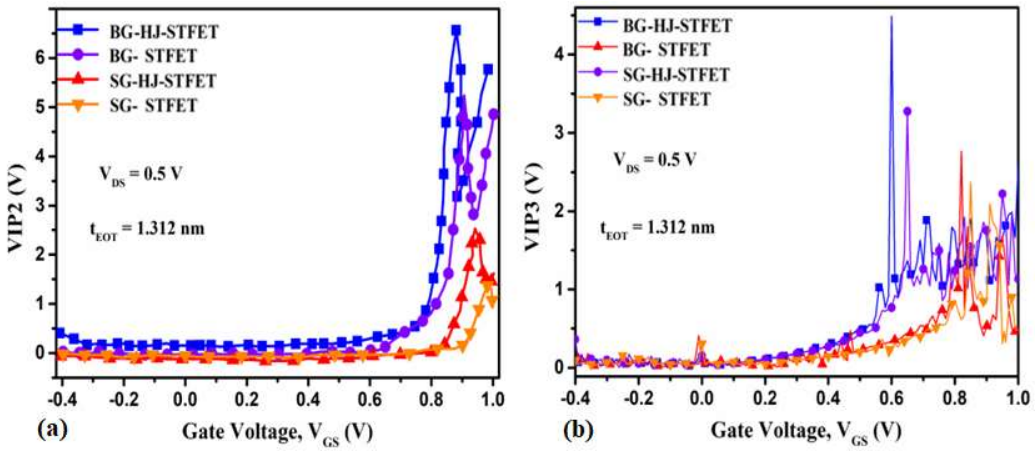

Figure 4.11 Plots of (a) VIP2, and (b) VIP3 of all mentioned devices with V_{GS} at V_{DS} = 0.5 V.

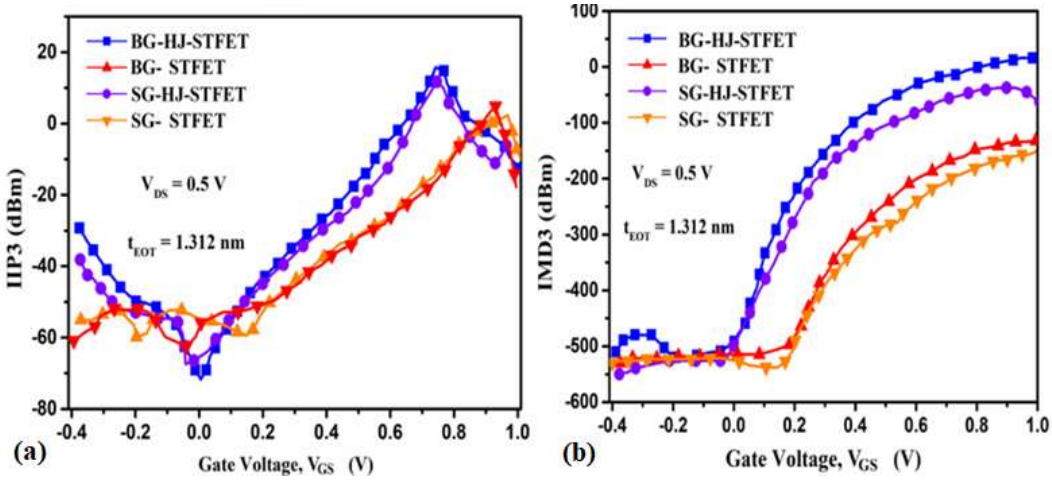

Figure 4.12 Plots of (a) IIP3 and (d) IMD3 of all mentioned devices with V_{GS} at V_{DS} = 0.5 V.

VIP2 is the voltage at which first and second harmonic voltages are the same

whereas VIP3 is the voltage at which 1st and 3rd harmonic voltages are the same [193]. The maximum value of VIP2 and VIP3 reflects the improvement of linearity and distortion performance of the device. It can be visualized from Figures 4.11 (a) and (b) that the VIP2 and VIP3 for the proposed BG-HJ-STFET is having higher values than other TFETs under study. Similarly, IIP3 is the power at which 1st and 3rd harmonics power are equal. It should be as high as possible to maintain linearity. From Figure 4.12 (a), it is found that the IIP3 for the proposed BG-HJ-STFET is better than all other TFETs under study. Another linearity parameter is IMD3. It also signifies the intermodal power distortion which should be as low as possible to have better linearity. Figure 4.12 (b) shows the IMD3 for all the TFETs presented for the study where the proposed BG-HJ-STFET is shown to have a lower value of IMD3 compared to other TFETs. For all the above studies of linearity parameters, it is found that the proposed BG-HJ-STFET has better linearity performance than other TFETs under study which approves it for use in next-generation communication systems.

4.4 Design of BG-HJ-STFET based Inverter

This section analyses the circuit-level performance where a digital inverter circuit has been implemented by considering the proposed BG-HJ- STFET only. In this regard, two sets of 2D lookup tables of current and capacitances are developed for both n-TFET and p-TFET using the exported data from the Silvaco ATLAS TCAD tool. The lookup tables are then implemented in the CADENCE tool with the help of the Verilog-A model to design an inverter circuit [194]. The DC, as well as transient performance, is analysed for the inverter based on the proposed BG-HJ-STFET. Figure 4.13 (a) shows the schematic diagram of the inverter circuit based on the proposed BG-HJ-STFET and the corresponding voltage transfer characteristics (VTC) of the inverter are shown in Figure

4.13 (c). Figure 4.13 (b) shows the transfer characteristics of both n-BG-HJ-STFET and p-BG-HJ-STFET at V_{DS} = 0.5 V and it is found that a good symmetry is obtained for the proposed TFET. The symmetry is obtained by taking the p-BG-HJ-STFET gate material work function to 4.5 eV. Voltage Transfer Characteristics (VTC) is a plot of an inverter between the output and input voltage and it is used to give the information related to the static noise margin (SNM) of the inverter [194]-[195]. To make this VTC plot, we have varied the V_{IN} from 0 to V_{DD} and the corresponding V_{OUT} is taken for every V_{IN} value. From Figure 4.13 (c), the static noise margin can be calculated by calculating V_{IL}, V_{IH}, $V_{OL,}$ and V_{OH}. Input low voltage (V_{IL}) and input high voltage (V_{IH}) are the voltages of an inverter where the $\frac{dV_{out}}{dV_{in}} = 1$ which is indicated in Figure 4.13 (c). It can be also observed from Figure 4.13 (c) that with the application of a small input voltage (V_{IN} = 0 V), the output voltage reaches the maximum (V_{OH}) value, and with a maximum input voltage (V_{IN} = V_{DD}) the output voltage retains to minimum (V_{OL}) value. The static noise margin for an inverter is the amount of noise that can withstand without flipping its contained. The static noise margin can be defined as follows [194]-[198]:

NM_L (Noise Margin Low) = $V_{IL} – V_{OL}$ = 0:36 - 0 = 0.36 V (4.9)

NM_H (Noise Margin High) = $V_{OH} – V_{IH}$ = 1 - 056 = 0.44 V (4.10)

So, the static noise margin low (NM_L) for the proposed BG-HJ-STFET is 0.36 V and the static noise margin high (NM_H) for the proposed BG-HJSTFET is 0.44 V. The transient analysis of the proposed BG-HJ-STFET is shown in Figure 4.13 (d). The proposed device is found to have a better transient response with a propagation delay of 90 ps and power dissipation of 250 Nano watts. The overshoot in the output voltage is due to the presence of miller capacitances in between different nodes of the BG-HJ-STFET.

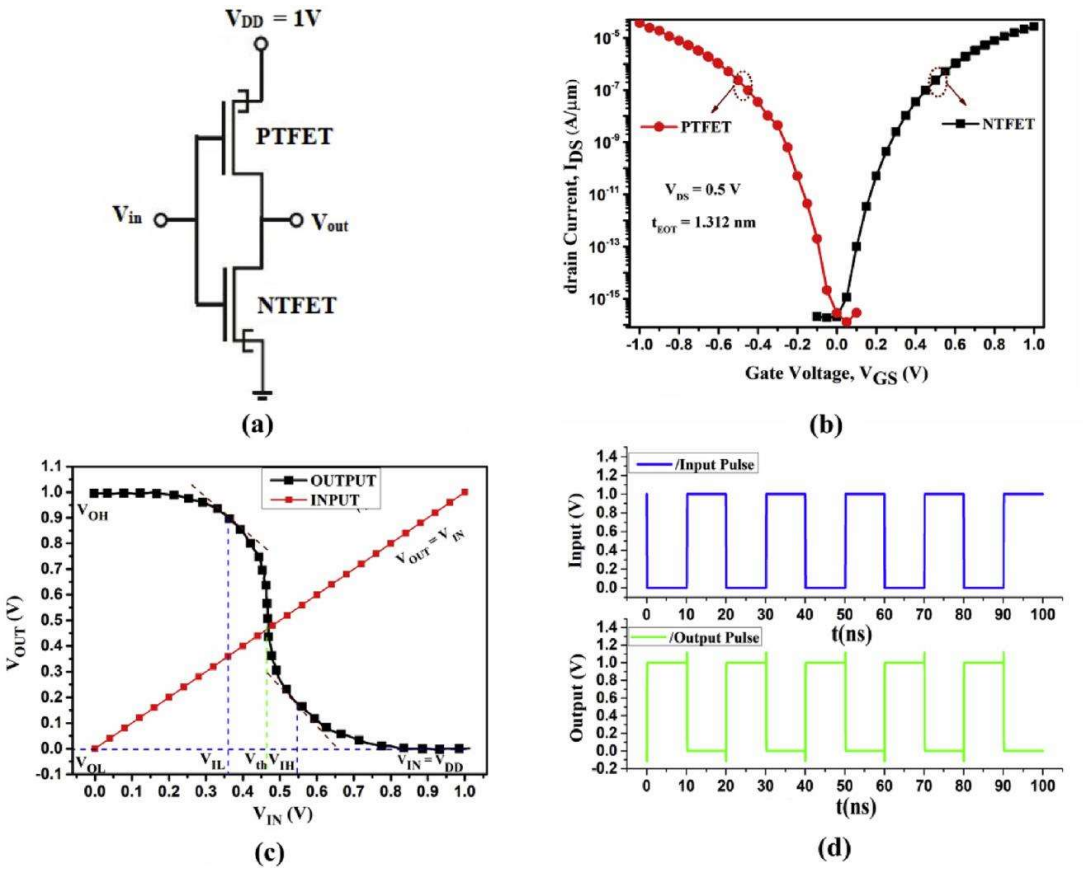

Figure 4.13 (a) Circuit diagram of inverter-based on BG-HJ-STFET (b) drain current versus V_{GS} plots of n-type and p-type BG-HJ-STFETs, (c) voltage transfer characteristics (VTC) of BG-HJ-STFET inverter (d) transient analysis of BG-HJ-STFET.

4.5 Conclusions

In this chapter, we have designed a back gated Si/Ge heterojunction TFET on SELBOX substrate (BG-HJ-STFET). The simulations of the presented TFETs are carried out using the SILVACO ATLAS™ TCAD tool. The proposed BG-HJ-STFET based on heterojunction shows better DC, RF, and linearity performance compared to other TFETs presented for the study i.e. SG-HJ-STFET, SG-STFET, and BG-STFET. Sub-threshold swing is found to be minimum for the proposed BG-HJ-STFET compared to other structures which makes it suitable for low-power applications. The linearity viability and high-frequency performance analysis are carried out using some figures of merit (FOMs)

such as higher-order of gm, VIP2, VIP3, IIP3, IMD3, and 1-dB compression point. All linearity analyses reveal that BG-HJ-STFET can be utilized in distortion-less communication systems. In addition, circuit-level performance shows that our proposed device i.e. BG-HJ-STFET is suitable for digital circuits because of its lower propagation delay. Lower power dissipation of the inverter designed using BG-HJ-STFET makes it suitable in low voltage electronics applications.