DEVICE MODELING AND LOGIC CIRCUITS DESIGN FOR SPIN-BASED COMPUTING

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Award of Degree

Doctor of Philosophy

By

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CHAPTER-5

Summary and Future Scope of Research

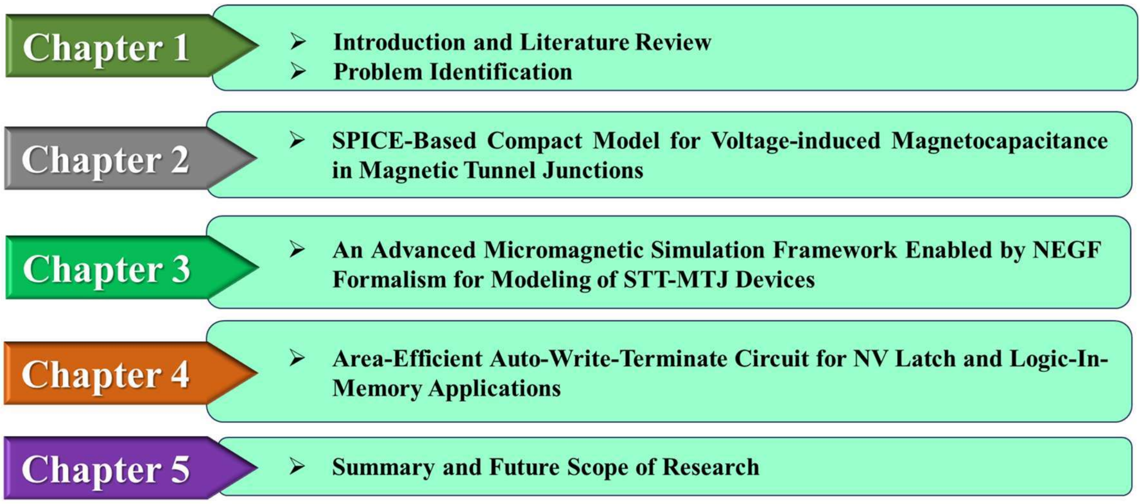

Figure 5.1 Thesis chapter outlines

In this thesis, a comprehensive study on the MTJ device modeling and logic circuits towards a spin-based computing architecture is presented. The main contributions of the thesis are illustrated in **Figure 5.1**. The first part of the thesis is dedicated to developing a compact model and micromagnetic simulation framework, which can be utilized for the design and analysis of the hybrid CMOS/MTJ circuits and MTJ devices, respectively. In the second part of the thesis, a novel STT-MTJ-based non-volatile latch with an AWT circuit is demonstrated. This design effectively eliminates redundant MTJ writing by terminating the write operation once they are completed, thereby enhancing reliability and minimizing power dissipation. The proposed design is compact since it reduces the area requirement.

5.1 Chapter-wise Summary

Chapter 1 presented an introduction to the thesis, encompassing a brief literature review covering the fundamentals and background of spintronics devices, with particular emphasis on the MTJ device. It began with a brief literature review that highlighted the advantages of MTJ devices over conventional technologies, followed by a study of their working principles and key properties, including magnetic anisotropy, TMR, TMC, and STT switching techniques. Furthermore, the chapter explored various modeling approaches for MTJ devices. It covered compact modeling, which is essential for designing hybrid CMOS/MTJ circuits, as well as micromagnetic modeling, which provided a detailed analysis of the magnetization dynamics in spin devices. The chapter also included the hybrid CMOS/MTJ logic-in-memory (LiM) architectures for spin-based computing, discussing its components such as sense amplifiers, write circuits, AWT circuits, and the nMOS logic tree used to design logic functions, as well as non-volatile latches and flip-flops. Finally, the chapter concluded with the problem statement for the thesis, setting the stage for the research contributions presented in the subsequent chapters.

Chapter 2 presented a compact model of MTJs compatible with the SPICE simulator. This model incorporated both the TMR and TMC effects of MTJ devices, accurately emulating their behavior with respect to bias voltage and frequency. Validation through HSPICE simulations demonstrated a strong alignment with experimental data, highlighting the robustness of the model. The integration of the TMC effect, known for its high magnetic sensitivity, thermal stability, and robustness against bias voltage, opened up new possibilities for designing and implementing spintronics applications. These included highly sensitive magnetic sensors, voltage-controlled electronic components, energy storage devices, read-out circuits for sensors, and neuromorphic computing.

Chapter 3 also focused on MTJ device modeling, where we developed an advanced simulation framework that integrates micromagnetic simulations with the NEGF formulation-based spin transport model. This framework enabled a more comprehensive analysis of STT switching behavior in MTJ devices, addressing limitations in previously developed embedded micromagnetic simulation frameworks that relied on an OOMMF evolver extension module, which lacked an appropriate spin transport module for accurate modeling of STT-MTJ devices. In this simulation framework, micromagnetic simulations were performed by updating critical MTJ parameters, which continuously evolved throughout the magnetization switching process, such as the magnetoresistance of parallel and anti-parallel states, in-plane and out-of-plane spin torque, and spin efficiency terms ($\in$ and $\in'$), derived from the spin transport model. Additionally, the framework incorporated NUCD distribution to further enhance its capabilities. This framework provided a more accurate representation of the STT switching process, offering a pathway to optimize STT-MTJ devices for practical applications in non-volatile memory and novel computing systems.

Chapter 4 presented a final contribution of the thesis work, wherein we explored the development of novel hybrid CMOS/MTJ circuits for spin-based computing. In this chapter, we introduced a novel STT-MTJ-based non-volatile latch featuring an AWT mechanism, which enhances reliability, improves read/write speed, and reduces the write power requirements. The proposed non-volatile latch design eliminates the need for additional write driver circuits, leading to a smaller footprint and separate read/write paths that eliminate the possibility of erroneous writing. The AWT circuit was particularly significant, as it monitored the write operation to prevent redundant writing and excessive current flow through the MTJ, resulting in substantial energy savings. Specifically, the proposed AWT circuit reduced total write energy by ~83 % with 75 % fewer transistors compared to conventional circuits. Overall, the thesis demonstrated that the novel latch and AWT circuits significantly improve area and power efficiency, which were designed and simulated using industry standard 130nm CMOS PDK and MTJ compact models.

5.2 Future Scope of Research

The future scope of research based on the work presented in this thesis includes several promising directions. The scope of Chapter 2 offered significant potential for applying the TMC effect to a wide range of applications and advancing MTJ modeling. Key areas for future exploration include:

- ***Design and implementation of circuits for emerging computing paradigms***: The developed compact MTJ model could be utilized to investigate various circuits for emerging computing architectures, such as neuromorphic computing or memory centric computing. The high sensitivity and thermal stability of the TMC effect suggested potential applications in highly sensitive magnetic sensors, voltage-controlled electronic components, energy storage devices, and adaptive AI circuits, providing a rich area for further research.
- ***Advanced MTJ modeling***: The compact MTJ model could be further advanced by the incorporation of new physical effects, to enhance the applicability of the model. For example, extending this model to include multi-layer MTJ stacks or other spintronic materials can be an idea for further exploration.
- ***Application in neuromorphic computing***: The unique properties of MTJs and the enhanced simulation framework could be leveraged for developing neuromorphic computing systems. Future research could explore the use of STT-MTJ devices in synaptic or neuronal architectures, taking advantage of their non-volatility and scalability for implementing brain-inspired computing systems.

The scope of Chapter 3 can be further extended to encompass other spintronic devices and MTJ switching mechanisms. Key areas for future exploration include:

- The advanced simulation framework developed in this chapter provided a strong foundation for the exploration of STT-MTJ devices. Future research could focus on refining the micromagnetic models to incorporate more complex material properties and magnetic interactions. The framework can be extended to skyrmionics and nano-magnet-based devices, which have the inherent capability of implementing logic.

The scope of Chapter 4 can be further expanded to design various arithmetic and logic applications using the area and energy-efficient non-volatile latches. Key areas for future research include:

- ***Development of spin-based, fully non-volatile applications***: The proposed non-volatile latch can serve as a fundamental building block for designing fully non-volatile LiM architectures. Further research could focus on designing power-efficient and compact circuits design for arithmetic and logic applications by exploring different CMOS technology nodes or alternative logic families.
- ***Energy-efficient circuit design***: The significant energy savings achieved by the AWT mechanism present opportunities for its application in other spintronic circuits beyond latches. Future research could explore the adaptation of the AWT concept to different types of non-volatile memory cells and logic gates.

By pursuing these avenues, the foundational work presented in this thesis could be extended and applied to a wide range of futuristic cutting-edge technologies, contributing to the advancement of spintronics and related fields.