Chapter 2

Literature Review

2.1 Two-level Dual-output Converters

The two-level voltage source inverter is designed to simultaneously supply two independent three-phase loads, such as dual motors or a six-phase machine, from a single DC source.

2.1.1 Back to Back (B2B) converter

A conventional configuration for realizing a dual-output converter (DOC) involves interfacing two voltage source inverters (VSIs) in a back to back (B2B) configuration, sharing a common dc-link capacitor or dc voltage source [29, 30]. The standard three-phase, two-level B2B converter comprises of twelve semiconductor switches as shown in Fig. 2.1. Each inverter leg operates independently, enabling the generation of two discrete output voltage levels, V_{dc} and 0, referenced to the negative DC terminal. The electrical decoupling of the two output terminals imparts significant operational flexibility, thereby facilitating its application across diverse domains such as microgrids, wind energy conversion systems (WECS), and AC/AC power conversion [31, 32, 33]. Furthermore, the inherent structural simplicity and modularity of the topology support the seamless implementation of advanced control strategies and modulation techniques [31, 32, 33]. A representative application of this topology is in wind turbine energy systems, as depicted in Fig. 2.2.

Drawbacks of the B2B Converter: The limited two-level output voltage characteristic of the B2B converter results in significant harmonic content, necessitating the use of bulky

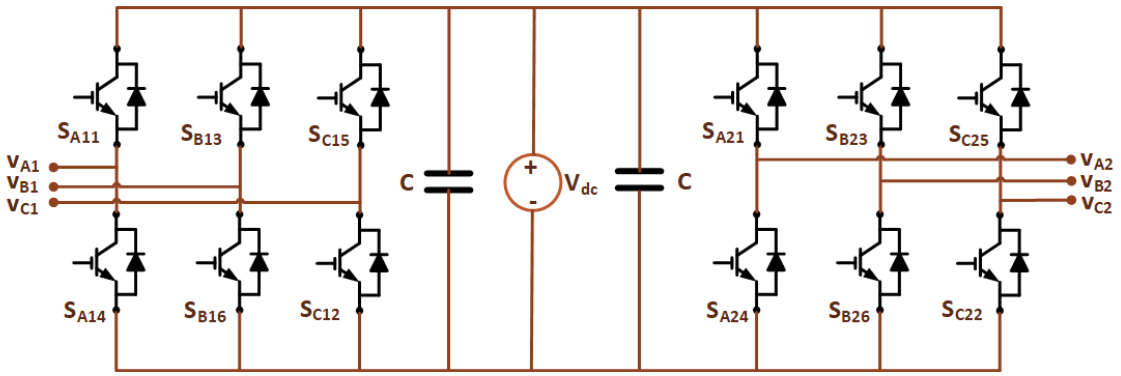


FIGURE 2.1: Three-phase back to back converter.

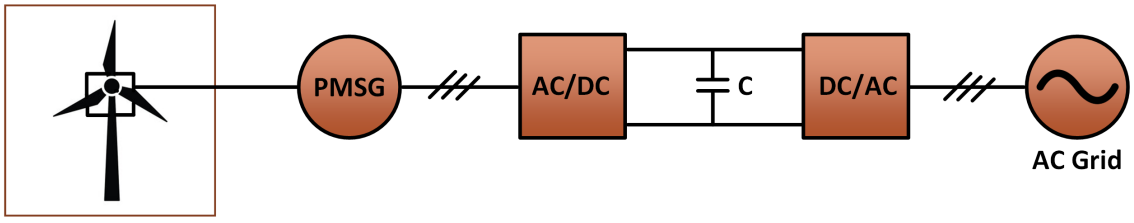


FIGURE 2.2: Application of the B2B converter in grid-tied wind turbine systems.

passive filters to attenuate high-frequency components. The switch count of the back-to-back (B2B) converter is further reduced to develop compact topologies capable of providing two three-phase outputs.

2.1.2 Evolution of Shared Leg DOCs

Early efforts to reduce the switch count of the conventional back to back (B2B) converter led to the development of the four-switch (B4) [34, 35], five-leg [36], and four-leg [37] dual-output converters (DOCs), all tailored for AC/AC power conversion. In a standard two-level inverter often referred to as the B6 topology six switches are employed. By omitting two switches from the B6 and tying the third phase directly to the midpoint of the DC-link, the B4 converter is realized; in this architecture, one output phase is routed to the DC-bus midpoint rather than through a dedicated inverter leg Fig. 2.3 [34, 35]. The four-leg DOC further optimizes the B4 converter by eliminating one inverter leg, thereby reducing the switch count. In this topology, phases A and B of each three-phase output are assigned to individual inverter legs, while both phase C outputs are connected directly to the DC-link neutral point, as illustrated in Fig. 2.4 [36]. The five-leg converter further economizes on hardware by having two AC ports share a common leg, in this case,

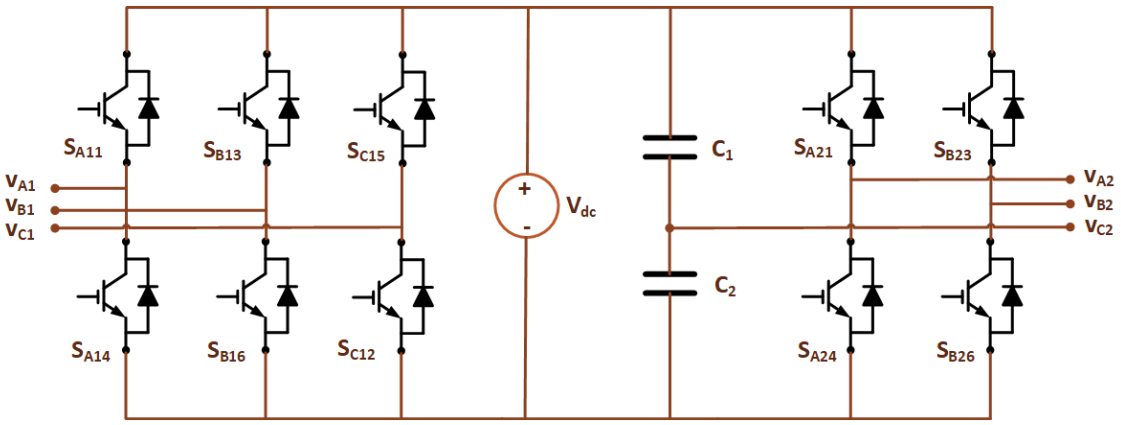


FIGURE 2.3: B4 converter.

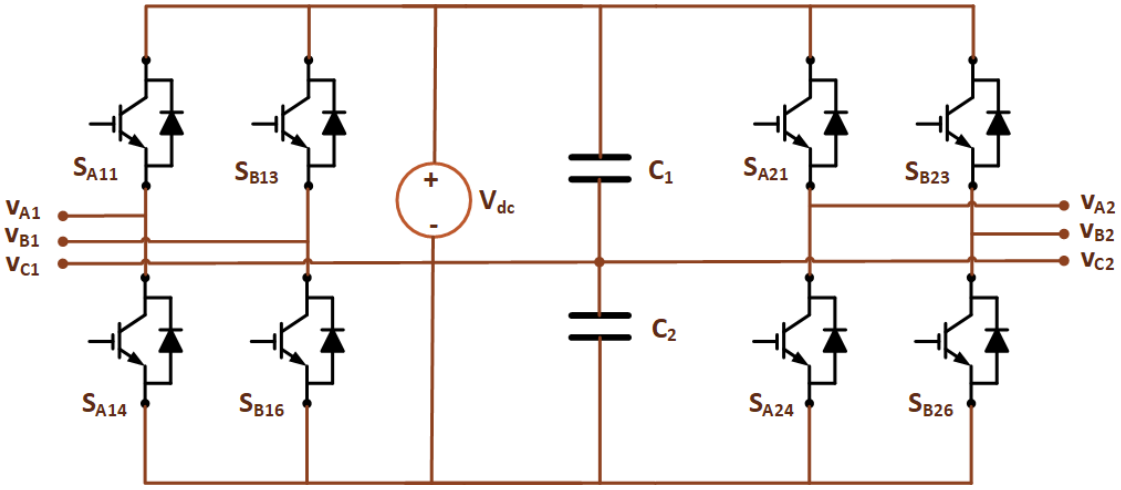


FIGURE 2.4: Four-leg converter.

phase C, thereby decoupling grid and load voltages from DC-link capacitor voltages and eliminating fundamental AC currents through the capacitor Fig. 2.5 [37].

Drawbacks of Shared-Leg DOCs

In comparison to the conventional B2B converter, shared-leg dual-output converters (DOCs) exhibit several drawbacks. Due to the coupling between output terminals, these converters require more complex control algorithms to manage the interactions between outputs, which are no longer fully decoupled. This coupling not only limits the operational flexibility but also results in reduced output power quality compared to the B2B topology. Additionally, shared-leg DOCs are unable to provide the full region of operation that is typically achievable with independently controlled outputs in the B2B configuration.

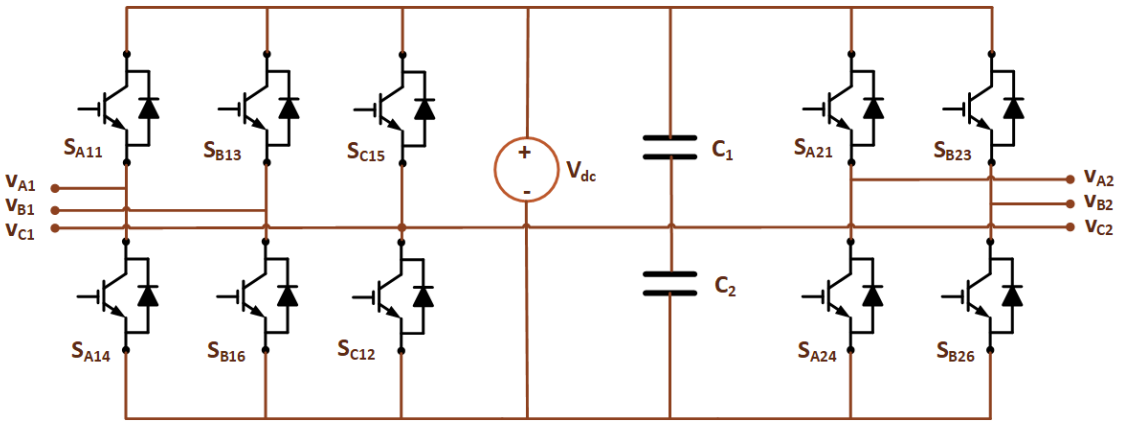


FIGURE 2.5: Five-leg converter.

2.1.3 Nine switch converter

The nine-switch inverter (NSI), introduced in [16, 17] and illustrated in Fig. 2.6, represents a notable dual-output converter topology. In comparison to the conventional back-to-back (B2B) three-phase and five-leg converters. The NSI offers a significant reduction in the number of power semiconductor devices, making it an attractive alternative for dual-load applications. It serves as a potential replacement for traditional B2B and parallel inverter configurations. Apart from its reduced switch count, the NSI also simplifies the gating logic required for switch control. For the operation of an NSI, two reference (modulating) signals are utilized, one for each output. The upper switches are gated by comparing the upper reference signal with a carrier waveform, while the lower switches by using the lower reference signal. The middle switch in each phase leg functions to transfer the output voltage from the upper terminal to the lower terminal, or vice versa. To prevent short circuit of the DC source, the gating signal for the middle switch is typically generated using an exclusive disjunction logic operation between the upper and lower gate signals. To avoid short-circuit conditions and continuous operation, the reference signal associated with the upper terminal must always be greater than or equal to that of the lower terminal. Each phase of the NSI is capable of producing two distinct voltage levels at each output terminal, and the maximum voltage stress on each switch is limited to V_{dc}. The switching states of the NSI and their corresponding output voltage levels are summarized in Table 2.1. The v_{x1} and v_{x2} are output voltages w.r.t the negative terminal, where "x" mentioned in the following part is, all x $\in$ {A, B, and C}. The NSI has received considerable attention in the literature, with numerous studies analyzing its performance and exploring its applications [16, 17, 38, 39, 40, 41, 42, 43, 44, 45].

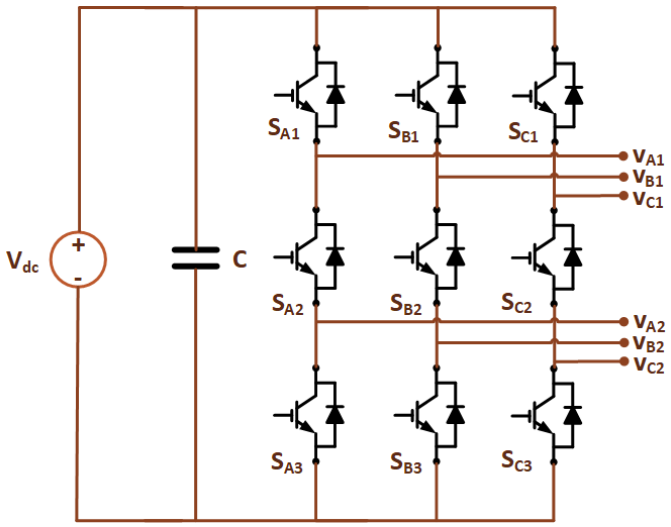


FIGURE 2.6: Nine-switch inverter.

TABLE 2.1: Switching signals and output voltages of the nine-switch inverter.

State No.	**Switching Signals**			**Output Voltages**	
	S_{x1}	S_{x3}	S_{x2} $(S_{x1} \oplus S_{x3})$	$v_{x1}(V_{dc})$	$v_{x2}(V_{dc})$
1	0	1	1	0	0
2	1	0	1	1	1
3	1	1	0	1	0

Drawbacks of the NSI: While the nine-switch inverter (NSI) achieves switch count reduction for dual-output applications, it retains the inherent limitations of conventional two-level converter topologies. Additionally, due to the series connection of the two output terminals, the outputs are no longer fully independent. This interdependence restricts the operational flexibility and narrows the achievable region of operation of output voltage combinations, thereby limiting the converter's overall functionality.

2.1.4 Advancements in the Nine-Switch Inverter Design

Numerous modifications have been proposed to enhance the performance of the Nine-Switch Inverter (NSI). One such enhancement involves integrating a Z-source inverter between the DC-link and the NSI, along with neutral-point clamping diodes, as illustrated in Fig. 2.7 [46]. This configuration enables voltage boosting capabilities, thereby overcoming the traditional NSI's limited input voltage range. In another approach, three switches from the standard nine-switch configuration are eliminated by connecting the load to the DC-link midpoints, resulting in a reduced six-switch topology, as shown in Fig. 2.8 [47]. This architecture not only simplifies the hardware but can also be effectively applied in

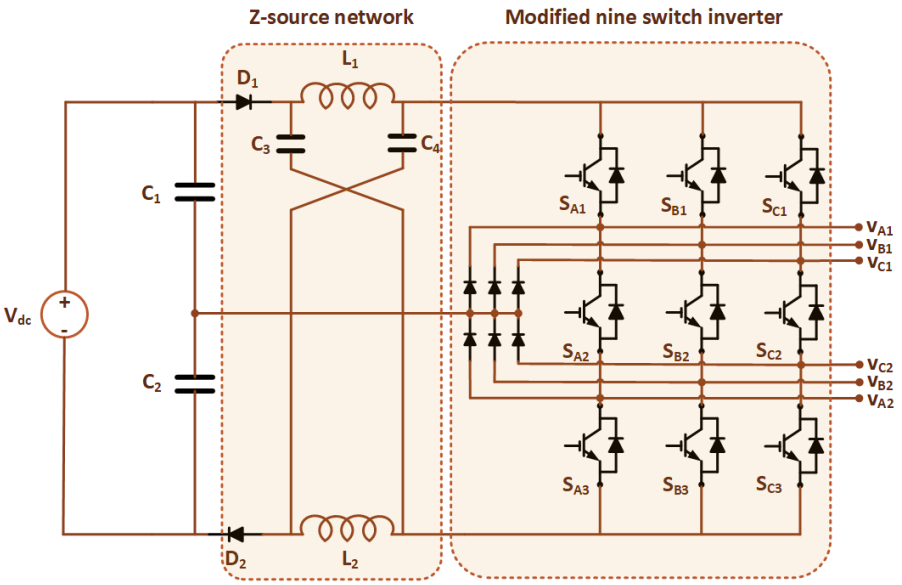


FIGURE 2.7: Z-source modified NSI.

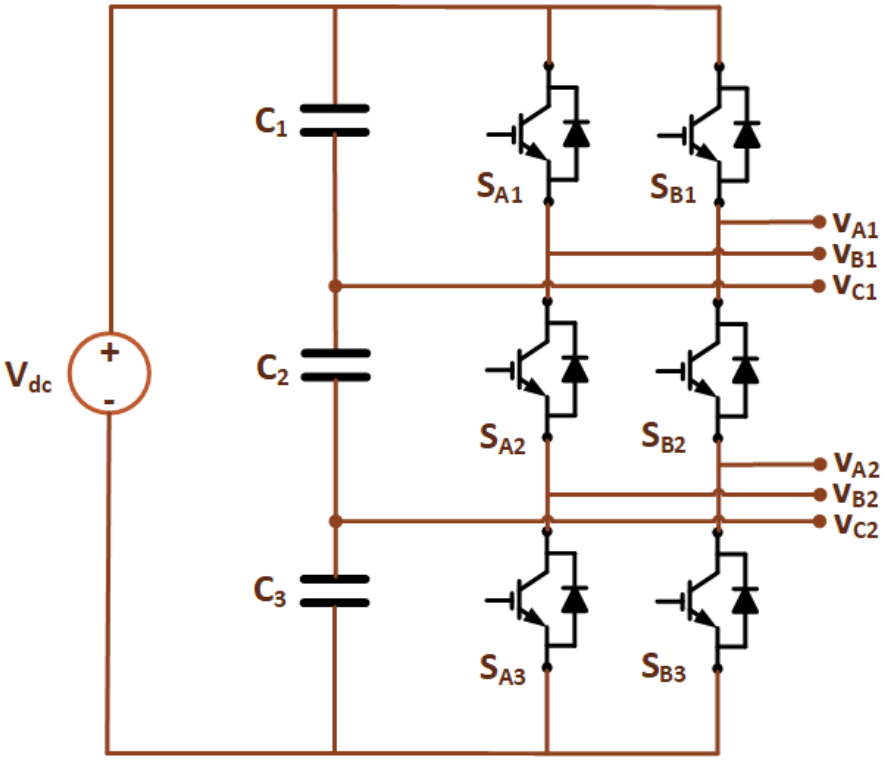


FIGURE 2.8: Six-switch dual-output inverter.

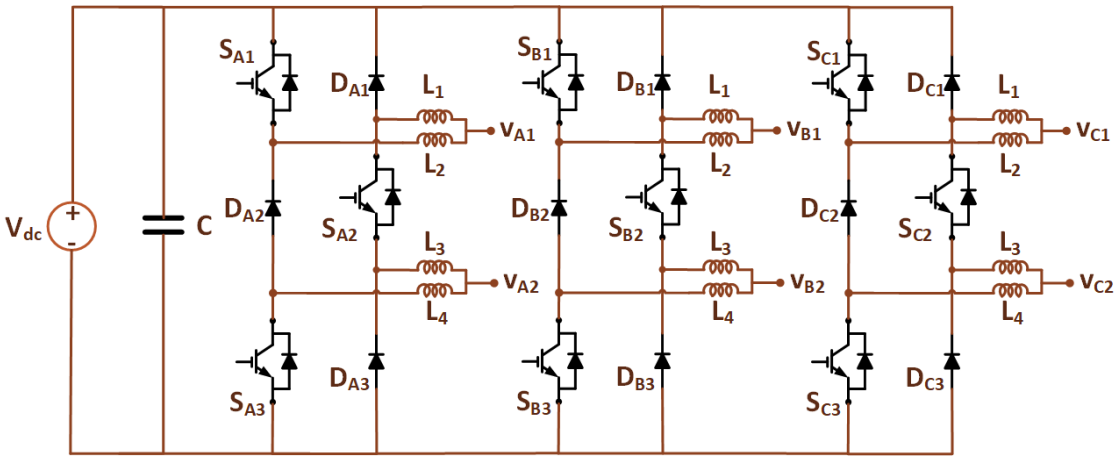


FIGURE 2.9: Three-switch dual-output inverter.

single-phase systems. A further modification introduces a dual-buck structure into the NSI framework, replacing the conventional IGBTs with MOSFETs and diodes, as seen in Fig. 2.9 [48]. This version, termed the three-switch dual-output converter, offers improved reliability and efficiency by reducing switching losses and enhancing thermal performance. While these architectural modifications offer performance gains, they do not fully resolve the inherent limitations of the conventional NSI, particularly with respect to output coupling and limited operational range.

Drawback of Two-level Topologies: Motor failures and damage have been frequently reported due to the high switching frequency PWM used in adjustable-speed drive inverters. The resulting high dv/dt has been identified as the primary cause of two major issues: motor bearing failure and winding insulation breakdown [49].

2.2 Multilevel Dual-output Converter

Multilevel dual-output converters are advanced topologies designed to supply two independent three-phase outputs with improved voltage quality. They offer lower dv/dt and reduced harmonic distortion, minimizing motor insulation stress and bearing failures. By using multiple voltage levels, they also reduce switching losses and enhance efficiency. These converters enable flexible control of dual motors or multiphase machines from a single power stage.

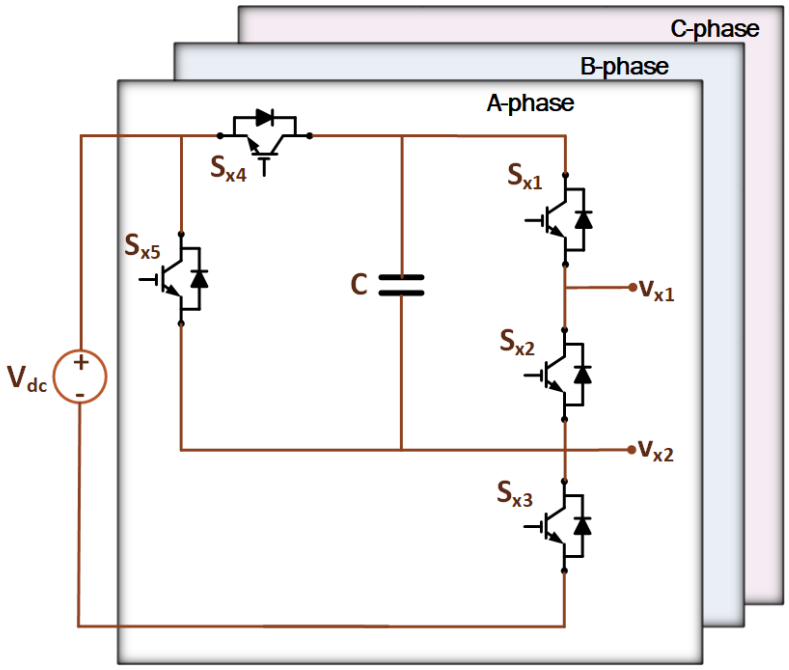


FIGURE 2.10: Three-phase three-port MLI (TPTPMLI).

TABLE 2.2: Switching signals and output voltages of the TPTPMLI.

State	**Switching Signals**					**Output Voltages**	
No.	s_{x1}	s_{x2}	s_{x3}	s_{x4}	s_{x5}	$v_{x1}(V_{\mathrm{dc}})$	$v_{x2}(V_{\mathrm{dc}})$
1	0	1	0	1	0	0	0
2	0	1	1	0	0	0	0
3	1	0	0	0	1	2	1
4	0	1	0	0	1	1	1
5	1	0	1	1	0	1	0

2.2.1 Three-phase Three-port Multilevel Inverter (TPTPMLI)

The three-phase three-port multilevel inverter (TPTPMLI) [50, 51] is a dual-output converter topology derived from the three-level Marx inverter architecture [52]. The three-phase equivalent circuit of the TPTPMLI is illustrated in Fig. 2.10. By incorporating a flying capacitor C that naturally maintains a voltage balance at V_{dc}, the inverter can generate three distinct voltage levels—$2V_{\mathrm{dc}}$, V_{dc}, and 0 at the v_{x1} output terminal. In contrast, the v_{x2} terminal supports only two voltage levels: V_{dc} and 0.

In this configuration, all switching devices experience a maximum voltage stress limited to V_{dc}. The complete set of switching states and corresponding output voltage levels are summarized in Table 2.2.

Drawbacks of the TPTPMLI: Despite its multilevel capabilities, the 3PPMLI exhibits notable limitations. Specifically, it can generate only two voltage levels at its second output terminal, which adversely affects the output power quality. Furthermore, as in the case of the Nine-Switch Inverter (NSI), the series-connected output configuration imposes coupling between the two outputs. This interdependence restricts the operational flexibility of the converter and limits its suitability for applications requiring fully independent outputs.

2.2.2 Three-level Twin Drive Inverter (TL-TDI)

A three-level twin-drive inverter (TL-TDI) for dual permanent magnet synchronous machine (PMSM) loads was introduced in [20], utilizing only 21 switching devices. The topology, illustrated in Fig. 2.11, combines features of both the Nine-Switch Inverter (NSI) and the conventional ANPC converter. Each phase leg comprises seven switches (s_{x1} to s_{x7}), with the output terminals derived from the nodes between s_{x2}, s_{x3}, and s_{x4}, and the neutral point formed between s_{x6} and s_{x7}.

The TL-TDI can produce three voltage levels at each output terminal. However, due to its series-connected output configuration, all voltage combinations are not independently realizable. The maximum voltage stress experienced by each switch remains limited to V_{dc}. A summary of the converter's switching states and corresponding output voltages is provided in Table 2.3.

TABLE 2.3: Switching signal combinations, output voltages, and capacitor currents of the TL-TDI.

State	**Switching Signals**							**Output Voltages**		**Capacitor Currents**	
No.	s_{x1}	s_{x2}	s_{x3}	s_{x4}	s_{x5}	s_{x6}	s_{x7}	$v_{x1}(V_{dc}/2)$	$v_{x2}(V_{dc}/2)$	i_{c1}	i_{c2}
1	1	1	1	0	0	0	0	1	1	$-i_{x1}-i_{x2}$	0
2	0	1	1	0	1	0	0	-1	-1	0	$i_{x1}+i_{x2}$
3	1	0	0	1	0	0	1	1	-1	$-i_{x1}$	i_{x2}
4	1	1	0	1	0	0	1	1	0	$-i_{x1}$	0
5	0	1	0	1	1	0	0	0	-1	0	i_{x2}
6	0	1	0	1	0	1	1	0	0	0	0

Drawbacks of the TL-TDI:

The TL-TDI is limited by its series-connected output terminal configuration, which restricts the achievable operating region. Furthermore, the use of seven power switches per phase results in a relatively high device count, increasing complexity and cost. In addition, this converter experiences significant conduction loss due to its longer conduction path in various switching states.

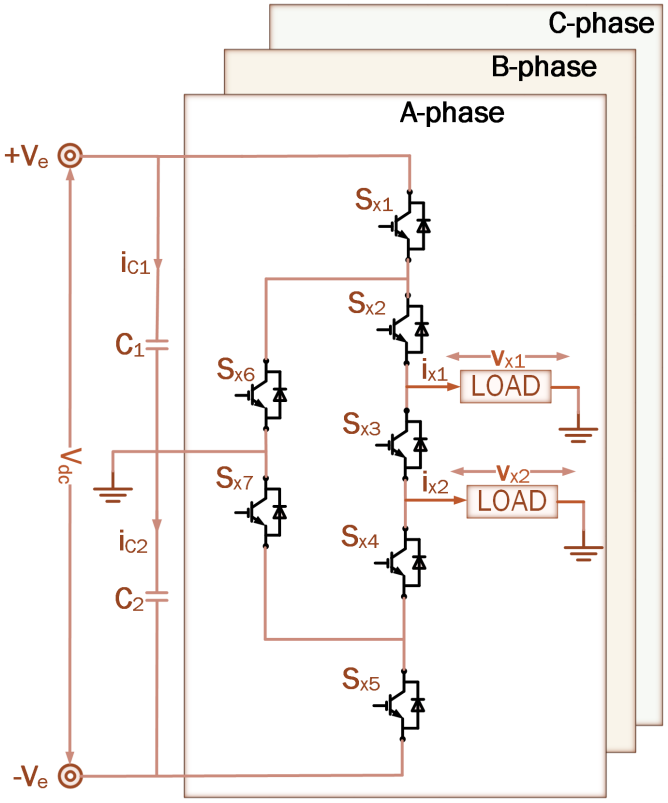


FIGURE 2.11: Three-level twin drive inverter (TL-TDI).

2.2.3 Neutral Point Piloted (NPP)

In [21], the conventional NSI was restructured into a T-type or neutral point piloted (NPP) topology, incorporating a novel loss-reduction strategy. The schematic of the NPP converter is shown in Fig. 2.12. Compared to the traditional neutral point clamped (NPC) multilevel inverter, which utilizes 24 switches and 12 clamping diodes [53, 54], the proposed NPP configuration significantly reduces the component count to just 21 switches.

The NPP converter employs three unidirectional switches (S_{x1}, S_{x2}, S_{x3}) and two bidirectional switches (S_{x4}, S_{x5}). Specifically, switch S_{x1} connects the upper output to the positive DC bus, while S_{x3} connects the lower output to the negative DC bus. Switch S_{x2} forms a bridge between the upper and lower outputs. The bidirectional switches S_{x4} and S_{x5} interface the upper and lower outputs with the neutral point, respectively. These bidirectional devices can actively block voltage and current in both directions [55]. This converter can generate three voltage levels -V_{dc}/2, 0, +V_{dc}/2 on both output terminals with respect to the neutral point. The valid switching combinations, corresponding output voltages, and capacitor currents are detailed in Table 2.4. Notably, switching states 1,

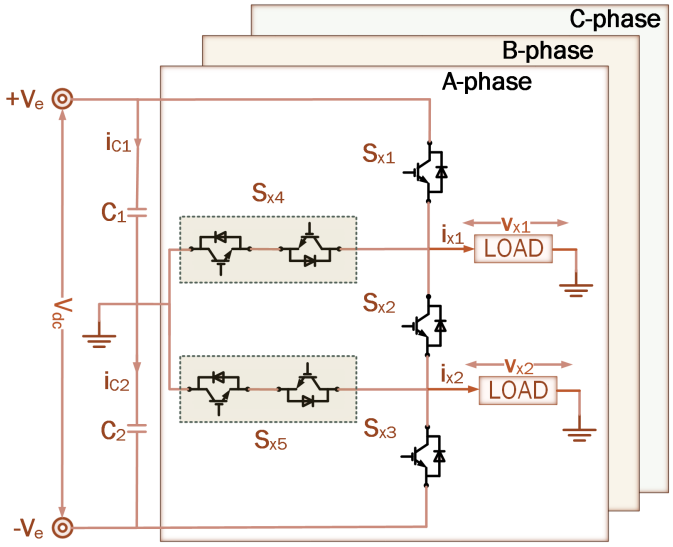


FIGURE 2.12: Neutral point piloted (NPP).

3, 4, and 5 are redundant for producing a zero-voltage output. These redundancies evenly distribute voltage stress across switches S_{x2}, S_{x4}, and S_{x5}. The available redundant states are used to lower the average switching frequency, reduce dynamic power losses, and balance the DC-link capacitors. Redundant switching states provide alternative pathways for current flow, which is critical in the event of a fault. By having multiple valid states for the same output voltage level, the converter can continue to operate even if certain switches or paths fail. The maximum voltage stress on the converter's switches is V_{dc}. Later, in [22], this converter's independent control of output voltages was accomplished using finite control set model predictive control (FCS-MPC).

TABLE 2.4: Switching signals, output voltages, and capacitor currents of the NPP converter.

State	**Switching Signals**					**Output Voltages**		**Capacitor Currents**	
No.	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	$v_{x1}(V_{dc}/2)$	$v_{x2}(V_{dc}/2)$	i_{c1}	i_{c2}
1	0	0	0	1	1	0	0	0	0
2	0	0	1	1	0	0	-1	0	i_{x2}
3	0	1	0	0	1	0	0	0	$-i_{x2}$
4	0	1	0	1	0	0	0	0	0
5	0	1	0	1	1	0	0	0	0
6	0	1	1	0	0	-1	-1	0	$i_{x1}+i_{x2}$
7	1	0	0	0	1	1	0	$-i_{x1}$	0
8	1	0	1	0	0	1	-1	$-i_{x1}$	i_{x2}
9	1	1	0	0	0	1	1	$-i_{x1}-i_{x2}$	0

Drawbacks of the NPP:

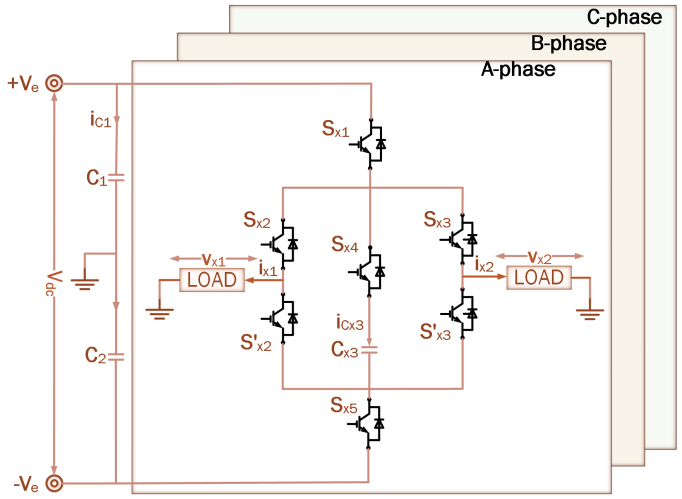


FIGURE 2.13: Three phase schematics of dual-output flying capacitor inverter (DO-FCI).

Although this topology offers several advantages, it also presents notable drawbacks. These include low DC-link voltage utilization, limited operating region, requirement for higher-rated devices, and seven switches per phase thus increasing the overall component count. Additionally, its dependence on two bidirectional switches makes practical implementation more complex and less favorable compared to other dual-output converter topologies.

2.2.4 Dual-Output Flying Capacitor Inverter (DO-FCI)

The parallel output dual-output topology with flying capacitor (FC) is illustrated in Fig. 2.13 [56]. Each single-phase leg comprises three parallel switch branches: two output half-bridge branches (formed by switches S_{x2}, S_{x3}, and another S_{x2}) and a third branch incorporating a switched flying capacitor (S_{x4}, C_{x3}). These branches are connected to the positive and negative terminals of the DC bus through switches S_{x1} and S_{x5}, respectively. Consequently, each phase of the DO-FCI includes seven switching devices and one flying capacitor.

A distinctive feature of this topology is its parallel output terminal configuration, which effectively addresses the operational limitations commonly encountered in series-output dual-output converters. Each output terminal of the DO-FCI can generate three voltage levels $V_{dc}/2$, 0, and $-V_{dc}/2$ provided the flying capacitor is maintained at $V_{dc}/2$ voltage. The maximum voltage stress on any switch within the topology is limited to V_{dc}. Additionally, two of the seven switches can be operated in a complementary fashion to optimize

switching. The valid switching states, along with the corresponding output voltages and flying capacitor currents, are summarized in Table 2.5.

TABLE 2.5: Switching signals, output voltages, and capacitor charging state of the DO-FCI

State	**Switching Signals**					**Output Voltages**		**FC Current**
No.	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x6}	$v_{x1}(V_{dc}/2)$	$v_{x2}(V_{dc}/2)$	C_{x3}
1	0	0	0	0	1	-1	-1	-
2	0	0	1	1	1	-1	0	i_{x2}
3	0	1	0	1	1	0	-1	i_{x1}
4	0	1	1	1	1	0	0	$i_{x1} + i_{x2}$
5	1	0	0	1	0	0	0	$-i_{x1} - i_{x2}$
6	1	0	1	1	0	0	1	$-i_{x1}$
7	1	1	0	1	0	1	0	$-i_{x2}$
8	1	1	1	0	0	1	1	-
9	1	0	1	0	1	-1	1	-
10	1	1	0	0	1	1	-1	-

Drawbacks of the DO-FCI:

The main drawback of the DO-FCI lies in its high component count, which includes both passive and active elements.

2.2.5 Reduced Switch Count Dual-Output T-type (RSC-DT) converter

To further reduce the switch count of NPP, a reduced switch count dual-output T-Type (RSC-DT) multilevel converter is introduced in [23] as shown in Fig. 2.14. This converter requires one less switch for three-level output voltages than NPP [21] at the cost of reduced redundant switching states.

The RSC-DT converter utilizes a T-type configuration and a multilevel modulation strategy (PD-PWM) along with a minimum energy cost function to control its operation. This approach balances the capacitor voltage and avoids additional stress on the converter components. The converter successfully maintains desirable multilevel output waveform quality while reducing both its power electronic components and associated control algorithm complexity.

The RSC-DT converter is further explored in [24] with the sine pulse width modulation (SPWM) technique with DC offset and renamed as a dual-output T-type three-level converter (DO-T-TLC). A simple SPWM technique is used for capacitor voltage balancing.

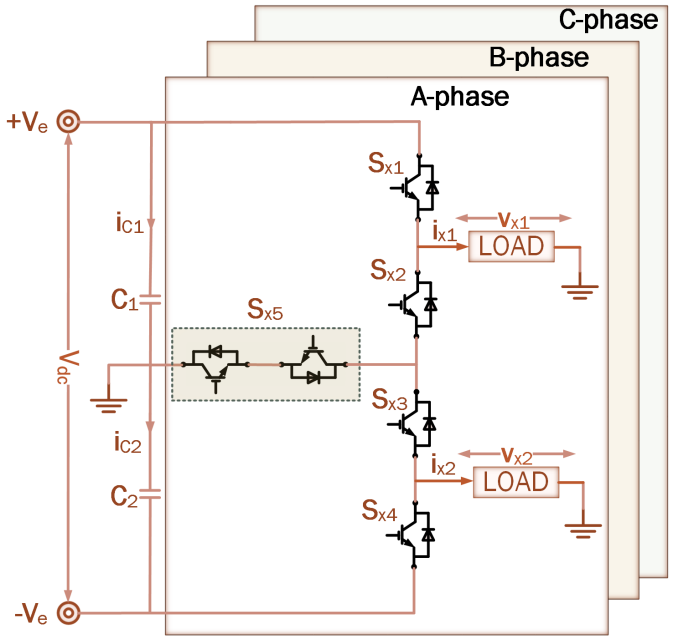


FIGURE 2.14: Three phase schematics of reduced switch count dual-output T-type (RSC-DT) converter.

The RSC-DT converter employs four unidirectional switches (S_{x1}, S_{x2}, S_{x3}, S_{x4}) and one bidirectional switche (S_{x5}). Specifically, switch S_{x1} connects the upper output to the positive DC bus, while S_{x4} connects the lower output to the negative DC bus. Switches S_{x2} and S_{x3} forms a bridge between the upper and lower outputs. The bidirectional switches S_{x5} interface the upper and lower outputs with the neutral point, through S_{x2} and S_{x3}. These bidirectional devices can actively block voltage and current in both directions. This converter can generate three voltage levels -V_{dc}/2, 0, +V_{dc}/2 on both output terminals with respect to the neutral point. The possible switching combinations for the RSC-DT converter, along with their corresponding output voltage levels and capacitor charging or discharging states, are presented in Table 2.6.

TABLE 2.6: Switching signals, output voltages, and capacitors charging state of the single-phase RSC-DT converter

State	**Switching Signals**					**Output Voltages**		C_1 **Charging State**		C_1 **Charging State**	
No.	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	$v_{x1}(V_{dc})$	$v_{x2}(V_{dc})$	$i_{x1} > 0$	$i_{x2} > 0$	$i_{x1} > 0$	$i_{x2} > 0$
1	1	1	1	0	0	1/2	1/2	↓	↓	-	-
2	0	1	1	1	0	-1/2	-1/2	-	-	↑	↑
3	1	0	0	1	0	1/2	-1/2	↓	-	-	↑
4	0	1	1	0	1	0	0	-	-	-	-
5	0	1	0	1	1	0	-1/2	-	-	-	↑
6	1	0	1	0	1	1/2	0	↓	-	-	-

↑ is for charging, ↓ is for discharging state and - for no change

The converter offers a total of six unique valid switching states; therefore, dc-link capacitor voltage balancing can be effectively achieved only under three-phase operation. For instance, in a three-phase configuration, there are a total of $6^3 = 216$ switching combinations. However, after transforming the phase voltages to line-to-line voltages, only 163 states remain unique. This redundancy can be leveraged to control the direction of current flow in the dc-link capacitors and aid in their voltage balance. The maximum voltage stress on the converter's switches is V_{dc}.

Drawbacks of the RSC-DT:

While this topology offers several advantages, it also presents some noteworthy drawbacks. Similar to the NPP converter, its reliance on a bidirectional switch increases implementation complexity and makes it less favorable in comparison to other dual-output converter topologies. Furthermore, this converter provides no redundant states under single-phase operation and offers a limited number of redundant states during three-phase operation, in contrast to the NPP converter.

2.2.6 Dual-Output Neutral-Point-Clamped Three-Level Inverter (DO-NPC-TLI)

An NPC-based dual-output three-level inverter (DO-NPC-TLI) with twenty switches and twelve diodes has been presented in [25]. The schematics of three phase DO-NPC-TLI is shown in Fig. 2.15. Each converter phase comprises six switches (S_{x1}–S_{x6}) and four clamping diodes (D_{x1}–D_{x4}). Additionally, two auxiliary switches (S_{o1} and S_{o2}) connect all phases to the neutral point through the clamping diodes. In contrast to other DOC topologies, the DO-NPC-TLI is divided into two converters that are alternatively controlled within a single sampling period. Converter 1 consists of S_{x1}, S_{x2}, S_{x3}, S_{x4}, D_{x1}, D_{x2}, and S_{o1}, while converter 2 comprises S_{x3}, S_{x4}, S_{x5}, S_{x6}, D_{x3}, D_{x4}, and S_{o2}. Each output terminal is capable of generating three voltage levels, namely $V_{dc}/2$, 0, and $-V_{dc}/2$, with a maximum voltage stress of $V_{dc}/2$ across each converter's switches. The respective switching tables for the two converters are presented in Table 2.7.

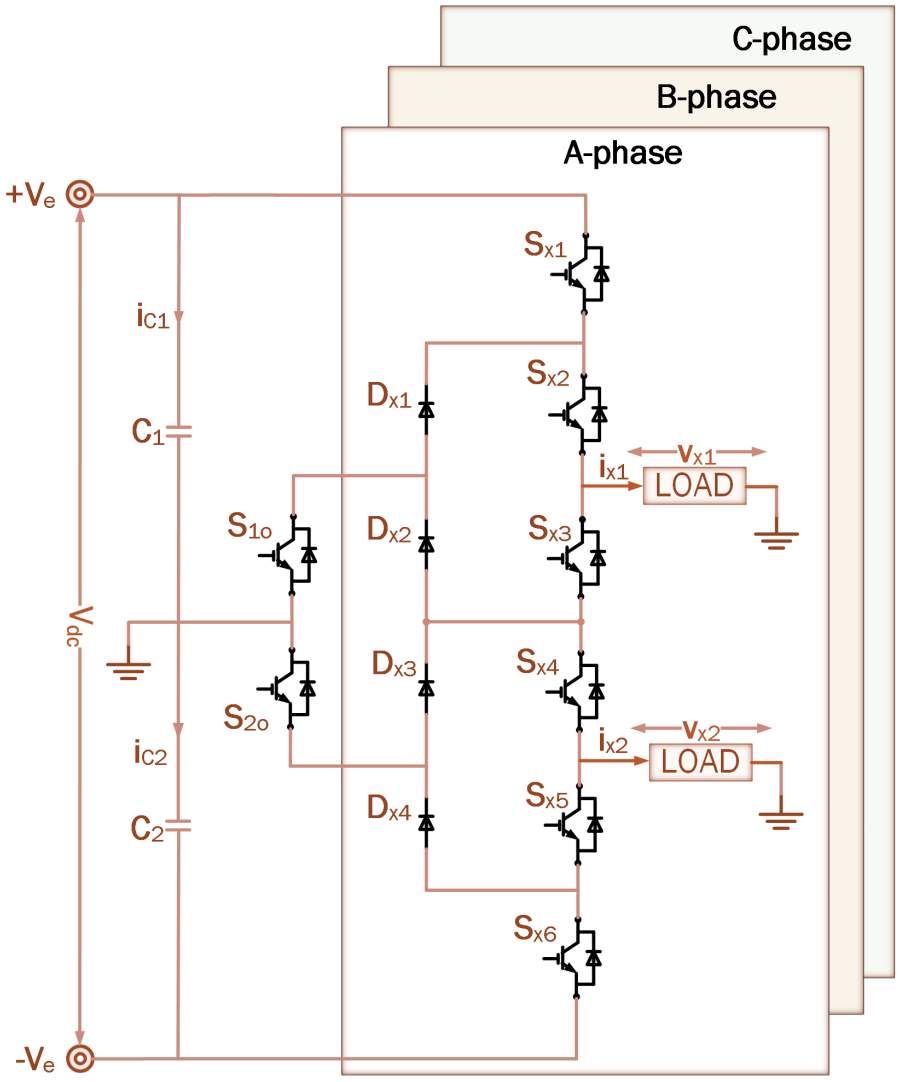


FIGURE 2.15: Three phase schematics of dual-output neutral-point-clamped three-level inverter (DO-NPC-TLI).

TABLE 2.7: Switching signals, output voltages, and capacitor currents of the DO-NPC-TLI

State	**Effective**	**Switching Signals**								**Output Voltages**		**Capacitor Currents**	
No.	**Converter**	S_{o1}	S_{o2}	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	$v_{x1}(V_{dc}/2)$	$v_{x2}(V_{dc}/2)$	i_{c1}	i_{c2}
1	Converter 1	1	0	1	1	0	0	1	1	1	0	$-i_{x1}$	0
2		1	0	0	1	0	0	1	1	0	0	0	0
3		1	0	0	0	1	1	1	1	-1	0	0	i_{x1}
4	Converter 2	0	1	1	1	0	1	1	0	0	1	$-i_{x2}$	0
5		0	1	1	1	1	1	1	0	0	0	0	0
6		0	1	1	1	0	0	1	1	0	-1	0	i_{x2}

Drawbacks of the DO-NPC-TLI:

The main drawback of the DO-NPC-TLI lies in the complexity of its control, which makes the implementation of conventional pulse-width modulation strategies challenging. Additionally, the converter utilizes a large number of components, employing a total of 32 active switches in its three-phase configuration. Furthermore, its series output configuration inherently restricts its range of operation. While the DO-NPC-TLI maintains the desirable feature that all diodes and switches are rated for only 50% of the DC-link voltage, its maximum modulation index for each output is limited to 0.5, regardless of whether it operates in the common-frequency (CF) or different-frequency (DF) mode. Consequently, this limitation necessitates doubling the DC-link voltage, thereby increasing the input supply cost.

2.2.7 Neutral Point Clamped Dual Output (NPC-DO) Converter

The neutral-point clamped dual-output (NPC-DO) converter [26] is a parallel-output converter, as illustrated in Fig. 2.16. Each converter leg comprises six semiconductor switches and two diodes. The topology is analogous to the conventional single-output NPC converter but includes two additional switches per phase. This modification enables the converter to provide a second output port with maximum DC-bus utilization, without imposing operational limitations on the first output. Furthermore, as each phase operates independently, the converter can be easily extended to accommodate a greater number of phases.

The single-legged NPC-DO converter comprises six switches (S_{x1}, S_{x2}, S_{x3}, S_{x4}, S_{x5}, S_{x6}) and two diodes (D_{x1}, D_{x2}). The switches S_{x1} and S_{x2} are shared by both outputs and are complementary to each other. Specifically, S_{x1} connects the positive DC bus to the first and second outputs through S_{x3} and S_{x5}, respectively, while S_{x2} connects the negative DC bus to the first and second outputs through S_{x4} and S_{x6}, respectively. The diodes D_{x1} and D_{x2} link the neutral point to the first and second outputs. This converter is capable of generating three output voltage levels $-V_{dc}/2$, 0, and $+V_{dc}/2$ with respect to the neutral point.

The respective switching states, output voltages, and capacitor charging and discharging conditions are summarized in Table 2.8. In comparison to the DO-FCI converter [56], the NPC-DO realizes only five out of the nine possible output voltage combinations. This reduction in available states comes at the expense of output voltage quality. However, this can be mitigated by increasing the controller's sampling frequency.

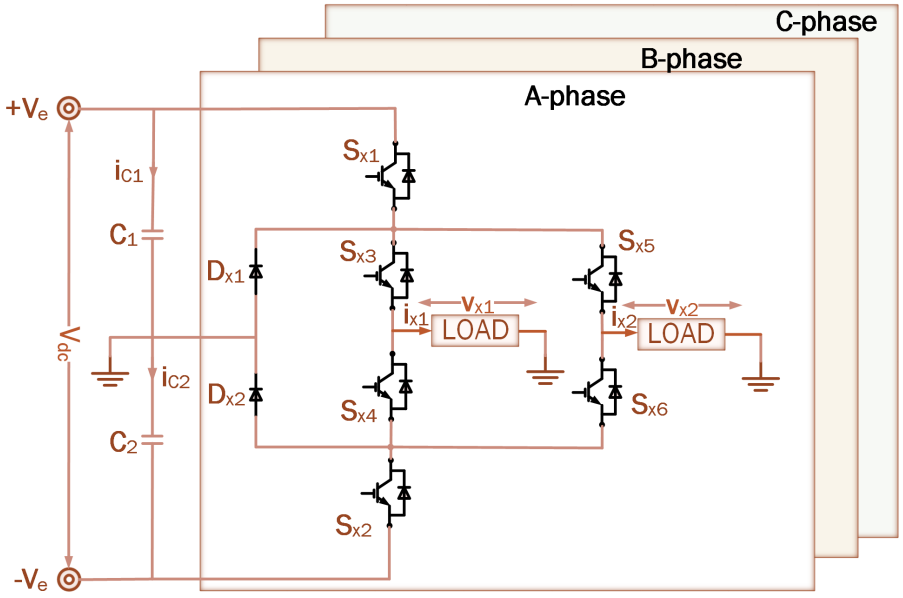


FIGURE 2.16: Three phase schematics of neutral-point clamped dual-output (NPC-DO) converter.

TABLE 2.8: Switching signals, output voltages, and capacitor charging state of the NPC-DO

State No.	Switching Signals						Output Voltages		Capacitor Currents	
	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	$v_{x1}(V_{dc}/2)$	$v_{x2}(V_{dc}/2)$	i_{c1}	i_{c2}
1	1	0	1	0	1	0	1	1	$-i_{x1}-i_{x2}$	-
2	0	1	0	1	0	1	-1	-1	-	$i_{x1}+i_{x2}$
3	1	1	1	0	0	1	1	-1	$-i_{x1}$	i_{x2}
4	1	1	0	1	1	0	-1	1	$-i_{x2}$	i_{x1}
5	0	0	1	1	1	1	0	0	-	-

Drawbacks of the NPC-DO:

The reduction in available states comes at the expense of output voltage quality. The NPC-DO converter offers an improved operational range in comparison to the previously discussed three-level dual-output converters. However, some output voltage states remain unavailable, thereby preventing the converter from fully utilizing its entire range of operation.

2.2.8 Cascaded Multi-output Multilevel (CMOM) Converter

In [27], a cascaded multi-output multilevel (CMOM) converter was implemented by cascading two legs of the NSI. This configuration resulted in a reduced number of power

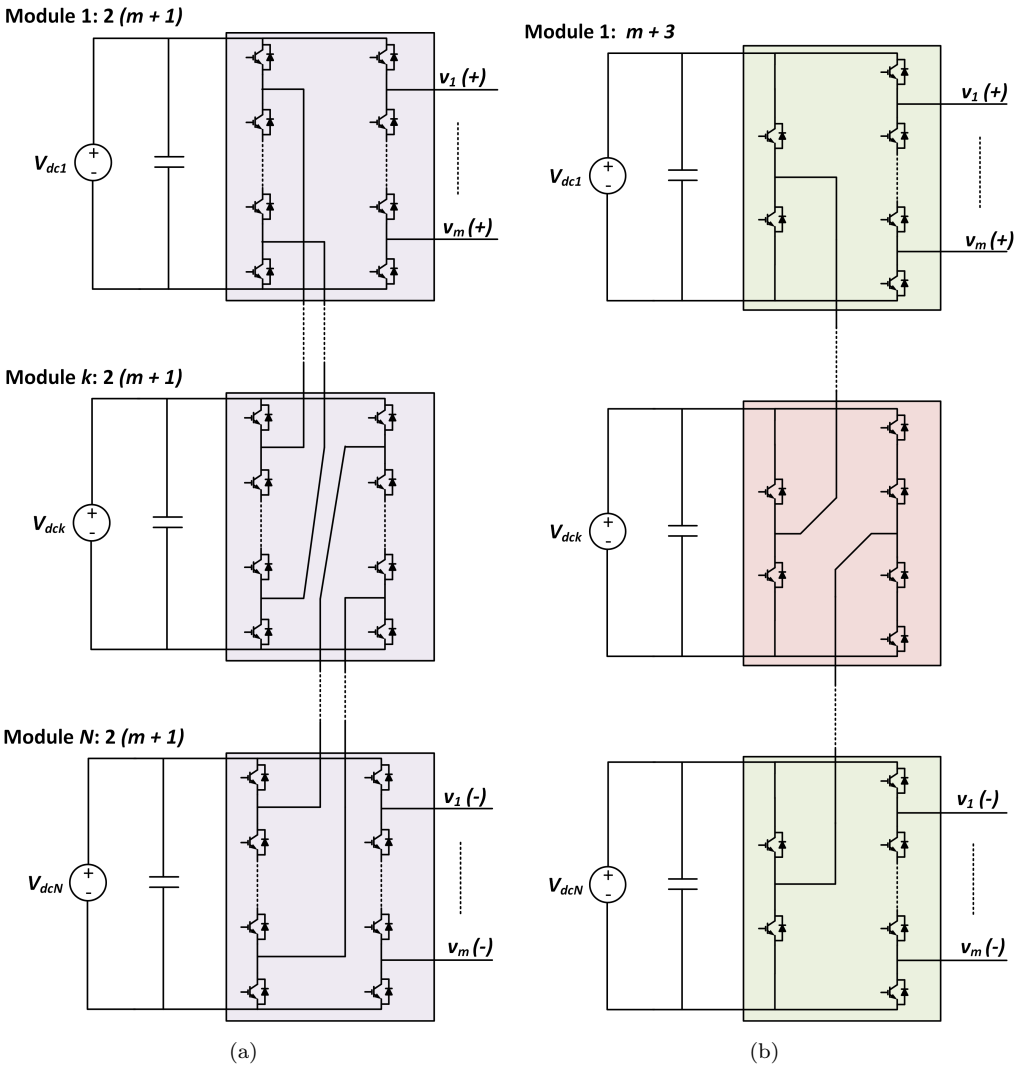


FIGURE 2.17: Generalized multi-input multi-output circuit diagram of (a) the CMOM converter and (b) the M-CMOM converters.

electronic switches while retaining the same number of output voltage levels as the NPP-based converter. Subsequently, in [57, 28], the CMOM converter was further optimized by reducing its switch count, and a phase disposition pulse width modulation (PD-PWM) strategy was introduced to maximize its performance. Specifically, for the case of dual-output operation, the converter is controlled using an optimal state and level-detection PD-PWM algorithm with the objective of minimizing its switching frequency. Furthermore, the converter's operating limits were investigated and subsequently verified through simulation and/or experimental results.

The generalized structures of the CMOM and its variant modified cascaded multi-output multilevel (M-CMOM) converters are illustrated in Fig. 2.17.

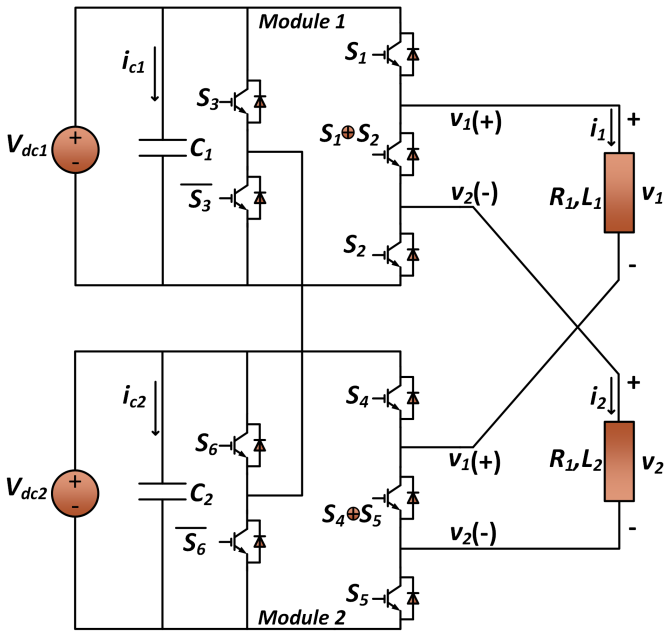


FIGURE 2.18: Circuit diagram of the M-CMOM converter (m = 2 and n = 5).

These converter topologies are composed of N modules ($N = 2, 3, \ldots$) and provide m output ports ($m = 2, 3, \ldots$). Assuming that all input sources are equal in voltage, the number of output voltage levels n can be determined by $n = 2N + 1$. The total number of switches in each converter (X_{sw}) is calculated according to,

$$\text{CMOM} : X_{sw} = (m + 1)(n - 1) \tag{2.1}$$

$$\text{Modified CMOM} : X_{sw} = 2(m + n - 2) \tag{2.2}$$

It can be observed that as the number of voltage levels increases, the number of power switches in the M-CMOM converter decreases exponentially, thereby yielding a significant reduction in converter complexity. It is worth noting that for $m = 1$, the CMOM converter reduces to a single-output cascaded H-bridge (CHB) converter. Thus, the M-CMOM converter can be regarded as a generalized form of the CHB converter. Furthermore, when $m = 2$, the M-CMOM converter realizes a cascaded dual-output multilevel converter, as illustrated in Fig. 2.18; this configuration is named as the modified cascaded dual-output multilevel (M-CDOM) converter.

The M-CDOM converter consists of two identical modules, each fed by its own independent power supply. Each module comprises five power switches, which are controlled by

a set of three switching signals, effectively representing control over three independent power switches. This configuration reduces the total number of switches from twelve, as implemented in the original CDOM converter [27], down to ten.

The connection between switches $(S_{A3}, \bar{S}_{A3})$ and $(S_{A6}, \bar{S}_{A6})$ enable the converter to produce the following combinations of input voltages: $-2V_{dc}$, $-V_{dc}$, 0, V_{dc}, and $2V_{dc}$. The two AC loads are connected across nodes $\{v_{A1}(+), v_{A1}(-)\}$ and $\{v_{A2}(+), v_{A2}(-)\}$ for loads 1 and 2, respectively.

Table 2.9 shows the possible switching combinations for the converter. A total of 36 valid states are available for control, which are formed by combining two states from each two-switch leg and additional states from the two respective three-switch legs ($2\times2\times3\times3 = 36$). For simplicity, the switching states are presented in decimal format. Each state can be directly converted back into its corresponding binary representation. For instance, state $(18)_{10}$ converts to $(010010)_2$ where each bit corresponds to a particular power switch (S_{A1}, S_{A2}, S_{A3}, S_{A4}, S_{A5}, and S_{A6}). This redundancy in the states can be utilized to minimize the average switching frequency of the converter's power devices.

TABLE 2.9: Modified CDOM converter switching states and corresponding output voltage levels and capacitor currents

State No.	**Switching Signals**	**Output Voltages (V_{dc})**		**Capacitor Currents**		**Count**
		v_{A1}	v_{A2}	i_{C1}	i_{C2}	
1	28	-2	-2	$\uparrow_{1+2}$	$\uparrow_{1+2}$	1
2	60	-1	-2	$\uparrow_{2}$	$\uparrow_{1+2}$	1
3	30	-2	-1	$\uparrow_{1+2}$	$\uparrow_{1}$	1
4	20, 29, 26, 44, 62	-1	-1	0, $\uparrow_{1+2}$, $\uparrow_{1+2}$, 0, $\uparrow$ 2	$\uparrow_{1+2}$, 0, 0, $\uparrow_{1+2}$, $\uparrow_{1}$	5
5	52, 61, 58	0	-1	$\downarrow_{1}$, $\uparrow_{2}$, $\uparrow_{2}$	$\uparrow_{1+2}$, 0, 0	3
6	22, 31, 46	-1	0	0, $\uparrow_{1+2}$, 0	$\uparrow_{1}$, $\downarrow_{2}$, $\uparrow_{1}$	3
7	54, 18, 36, 27, 45, 63, 21, 42	0	0	$\downarrow_{1}$, 0, $\downarrow_{1+2}$, $\uparrow_{1+2}$, 0, $\uparrow_{2}$, 0, 0	$\uparrow_{1}$, 0, $\uparrow_{1+2}$, $\downarrow_{1+2}$, 0, $\downarrow_{2}$, 0, 0	8
8	50, 59, 53	1	0	$\downarrow_{1}$, $\uparrow_{2}$, $\downarrow_{1}$	0, $\downarrow_{1+2}$, 0	3
9	38, 47, 23	0	1	$\downarrow_{1+2}$, 0, 0	$\uparrow_{1}$, $\downarrow_{2}$, $\downarrow_{2}$	3
10	34, 43, 19, 37, 55	1	1	$\downarrow_{1+2}$, 0, 0, $\downarrow_{1+2}$, $\downarrow_{1}$	0, $\downarrow_{1+2}$, $\downarrow_{1+2}$, 0, $\downarrow_{2}$	5
11	51	2	1	$\downarrow_{1}$	$\downarrow_{1+2}$	1
12	39	1	2	$\downarrow_{1+2}$	$\downarrow_{2}$	1
13	35	2	2	$\downarrow_{1+2}$	$\downarrow_{1+2}$	1
Total						36

$\uparrow$ 1+2: $i_{A1} + i_{A2}$, $\downarrow$ 1+2: -($i_{A1} + i_{A2}$), $\uparrow$ 1: i_{A1}, $\downarrow$ 1: -i_{A1}, $\uparrow$ 2: i_{A2}, $\downarrow$ 2: -i_{A2}

Drawbacks of the CMOM and M-CMOM:

The CMOM and modified CMOM converters do not provide full-region operation, are subject to modulation index-related restrictions, and require multiple DC power supplies for their operation.

2.3 Operation Limits of Dual-output Converters

The operational limits of the dual output converter (DOC) require solving inequality constraints that depend on the modulation indices, phase shifts, and frequencies of both outputs, also influenced by the specific converter topology. The modulation constraint establishes an inequality relationship between m_1 (M_{TOP}) and m_2 (M_{BOT}). These constraints define the allowable ranges of modulation magnitude and relative phase shift, as presented in the following equations:

Common frequency mode:

$$M_{Bot} \leq 1 \leq M_{Top} + \frac{2 - 2M_{Top}}{1 + sin(wt)} \tag{2.3}$$

Common frequency mode with phase-shift:

$$M_{Bot} = M_{Top} \leq \frac{2}{2 - 2cos(wt + \frac{\theta}{2})sin(\frac{\theta}{2})} \tag{2.4}$$

Different frequency mode:

$$M_{Bot} + M_{Top} \leq 1 \tag{2.5}$$

Furthermore, these inequalities need to be adapted for either single-phase or three-phase operation [58]. This process can become increasingly challenging and time-consuming as the number of voltage levels and the converter's complexity grow. To simplify this analysis, the operational limits of the converter are often represented graphically, enabling a clear visualization of the feasible modulation region. This approach allows the target operating point to be easily projected onto the modulation boundary, facilitating a quick and intuitive assessment of its validity..

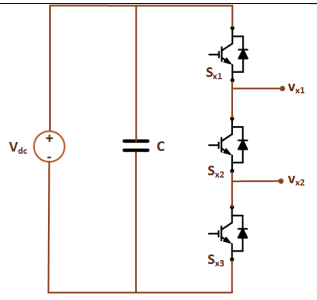
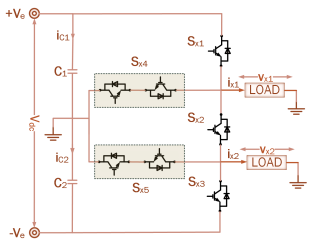
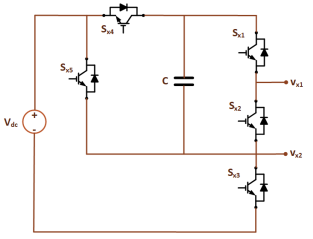
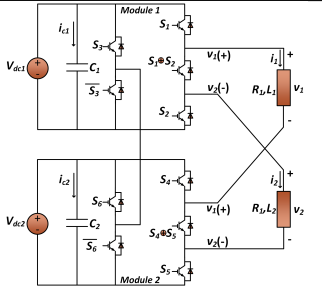
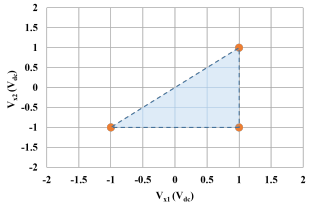
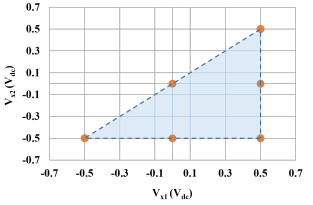
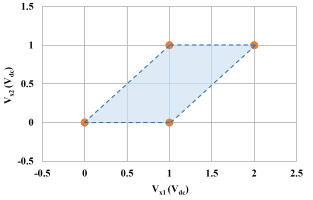
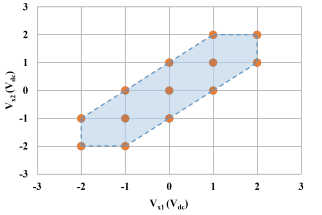
2.3.1 Modulation indices limits

For the generation of a PWM signal, dual-output converters (DOCs) utilize two reference signals to generate the required output voltages. However, if these references fall outside the converter's feasible operating region, the desired voltages cannot be produced. Since the achievable output voltages are inherently restricted by the converter's available switching states, this switching set can be directly analyzed to define the converter's operational boundaries. Consider a DOC with M switching states, represented by $(S_1, S_2, \ldots, S_M)$, and output voltages v_1 and v_2. The data point $(v_1(S_k), v_2(S_k))$ for each state can be plotted on a Cartesian (x–y) plane, where the resulting region enclosed by the group of M points, if any, is defined as the operation region of the DOC. Furthermore, if the voltage reference signals $v_{\mathrm{ref}_1}(t)$ and $v_{\mathrm{ref}_2}(t)$ are bounded by:

$$|v_{\mathrm{ref}_i}(t)| \leq 1 \quad \forall \quad i \in \{1, 2\}$$

the plot's axes should be scaled to match these limits, ensuring that the reference signals can be accurately projected. A representation of different operation regions of a few DOCs such as two-level nine switch inverter (NSI), three-level neutral point piloted (NPP), five-level, modified cascaded multi-output multilevel (CMOM) converter in the literature and their classification is presented in Table 2.10.

TABLE 2.10: Graphical representations of different types of operation regions classified by DOC

Topology	Two level	Three-level		Five-level
Name	NSI [16]	NPP [21]	3PPMLI [50]	Modified CMOM [28]
Single-leg Schematics				
Boundary Region				
Legend	Operating Region	Operating Boundaries	Switching State	

2.3.2 Phase Shift Limits

If a DOC is operated under common frequency mode ($f_1 = f_2$), then, for a certain combination of $v_{\text{ref}_1}(t)$ and $v_{\text{ref}_2}(t)$, there exists a boundary on the maximum possible phase shift (ϕ) between the two references. The maximum phase-shift angle should be within the boundary region for the continuous operation of the converter. This angle can be obtained by evaluating all possible combinations of modulation indices ($\forall m_{1,2} \in [0:1]$) of the reference signals. For each combination, the phase shift is slightly incremented until the references violate the operation boundary, which is either determined by the method in subsection 2.3.1 or until the maximum phase shift of 180° is reached. An example of this process is shown in Fig. 2.19.

2.3.3 Three-phase Operation Limits

By extending the DOC topologies to three-phase operation, the utilization of the input voltage source is increased to a maximum of $2V_{dc}/\sqrt{3}$. To achieve this additional utilization, the reference signals can be modified by various means [58], e.g., min–max zero sequence injection. While the operation boundaries remain fixed, the modified signal will have a different trajectory on the operation space compared to the original one. Hence, the space of valid modulation indices and phase shifts will differ and is empirically found to be larger than the one of the single-phase operation, as expected.

2.3.4 Dual-output converters with No Operating Limits

Using the proposed methodology, DOCs without operational limitations can also be identified. A converter with no such limitations, for instance, a back-to-back converter is one that provides two independent outputs, yielding a square-shaped operational boundary. Such converter are Back, dual conventional three-level ANPC (CTL-ANPC), and dual flying capacitor ANPC (DFC-ANPC) etc. Examples of these converters and their respective operational range representations are illustrated in Table 2.11.

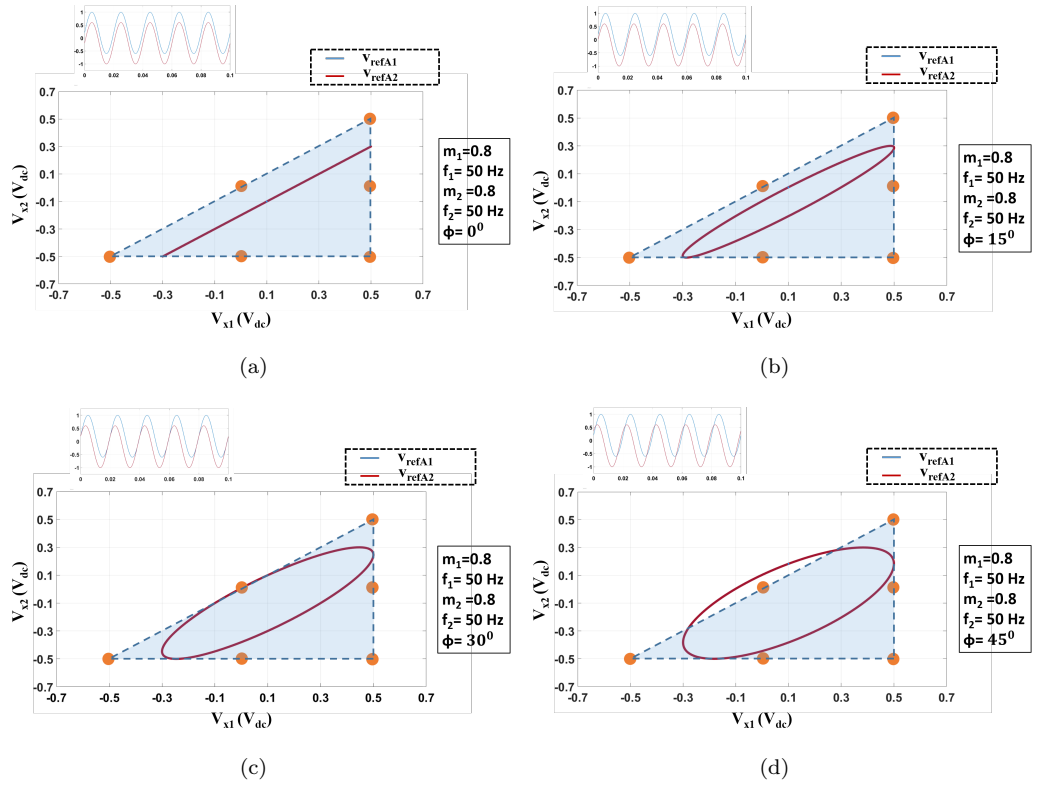
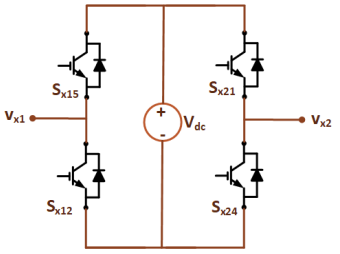
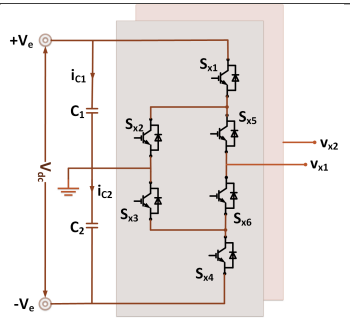
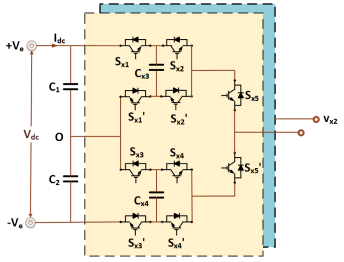
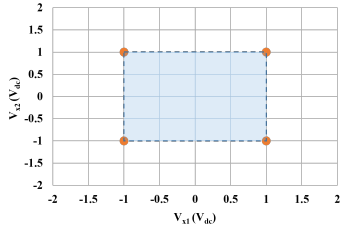
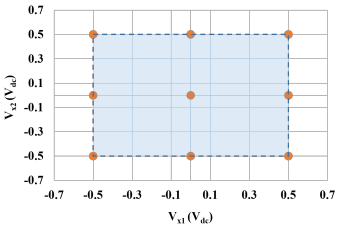
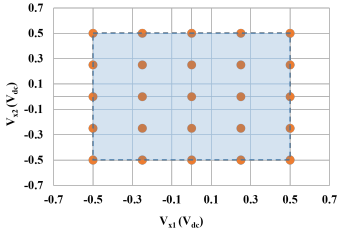


FIGURE 2.19: The evaluation process of the maximum allowable phase shift for the NPP Converter at modulation indices $m_1 = m_2 = 0.8$ reveals that: (a–c) when the phase shift varies from 0° to 30°, both reference signals remain within the permissible operating boundaries; (d) however, beyond 30°, the reference vectors exceed the feasible region, violating the converter's modulation constraints.

TABLE 2.11: Graphical representations of different types of operation regions classified by DOC: Back to Back, dual conventional three-level ANPC (CTL-ANPC), and dual flying capacitor ANPC (DFC-ANPC)

Topology	Two level	Three-level	Five-level
Name	Back to Back [30]	Dual CTL-ANPC [59, 60]	DFC-ANPC [61]
Single-leg Schematics			
Boundary Region			
Legend	Operating Region	Operating Boundaries	Switching State