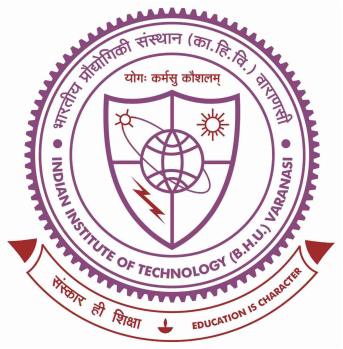
Some Methods for Performance Improvement of Multi-core clusters



Thesis submitted in partial fulfillment

for the Award of Degree

DOCTOR OF PHILOSOPHY

by

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I dedicate this thesis to my beloved family, whose unwavering support and encouragement have been my constant source of strength and motivation throughout this academic journey. Their love and sacrifices have been the cornerstone of my achievements, and I am deeply grateful for their enduring faith in my pursuits. . .

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It is certified that the work contained in this thesis entitled "Some Methods for Performance Improvement of Multi-core clusters" by "Navin Mani Upadhyay" has been carried out under my supervision and that it has not been submitted elsewhere for a degree.

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- Navin Mani Upadhyay

ABSTRACT

This thesis delves into various performance improvement techniques for multi-core clusters, which are critical for advancing High-Performance Computing (HPC). Multi-core clusters are fundamental in supporting complex computational tasks, and optimizing their performance can significantly enhance computational efficiency and system reliability.

The research begins by identifying key challenges in the HPC environment, particularly focusing on memory congestion, resource prediction, and load balancing. It introduces an innovative scheme designed to mitigate memory congestion, thereby improving data throughput in multi-core systems. This scheme employs advanced parallel data mining techniques on public datasets, allowing for the development of predictive models that can forecast CPU performance. These models are instrumental in facilitating more efficient scheduling and resource allocation.

A significant portion of the thesis is dedicated to exploring load balancing mechanisms. It evaluates various algorithms and their effectiveness in heterogeneous cloud environments, offering a comprehensive survey of existing techniques and proposing new methodologies. The proposed solutions are validated through extensive simulations and real-world applications, demonstrating substantial improvements in computational efficiency.

Additionally, the research addresses dependency prediction of long-term resource usage in HPC environments. By employing machine learning techniques, the study develops models that can predict resource usage patterns, thus enabling better resource management and allocation strategies.

The thesis also examines the impact of different scheduling algorithms on system performance. It introduces an effective scheme for memory congestion reduction and

evaluates its performance through detailed experimental analysis. The results indicate a significant reduction in memory congestion, leading to enhanced system performance and reliability.

Moreover, the research explores the integration of advanced load balancing techniques with existing HPC infrastructures. It proposes a hybrid approach that combines multiple algorithms to optimize load distribution across multi-core clusters. This approach is shown to improve overall system performance, reduce processing time, and enhance system scalability.

In conclusion, this thesis makes significant contributions to the field of HPC by providing scalable and adaptive methods for improving the performance of multi-core clusters. The findings pave the way for the development of more robust and efficient computing infrastructures, which are essential for meeting the growing demands of complex computational tasks. These advancements are expected to have a profound impact on the future of HPC, enabling more efficient and reliable computational environments.

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Abbreviations

ALU	**A**rithmetic and **L**ogical **U**nit
AMD	**A**dvanced **M**icro **D**evices
ARE	**A**bsolute **R**oot **M**ean **E**rror
ARRE	**A**ccuracy and **R**elative **R**untime **E**rror
BFS	**B**est **F**irst **S**earch
BN	**B**ayesian **A**pproach
CACH	**C**ache **M**emory (in KBs)
CG	**C**onjugate **G**radient Kernel
CHMAX	**M**aximum **C**hannels (in Groups)
CHMIN	**M**inimum **C**hannels (in Units)
CPU	**C**entral **P**rocessing **U**nit
DIV	**D**ivision
DMA	**D**irect **M**emory **A**ccess
DNN	**D**eep **N**eural **N**etwork
DT	**D**ecision **T**ree
EM	**E**xpectation **M**aximization
FBCA	**F**eature **B**ased **C**apatibility **A**lgorithm
FCFS	**F**irst **C**ome **F**irst **S**erve
FFT	**F**ast **F**ourior **T**ransformation
FNN	**F**uzzy **N**eural **N**etwork
FP	**F**loating **P**oint
FT	**F**ault **T**olerance Kernels

FU	**F**unctional **U**nits
GBT	**G**radient **B**oosting **T**echniques
GEM	**G**aussian **E**xpectation **M**aximization
HPC	**H**igh **P**erformance **C**omputing
I	**I**nteger based
IPC	**I**nter **P**rocess **C**ommunication
KNN	**K** **N**earest **N**eighbor
L1	**L**ayer-**1**
L3	**L**ayer-**3**
LLC	**L**ast **L**ayer **C**ache
LP	**L**inear **P**rogramming **M**odel
LR	**L**ogistic **R**egression
LU	**L**ower **U**pper Kernel
MAE	**M**ean **A**bsolute **E**rror
MCI	**M**emory **C**ontroller **I**mbalancing
MEI	**M**ining **E**rasable **I**tem-set
MG	**M**ulti **G**rid Kernel
MMAX	**M**aximum **M**ain **M**emory (in KBs)
MMIN	**M**inimum **M**ain **M**emory (in KBs)
MPI	**M**essage **P**assing **I**nterface
MUL	**M**ultiplication
MYCT	**M**achine **C**ycle **T**ime (in Sec)
NAS	**N**umerical **A**erodynamic **S**imulation
NIC	**N**ode **I**nformation **C**ommunication
NPB	**N**AS **P**arallel **B**enchmark
NUMA	**N**on-**U**niform **M**emory **A**rchitecture
PC	**P**ersonal **C**omputer
PCA	**P**rinciple **C**omponent **A**nalysis
PDF	**P**robabiltiy **D**enisity **F**unction

PEDS	**P**arallel and **D**iscrete **S**imulation **E**nvironment
PMEI	**M**ulti-core based **M**ining **E**rasable **I**tem-set
QoS	**Q**uality **o**f **S**ervices
RCLB	**R**educing **C**ongestion **W**ith **L**oad **B**alancing
RMSE	**R**oot **M**ean **S**quare **E**rror
SD	**S**tandard **D**eviation
SKU	**S**tock **K**eeping **U**nits
SMPI	**S**imulator for **M**essage **P**assing **I**nterface
SOS	**S**ocial **O**pinion **S**ystem
SPEC	**S**tandard **P**erformance **E**valuation **C**orporation
SVM	**S**upport **V**ector **M**achine

Symbols

M	Memory Bandwidth
i	Number of interconnections
$S(x)$	processing speed of a processor
$t(x)$	Execution time of problem
X	Total Performance of associate processors in a cluster
x	Individual Performance of interconnected processor
N	Number of Nodes
W	Total Data Transfer Direction
θ	Data Transfer Direction of a single Processor
μ	Ratio between performance of fast and slow CPU
c	Numeric coefficient for scaling the system
$A_{\mu}^{W}(N)$	Performance advantage of all Nodes (achievable gain)
L_p	Master fraction of Load and Processor
α, β	Normalize values
S_0	All possible solutions or slices
$L_{balance}$	Load balance
L_{ik}	Load on processor p
W_i	Weighted sum of load resources
I_1, I_2	Individuals to share the information.
M_{info}	Mutual Information
H_I	Entropy

D_I	Normal distribution
$Norm()$	Normalized Information
I_{contri}	Contribution of I candidate
f_{cap}	Feature capabilities
I_{select}	Selected feature
SD	Standard Deviation
μ	Mean
$E(I_{contri})$	Evaluation of contribution of I candidate
PBM	Predicted Base Model