CHAPTER-2

Junctionless Accumulation-Mode SOI Ferroelectric FinFET for Synaptic Weights

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Abstract:

In this work, a novel SOI-based JAM FeFinFET is proposed along with its fabrication process flow at a 3-nm node for synaptic weights. The proposed JAM FeFinFET device can be easily integrated with the fabrication flow of p-FinFET in SOI process flow. The proposed device can be easily incorporated into standard FinFET SOI technology and thus is very attractive with respect to previously proposed devices. Further, using a well-calibrated 3-D TCAD simulation setup, we show that the device effectively replicates the behavior required for neuromorphic computing applications. The outcomes of the proposed study emphasize the significance of using the JAM FeFinFET as a synaptic weight device that exhibits a 76 % higher nonvolatile conductance range in the ON-state over existing junctionless and conventional FeFinFET devices. Our simulations show that the proposed device offers continuous linear conductance variation and symmetric switching characteristics, which are essential for neuromorphic applications.

2.1 Introduction:

Modern general-purpose electronic devices use Von-Neumann architecture for their computing systems, which separates memory and logic elements, causing higher latency and power consumption. This traditional architecture faces several bottlenecks due to its memory hierarchy and logic-memory separation. Neuromorphic computing is believed to be more efficient for artificial intelligence applications. In an era of rapidly evolving technology, synaptic devices, including synaptic memristors and synaptic transistors, are expected to replace conventional data storage like SRAM, DRAM, and Flash memory. The human brain performs computation using spiking networks consisting of neurons connected through synapses.

Neuromorphic computing involves mimicking this biological approach to achieve energy efficient next generation computing paradigm [127]. The traditional data storage options do not have the ability to remember the voltage previously applied to them for synapse application in neuromorphic systems [15]. Hence, the focus of this chapter is synaptic device whose state at any given time is not solely determined by the current input but is also influenced by past input patterns and the sequence of operations it has undergone. The traditional memory counterparts do not offer these properties especially DRAM and SRAM. So far, many solutions have been proposed to fulfill the necessities of high-speed, low-power, non-volatile memory elements that implement an artificial synapse, such as spin-based magnetic tunnel junctions [25], resistive memory devices [128] and phase change memory devices [24]. However, commercial viability and reliability are some important aspects that researchers are working on before large-scale productivity. Also, the two-terminal memory devices need other circuit elements for accessing a target location, when they are integrated in a system [129]. In the last decade, ferroelectricity in $Hf_{0.5}Zr_{0.5}O_2$ (HZO)-based thin films and the integration of ferroelectric field effect transistors [105] into standard CMOS platforms have gained a great deal of attention as promising devices in the field of neuromorphic computing for synaptic devices. Due to CMOS compatibility and outstanding scalability, ferroelectric HZO has created a rising interest in FeFET for neuromorphic computing [100]. The successful integration of FeFET into advanced technology nodes further highlights their promise for these applications [59].

Recently, BEOL-compatible junctionless FeFET devices have been reported by Halter *et al.* [82]. They have shown noteworthy advancement, however, the BEOL process overhead

can be quite costly. Further, the device has a planar structure, FinFET offers better power efficiency, performance, scalability, and superior control over short channel effects, hence, FinFET architecture can be better for forthcoming innovations. FEOL FeFinFET synaptic device has been demonstrated in Ref. [84], here a separate process flow is required for the fabrication of the device. Further, the ability of this devices to change the conductance or resistance in response to electrical stimulation can be limited due to high operating voltage. Hence, in this chapter, FEOL JAM FeFinFET is proposed and demonstrated, which is fully compatible with SOI process flow. In the proposed synaptic weight device, we were able to successfully mimic the conductance variations more effectively and at low operating voltage. Furthermore, it has zero process overhead and can be integrated very well with pristine Fin-FET SOI technology.

The remaining chapter has been organized into six sections. Section 2.2 presents the TCAD simulation setup, device architecture, and operation of SOI JAM FeFinFET. Fabrication methodology and comparison with existing process flow are presented in section 2.3. Section 2.4 discusses the transfer and memory cell characteristics of the proposed device. Further, we have characterized the proposed synaptic device by performing various simulations using different types of inputs and observing the corresponding polarization and drain current characteristics in section 2.5. The chapter is concluded through a brief section 2.6.

2.2 Background, Device Structure, Operation, and Simulation Methodology

The 3-D structure of the proposed JAM FeFinFET device, which was generated using process emulation in Sentaurus TCAD [130], is shown in **Figure 2.1** with an MFIS gate stack

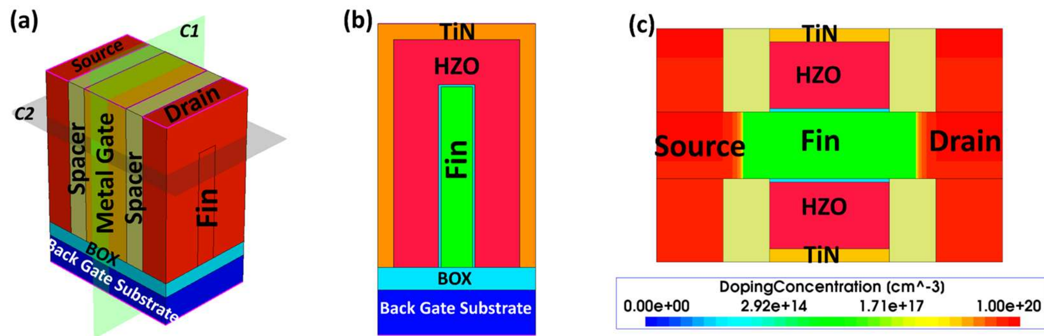

Figure 2.1 (a) 3-D NMOS SOI JAM FeFinFET structure, generated using process emulation. The two-dimensional cross-section of the 3-D JAM FeFinFET along (b) Cut-plane *C1*, (c) Cut-plane *C2*.

that covers the entire fin. The structure is based on the SOI device architecture. The proposed device and its physics have two parts: firstly, JAM FinFET structure and its properties/physics are discussed in subsection 2.2.1, and secondly, the physics of FE capacitor is discussed along with the proposed JAM FeFinFET structure in subsection 2.2.2. Wherein the ferroelectric HZO layer is placed on top of the gate-oxide layer [131] is incorporated. It uses ferroelectric polarization to regulate the conductance of the channel in our proposed architecture. Further, subsection 2.2.3 delineates the incorporated contact physics, which is benchmarked with experimental data. The overall operation is discussed in subsection 2.2.4.

2.2.1. JAM FinFET structure and physics

In n-channel accumulation-mode (AM) devices, the source, channel, and drain regions have an n + -n- n + structure, while p-channel devices have a p + -p- p + doping for the same regions. Compared to conventional inversion-mode FETs, the JL FETs [132] offer relative ease of fabrication. High parasitic resistance in the Source/Drain is a significant challenge for JL FETs. To address this issue, researchers have proposed a JAM FET [89] with additional S/D implantation. This technique has proven effective in reducing S/D parasitic

resistance [74]. JAM FETs are also called pseudo-JL [88] since the heavily doped S/D region are present, and there exists an interface between the heavily doped S/D and the lightly doped channel region. In addition, the accumulation mode device offers greater immunity against short-channel effects. **Figure 2.1 (a)** describes the structure of 3-D JAM FinFET in which the fin region will be of n-type, and source-drain will be of n + type, turning the conventional SOI FinFET into a JAM device. The nominal parameters used are shown in **Table 2.1**. The two-dimensional cross-section of the 3-D JAM FinFET, along the cut-plane *C1* and *C2*, are shown in **Figures 2.1 (b)** and **(c)**, in which the doping of the source and drain is shown. The presence of a buried insulator effectively prevents any substrate current, and confirming the thin n-type fin as the channel for the device. The fin is doped with an n-type concentration of 1×10^{16} cm^{-3} to ensure that the resistance of the channel is moderate [88]. The JAM Fin-FET structure depicted in **Figure 2.2 (a)** is simulated using TCAD. To perform this study, firstly, a baseline 3-D SOI JAM FinFET TCAD deck was set up at a 3 nm node.

The simulation setup is calibrated with experimental data on a pristine FinFET structure at a 3 nm node [133]. The calibration of FinFET electrostatics and transport properties was performed by comparing them to the experimental data obtained from Intel’s 10-nm measurements, as in Ref. [133]. Since there is a spatial proximity between the valence band of the channel region and the conduction band of the drain region in JAM FinFET, Band to Band Tunneling (BTBT) of electrons from the channel to the drain region is inevitable [88]. Further, BTBT model parameters are used from Ref. [88].

To account for the physics of the JAM device, *S. Sahay and M. J. Kumar* [88] have benchmarked BTBT model parameters against experimental data for junctionless and

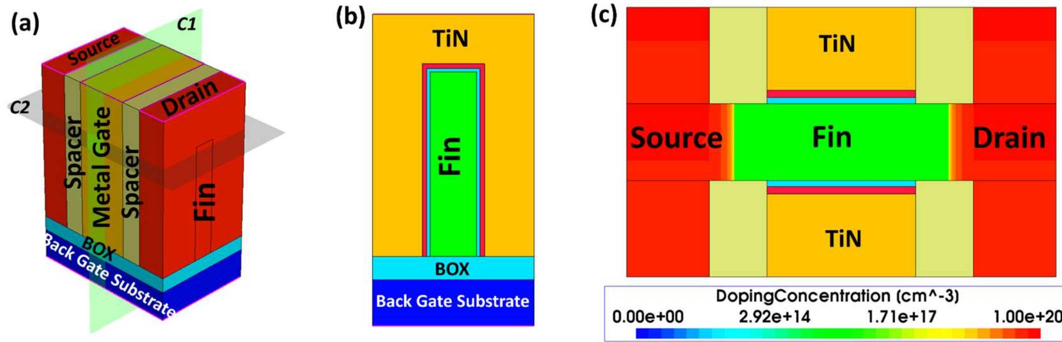

Figure 2.2 (a) 3-D NMOS SOI JAM FinFET structure, generated using process emulation. The two-dimensional cross-section of the 3-D JAM FinFET along (b) Cut-plane *C1*, (c) Cut-plane *C2*.

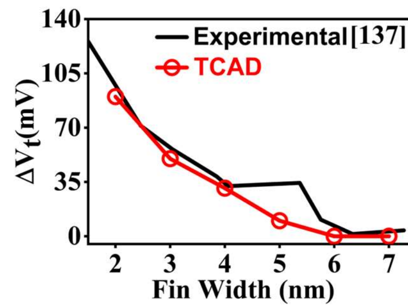

Figure 2.3 Calibration of the density-gradient model to precisely capture quantum-confinement in JAM FinFETs.

Table 2.1 TCAD simulation deck parameters [133],[134],[135].

Parameter	Value
Fin Width	10 nm
Fin Height	40 nm
Gate length	18 nm
Fin Doping (n-type)	1 x 10^{16} (cm^{-3})
Source/Drain Doping (n+ type)	1 x 10^{20} (cm^{-3})
Interface Oxide (SiO_2)	0.75 nm
HZO thickness	10 nm
Spacer width	7 nm
Gate Work-function	4.5 eV
Contact resistivity (ρ_c)	5 × 10^{-10} Ω-cm^2

JAM devices [136]. To accurately account for quantum-confinement, the density-gradient quantum-confinement model is well calibrated against the experiment results in [137], wherein the sensitivity of FinFET device parameters, such as V_T and I_{ON}, to such scaled fin-

widths, is dealt with [see **Figure 2.3**].

The following other physics models are also included in the TCAD deck. The mobility degradation due to the impurity scattering mechanism is captured, wherein for conventional mode FinFET, we have used Inversion and Accumulation Layer Mobility (IALMob) model while for JAM FeFinFET, Philips Unified Mobility model (PhuMob) is used. The Canali model was used to capture high-field saturation [130]. The Lombardi mobility model was used to account for interface roughness scattering. Shockley–Read–Hall-Recombination (SRH), Old Slotboom, and Hurkx models are used to account for recombination, bandgap narrowing, and trap assisted tunneling, respectively, as done in Ref. [133] for pristine FinFET simulation. The BTBT model is used for JAM FinFET, and the density gradient quantum confinement model is included in all the simulation results presented in this chapter.

2.2.2. Ferroelectric capacitor

The proposed structure of JAM FeFinFET, shown in **Figure 2.1**, consists of a 10 nm thick HZO in the gate stack to incorporate the non-volatile characteristics. This layer of ferroelectric material is capable of maintaining a continuous and stable polarization. The stored polarization, representing logic ’1′ or logic ’0′, persists even after removing the applied electric field due to hysteresis [138]. The history dependence of ferroelectric capacitor (FeCap), as well as the transient behavior in ferroelectric was included using a computationally efficient

Table 2.2 Experimentally calibrated model parameters of FeCap.

Parameter	Value
HZO thickness	10 nm
Coercive Field (F_C)	1×10^{6} V cm^{-1}
Remnant Polarization (P_r)	25×10^{-6} C cm^{-2}
Saturation Polarization (P_s)	42×10^{-6} C cm^{-2}

ferroelectric capacitor model [130],[139]. The model parameters were tuned [see **Table 2.2**] to accurately replicate the polarization-voltage characteristics that were experimentally observed in Ref. [140]. The corresponding comparison is shown in **Figure 2.4** for a FeCap, which shows accurate replication of the Preisach hysteresis and all the key properties in our simulations.

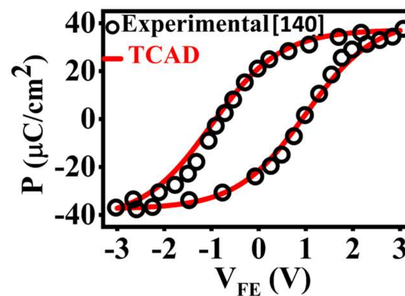

Figure 2.4 P-V calibration of FeCap with experimental data [140].

2.2.3. Contact physics

In aggressively scaled FinFET devices, the contact area in the S/D region is progressively reduced. This downsizing process leads to a significant increase in contact resistance [141]. Consequently, contact resistance strongly influences the ON-state resistance of the device. Hence, contact physics has been accounted for by adding contact resistance at the source and drain terminal. To ensure precise calculation of contact resistance in our device, we have introduced a total resistance (R_T) in series with the source and drain terminal, as shown in **Figure 2.5 (a)**. Herein, R_T is the combination of plug resistance (R_{plug}), silicide resistance (R_{slcd}), and contact resistance (R_c) in between the silicide and the epitaxial layer of the S/D, which is shown pictorially in **Figure 2.5 (b)**. The two-dimensional cross-section of the contact, along the cut plane *C1,* is shown in **Figure 2.5 (c)**. The contact resistivity (ρ_C)

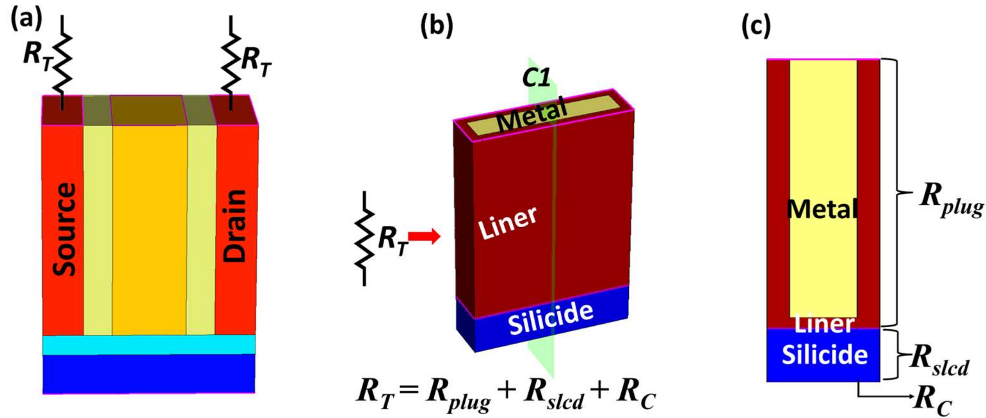

Figure 2.5 (a) JAM FeFinFET with contact at source/drain (b) 3-D contact structure, generated using structure editor in TCAD. (c) Two-dimensional cross-section of the contact along the cut-plane *C1*.

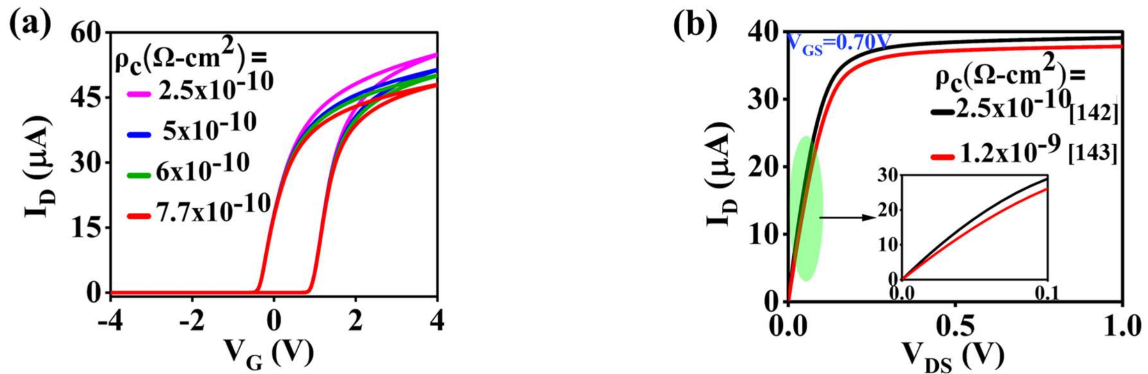

Figure 2.6 (a) I_D-V_G curve of JAM FeFinFET. (b) I_D-V_D curve of JAM FinFET without the ferroelectric material, here gate dielectric consists of $HfO_2 + SiO_2$ = (1+0.75) nm =1.75nm.

value between the silicide and the n-type epitaxial layer is obtained from experimental data in Refs. [134],[142],[143] for 7 nm and beyond aggressively scaled FinFETs.

The I_D-V_G characteristic of the proposed JAM FeFinFET after incorporating contact resistance is shown in **Figure 2.6 (a)**. The ON current of the device is reduced as there is an increase in the contact resistance. However, the memory window remains the same [see **Figure 2.6 (a)**]. The same is also verified through I_D-V_D characteristics of JAM FinFET without the ferroelectric layer in the gate stack [see **Figure 2.6 (b)**].

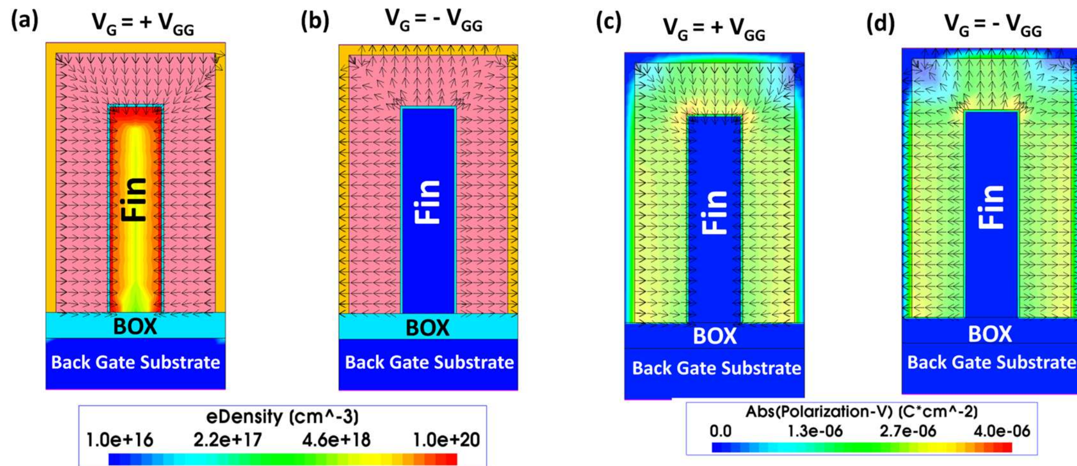

Figure 2.7 TCAD simulated (a) Electron density due to down polarization, (b) Electron density due to up polarization, (c) Absolute polarization due to positive gate voltage, and (d) Absolute polarization due to negative gate voltage.

2.2.4. Working of JAM FeFinFET

In the proposed JAM FeFinFET, the dopant used for the source and drain is the same as that used for the Fin. The ferroelectric material in JAM FeFinFET sustains the channel state when the gate voltage is not applied by virtue of its spontaneous polarization (P) [8]. The SOI structure provides complete dielectric isolation, which enables the use of AM devices. Most SOI structures, including FinFETs, can utilize accumulation-mode technology [89].

In JAM n-type ferroelectric FinFET, through TCAD simulations, we confirmed that when a positive gate voltage (V_{GG}) is applied, then a channel is formed due to the accumulation of electrons under the gate oxide layer. This channel is retained in the device due to the down polarization (towards the fin) in the ferroelectric material layer, as shown in **Figure 2.7 (a)**. Subsequently, at V_{GG} = -4 V, then the polarization of ferroelectric material becomes upwards (outwards from the fin). In this case, there is a reduction in the number of charge carriers (electrons) under the gate oxide layer. Hence, the channel conductance decreases [see **Figure 2.7 (b)**]. The TCAD simulated result of the proposed device for the V_{GG} sweep from ± 4 V

and ∓ 4 V, along with the electron density profile in the channel, is shown in **Figure 2.7 (a)** and **(b)**. **Figures 2.7 (c)** and **(d)** demonstrate the TCAD outcomes of absolute polarization when V_{GG} is swept in forward and reverse directions, respectively. This change in polarization induces hysteresis in the transfer curve of JAM FeFinFET, depending on the gate voltage, which is discussed in the next section.

2.3 Fabrication Methodology and Comparison with Existing Process Flow

The proposed JAM FeFinFET can be fabricated in the same way that the p-type pristine FinFET device is fabricated in SOI process flow but with one additional mask. **Figure 2.8** depicts the fabrication steps. The BOX layer can be created by implanting oxygen ions into silicon followed by annealing [144]. Further, we have taken the fin doping in the proposed device, the same as p-FinFET [145], and source, drain doping is similar to n-FinFET [146] so that the steps leading to deposition of the ferroelectric layer are compatible with p-type pristine FinFET during the process emulation. The steps involved during the creation of the structure using Sentaurus TCAD process emulation are shown in **Figure 2.8**. Herein, only one extra mask is required in step (i) to deposit ferroelectric material HZO after gate oxide deposition. The proposed process flow [see **Figure 2.9 (a)**] enables that one can fabricate the proposed device with a single extra mask as opposed to the JL device demonstrated in Ref. [84] for synapse application. The process flow of n-channel JL FeFinFET [see **Figure 2.9 (b)**] as described in Ref. [84] is also shown for comparison. Herein, the fabrication flow requires several additional processes that are not part of pristine p-type FinFET. For example, the implantation steps required are quite different from those required in the fabrication of conventional FinFETs. Hence, the proposed architecture involves zero process overhead and

compatibility with pristine FinFET process flow.

2.4 Transfer and Memory Cell Characteristics

To ensure the retention of non-volatile data, the I_D-V_G curve of the synaptic device is obtained under both forward and reverse bias conditions which is described in subsection 2.4.1. Further, the working of JAM FeFinFET-based memory cell is discussed in subsection 2.4.2.

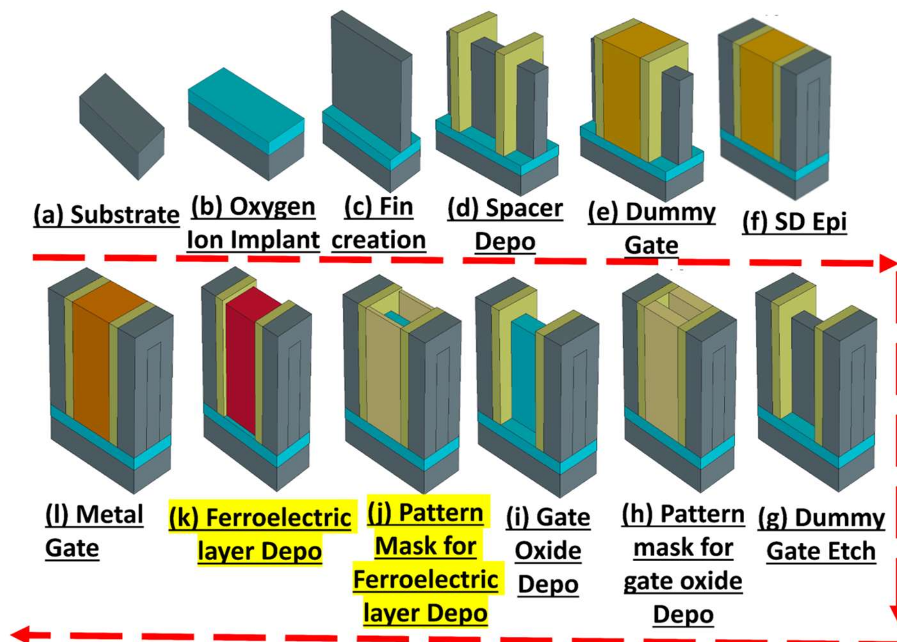

Figure 2.8 The proposed process flow of JAM FeFinFET.

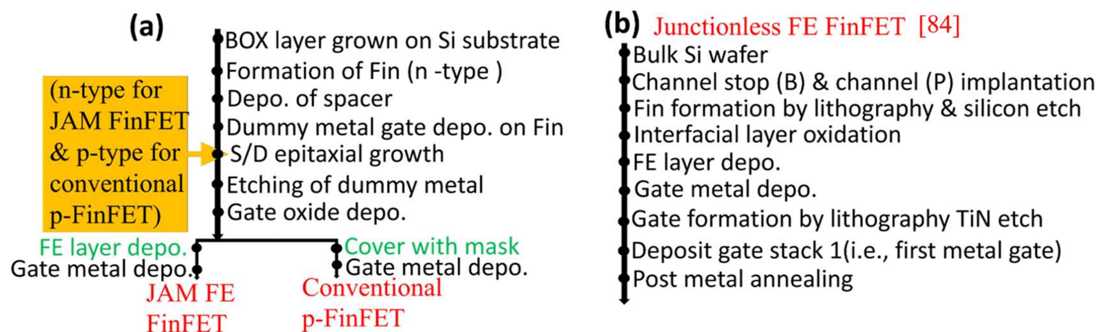

Figure 2.9 Comparison of fabrication process.

2.4.1. Transfer characteristics and memory window of JAM FeFinFET

Figure 2.10 (a) demonstrates the hysteretic nature of JAM FeFinFET, which is due to the presence of a ferroelectric layer in the gate stack. The calculated value of the memory window (MW) from the I_D-V_G curve is 1.30V for T_{Box} = 5 nm. Here, in the case of forward sweep (-4 V to +4 V), the device exhibits a threshold voltage of 0.90 V, whereas, under reverse sweep (+4 V to -4 V), it demonstrates a threshold voltage of -0.4 V. The benchmark for obtaining the threshold voltage is a drain current of 10^{-6} A at V_{DS} = 0.1 V. **Figure 2.10 (b)** shows the I_D-V_G characteristics of conventional FeFinFET, which has a p-type doping in the fin with a dopant concentration of $1\text{x}10^{16}$ cm^{-3}. The other device parameters are kept the same as given in **Table 2.1**.

The proposed JAM FeFinFET shows high on-current and significantly high variation in conductance [shown in **Figure 2.11 (a)**] for the same biasing condition in comparison to the result from conventional FeFinFET. The variation in conductance in the ON-state is quite important for synapse applications. Due to this, our proposed JAM FeFinFET is better suitable for synaptic device as compared to conventional FeFinFET and JL FeFinFET.

2.4.2. 2T JAM FeFinFET-based memory cell

In order to demonstrate the capability of the JAM FeFinFET device for data storage and justify the memory cell characteristics, transient mixed-mode simulations are carried out in Sentaurus TCAD for a 2T memory cell circuit implemented in [107], also shown in **Figure 2. 11 (b)**. Herein, the conventional FeFET is replaced by JAM FeFinFET (T2) to show write and read operation. Due to the three-terminal configuration of the FeFET, the cell is designed to have separate read and write paths, which facilitates simultaneous optimization of the read

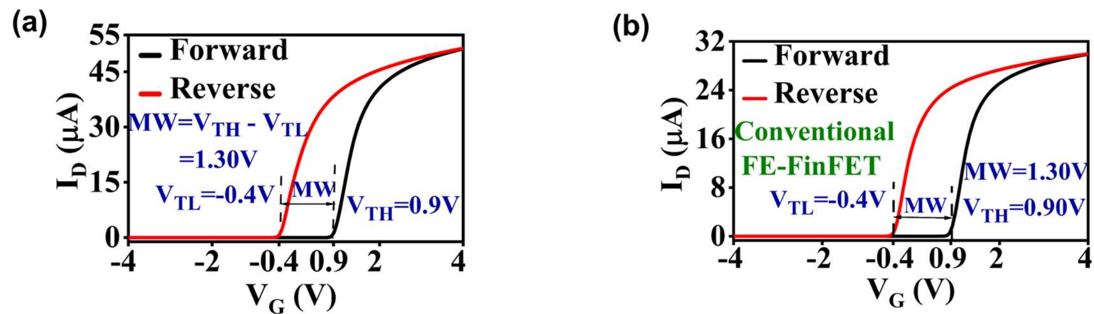

Figure 2.10 I_D-V_G characteristics demonstrating the MW of (a) JAM FeFinFET, (b) Conventional FeFinFET.

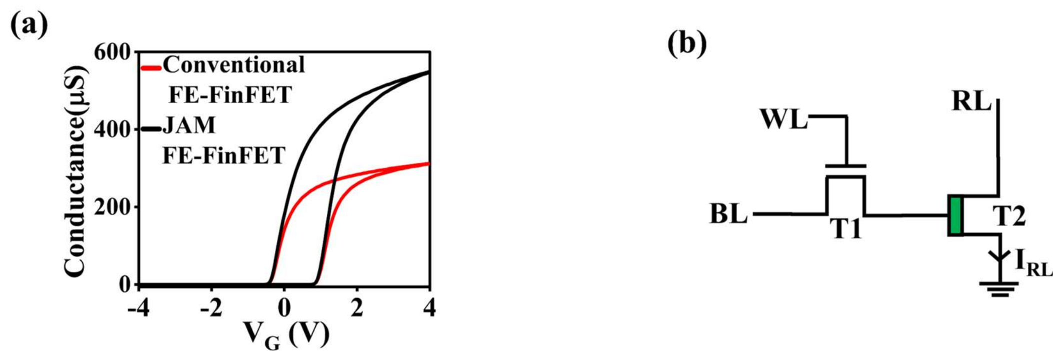

Figure 2.11 (a) Comparison of conductance. (b) 2T JAM FeFinFET-based memory cell.

and write operation. The write path has a pristine n-FinFET (T1) as an access transistor, which is controlled by a write select line (WL), enabling selective write operation to the cell when WL is 'HIGH'. The read path consists of T2 with the read select line (RL) connected to the drain and sense line tied to the source (ground). During the write operation, RL remains in a 'LOW' state, whereas during a read operation, RL is in a 'HIGH' state. The write and read are demonstrated subsequently using transient analysis in **Figure 2.12**.

Write operation

- Throughout the write operation, the RL is 'LOW,' and WL is 'HIGH.'
- To perform the write '1', a positive voltage is applied to the bit line (BL), causing T2 to

go into a low resistance state (LRS). Conversely, to write ‘0’, a negative voltage is applied on BL, which causes the V_{GS} of T2 to be negative and leads to the high resistance state (HRS) of T2. The LRS and HRS are verified by the current obtained at RL through simulations during read operation also shown in **Figure 2.12** and discussed further.

Read operation

- Throughout the read operation, the RL and WL are ‘HIGH.’ The BL is set to ‘LOW’ to ensure that the gate of T2 is unbiased for an accurate read operation. The RL voltage applied to the drain terminal senses the stored bit normally through a sense amplifier. The resulting drain current in T2 is influenced by the stored polarization, as shown in **Figure 2.12**, verifying the memory cell characteristics. The current is high (5.5µA) when JAM FeFinFET is in LRS and low (0.12µA) when it is in HRS.

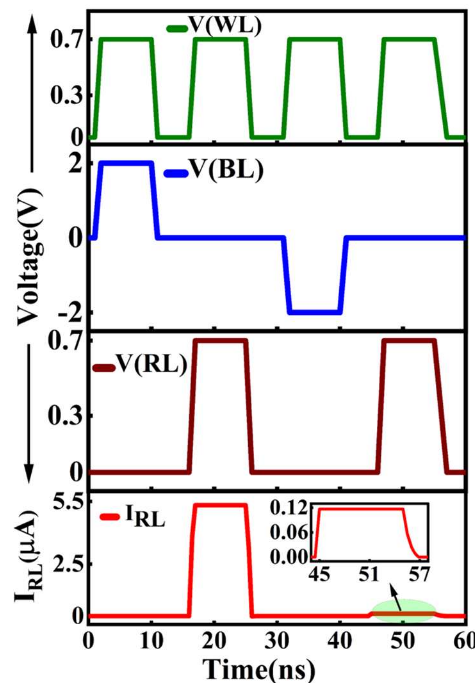

Figure 2.12 2T JAM FeFinFET memory cell transient waveform.

This 2T memory cell circuit is the basic building block of a crossbar array using FeFET. In this crossbar array, each synaptic weight unit cell has one access transistor, and one FeFET is used as a synaptic/storage device. In the next section, through device-level TCAD simulations, we demonstrate the different synapse characteristics of the proposed JAM FeFinFET.

2.5 Device Characterization and Discussion

Precise modulation of synaptic weight is facilitated by the minor loop trajectory in synaptic devices. Through the meticulous design of voltage pulses and the trajectory of ferroelectric polarization, it becomes feasible to attain targeted alterations in the synaptic weight. This level of detailed control over synaptic plasticity [147] is crucial for the implementation of intricate learning and memory processes in neuromorphic systems. In subsequent subsections 2.5.1–2.5.4, the proposed device is characterized using TCAD simulations by examining the ferroelectric history and minor loop trajectory, drain current characteristics, program-erase operation, and read-write operation.

2.5.1. Ferroelectric history and minor loop trajectory

Firstly, in order to show the minor loops, the proposed synaptic device was tested with various complex asymmetric input signals. The curve in **Figure 2.13** displays minor loop trajectories corresponding to three bias conditions as analyzed in Ref. [140]. Our results show that the proposed device allows multi-level programming. Further, it can be inferred that the ferroelectric material can be set to multiple polarization states within a single pulse cycle. This capability enables the encoding of analog information in the synaptic weights in terms of device conductance, which is closer to the processing of information in conventional synapses. Additionally, to demonstrate the extended spectrum of polarization states available in

the proposed synaptic device within a single pulse cycle and enable a more analog-like encoding of information in the synaptic weights, we have conducted simulations of the proposed device using a particular asymmetric input signal depicted in **Figure 2.14 (a)**. The corresponding P-V curve [see **Figure 2.14 (b)**] obtained from TCAD simulations exhibited a hysteresis loop with a spiral shape due to the input pulse, thereby conforming to the behavior of a synaptic device.

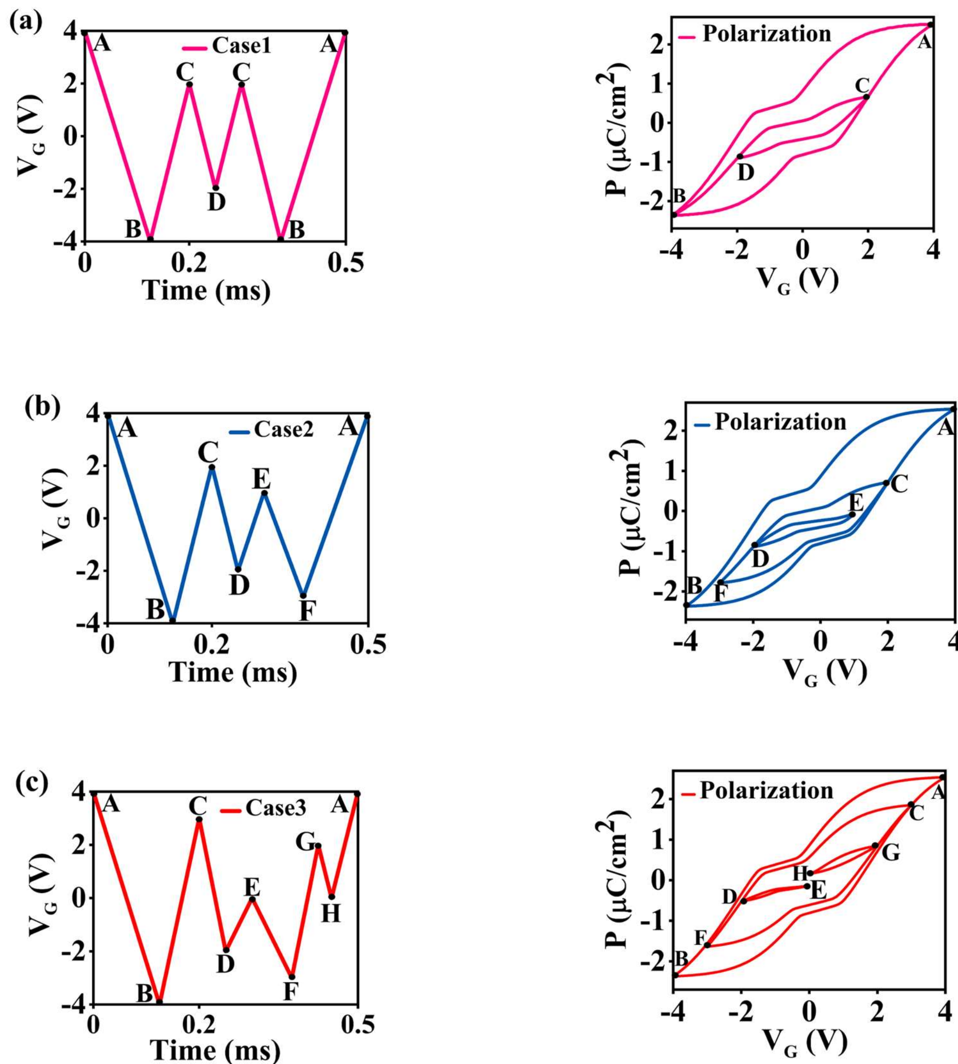

Figure 2.13 The simulated P-V curve of the proposed synaptic device for three different non-periodic asymmetric input signals, namely (a) case I, (b) case II, and (c) case III. Herein, P_r =2 μC/cm², P_s =3 μC/cm².

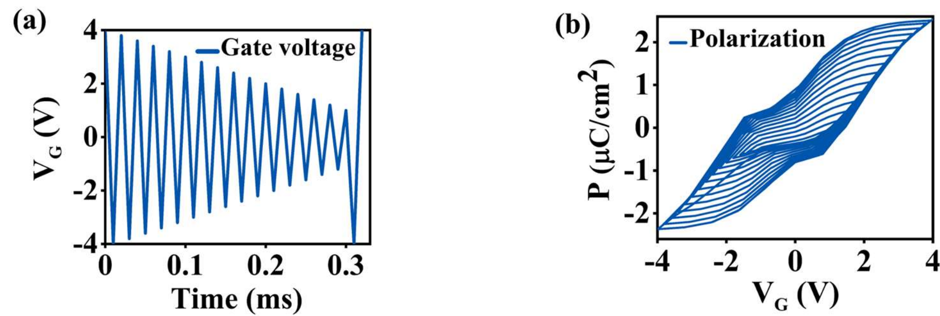

Figure 2.14 (a) Applied asymmetric input gate pulse (b) Obtained P-V hysteresis spiral curve.

2.5.2. History-dependent drain current characteristics

The FeFinFET-based synaptic device exhibits a history effect wherein the switching behavior of the ferroelectric material is impacted by the device's prior states. Consequently, the synaptic weight (charges retained within the ferroelectric material) or device state at any given time is not solely determined by the current input but is also influenced by past input patterns and the sequence of operations it has undergone.

The stored charges within the device reflect the strength of the connection between two artificial neurons when used in a neural network. So, to observe this behavior, we read the drain current characteristics of the device after applying three gate bias voltages with the same initial and final points but via different routes at a drain voltage of 0.1 V. **Figure 2.15 (b)** shows the history-dependent drain current characteristics of the JAM FeFinFET for three different cases. The biasing scheme is shown in **Figure 2.15 (a)**. The history-dependent polarization states have a considerable impact on the drain current of the FeFinFET, which leads to significantly different conductance in all three cases.

The significance of the history effect, as projected by the proposed TCAD simulations, lies in its direct influence on the synaptic behavior and plasticity of synaptic devices [148].

This influence holds immense importance in the area of emulating synaptic functions for applications in neuromorphic computing and artificial intelligence.

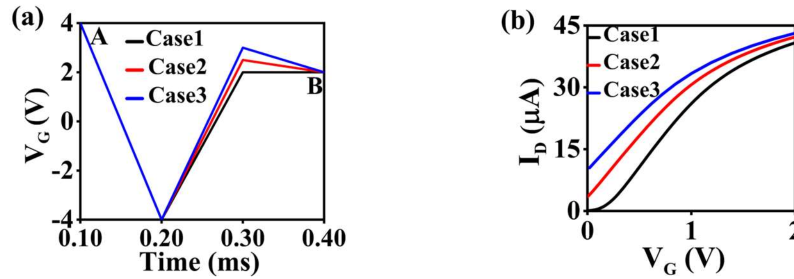

Figure 2.15 (a) Three different biasing voltages with the same initial and final voltage but different paths (b) History-dependent I_D-V_G characteristics of our proposed synaptic device.

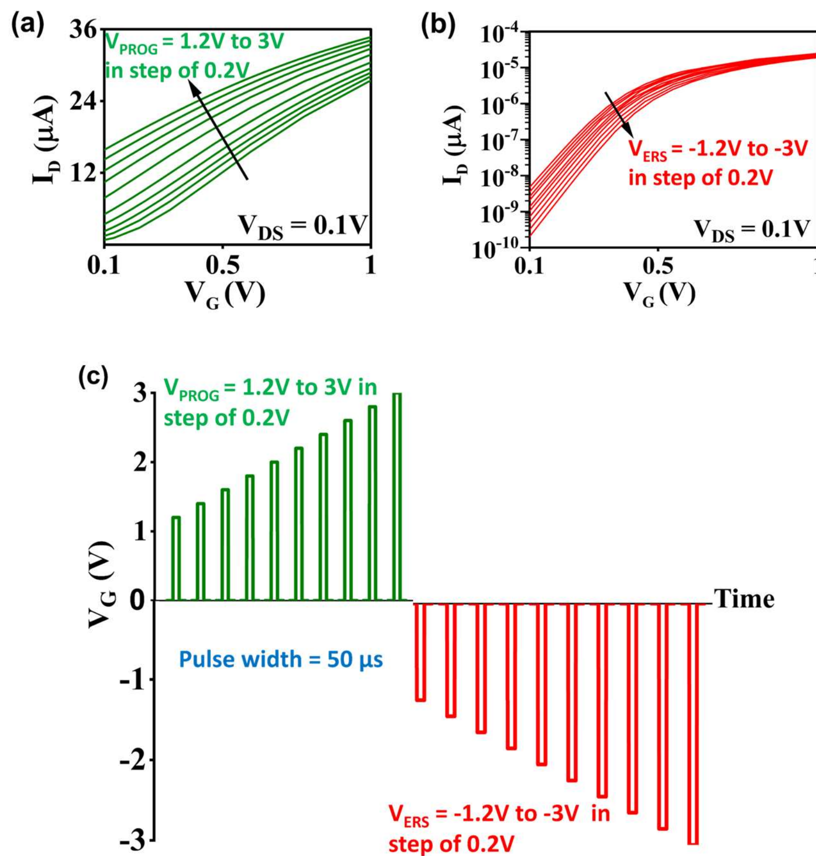

Figure 2.16 The JAM FeFinFET I_D-V_G characteristics were obtained for each polarization state during (a) The program and (b) Erase voltages while conducting the read process, (c) The scheme used for biasing during the program (shown in green color) and erase (shown in red color) cycles.

2.5.3. Program-erase and device conductance

In **Figure 2.16**, the relationship between the drain current and the gate-source voltage is depicted for both program and erase voltages at a constant drain-source voltage of 0.1 V. To program the device, the voltage amplitude is increased from 1.2 V to 3 V in increments of 0.2 V, as shown in green color in **Figure 2.16 (c)**, while maintaining a pulse width of 50 μs. After each programming pulse, the drain current for each polarization state is measured and plotted in **Figure 2.16 (a)** and **(b)**.

Similarly, to erase the device, a pulse is applied in the opposite direction, from -1.2 V to -3 V, in steps of - 0.2 V, as shown in red color in **Figure 2.16 (c)**. Here, the drain current is measured for each polarization state after each erase pulse, and the corresponding results are plotted in **Figure 2.16 (b)**. By utilizing the increasing/decreasing or program/erase characteristics, one can conclude that the device possesses the capability to retain the memory of previous input patterns. This ability enables the device to demonstrate long-term potentiation (LTP) or long-term depression (LTD) behavior, crucial for synaptic plasticity and learning. The fundamental characteristic of a synapse, which involves the ability to remember and recall past information, is thereby replicated.

The polarization state of the ferroelectric material can be altered, resulting in changes in the conductance of the channel. This conductance modulation allows for the adjustment of synaptic weights, enabling synaptic plasticity and learning in neuromorphic systems. **Figure 2.17** displays the confirmed relationship between the number of pulses and the gradually modulated channel conductance. The variations of conductance for each polarization state were measured at a V_{GS} of 0 V, 0.6 V, and 1 V, which is larger than the conductance reported

in Ref. [84] for the JL FeFinFET.

2.5.4. JAM FeFinFET read write

The difference in the drain current characteristics was observed by performing read-write operations and applying various program-erase voltages, as illustrated in **Figure 2.18**. To achieve a complete erase of the device in all cases, a rectangular pulse of -2.5 V/1 ms duration is applied to the gate of JAM FeFinFET for initialization. Following the initial erase pulse,

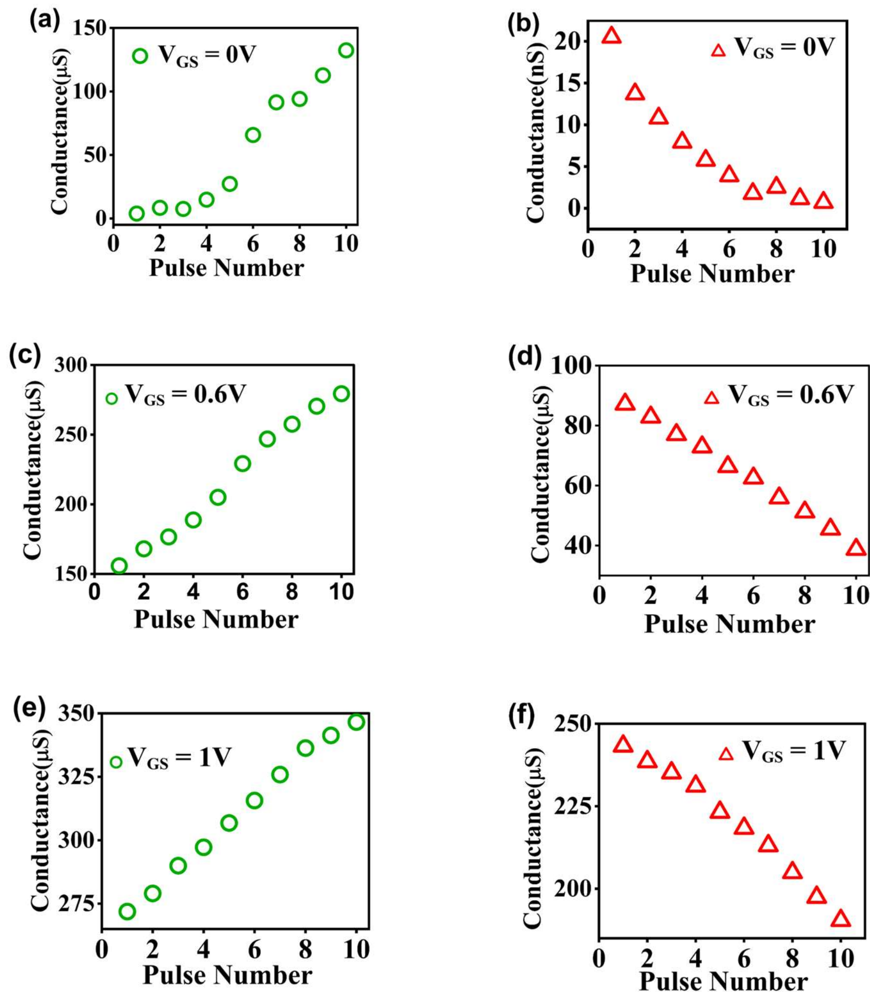

Figure 2.17 Conductance vs pulse number characteristics of JAM FeFinFET at different gate voltage during read cycle after each prog-erase pulse [shown in **Figure 2.16(c)**], (a)-(b) At V_{GS}= 0V, (c)-(d) At V_{GS}= 0.6V, (e)-(f) At V_{GS}= 1V.

a series of three distinct sets of continuous rectangular pulses with amplitudes of V_1/1 ms (program pulse), -V_2/1 ms, and -V_3/1 ms (erase pulse) are administered, as depicted in **Figure 2.18 (a)**. The drain current of the JAM FeFinFET was measured after each write pulse by sweeping the gate voltage from -0.3 V to 1 V using a triangular pulse while maintaining a constant drain voltage of 0.1 V. In **Figure 2.18 (b)**, the I_D–V_G characteristics after applying a different amplitude of gate voltage, *i.e.*, V_1 = 2.5 V, V_2 = -1 V, and V_3 = -1.4 V, are shown. Herein, the initial program voltage of 2.5 V/1 ms is applied, and the corresponding drain current is sensed, shown in red color. Afterward, a -1 V/1 ms and -1.4 V/ 1ms voltage pulse is applied at the gate, and for this voltage, the drain current is also plotted in **Figure 2.18 (b)** using blue and black colors, respectively. Hence, we have analyzed the drain current under three different gate voltages. It is evident that our proposed JAM FeFinFET exhibits higher current levels with positive gate pulse/voltage while demonstrating relatively lower current levels with negative gate pulse. This illustrates the capability of the device to operate at low operating voltage/power and the high sensitivity of the proposed device towards read operation.

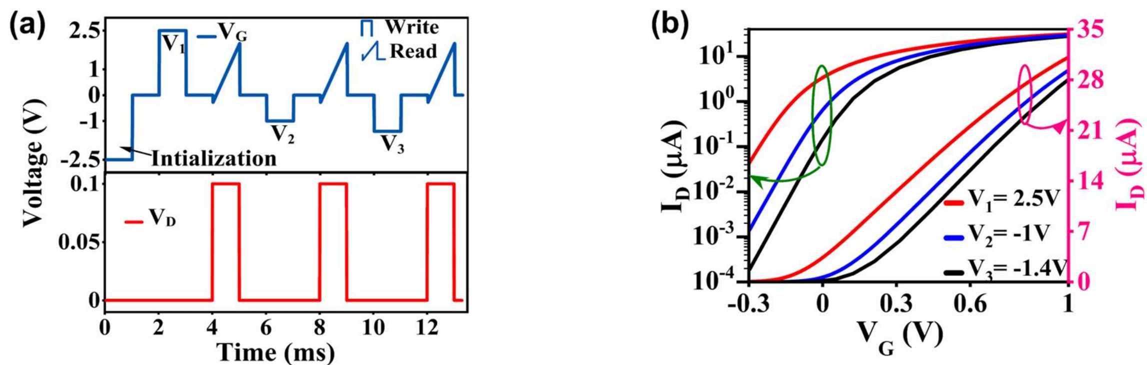

Figure 2.18 (a) Waveform designed to program the 18-nm JAM FeFinFET to different states and then read the drain current (b) Measured I_D –V_G characteristics after each program pulse, read after V_1 (Red color), after V_2 (Blue color), after V_3 (Black color) for each case.

2.6 CONCLUSION

In this article, we proposed a 3-D JAM FeFinFET architecture as a synaptic device for neuromorphic applications. The proposed JAM FeFinFET had a memory window of 1.30 V with 18 nm gate length and 10 nm ferroelectric thickness. We showed the non-volatile conductance and history-dependent memory behavior by applying different asymmetric inputs with the same initial and final point through different biasing schemes. Our results showed the high suitability of the proposed JAM FeFinFET device for neuromorphic applications. The proposed device exhibited a significant advancement in terms of a larger range of history dependent conductance and lower power operation as compared to previously reported synaptic devices.