Chapter 1

Introduction and Scope of the Thesis

1.1 Introduction

The revolution in the electronic industry started with the invention of the bipolar junction transistors (BJT) by William Shockley, John Bardeen, and Walter Brattain at the Bell Laboratory in 1947. The next revolutionary breakthrough took place with the invention of integrated circuit (IC) technology separately by Jack Kilby [9] and Robert Noyce [6] in 1958. BJT was the main active component in the ICs till 1990. Later, the metal-oxide-semiconductor field-effect-transistor (MOSFET), first demonstrated by Kahng and Atalla [5] at the Bell Laboratory in 1960, has become the primary component of modern ICs. Better feasibility of size miniaturization through the process of scaling along with lower power dissipation and higher speed of the MOS transistor over BJT has made it an important active component of the modern days ICs for low-power and high-speed VLSI applications [22],[49]. The complementary-MOS (CMOS) structure obtained by combining a p-channel and an n-channel MOSFET on a single substrate gave birth to a new IC technology called the “CMOS technology”. This technology is extensively getting explored in creating modern day microprocessors, microcontrollers, memory chips, and other digital logic circuits. The endless aspiration of designing complex multifunctional microprocessor systems by integrating billions of CMOS transistors on a single wafer of particular size for high-performance computing

and communication applications have led to the miniaturization of the MOSFETs in the ICs through scaling.

1.2 MOSFET Scaling and Moore's Law:

By observing the rate of growth of components in the ICs, Gordon E. Moore, one of the co-founders of *Fairchild Semiconductor* and *Intel*, had forecasted in 1965 that the number of components (specially transistors) in an IC would get double in every year at least for a decade [11]. Later in 1975, Moore modified his prediction and told that number of components in ICs would double in every two years for the next one decade [13],[35]. This prediction of G. E. Moore, commonly known as *Moore's law*, has paved the way for seamless growth and development of the IC technology in the modern day's microelectronics industry for over four decades. As a result, the number of transistors in the ICs of different generations of microprocessors has increased from hundreds to billions during last four decades as demonstrated in Fig. 1.1 [Internet resource (IR1)]. The accommodation of more and more number of transistors in an IC has been possible

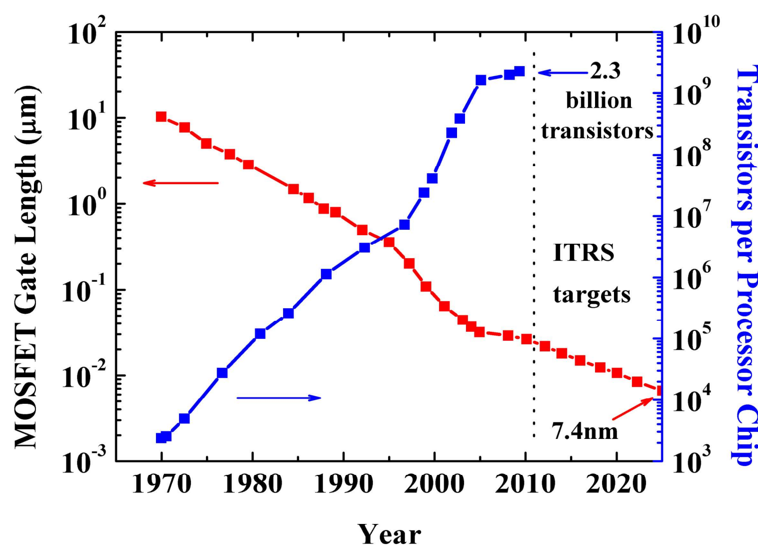

Fig. 1.1: The ITRS roadmap of transistor development [Internet resource (IR1)].

through the reduction in device dimensions through dimension scaling. Starting from the gate length 10 μm in 1970 of the MOSFETs, Fig.1.1 shows that the gate length of the MOS transistors will reach to a value of 7.4 nm in 2025.

In principle, scaling of MOSFETs is the miniaturization of the device dimensions without making any intervention to its performance. In this process, other device parameters such as the thickness of gate dielectric, thickness of channel, applied bias voltages, threshold voltages, doping concentration etc. needs to be changed accordingly in order to achieve the optimum device performance. Keeping these aspects in mind, two types of primary scaling rules have been adopted: constant electric field scaling [12] and constant voltage scaling [29]. In constant electric field scaling the device dimensions are scaled in such a way that the electric field remains same as the corresponding electric fields of the original device before scaling. Under this scaling principle, if the channel length of a MOS device is scaled by a factor 'α', then the supply voltages, source/drain channel junction depth, channel thickness, gate-oxide thickness, and the threshold voltage are also scaled by the same factor 'α'. The substrate doping is increased by the factor 'α' to make the overall electric field constant before and after scaling. The major pitfall of this scaling theory is the requirement of different supply voltages for differently scaled transistors. Further, the supply voltage cannot be scaled indefinitely for practical operation of the transistors. To overcome this issue in constant field scaling, constant voltage scaling was introduced by Taur and Ning [29]. Here the scaling is made in such a way that the supply voltage remains the same before and after the device scaling. In this regard, device dimensions are reduced by a factor 'α' and the doping concentration is increased by the same factor 'α' by keeping the supply voltage fixed. However, this constant voltage scaling leads to a drastic increase

in the electric fields in the channel which may result in many adverse effects like the velocity saturation of channel carriers [30], hot carrier effects [31],[33], avalanche breakdown [29] etc. Therefore, the requirement of the scaling in supply voltage (V_{DD}) and the threshold voltage (V_{th}) of the MOS transistors is also essential along with the reduction in the device dimensions. To create a bridge between the constant field and constant voltage scaling rules discussed above, several generalized scaling rules have been proposed in the literature [23]. Since the supply voltage (V_{DD}) cannot be allowed to decrease beyond a certain limit, it has been fixed at approximately 1V for 90 nm technology node and beyond [48].

1.3 Adverse Effects of Scaling on Subthreshold Characteristics of MOSFETs:

The increased demand for the miniaturization transistors to enhance the functionality of the ICs has imposed insurmountable barriers to the power management of the ICs due to the increase in the active power ($P_{Activec}$) dissipations and sub threshold power (P_{Sub}) or static power dissipations described by [48] as follows:

$$P_{Activec} = fC_{load}V_{DD}^2 \tag{1.1}$$

$$P_{Sub} = V_{DD}I_{OFF} \tag{1.2}$$

where, C_{load} is the load capacitance; f is the frequency; and I_{OFF} is the OFF-state current of MOSFET.

The increase in the power dissipations with the decreased gate lengths under various technology nodes is shown in Fig. 1.2 [42]. The increase in active power dissipation is

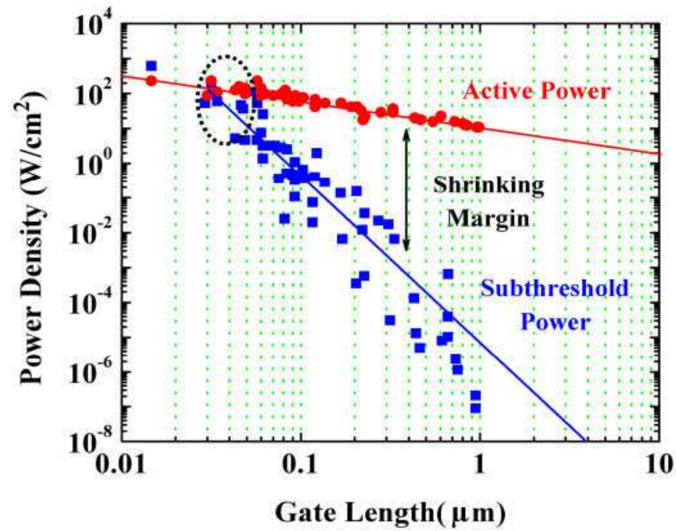

Fig. 1.2: Variation of power density against gate length scaling of MOS device [42].

mainly due to the increase in the operating frequency of the MOSFETs, whereas the increase in static power dissipation is mainly attributed to the increase in sub-threshold leakage current resulted from threshold voltage degradation due to the short-channel effects.

Figure 1.3 shows the typical drain current (I_d) versus gate-source voltage (V_{GS}) characteristics of three different MOSFETs having different threshold voltages but with ideal subthreshold swing (SS) of 60 mV/decade at room temperature. The threshold voltage is decreased with the gate lengths of the MOSFETs, which, in turn, increases the OFF-state current (I_{OFF}) as depicted in Fig. 1.3. Since the increase in I_{OFF} results in the increase of the subthreshold power dissipation (see Eq. (1.2)), we can't scale down the threshold voltage parameter aggressively for the MOSFETs below a certain level. On the other hand, we can't scale MOSFETs with a high threshold voltage since larger threshold voltage (due to larger gate lengths) results in the smaller ON-current (see Fig. 1.3) and hence smaller operating speed of the device [69].

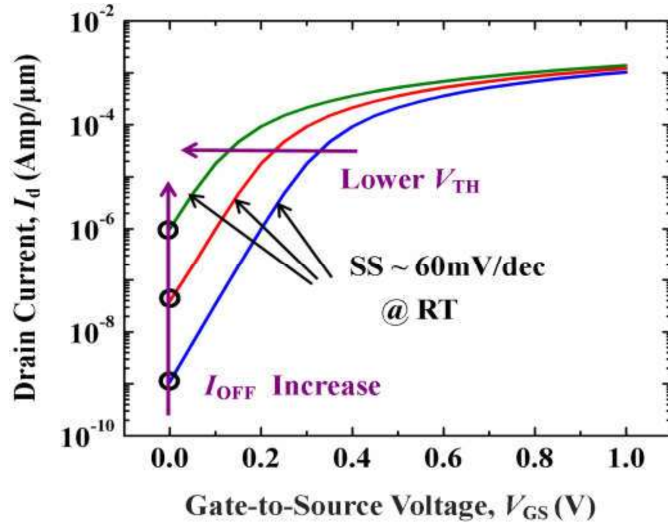

Fig. 1.3: Variation of drain current against gate-to-source voltage of MOS device [Internet resource (IR2)].

Figure 1.4 demonstrates the reduction in the supply voltage (V_{DD}) and threshold voltage (V_{th}) by approximately one-fifth and half of their corresponding original values due to scaling of CMOS from 1.4 µm to 65 nm technology node [50]. Further, it can also be seen from the figure that with the decrease in the gate overdrive voltage with the technology generation nodes, the switching performance of the MOS transistors is getting degraded due to the deterioration of the ratios of I_{ON}/I_{OFF} and $C_g V_{DD}/I_{ON}$ where C_g, I_{ON} and I_{OFF} are the gate capacitance of ON-current and OFF-state current of the MOSFET, respectively.

The subthreshold swing (SS) is an important parameter of the MOSFETs. It is defined as the minimum gate voltage required to change the subthreshold drain current of the MOS transistor by one decade. The SS parameter defines the switching characteristics of the MOSFETs which can be mathematically expressed as [114]:

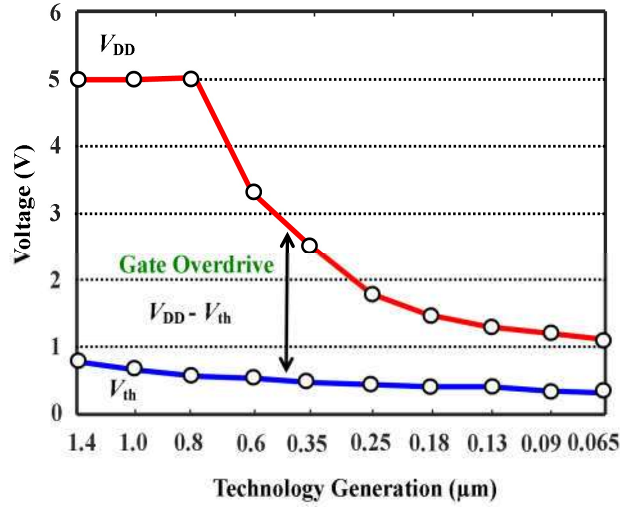

Fig. 1.4: Variation of supply voltage and threshold voltage against technology generation [50].

$$SS = \frac{\partial V_{GS}}{\partial(\log I_d)} = \frac{\partial V_{GS}}{\partial \psi_S}\frac{\partial \psi_S}{\partial(\log I_d)} = \underbrace{\left(1+\frac{C_{Dep}}{C_{ox}}\right)}_{m}\underbrace{\left(V_T \ln 10\right)}_{n} \tag{1.3}$$

where, $V_T = kT/q$ is the thermal voltage, V_{GS} is the gate-to-source voltage; I_d is the drain current; ψ_S is the surface potential; C_{Dep} is the depletion capacitance and C_{ox} is the gate-oxide capacitance of the MOSFET.

It may be noted that $m = (1 + C_{Dep}/C_{ox}) \geq 1$ represents the coupling efficiency of the gate voltage to the channel potential while the value of the factor $n = V_T \ln 10 = 60$ mV/decade at room temperature is associated with the thermal distribution of mobile charge carriers at room temperature [34]. Thus, $SS \geq 60$ mV/decade at room temperature for conventional bulk MOSFETs, is known as the Boltzmann's limit of the SS. It is worth mentioning that for ideal switching, the

device SS should be zero. However, the constraint of SS >60 mV/decade in conventional bulk MOSFETs compelled the researchers to search for non-conventional MOS structures with reduced threshold voltage degradation (hence smaller increase in both I_{OFF} and P_{Sub}), high ON-current to OFF-state current ratio (I_{ON}/I_{OFF}) and small SS (below the Boltzmann limit of 60 mV/decade) for designing low-power and high performance future generation microprocessor systems. The tunnel field effect transistor (TFET) has emerged as one of such non-conventional MOS devices which has an inherent feature of achieving extremely low subthreshold current, low $SS < 60\text{ mV/decade}$ and high I_{ON}/I_{OFF} [51],[53],[89]. Unlike the conventional MOS transistors, the TFETs possess the SS below the Boltzmann limit (of 60 mV/decade at room temperature) due to $m = (1 + C_{Dep}/C_{ox}) < 1$ (see Eq.(1.3)) resulted from the negative gate capacitance effect [36],[53].

The present thesis investigates the device and circuit level performance of some vertically grown stacked gate-oxide and source pocket engineered TFETs with a low bandgap material in the source region of the device. The following section is thus devoted to introduce the basic TFET structure, its working principle and fundamental theory behind the operation of this device.

1.4 Introduction to Tunnel Field Effect Transistor (TFET)

Tunnel field effect transistor (TFET), also known as "Green Transistor" [60], has evolved as a potential candidate to achieve the subthreshold swing (SS) below the Boltzmann limit of 60 mV/decade which is the minimum SS value of the conventional MOS transistors [43],[53],[54],[59],[61],[81]. Unlike the surface inversion phenomenon in the conventional MOSFETs, the working of TFET device is based on the tunneling of

electrons from the valence band of the source to the conduction band of the channel at the source/channel junction. TFET not only has smaller SS value but also has extremely lower OFF-state leakage current as compared to other conventional (i.e. without using non-ferroelectric as gate-dielectric) MOS structures. As a result, the TFET has been the locus of attraction for many because of high-speed and low-power VLSI applications [44]. However, the major huddles for the TFET are its low ON-current and ambipolar conduction current [41],[51],[59].

The schematic structures of the basic n-channel MOSFET and TFET are compared in Fig. 1.5(a) and (b) respectively. The basic structural difference between n-MOSFET and n-TFET is the use of an asymmetric doping in source and drain region in TFETs which is making it a p^{++}-i-n^{+} gated diode structure unlike in MOSFETs which is lateral n^{+}-p^{-}-n^{+} transistor with symmetric source and drain doping. In addition, the current conduction mechanism of TFETs is entirely different from the conventional MOSFETs. The basic carrier transport phenomena of the MOSFETs and TFETs can be understood from Figures 1.6(a) and (b) respectively. Figure 1.6(a) shows the energy band diagram of the lateral n^{+}-p^{-}-n^{+} transistor structure of the MOSFET shown in Fig.1.5(a) whereas Fig. 1.6(b) shows the energy diagram of the p^{++}-i-n^{+} structure of the lateral TFET device considered in Fig.1.5(b). In the conventional MOSFETs, the energy barrier at the source-channel junction is required to be reduced by applying a gate voltage to enhance the number of carriers entering from the source into the channel region by the process of thermionic emission. Then carrier transport in the channel takes place by the drift-diffusion mechanism depending on the channel length of the device. However, in the case of TFET device, the gate voltage is applied to create a condition for electron tunneling from the valence band of the source to empty energy states of the conduction

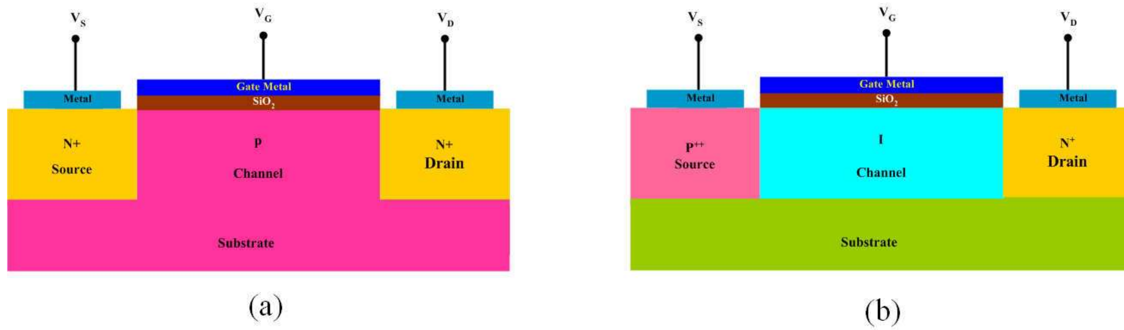

Fig. 1.5: 2-D schematic view of an n-channel (a) MOSFET and (b) TFET

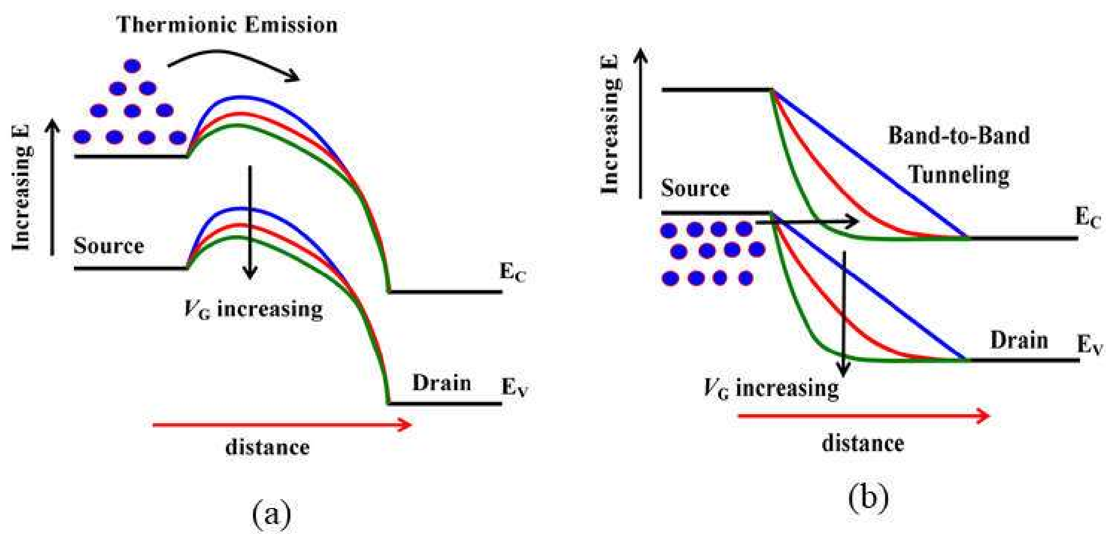

Fig. 1.6: The current conduction mechanism of (a) MOSFET and (b) TFET [94]

band of the channel region by reducing tunneling energy barrier at the source-channel junction. As a result of different carrier transport mechanisms, the conventional MOSFETs result in a much higher drain current in the range of mA/µm than that of the TFETs which have drain current in the range of µA/µm. At the same time very pertinent point to discuss here is that MOSFETs do have higher OFF-state current in the range of nA/µm whereas TFETs have much lesser OFF-state current in the range of fA/µm making it more suitable for low power applications [29],[73],[89]. A brief detail of the working principle of the TFETs be is described in the following subsection.

1.4.1 Working Principle of a TFET

As shown in Fig. 1.5(b), n-channel TFET is like a gated p-i-n diode in which the drain current results from the tunneling of carriers from the valence band of the source to the conduction band of the channel controlled by the applied bias voltage to the gate electrode placed over the intrinsic (*i.e., i*-region) of the device [4],[17],[19]. In case of n-type TFETs, the source, channel and drain are heavily doped p^+, intrinsic or lightly doped p^- and heavily doped n^+ regions respectively as shown in Fig.1.7(a). On the other hand, in p-type TFETs, the source, channel and drain are heavily doped n^+, intrinsic or lightly doped p^- and heavily p^+ regions respectively as shown in Fig. 1.7(b). The concept of tunneling of carriers in the p-i-n diode was first proposed by Clarence Melvin Zener in 1934 [1]. In addition, tunneling phenomena in diode was also observed by Leo Esaki in 1976 [14]. For both the n-channel MOSFETs and TFETs, positive bias voltage is applied to the gate and drain terminals to make the channel-drain junction reverse biased in both the devices. However, the source-channel junction is set to zero volt in MOSFETs while it is reverse biased with respect to the source in case of TFET device. The basic working principle of the conventional n-TFET device of Fig. 1.7(a) can be explained by the energy band diagrams of the p-i-n diode under the OFF-state (*i.e.,* with

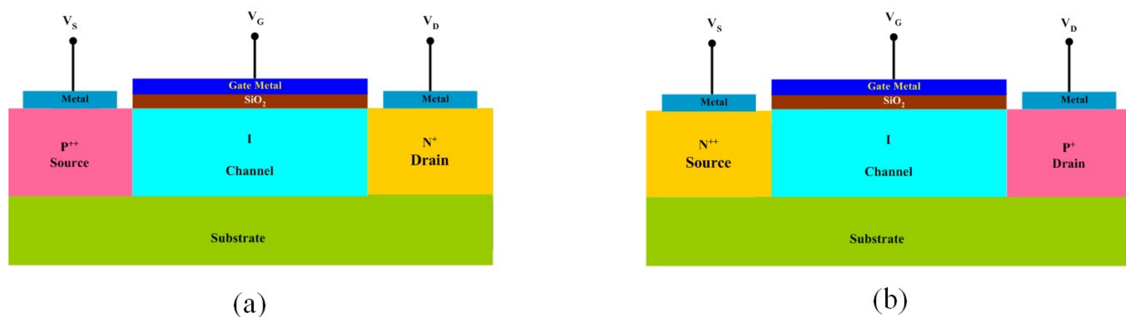

Fig. 1.7: Conventional structure of (a) n-TFET device and (b) p-TFET.

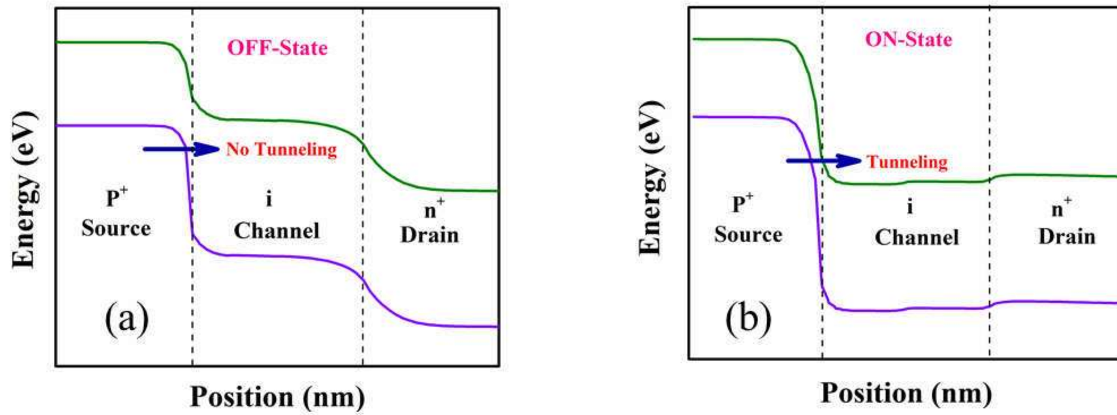

Fig. 1.8: Energy band distribution of a typical TFET under (a) OFF-state and (b) ON-state.

an insignificant drain current) and ON-state (*i.e.,* with a significant drain current) conditions of the device shown in Fig. 1.8(a) and (b) respectively. In OFF-state condition, the gate and source terminals are kept grounded while the positive voltage is applied to the drain terminal of the device. Under this bias condition of the TFET, the tunneling barrier width is thicker and electrons in the valence band of the source do not find empty states in the conduction band. As a result, electrons cannot tunnel from the valence band of the source to the conduction band of the channel region. Therefore, in OFF-state, the drain current is extremely low and generally it is in the order of femtoampere (fA). However, with the application of a positive gate voltage, the energy tunneling barrier width decreases due to the reverse biased source/channel junction. In this case, valence band of the source gets aligned with the conduction band of the channel region so that valence band electrons of the source can easily tunnel to channel region. This results in a significant amount of drive current and this condition is known as ON-state of the TFETs. Thus, the operating principle of TFET is based on the modulation of the tunneling barrier width which varies with the application of the gate voltage. It is observed from the figure that the tunneling barrier width decreases with

the increase in the gate voltage for the relevant TFET operation. The BTBT phenomena in TFETs results in a much lower ON-current than the conventional MOSFETs. The higher gate biasing voltage with a fixed $V_{DS}=V_{DD}$ reduces the tunnelling of carriers because the valence band electrons of the source face a higher potential barrier. This is so-called tunnelling resistance [89]. This results in a relatively low ON-current.

1.4.2 Band-to-Band Tunneling Current in TFETs

It is apparent from the above discussions that the drain current in the TFET results from the band-to-band tunneling (BTBT), which is a quantum-mechanical phenomenon for transporting charge carriers from the valance band of the source to conduction band of the channel region through the energy band gap existing at the source/channel junction.

If the energy barrier is thick enough to prevent the quantum tunneling of the carriers (valence electrons), we say that the device is under the OFF-state. The ON-state energy band diagram and corresponding triangular potential barrier for a typical TFET are shown in Fig. 1.9(a) and (b) [54]. Figure 1.9(a) shows that the charge carriers can

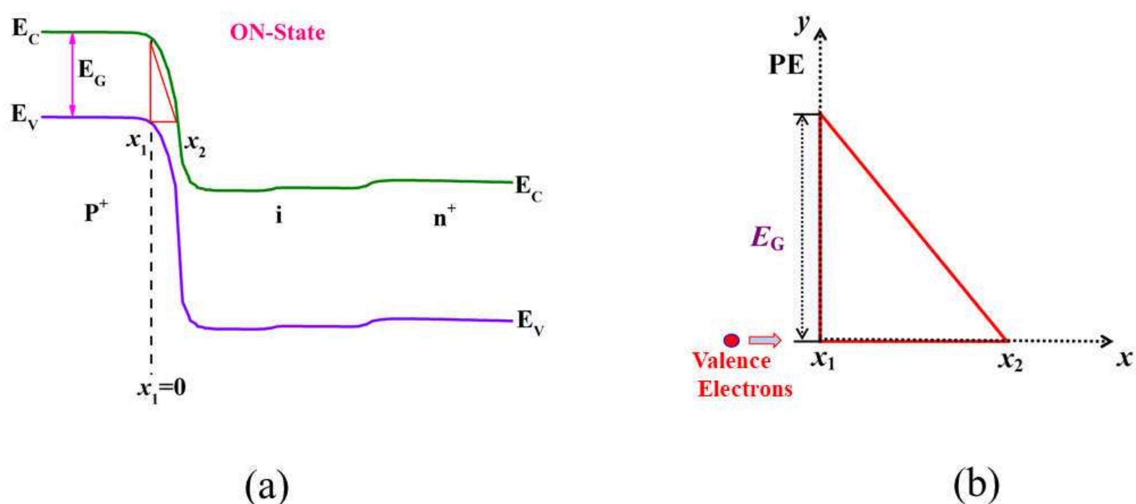

Fig. 1.9: (a) The ON-state energy band distribution and (b) its corresponding triangular potential barrier for typical TFET.

tunnel from x_1 point to x_2 through a triangular energy barrier as shown in Fig. 1.9(b). The probability of tunneling (T_P) of the charge carriers (valence electrons) through an energy barrier of finite height and width can be obtained from the Wentzel-Kramers-Brillouin (WKB) approximation technique as [4],[17]:

$$T_p \approx \exp\left[-2\int_{x_1}^{x_2} |k(x)| dx\right] \tag{1.4}$$

where, $k(x)$ is the wave vector of the charge carriers inside the barrier; x_1 and x_2 are the classical turning points as shown in Fig. 1.9(a). From the E-k relationship, $k(x)$ can be written as [17]:

$$k(x) = \sqrt{\frac{2m^*}{\hbar^2}(PE - E)} \tag{1.5}$$

where, PE and E are the potential energy and the incoming energy of the charge carriers, m^* is the reduced tunneling mass of the charge carriers (valence electrons) and $\hbar$ is the reduced Plank's constant.

It can be seen from the figure that the potential energy at the coordinate axis x_2 is equal to zero *i.e.,* $E = 0$ and the incoming energy of charge carriers (PE) is replaced by $E_g/2 - qFx$, where F and E_g are the electric field at the tunneling junction and energy band gap of the substrate material respectively. Then, the wave vector can be expressed as [17]:

$$k(x) = \sqrt{\frac{2m^*}{\hbar^2}\left(\frac{E_g}{2} - qFx\right)} \tag{1.6}$$

Putting the wave vector in tunneling probability equation (1.4), we get

$$T_p \approx \exp\left[-2\int_{x_1}^{x_2}\sqrt{\frac{2m^*}{\hbar^2}\left(\frac{E_g}{2}-qFx\right)}dx\right] \tag{1.7}$$

which can be further simplified as

$$T_p \approx \exp\left[\frac{4}{3}\frac{\sqrt{2m^*}}{q\varepsilon\hbar}\left(\frac{E_g}{2}-qFx\right)^{3/2}\right]_{x_1}^{x_2} \tag{1.8}$$

From the triangular shape of energy barrier shown in Fig. 1.9(b), we can write $(E_g/2-qFx)=E_g$ and $(E_g/2-qFx)=0$ at $x=x_2$. Thus, tunneling probability (T_P) can be written as [17],[72]:

$$T_p \approx \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3q\hbar F}\right) \tag{1.9}$$

Since the band-to-band tunneling current (I_d) is directly proportional to the tunneling probability (*i.e.,* $I_d \propto T_p$), we can write [4]:

$$I_d \propto \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3q\hbar F}\right) \tag{1.10}$$

Using the Kane's model, Eq. (1.10) can be expressed as [4]:

$$I_d = A_{Kane}F^{\alpha}\exp\left(-\frac{B_{Kane}}{F}\right) \tag{1.11}$$

where, $A_{Kane} = q^3\sqrt{2m^*/E_g}/4\pi^2\hbar^2$, and $B_{Kane} = 4\sqrt{2m^*}E_g^{3/2}/3q\hbar$ are known as the Kane's parameters and "α" is a material dependent constant parameter; q is the elementary charge; m^* is the reduced tunneling mass of the charge carriers; and $\hbar$ is the reduced Planck's constant [4],[17].

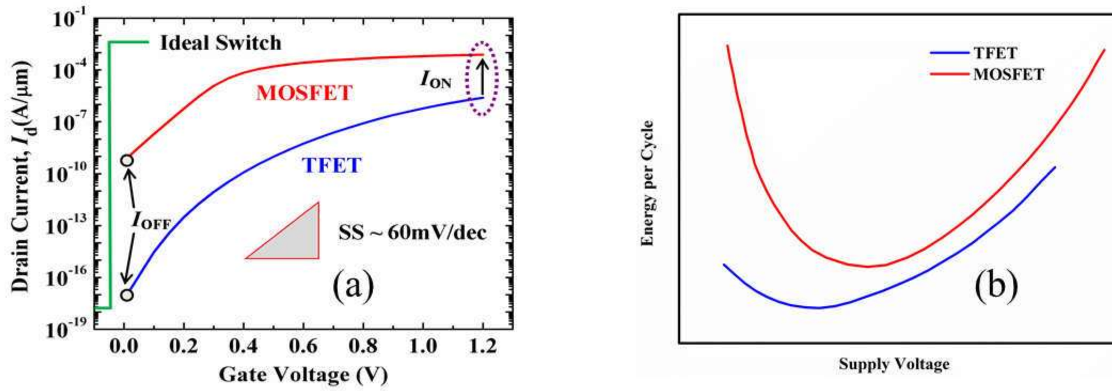

Fig. 1.10: (a) Transfer characteristics for Ideal device, Bulk MOSFET and TFET [34] and (b) Comparison of the energy consumption per cycle with respect to supply voltage for TFET and MOSFET having same I_{ON}/I_{OFF} ratio [89].

The typical transfer characteristics for an ideal switching device, bulk n-MOSFET and n-TFET have been compared in Fig. 1.10(a). It is clearly observed that while the much smaller OFF-state current of the TFET has a significant advantage over MOSFET, the smaller drain current of the TFET over the bulk MOSFET is a matter of great concern for respective practical switching applications. Fig. 1.10(b) shows the plot of energy consumption per cycle verses supply voltage for both TFET and MOSFET having same I_{ON}/I_{OFF} ratio. Form this figure it can be concluded that for low power applications TFET is more advantageous than MOSFET. Thus, to make the TFET as a potential substitute for high speed switching and low power applications, there is a need for attention for improving the ON-current of TFET devices as per ITRS requirement.

1.5 Possible Techniques for Performance Improvements of TFETs

Theoretical principles, experimental studies and TCAD based simulation results show that the low ON-current and ambipolar conduction mechanisms of the TFETs make difficult for inverter-based logic circuit applications [62],[66],[130]. The poor ON-

current of the device reduces the speed of operation of the logic circuits by affecting the charging and discharging times. Experimental [66] and simulation [101] studies show that the TFETs possess higher Miller capacitance than the conventional MOSFETs. The high Miller capacitance, resulted mainly from the high gate-to-drain capacitance (C_{gd}), increases the loading effect significantly thereby enhancing the overshoot and undershoot in the TFETs based inverter circuits. Theoretical [130] and experimental [56] studies show that the drain current due to ambipolar conduction in the TFETs, the overall performance of TFETs based digital logic circuits are getting hampered. In addition, experimental analysis also shows that an asymmetric doping in the TFETs enhances the unidirectional operation and hence lowers the read and write margins of TFET based 6T SRAMs [75],[82]. Researchers have explored a number of different techniques such as gate engineering, source pocket engineering, structural (vertical growing process) engineering, heterojunction engineering with low bandgap source material etc. for improving the ON-current and suppressing the ambipolar conduction in the TFETs. The following subsections have been devoted to introduce some of the important techniques for improving the ON-current with optimizing ambipolar current characteristics of the TFETs.

1.5.1 Gate Engineering Techniques

The gate engineering techniques are basically the modifications in the conventional single gate structure into multi-gate structure for the enhancement of ON-current with minimum ambipolar conduction. There are different gate engineering techniques which

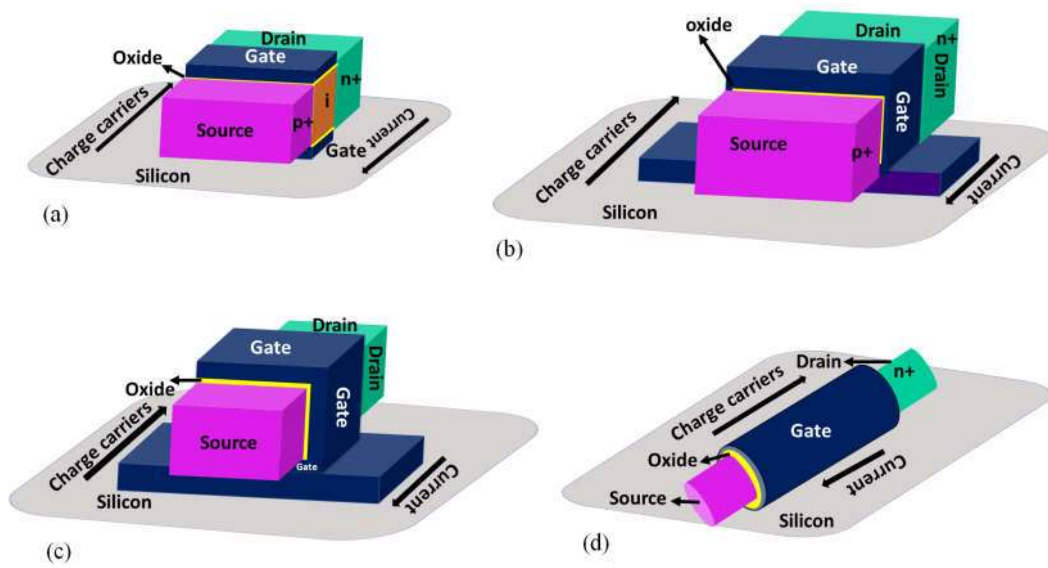

Fig. 1.11: (a) Double Gate TFET Structure (b) Tri-Gate TFET Structure (c) Quadruple Gate TFET Structure and (d) Cylindrical Gate TFET Structure.

may be employed for improving the performance of the TFETs. These multiple-gate engineered structures include double-gate TFET [52],[86], tri-gate TFET [139], quadruple gate TFETs [102], and gate-all-around (GAA)/cylindrical Gate TFETs [81],[99],[141]. Among the above, the double-gate (DG) TFETs and cylindrical TFETs are the most widely explored Tunnel FET structure for future generation IC technology. It can be planar or vertical depending on the way in which different layers of TFETs such as source, drain, and channel grown on substrate [41],[54],[81]. In double gate structure as shown in Fig. 1.11(a), gate controllability over channel region is enhanced which increases ON-current and minimizes the OFF-state current. The tri-gate TFET configuration can be achieved by simply surrounding the channel region along three sides with gate dielectric layer which improves the drive current as depicted in Fig. 1.11(b) [139]. The quadruple-gate TFET structure is shown in Fig.1.11(c) to introduce the gate control from all sides of the channel [102]. Figure 1.11(d) shows the

cylindrical TFET structure [36],[40],[81],[119],[141],[144] in which the gate electrode is wrapped around the channel region to exhibit excellent control of the gate on the tunneling in the device. The cylindrical gate TFET structure is expected to have better scalability with higher ON-current, better I_{ON}/I_{OFF} current ratio and steeper SS over other multi-gate TFET structures [99]. However, the fabrication complexities of such TFET structures is the major limitation for the large-scale IC applications.

1.5.2 Source Pocket Engineering

Source pocket engineered structure in TFET has garnered significant attention in recent time because of its improved sub-threshold performance in terms of steeper subthreshold slope, better ON-current, a reduced threshold voltage and improved reliability [61],[78],[83],[84],[95],[100],[110]. Smaller tunneling distance has been found to be achievable using a highly doped pocket between source and channel region of TFET [61],[78]. The source pocket width along with its doping level control the energy band profile and tunneling barrier width. It is preferred to have narrowest source pocket with sharp doping profile to have higher I_{ON} along with steeper SS [83]. Sometimes a thin freezing layer is grown on source pocket to prevent surface segregation of grown material atoms into single-crystal silicon during subsequent growth using MBE process [83]. The schematic diagram of aforesaid fabricated vertical TFET with a source pocket layer along with a very thin freezing layer is shown in Fig. 1.12(a). In addition, source pocket has been also found to address the reliability properties in terms of improvement in the electric field direction near the tunneling junction, shift in the threshold-voltage induced by dielectric charge, and the threshold voltage variations due to device size fluctuations over conventional p-i-n TFET [84].

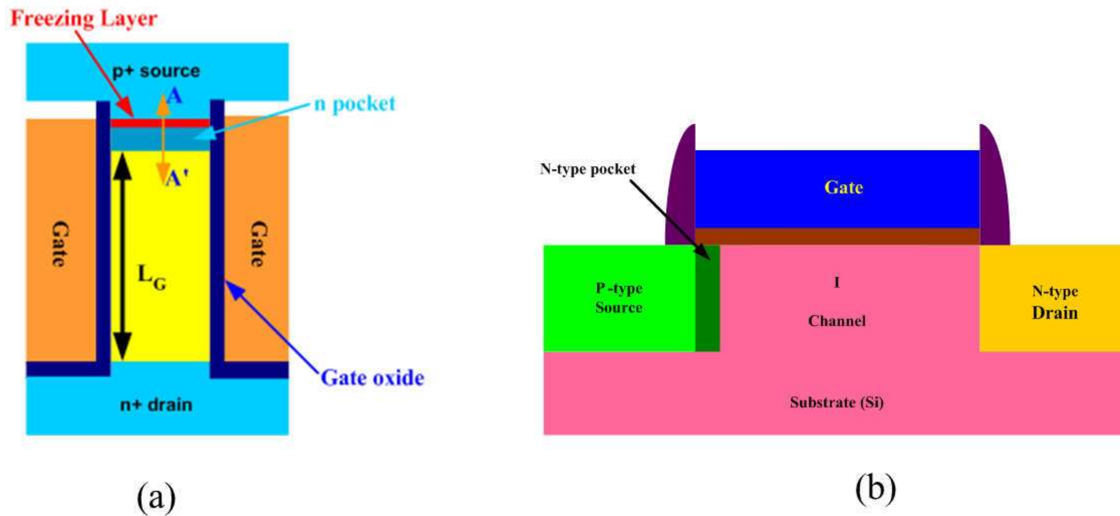

Figure 1.12: Source pocket Engineered tunnel field effect transistor with (a) Vertical process flow technique [83], (b) Lateral process flow technique [78]

Further, it is found that the presence of source pocket reduces interface traps. This in turns improves the reliability of the device by reducing the vertical electric field in the channel [84]. N-type Si TFET with p+ source pocket fabricated using laser annealing method is found to have improved carrier tunneling which in turns enhances I_{ON}/I_{OFF} ratio along with steeper subthreshold swing [95]. The device structure for the same is given in Fig. 1.12(b) which is a lateral TFET. The heavily doped source pocket region improves the performances over the conventional TFETs by forming a local minimum at the edge of the conduction band for zero gate voltage [110]. In addition, the source pocket increases the longitudinal electric field, which in turn, enhances the ON-current of the TFET [61],[110]. Therefore, it is of great interest of many device engineers to grow a thin heavily doped source pocket layer in between source and channel to improve overall performance of TFET.

1.5.3 Vertically Grown TFET Structure

Vertical growth technique in which different layers of a tunnel field effect transistor are grown in a vertical manner using Molecular Beam Epitaxy (MBE) method [32]. For the first time vertical, MOS gated tunneling transistor using silicon as basic material was fabricated [32] where sharp doping profile structure created by means of molecular beam epitaxy (MBE). Clear transistor action due to Esaki tunneling was demonstrated at room temperature where low supply voltage and exponential current increase make this device attractive for ULSI applications [32]. Vertically grown tunnel field–effect transistor (FET) with several striking properties was realized by means of both experimental results as well as 2D computer simulations. The device consists of an MBE-grown vertical p-i-n structure [39],[41]. The main objective of using vertical grown technique is to accommodate a greater number of tunnel transistors in IC to increase the device density so that the functionality of the chip will increase over lateral TFET [65],[81]. Vertically grown TFET has shown improved overall performance over lateral TFET due to very sharp dopant profile [83]. Vertical TFET has also got advantages like providing better electrostatic control of the gate over channel region [81],[105]. A fundamental advantage of the vertical transistor design to realize high quality in-situ doped junctions which enables observation of NDR effects at room temperature and reduction of OFF-state reverse biased p+/i/n+ leakage [74],[136]. Better process control can be achieved for realizing vertical TFETs compared to lateral TFETs [65],[81],[145]. Also, the vertical TFET structure shows better integration density, low leakage current and less trapping related issues [136]. Vertical TFETs can also have the advantage of observing NDR effects at room temperature. A vertical TFET can have either rectangular geometry with a double gate or cylindrical geometry

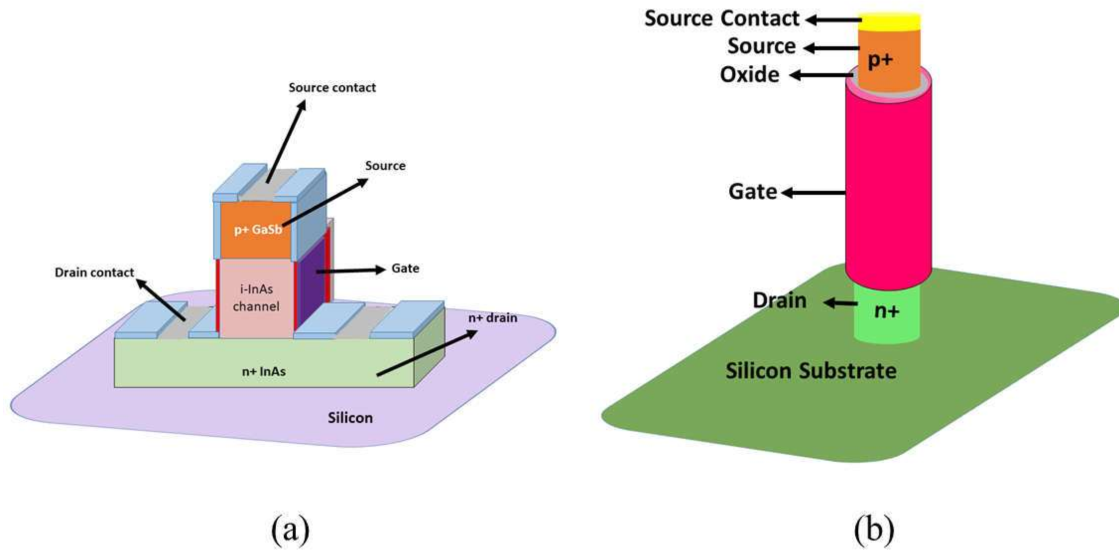

Figure 1.13: Schematic view vertically grown TFET (a) with rectangular geometry [126], and (b) with gate all around or cylindrical geometry [81].

with a gate-all-around architecture [155]. Vertical TFET with rectangular geometry [126] and cylindrical geometry [81] is shown in Fig 1.13 (a) and (b) respectively. Due to all these mentioned advantages vertical TFET can be preferred over lateral TFET.

1.5.4 Band gap Engineering Techniques

In this technique, either a different material with different band gap energy other than Si is used in the TFETs or the Si of one or more of the source, drain and channel regions is/are replaced by another material to enhance the ON-current and minimize the ambipolarity effect. The TFETs using a single material for its source, channel and drain regions are called homojunction based-TFET device. However, when two different materials are used for the source and channel regions of the TFETs, they are called heterojunction based-TFET device. A heterojunction is formed between two different semiconductors or between a semiconductor and a metal (i.e. the Schottky contacts) [7],[8],[10]. Due to difference in energy gap between two semiconductors, many

interesting properties can be derived for different semiconductor-device applications. In addition, difference in the electron affinities of these semiconductors needs to be considered in device applications. This leads to creation of three different combinations of alignment in conduction band energy E_C and valence band energy E_V at the heterojunction interface. Accordingly, three groups of heterojunctions are formed as shown in Fig. 1.14(a) Type I or straddling gap heterojunction, Fig. 1.14(b) Type-II or staggered gap heterojunction, and Fig. 1.14(c) Type-III or broken-gap heterojunction [46]. In a Type-I (straddling gap) heterojunction, one material has both lower energy in conduction band (CB), and higher energy in valence band (VB) than the other material as shown in Fig. 1.14(a). In a Type-II (staggered gap) heterojunction, one material with lower energy in conduction band, and higher energy in valence band is found. Thus, electrons being collected at lower energy in conduction band, and holes being collected at higher energy in valence band, are confined in different spaces. A Type-III (broken-gap) heterojunction is a special case of Type-II where lower energy in conduction band for one material/side is lower than the higher energy in valence band of other material/side. Here the conduction band overlaps with the valence band at the heterojunction interface, hence the name coined for this type of heterojunction is broken gap. The TFETs based on heterojunction is always superior to TFETs made up of homojunctions in terms of higher drive current, better switching performance and lower SS [59],[79],[85],[109],[113],[117],[119],[126],[135],[146],[154],[158] due to the increase in the BTBT probability, resulted from the decrease in the effective energy band gap at the tunnel junction of the device. Out of all these reported articles, Krishnamohan *et al.* [59], Tomika and Fukui [109], Nerves *et. al.* [119], Kato *et al.* [158] have demonstrated the advantages of heterojunction experimentally whereas Cho

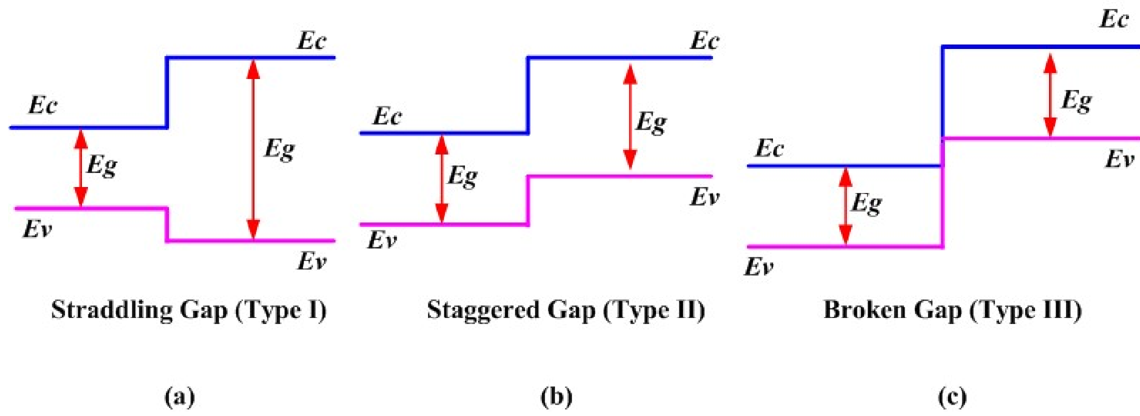

Fig. 1.14: (a) Type-I or straddling gap heterojunction, (b) Type-II or staggered gap heterojunction, and (c) Type-III or broken-gap heterojunction [46].

et al. [79], Smith *et al.* [85], Chander and Baishya [113], Sant and Schenk [117], Sharma *et al.* [126], Kondekar *et al.* [135], Guan *et al.* [146], Wang *et al.* [154] have demonstrated the advantages of heterojunction through TCAD simulations. All the three types of heterojunction discussed earlier like type-I, type-II, and type III have been explored for making heterojunction TFETs. The used materials for the heterojunctions in TFETs along with their band gaps, electron affinities, lattice constants, and effective masses have been listed in Table-1.1.

Sant and Schenk [117] and Cho *et al.* [79] have propounded the advantages of straddling heterojunction based TFETs whereas Krishnamohan *et al.* [59], Tomika and Fukui [109], Lu and Seabaugh [103], Kondekar *et al.* [135], Guan *et al.* [146], Wang *et al.* [154], and Kato *et al.* [158] have enumerated advantages of heterojunction TFETs using staggered heterojunction. Similarly, researchers have also explored broken heterojunction based TFETs where better sub-threshold performances have been observed over homojunction counterpart [85],[126]. Thus, deeper insights into materials

TABLE 1.1

DIFFERENT PARAMETERS OF THE USED MATERIALS FOR HETEROJUNCTIONS IN TFETS

Material used in forming heterojunction in TFETs	Band gap in eV at room temperature	Lattice constant in ^{0}A at room temperature	Electron affinity in eV at room temperature	Effective mass of hole (m_h*) and electron (m_e*)
Si	1.12	5.43	4.05	$m_h^* = 0.24m_o$ $m_e^*=0.20m_o$
Ge	0.67	5.65	4.01	$m_h^* = 0.084m_o$ $m_e^* =0.092m_o$
$In_{0.53}Ga_{0.47}As$	0.74	5.84	4.5	$m_h^* = 0.457m_o$ $m_e^* =0.041m_o$
InAs	0.36	6.05	4.9	$m_h^* = 0.41\ m_o$ $m_e^* =0.023\ m_o$
GaSb	0.7	6.09	4.06	$m_h^* = 0.4m_o$ $m_e^*=0.0410m_o$
InSb	0.17	6.47	4.59	$m_h^* = 0.43\ m_o$ $m_e^* =0.014\ m_o$
InP	1.35	5.8687	4.38	$m_h^* = 0.6\ m_o$ $m_e^* =0.08\ m_o$
GaAsSb	0.7-1.43	5.65-6.09	4.07	$m_h^* = 0.51\ m_o$ $m_e^* =0.063\ m_o$
GaAs	1.43	5.653	4.07	$m_h^* = 0.51\ m_o$ $m_e^* =0.063\ m_o$

engineering techniques may be required to include any combination of heterojunction in TFETs.

The heterojunction in TFET can be made by replacing the source region with a material which is different from channel or drain region. This technique of forming heterojunction with a different source material is known as source material engineering technique which can be used for improving the drive current and subthreshold swing characteristics of the device. In this technique, the source region of the TFET uses a narrow band gap material such as Ge and InAs, InGaAs while keeping Si in channel and drain regions to form a source/channel heterojunction [111],[113]. Although Ge is mostly used in forming heterojunction with Si, III-V materials like InAs, InGaAs, GaSb and InSb can also be used because of its narrower and direct bandgap which leads to more ON-current [100],[129]. The schematic diagram of a low bandgap semiconductors InAs, GaSb, InGaAs, Ge (source)/Si (channel) heterojunction-based DG TFET structure is shown in Fig.1.15(a) whereas compound semiconductor-based heterojunction DG TFET is shown in Fig. 1.15(b). Other source/channel heterojunctions such as GaAs/Ge [135], InGaAs/InP [117], GaSb/InAs [126] and GaAsSb/InGaAs [146] have also been reported in the literature. In general, such type of source material engineering provides better analog/RF performance in addition to improving the ON-current with optimized ambipolar current of the TFETs [59].

The tunneling probability of charge carriers in the TFETs is inversely proportional to energy band gap of the substrate materials [64]. So, it is clear that higher BTBT rate can be achieved by a using narrow band gap material (*e.g.,* Ge, InAs, GaSb etc.) than Si in the TFETs. Figure 1.15 (a) illustrates the systemic picture of a narrow-band gap materials based-DG TFET structure. Although Ge/Si heterojunction TFET has been fab-

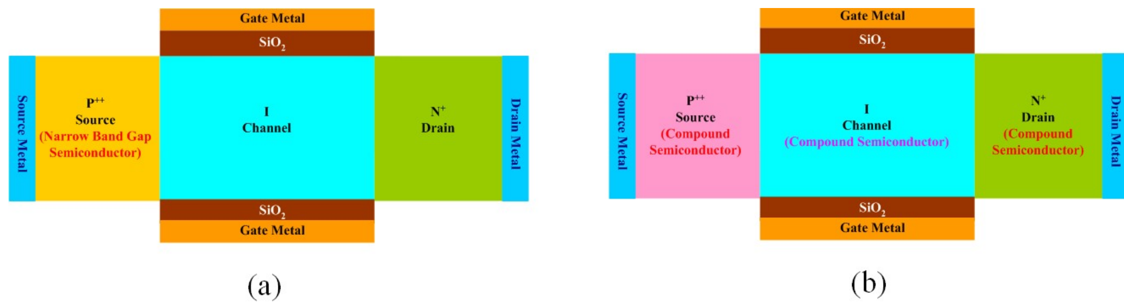

Fig. 1.15: Cross sectional view of heterojunction double gate TFET based on (a) Narrow band gap materials (source) and Si (channel), and (b) compound semiconductor (source)- compound semiconductor (channel).

ricated InAs/Si and GaSb/Si still have some fabrication related issues because of higher mismatching in lattice constant and thermal co-efficient. With the advancement in technology, these problems are going to be resolved in the near future. The fabrication feasibility of GaSb/Si heterojunction is explored in recent time where GaSb is grown on clean Si substrates [134],[147],[156]. The narrow band gap materials in comparison to the Si in the source region of TFETs can provide improved drive current and frequency characteristics to the device [128]. The enhancement in the analog/RF performances in terms of higher transconductance, higher intrinsic gain, higher unity gain cut-off frequency in the band gap engineered TFETs have been reported in the literature [104],[125],[148]. However, the major drawback of such TFETs is its increased OFF-state current in lieu of the improved ON-current and analog/RF performances.

1.5.5 Gate-Dielectric Engineering

In gate-dielectric engineering technique, the conventional SiO_2 is replaced by a high-*k* dielectric for enhancing the scalability of gate oxide thickness [54]. A combination of low-*k* and high-*k* dielectric in the form of either a lateral [70],[92],[99],[112],[142] or a vertical [127],[132] stacked gate-oxide structure can also be explored as shown in Fig.

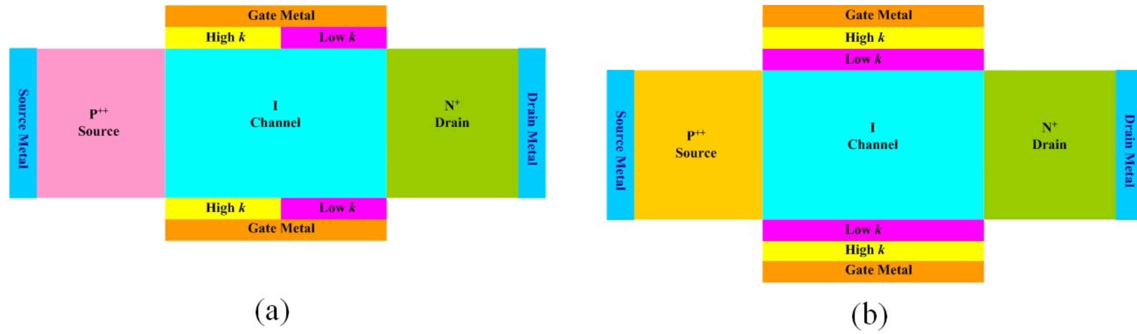

Fig. 1.16: Cross sectional views of Double Gate TFET structure with (a) Lateral Stacked Gate (high-*k*/low-*k*) and (b) Vertical Stacked Gate (low-*k*/high-*k*).

1.16(a) and (b) respectively. In case of lateral gate oxide stacking, gate oxide with higher k value is deposited near to the source and gate oxide with lower k value is deposited near to the drain of the tunnel FET [70],[112]. In lateral gate oxide stacking, gate oxide with higher value of dielectric constant increases ON-current at source side whereas, the gate oxide having lower dielectric constant reduces ambipolar conduction at drain side [92]. In vertically stacked gate structures, the high-*k* is normally placed over the low-*k* to form the effective gate-oxide structure in TFETs [127],[132]. The basic idea behind using a high-*k* gate oxide is to enhance the drive current of the device without disturbing the leakage current [52],[70],[92],[118],[122]. Based on the simulation study, the gate-oxide engineering technique in the form of the heterogeneous gate dielectric double gate (DG) TFET structure is demonstrated to have higher ON-current, steeper SS and smaller ambipolar behavior than the conventional DG TFET structures [70]. TFETs with single gate structure, double gate structure, and gate all around structures with heterogeneous gate dielectric in lateral stacked form have been found to have better DC parameters over conventional TFETs [70],[92],[99],[142]. Narang *et al.* [91] have studied both device and circuit level behavior of different types of gate oxide engineered TFETs with and without source pocket. They have found that

source pocket engineered DG TFET with heterogeneous gate dielectric (HGD) has shown better performance over other presented TFETs. Wang *et al.* [131] have proposed HGD on DG TFET with a source pocket for the enhancement in the ON-current with suppressed ambipolar conduction in the device. Madan and Chaujar [142] have proposed lateral gate dielectric stacked TFET with gate all around structure where they have conducted reliability study by varying the temperature from 200 K to 500 K which shows DC and RF parameters are less sensitive to temperature for the HGD based gate all around (GAA) TFET over GAA TFET without HGD structure. Moreover, HGD TFETs are found to have better performance characteristics over TFET without HGD.

1.6 Circuit Level Performance using TFETs

TFET with a gate-controlled tunnel junction at the source is of great interest for the replacement of MOSFET. The reverse biased tunnel junction in the former device avoids the high-energy tail of the Fermi distribution of valence band electrons in the source region which allows for abrupt turn-on near the OFF-state. Although TFET has established itself as a potential candidate to replace MOSFET for low power applications; asymmetric source and drain region-doping leads to considerably different I-V and C-V characteristics over MOSFET impeding circuit level performance. The major issues in TFET such as lower ON-current than MOSFETs [51], ambipolar conduction which affects OFF-state performance [108], super linear onset along with high saturation voltage of device output characteristics [88],[116] as shown in Fig. 1.17 where a comparison of output characteristics is made for both TFET and MOSFET. Miller effects associated with the typically high gate–drain capacitances in TFET are

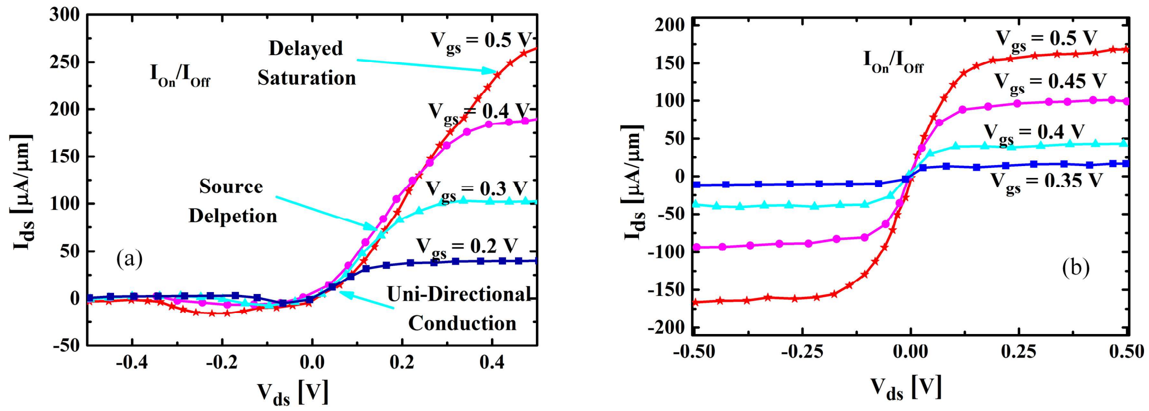

Fig. 1.17: Comparison of output characteristics for (a) TFET, and (b) MOSFET [82].

mostly responsible for delayed saturation characteristics [66],[68]. Heterostructures TFETs with staggered or broken energy band alignment can be adhered to enhance the ON-current, whereas optimization of the device geometry and doping levels should be carefully done to improve output performance. Keeping all these aspects in mind, a deeper insights into circuit-level performance study of TFET is as important as device-level performance study. Flude *et al.* [57] for the first time implemented circuit-level analysis of complementary multi gate TFET where they have implemented a voltage reference circuit. They have found that multi gate TFET can be potential candidate for circuit level applications. Kam *et al.* [58] designed nanoscale relays for the first time using both MOSFET and TFET where they have found that relays using TFET is much more energy efficient than that of the relays designed with MOSFET.

Kim *et al.* (2009) [67] and Mookerjea et al (2009) [66] have studied the effects of capacitance between gate and drain, which is termed as the Miller capacitance for TFET. Unlike MOSFET, TFET does possess higher gate to drain capacitance (C_{gd}) which significantly affects loading. Fig. 1.18 shows a comparison plot of C-V characteristics for both TFET and MOSFET where C_{gd} for TFET is comparatively high

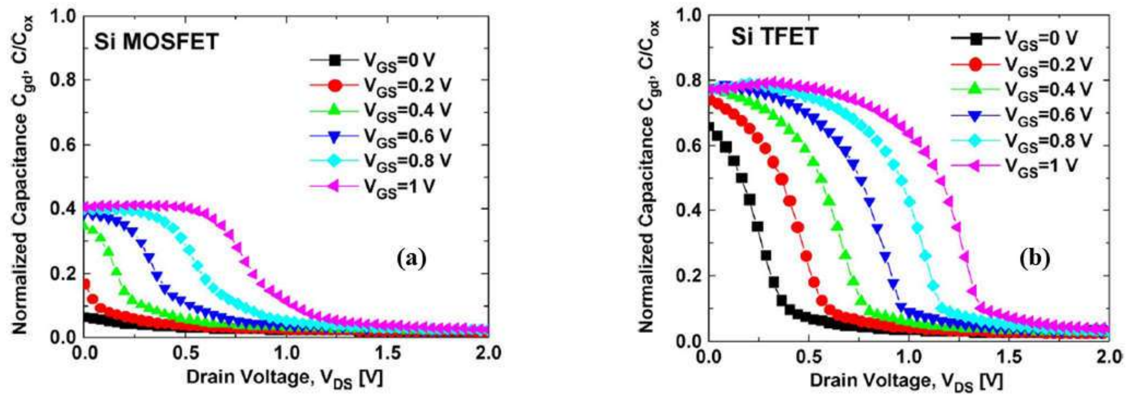

Fig. 1.18: Comparison between normalized gate to drain capacitance (C_{gd}) with different gate to source bias (V_{gs}) of a silicon (Si) material based (a) MOSFET, and (b) TFET. Copyright @ 2009, IEEE [66].

than MOSFET, which is causing loading effect. Due to higher C_{gd} in TFET, overshoots and undershoots during voltage transitions can be realized due to capacitive coupling between input and output of the gate as shown in Fig. 1.19(a) which results in additional capacitive loading. Their study shows that TFET has much higher Miller capacitance almost double the amount than the MOSFET as shown in Fig. 1.19(a). This higher Miller capacitance in TFET results from the linking of the inversion layer in TFET to the drain region rather than the source region unlike MOSFET. First time an in-depth performance comparison between TFETs and conventional MOSFETs considering carbon nanotube as material was carried out by Koswatta *et al.* [63] at Purdue University. TFETs despite having lower ON-current were found to have smaller switching energy than conventional MOSFETs, and could switch faster at higher Ion/Ioff ratios than MOSFETs. The impact of larger Miller capacitance in TFETs is evaluated at a supply voltage of 0.5 volt in terms of average overshoot and undershoot and compared to that of MOSFET in commercial 45nm CMOS technologies as shown in Fig 1.19(b). They have found out that although TFET has higher Miller capacitance,

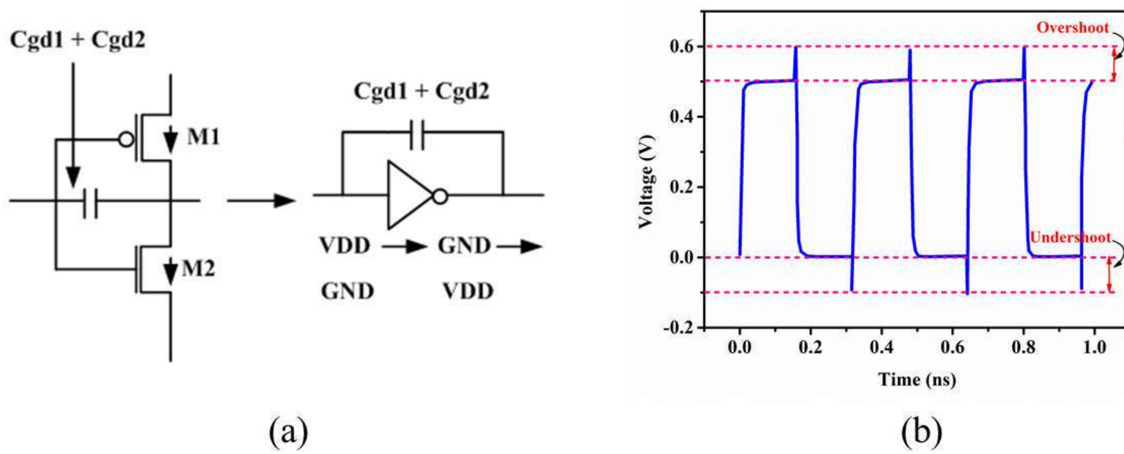

Fig. 1.19: (a) Enhanced capacitive loading in TFET because of two times increase in Miller capacitance; and (b) Overshoot and undershoot caused due to capacitive loading [101].

it does not have significant impact on circuit level performance. The asymmetric current flow of TFET, places restrictions on the use of pass-gate and transmission-gate as bidirectional current conduction is not possible. Although this limitation is not severe for many logic circuits based on TFET, it poses another significant problem for the standard 6T SRAM as shown in Fig. 1.20 where mostly pass gates based on TFET are used for access transistors (both inward access TFET as shown in Fig. 1.20 (a) and outward access TFET as shown in Fig. 1.20 (b)). Zhuge *et al.* (2011) [80] have demonstrated the use of short-gate heterostructure in TFET can significantly lower the gate to drain capacitance and it is most favorable for low power and energy efficient digital applications. In addition, they have observed low delay and low energy consumption especially with supply voltage scaling in heterojunction TFETs. Mookerjea *et al.* (2009) [68] for the first time demonstrated a novel 6T TFET SRAM cell using virtual ground assist which can work properly irrespective of asymmetric source/drain configuration of TFETs. The low read and write margin in outward and inward accessed transistor based 6T SRAM can be vanquished by using the novel trans-

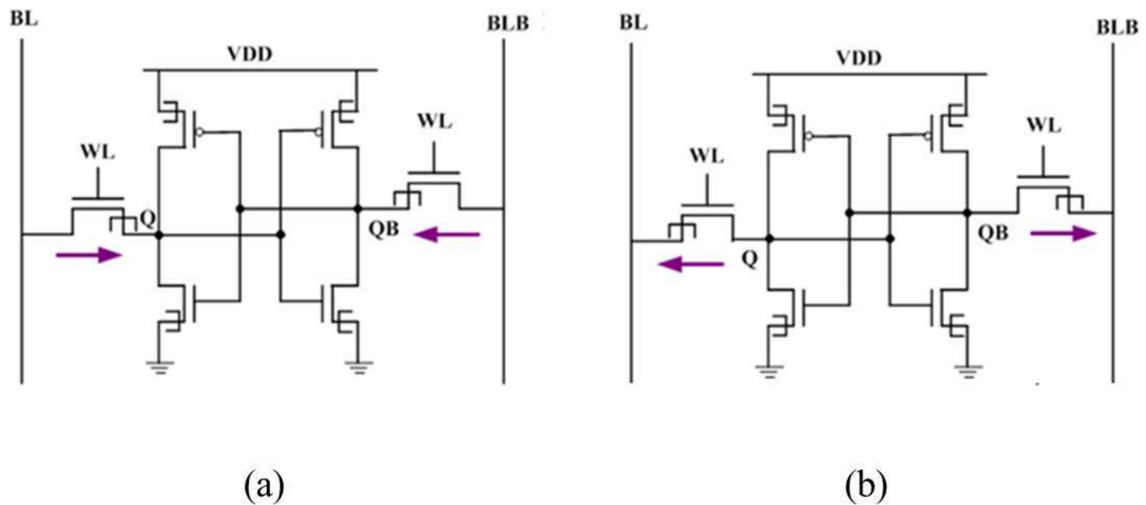

Fig. 1.20: Schematic of 6T SRAM designed with TFETs having (a) inward access transistors (I-6T), and (b) outward access transistors (O-6T).

-istor technique consisting of virtual ground. Strangio *et al.* (2015) [115] have analyzed the impact of unidirectional current conduction and ambipolarity on 6T SRAM performance based on TFET. They have found 6T SRAM configuration with outward ATs could achieve both acceptable read and write SNMs with higher delays. There are different methods used by different researchers to have better read and write ability of 6T SRAM based on TFETs [68],[75],[82],[98],[150],[151] 8T SRAM based on TFET can be a suitable candidate for better read and write noise margin with low read and write delays.

Due to unavailability of accurate compact models for tunnel field effect transistors, the circuit level analysis of TFET is mostly carried out by the use of look-up table-based models in Verilog-A followed simulation using the Cadence Virtuoso tool or HSPICE tool [106],[107],[157]. For complementary TFETs, the p-type characteristics are considered mirror images of n-type TFETs current characteristics [107]. Due to their sub-60 mV/decade operation, TFETs are promising candidates to replace MOSFET for

low-power circuit operations. Many researchers have compared the TFET based inverter performance with the MOSFET and have found increased noise margins and better speed operation in the TFETs with respect to CMOS technology [101],[108]. The tunnel-field effect transistors have also shown to have improved circuit performance in both analog and digital circuit domain for low-voltage applications [143],[152].

1.7 Review of Some State-of-the-Art Research Works on TFETs

After discussing various techniques explored for the performance improvements of the TFET, the following subsections will review some state-of-the-art research on TFETs. Important experimental, theoretical and TCAD simulation results on TFET devices have been discussed first. Finally, some important literatures on circuit level applications of the TFETs have been reviewed.

1.7.1 Review of Some Experimental Research works on TFETs

The first TFET as a gated p-i-n diode structure was fabricated by Quinn *et al.* [16] at the Brown University in 1978. In this direction, Toshio Baba [21] fabricated the surface tunnel transistors (STT) by using molecular beam epitaxy (MBE) technique to mesa structures. At the Cambridge University, Reddick and Amaratungaa [25] performed an experimental study of silicon surface tunnel transistor (STT) working on the principle of band-to-band tunneling phenomenon. The proposed STT device was reported to have no punch-through related limitations and hence was considered as improved version of the existing FETs. The STT has been used as high-frequency gate-controlled detectors and oscillators in conventional Si integrated circuit. Kogaa and Toriumi [27] experimentally demonstrated the working of a three-terminal Si tunneling device showing negative differential conductance with its drive current mostly controlled by the applied gate

bias.

Hansch *et al.* [32] fabricated a vertical Esaki tunneling transistor for the first time to illustrate the saturation behavior of the transfer characteristics of the device. Aydin *et al.* [38] fabricated a lateral inter-band tunneling transistor on a SOI substrate using heavily doped source and drain regions. Appenzeller *et al.* [36] fabricated a carbon nanotube based TFET with a dual gate (*i.e.,* a back and top gate) structure and demonstrated that the band-to-band tunneling (BTBT) of the charge carriers from the valence band of the source into the conduction band of the channel could be enabled or disabled by changing the applied gate bias of the device. Bhuwalka *et al.* [39] of German Federal Armed Forces University fabricated a vertical Si-TFET with a SiGe delta layer at the source junction grown by MBE technique. They demonstrated that the use of SiGe delta layer in the device could improve the ON-current of the device drastically. They have also reported the I-V characteristics of n-channel and p-channel devices. In an another work, Bhuwalka *et al.* [41] found exponential input characteristics, perfect saturation in the output characteristics, and low OFF-state current in the order of 1 fA/m for sub-100 nm channel lengths for the vertical TFETs. The used a p+ SiGe layer at the p-source end to show improvements in the ON-current, threshold voltage and subthreshold swing characteristics. However, the OFF-state current was increased with increase in the Ge content. Importantly, they also observed that the performance parameters of the TFETs are nearly independent of the channel length scaling. Choi *et al.* [53] reported a subthreshold swing (SS) below 60 mV/dec in the TFETs for the first time. They measured the SS of nearly 58.5 mV/dec.

Based on the experimental as well as theoretical investigations, Nagavarapu *et al.* [61]

observed that the SOI-based PNPN TFET structures possess higher ON-current, I_{ON}/I_{OFF} current ratio, and smaller SS over the conventional SOI-TFET structures. Krishnamohan *et al.* [58] have experimentally demonstrated a record high ON current in the order of ~ 300μA/μm with a low SS in the order of ~50mV/dec in the stained-Ge based DG TFET structures. They [58] have also illustrated that the lateral heterostructure is the most effective approach to reduce the ambipolar conduction in the TFETs. Nagavarapu et al. [61] have implemented source pocket for the first time with steeper SS and improved I_{ON} in a n-TFET and the configuration was P-N-P-N TFET.

Mookerjea *et al.* [68] have investigated the transfer characteristics of vertical $In_{0.53}Ga_{0.47}As$ TFETs with high-k gate-oxides like Al_2O_3. They have suggested that Al_2O_3 may have compatibility in conventional CMOS technology. Gandhi *et al.* [81] have fabricated a CMOS-compatible vertical gate-all-around TFET structure and observed a very low SS of 30 mV/decade at room temperature. Tura *et al.* [83] have fabricated a TFET with a pocket by molecular beam epitaxy (MBE) technique. They have measured a 30% lower SS and 3-times higher I_{ON} over the conventional TFETs.

A III-V material based TFET employing a thin gate oxide, heterojunction engineering and high source doping was reported by Dewey *et al.* [87]. They observed a steeper SS in the heterojunction TFET than that of the homojunction counterpart. Riel *et al.* [96] experimentally analyzed the performance of a vertically grown InAs–Si heterojunction TFET with gate-all-around architecture and high-k gate oxide and observed the SS of 150 mV/dec. The performance of a Ge/Si heterojunction TFET was invested experimentally by Rooyackers *et al.* [105] using a novel source replacement approach which is used to prevent the gate-dielectric from damage during the fabrication process

flow. Memisevic *et al.* [145] fabricated a vertical InAs/InGaAsSb/GaSb nanowire TFET with channel diameter scaled down to10 nm and observed the point SS of 35 mV/decade at V_{DS} =0.05V.

1.7.2 Review of Some Simulations and Modelling works on TFETs

The concept of Zener tunneling was first analytically modelled for the tunnel diodes by Kane *et al*. [4] using the WKB approximation method. Banerjee *et al*. [19] reported a closed-form analytical model for the drive current of three-terminal tunnel device by using a p-region instead of an *i*-region under the gate. An analytical model for the threshold voltage of TFETs was proposed by Zhang *et al.* [43]. Boucart and Ionescu [51] simulated a DG TFET for the first time to demonstrate its better performance over the single gate TFET device. In another work, Boucart and Ionescu [52] have demonstrated better scalability of the DG TFETs with a high-*k* gate oxide over the DG TFET with conventional SiO_2 as gate oxide. The transconductance method is used to propose a new definition for the threshold voltage in TFETs by Boucart and Ionescu [52]. Koswatta *et al.* [63] have reported a smaller quantum capacitance in CNTs channel based TFETs over conventional MOSFETs. The fringing field effects in high-*k* dielectric oxide based TFETs have been shown to achieve higher ON-current and a steeper SS below the Boltzmann limit of 60 mV/decade over the conventional MOS devices.

The gate capacitance characteristic in TFETs was investigated by Yang *et al.* [71] using TCAD simulation method. Choi *et al.* [70] have proposed a hetero-gate-dielectric TFET structure obtained by using a high-k material at the source side and a low-k dielectric at the drain side to enhance the ON-current and suppress the ambipolar conduction in the

device. Abdi *et al.* [110] have demonstrated the merits of the source-pocket engineered TFETs over the conventional TFETs. The use of a source pocket is shown to increase the longitudinal electric field enhance the ON-current of the TFET. The device is also shown to have better the reliability over the conventional TFETs without a pocket.

Liu *et al.* [133] have reported a theoretical performance analysis of a strain-engineered Ge/$In_xGa_{1-x}As$ staggered heterojunction TFET. where the theoretical performances have been evaluated. Higher ON-current and smaller SS in both n- and p-channel Ge/$In_xGa_{1-x}As$ TFETs have been reported as compared to those of strain-engineered Ge homojunction TFETs. Sharma *et al.* [126] have used 2-D ballistic simulations using self-consistently coupled nonequilibrium Green's function-Poisson approach to analyze the performance of sub-10-nm n-/p-type GaSb–InAs double-gate vertical TFETs. A 2-D analytical model for different electrical parameters of a DG TFET with vertical gate stacking of SiO2/HfO2 was proposed by Kumar *et al.* [127] to demonstrate the improvement of ON-current by using SiO2/high-k vertical gate stacking technique. Kurniawan *et al.* [136] have compared the performances of a 10 nm gate-length based nanowire Ge-Si heterojunction TFET with the Si TFETs by including quantum effects. Convertino *et al.* [149] have investigated the performances of InAs/GaSb heterostructure based conventional TFETs and vertical TFETs including defects at the heterojunction interface and oxide-channel traps.

Based on the literature reviews discussed above, the following vertical TFETs (VTFETs) structures including the source pocket engineering, gate engineering, gate oxide engineering, bandgap engineering are expected to provide the flexibility in the performance optimization of the TFETs.

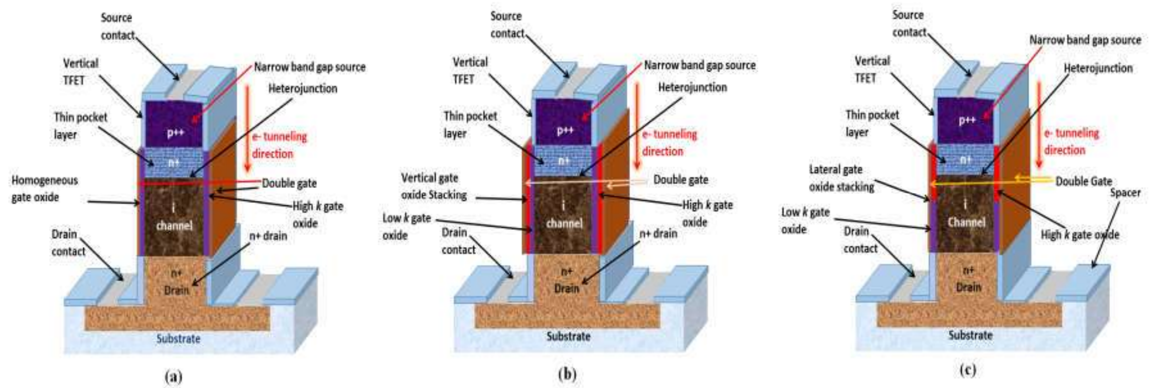

Fig. 1.21: (a) Homogeneous gate oxide VTFET, (b) Vertical gate oxide stacked VTFET, (c) Lateral gate oxide stacked VTFET based on the literature review.

1.7.3 Review of Some TFETs Based Circuits

Application aspects of complementary Multiple-Gate TFETs along with fabrication was first demonstrated by Fulde et al. [57]. They analyzed both digital and analog device performance for the first time. Circuit-level metrics were analyzed for TFET by Kam et al. [58] where TFET technology appeared to be compelling for sub100MHz applications. They have found that for applications below 500 MHz, TFETs are more energy-efficient than conventional MOSFETs.

Koswatta *et al.* [63] at Purdue University made extensive studies on performance comparison between TFETs and conventional MOSFETs where carbon nanotube was used as the basic material for device fabrication. They observed TFET had smaller switching energy than conventional MOSFETs in spite of having lower ON-current in the former structure. Thus, TFETs can be applicable for faster switching applications over MOSFETs.

Miller capacitance effects were analyzed for TFET based circuit by Kim *et al.* [67] and

Power consumption was shown to be very less for TFETs over MOSFETs. They have compared the TFET based ring oscillator with CMOS ring oscillator by the use of look-up table (LUT) based model. Same value of the oscillation frequency was obtained at lower supply voltage in TFETs as compared to CMOS technology. They have also reported an SRAM cell based on heterojunction TFETs which showed leakage current reduction in comparison with conventional CMOS devices. Mixed-mode device and circuit simulation were analyzed for delay estimation of unloaded TFET inverters by Mookerjea *et al.* [66] were the first to observe enhanced value of C_{gd} in TFETs. They found out that the gate capacitance C_{gg} in TFET is dominated by C_{gd} as compared to C_{gs}. They have observed that the effective load capacitance for TFET-based unloaded inverters is double the amount of the gate capacitance. The increased parasitic capacitances were attributed to increased delay in TFETs circuits. They have explained the procedure to extract effective ON-current and output capacitance for TFET delay calculations.

Simulation of TFET for low-power digital applications with a lower supply voltage (<0.5 V) were reported by Zhuge1 *et al.* [80] where they have found out that better energy delay product can be achieved in the heterostructure TFET compared to MOSFET.

Saripalli *et al.* [82] presented the effect of various parameters on different SRAM configurations like 6T, 8T and Schmitt trigger based 10T cells based on complementary-TFETs and CMOS. The TFETs show considerable improvement in energy requirements and power dissipation. Chen *et al.* [98] presented a detailed analysis of TFET circuit switching performance and the physics behind it. The performance of several TFET SRAM cells are analyzed using atomistic technology

computer aided design mixed-mode simulations. They have also used the source pocket in their TFET to analyze the effect of source pocket on circuit-level performance especially in SRAM. In addition, they have proposed a 7T-SRAM cell using an extra read transistor to increase the RSNM of the SRAM cell by eliminating read disturb of the storage node. Presented analysis of TFET SRAM performance using source pocket shows 7T DL TFET SRAM has better performance over other SRAM configurations.

Baravelli *et al.* [108] found out that cointegrating optimized n- and p-type TFETs to make CMOS circuits is a major challenge associated with the TFET architecture in addition to other challenges like reaching acceptable I_{ON}, suppressing ambipolar conduction affecting the OFF-state performance, super-linear onset and high saturation voltage of TFET output characteristics, reducing Miller effects associated with the typically high gate–drain capacitance C_{gd} which influences its overall circuit performance. They [108] have observed that the use of heterojunctions with staggered or broken gap can be used to boost the ON-current whereas careful optimization of the device geometry, doping levels, and gate oxide stacking is required to improve output performance of the circuits based on TFETs. Morris *et al.* [107] have investigated tunnel field-effect transistor (TFET) in digital circuits applications where they have found that TFET is a suitable candidate for energy efficient logic operation at low voltage because of its steep SS and performed 4 times better than MOSFET at a 400-mV supply voltage. In addition, they have found that presented TFET's asymmetric conduction can be the cause of potential circuit failures.

Strangio *et al.* [115] have presented mixed device-circuit simulations to predict the performance of 6T SRAM configuration with outward access transistors (Ats) and

concluded both acceptable read and write SNMs with higher delays can be achieved for their proposed SRAM. They have also analyzed the impact of TFET ambipolarity on SRAM operation. Strangio *et al.* [152] proposed the use of outward-6T SRAM cell by using bit lines pre-charge to half of the supply voltage to improve the read delays and RSNM of the SRAM. Ahmad *et al.* [151] have reported a 7T based SRAM cell employing bit-line collapse to improve the circuit level performance of the SRAM cell in terms of RSNM, WSNM read delays and write delays. Improved parameters were reported for the Dual-gate TFET (DGTFET) as compared to the conventional TFET.

Strangio *et al.* [152] have made TCAD simulations-based circuit-level performance study of TFET of basic digital circuits, analog circuits, and mixed-signal circuits for ultra-low power application. Nogueiral *et al.* [157] studied the silicon nanowire based TFET performance for analog-based circuit applications. The proposed device reported 20 dB higher voltage gain and almost three order of magnitude smaller power consumption than the CMOS counterpart.

Several studies have also been carried out by different researchers for employing TFETs in different logic circuits like inverter, memory organizations etc. of which SRAM is an integral part. Various configurations of SRAMs have been proposed to improve the SRAM operation.

Based on the above circuit-level applications of TFET related literature survey, the following table (Table-1.1) has been added which summarizes some reported articles based on device and circuit-level implementation of TFETs where the materials considered for designing TFET along with the approaches for circuit-level simulations have been listed.

TABLE 1.2

TFETS BASED CIRCUIT LEVEL SIMULATIONS

Ref. no. & Year	Title	Highlights	Approach	Material used in TFET
[57] 2008	Fabrication, Optimization and Application of Complementary Multiple-Gate Tunneling FET	➢ Fabrication, optimization and application aspects of complementary Multiple-Gate Tunneling FETs had been discussed. ➢ Digital and analog device performance was analyzed for the first time.	Fabrication along with **mixed mode simulation** were done using Sentaurus TCAD tool	**Si** (silicon)
[66] 2009	Effective Capacitance and Drive Current for Tunnel FET (TFET) CV/I Estimation	➢ Device and circuit simulation were analyzed for delay estimation of unloaded TFET inverters ➢ Effective load capacitance for TFET-based unloaded inverters can be more than twice the gate capacitance	**Mixed-mode simulation** using Sentauras TCAD tool	**InAs** (Indium Arsenide)
[67] 2009	Low Power Circuit Design Based on Heterojunction Tunneling Transistors	➢ Miller capacitance effects were analyzed on circuit level behavior of TFETs and MOSFETs.	**Look-up table-based method** using Verilog-A	**Si and SiGe**

	(HETTs)	➢ Power consumption was shown to be very less for TFETs over MOSFETs.		
[82] **2011**	Variation-Tolerant Ultra Low-Power Heterojunction Tunnel FET SRAM Design	➢ Presented 8T and 10T TFET SRAM cells, including Schmitt-Trigger (ST) based cells. ➢ Uni-directional conduction due to TFET asymmetric source-drain architecture, and their delayed output saturation characteristics impact were analyzed in SRAM performance.	**Look-up table-based method**	**GaSb** and **InAs**
[98] **2013**	Design and Analysis of Robust Tunneling FET SRAM	➢ Presented analysis of TFET SRAM performance using source pocket ➢ 7T DL TFET SRAM shows better SRAM performance compared to other SRAMs.	**Mixed mode simulations** using Sentaurus TCAD tool	**Si**
[107] **2014**	Design of Low Voltage Tunneling-FET Logic Circuits Considering Asymmetric	➢ Presented TFETs asymmetric conduction can be the cause of potential circuit failures	**Look-up table-based method** using Cadence as circuit	**GaSb and InAs**

	Conduction Characteristics	➢ TFET circuit performance is 4X better than the MOSFET.	simulator	
[115] 2015	Impact of TFET Unidirectionality and Ambipolarity on the Performance of 6T SRAM Cell	➢ Presented mixed device-circuit simulations to predict the performance of 6T static RAM ➢ 6T SRAM configuration with outward ATs could achieve both acceptable read and write SNMs with higher delays	**Mixed-mode simulation** using Sentaurus TCAD tool	**Si and SiGe**
[143] 2017	Understanding the Potential and Limitations of Tunnel FETs for Low-Voltage Analog/Mixed-Signal Circuits	➢ Presented analog/mixed-signal performance evaluation at device and circuit levels for a III-V nanowire TFET ➢ TFETs circuit-level figures of merit outperform FINFETs.	**Look-up table-based method** using Sentaurus as device simulator and Cadence as circuit simulator	**InAs** and **AlGaSb**

From the above table, it may be concluded that the look-up table based modeling has gained more attention because of its fast turnaround time along with a very good accuracy for generating compact models, either from different TCAD tools or from the experimental data.

1.8 Summary of the Literature Review: Motivation behind the Present Thesis

We have already reviewed some important state-of-the-art research works related to performance analysis of various TFETs structures obtained by employing multi-gate engineering (double-gate, tri-gate, quadruple gate, cylindrical gate), source pocket engineering, vertical architecture, gate-oxide engineering (high-*k* dielectric, vertical or lateral low-k/high-*k* stacked oxide etc.), and heterojunction architectures with source material engineering (*i.e.,* use of a low band gap material in the source region). Review of some important literatures on some circuit level applications of TFETs has also been considered. The major observations of the literature survey may be outlined in the following-

- As compared to the conventional lateral TFETs, the vertical TFET structures are better suitable for increasing the transistor density in the ICs [65],[81]. The vertical TFETs also have low leakage current and less trapping related issues [136].
- The vertical TFETs with in-situ doped junctions are realized using MBE process enable us to observe NDR effects at room temperature along with reduction of off-state reverse biased p+/i/n+ leakage [68],[74]. Due to comparatively easier fabrication, the vertical TFETs are also preferred over the lateral structure of TFET [65],[81],[145].
- The vertically grown TFETs have better overall performance over the lateral TFET structures [83]. They have better electrostatic control of the gate over channel region [81,[105] as compared to the lateral TFET structures.

- Source pocket engineered TFET structure [61],[78],[83],[95],[100],[110] has better sub-threshold performance in terms of steep subthreshold slope, higher ON-current, smaller tunneling voltage drop and better reliability over the conventional TFETs without any source pocket. Smaller tunneling length can be achieved by using a highly doped pocket between the source and the channel region of TFET [61],[78]. The source pocket also improves the reliability properties in terms of improvement in the direction of the electric field near the tunneling junction, the threshold-voltage shift induced by dielectric charge, and the variation of the threshold voltage due to device size fluctuations over conventional p-i-n TFET [79]. Further, it reduces interface traps and hence improves the reliability of the device by reducing the vertical electric field in the channel [84].
- The heterojunction TFET structure [4],[17] may provide better flexibility for improving the electrical characteristics such as reduction in ambipolar conduction, higher drive current, higher I_{ON}/I_{OFF} ratio and lower subthreshold swing [59],[79],[85],[103],[109],[113],[126],[135],[146],[154],[158] over the conventional homojunction TFETs. As compared to the conventional TFETs, the heterojunction TFET devices have (i) larger tunneling probability of charge carriers from the valence band of the source to the conduction band of the channel due to lowering of tunneling barrier width owing to the decreased energy band gap of the source [59][83] and (ii) reduced ambipolar conduction current due to lower electric field at the drain/channel junction [59],[67].
- All the three types of heterojunctions namely straddling heterojunction [79],[117], staggered heterojunction[59],[103],[109],[135],[146],[154],[158] and

broken heterojunction [85],[126] based TFETs have better sub-threshold performances over the homojunction TFETs.

- Low bandgap materials such as Ge and InAs and InGaAs, InSb as source material and Si for both the channel and drain regions of the TFETs are used to improve the ON-current of the device [111],[113],[129].
- Gate-oxide engineered TFETs with vertical/lateral gate stacking (high-*k*/low-*k*) structures [70],[97],[99],[112],[127],[132],[142] have larger ON-current, better transconductance, reduced ambipolar current and lower SS characteristics over the conventional TFETs due to the decreased tunneling barrier width of the device.
- The TFETs with a gate-controlled tunnel junction at the source has garnered attention for the low-power IC applications. However, asymmetric doping in the source and drain leads to different I-V and C-V characteristics which create some difficulties for circuit-level applications. The lower ON-current [51], ambipolar conduction [108], super linear onset along with high saturation voltage of device output characteristics [88], and larger Miller effects associated with the typically high gate to drain capacitances [66],[101] may severely affect the performance of TFET based circuits. Higher gate to drain capacitance (C_{gd}) increases the Miller capacitance loading effects, which causes overshoots and undershoots during voltage transitions in the TFET based circuits. The asymmetric current flow of TFETs due to ambipolar conduction places restrictions on the use of pass-gate and transmission-gate. Although this effect does not hamper many TFET based logic circuits, however, the TFET based 6T SRAMs using pass gates as access transistors to determine read and write

margins face some significant problems. However, the heterojunction TFETs with staggered or broken energy band alignment can be explored for optimization of their performance.

It is observed that there are ample opportunities for investigating the performance characteristics of some source pocket engineered vertical/lateral gate-oxide stacked hetero-junction vertical TFETs. The source material with lower bandgap can be adopted to significantly improve ON-current. The vertical structure with a thin heavily doped source pocket along with different gate oxide engineering could be of great interest to the researchers working in the device and circuit level simulation of advanced TFETs for next generation CMOS technology for ultra-low power applications. Based on the above observations from the literature, we will now define the scopes of the present thesis in the following section.

1.9 Scopes of the Thesis

The basic objective of this thesis is to carry out TCAD simulation based device and circuit-level performance investigations of some source pocket engineered and gate-oxide engineered heterojunction TFETs based on vertically grown technique due to its ease of fabrication, negligible trapping related issues, less leakage current from the buffer layer, and less difficulty in forming wrap-gated architectures as discussed earlier. The source pocket is a thin layer of heavily doped material sandwiched between source and the channel region of TFET is used to enhance the drive current, reduce sub-threshold swing and ambipolar conduction current, and to improve the RF performance of the device. Vertical/lateral stacked gate-oxide structure of Al_2O_3 and HfO_2 have been explored to improve the various performance parameters of both the homojunction and

heterojunction vertical source pocket engineered TFETs. The effects of source pocket and gate-oxide engineering are shown to improve the I_{ON}/I_{OFF} ratio, subthreshold swing characteristics and RF figures of merit of the GaSb/Si heterojunction vertical TFET structures. Finally, circuit level applications of the source pocket engineered GaSb/Si heterojunction vertical TFETs in the digital inverter and 8T SRAM circuits have been discussed. The entire thesis has been presented in SIX Chapters including the present one. The contents of the remaining FIVE chapters of the thesis are outlined as follows:

Chapter-2 investigates the DC and RF performance of GaSb/Si heterojunction vertical TFETs with and without source pocket engineering. The SILVACO ATLAS^{TM} 2D/3D Device Simulator has been used in the present study. The possibility of GaSb for the source region material to enhance carrier tunneling through the source (GaSb)-channel (Si) interface has been analyzed for the first time. The effects of temperature on sub-threshold swing (SS) and I_{ON}/I_{OFF} ratio are investigated for the proposed heterojunction vertical TFETs. Different analog/RF figures of merit (FOMs) such as transconductance (g_m), output conductance (g_d), gate to drain capacitance (C_{gd}), gate to source capacitance (C_{gs}), cut-off frequency (f_T), gain bandwidth product (GBP), maximum frequency (f_{max}), transit time (τ), transconductance generation factor (TGF) and transconductance frequency product (TFP) are also analyzed for the GaSb/Si heterojunction vertical TFETs with and without source pocket. Device-level performance parameters of the proposed vertical TFETs have been compared with some recently reported TFETs. The performance characteristics of the proposed source pocket engineered GaSb/Si heterojunction vertical TFET (SPE GaSb/Si HJ VTFET) have been compared with an all-Si source pocket engineered vertical TFET (SPE All-Si VTFET). The effects of temperature on the sub-threshold swing (SS) and I_{ON}/I_{OFF} ratio of the proposed TFETs

have been thoroughly investigated and compared with the SPE All-Si VTFET. Different analog/RF parameters are also extensively studied for both the TFETs.

Chapter-3 presents the impact of vertical and lateral HfO_2/Al_2O_3 gate-oxide stacking on the device-level performance of the source pocket engineered vertical GaSb/Si heterojunction TFET (SPE GaSb/Si HJ VTFET) considered in Chapter-2. In the vertical gate-oxide stacking, the high-*k* (HfO_2) is placed over the low-*k* (Al_2O_3) to form the effective gate-oxide structure of the proposed TFET. On the other hand, the high-*k* (HfO_2) oxide is placed near the source side and the low-*k* (Al_2O_3) oxide near the drain side in a cascaded manner to form the resultant gate-oxide structure of the proposed device. The effect of later/vertical HfO_2/Al_2O_3 on the sub-threshold swing (SS), I_{ON}/I_{OFF} ratio along, intrinsic capacitances and analog/RF figures of merit (FOMs) such as transconductance, output conductance, cut-off frequency, gain bandwidth product, transconductance generation factor (device efficiency), and transconductance frequency product have also been analyzed for the proposed gate-oxide and SPE GaSb/Si HJ VTFETs under study. The commercially available SILVACO ATLAS^{TM} 3-D TCAD tool has been used for the present study.

Chapter-4 reports the performance analysis of 8T SRAM circuits designed by our proposed lateral and vertical stacked gate-oxide structure based SPE GaSb/Si HJ VTFETs considered in Chapter-3. The circuit-level simulations have been performed by using 2D look up table-based Verilog-A model in the CADENCE Virtuoso tool. The effects of the lateral/vertical gate-oxide stacking on various performance parameters such as the write margin, read margin, write delay and read delay of the proposed 8T SRAM circuits have been investigated in details. The effect of intrinsic gate capacitance on the performance of 8T SRAM has also been thoroughly analyzed.

Chapter-5 reports a comparative study of the device and circuit-level performances of the source pocket engineered GaSb/Si heterojunction vertical TFET (SPE GaSb/Si HJ VTFET) and source pocket engineered Ge/Si heterojunction vertical TFET (SPE GaSb/Si HJ VTFET). First, the DC and RF performances of the two devices have been compared. Then the performances of the digital logic inverter and 8T SRAM circuits designed by SPE GaSb/Si HJ VTFET and SPE Ge/Si HJ VTFET have been compared. Device simulation has been carried out using commercially available SILVACO ATLAS™ 3-D TCAD tool whereas the circuit simulation has been performed using 2D look up table-based Verilog-A model in the CADENCE Virtuoso tool.

Chapter-6 is devoted to summarize the major observations and findings of the thesis. Finally, some future scopes of research related to the thesis have been briefly discussed at the end of this chapter.