Chapter 3

Active Switched Quasi Z-source Converter

3.1 Introduction

In the preceding chapter, the impedance source DC-DC converter was thoroughly discussed. Nonetheless, the lack of common ground between the source and the load results in concerns about electromagnetic interference (EMI). To solve the limitation of the traditional Z- source network, numerous topologies were reported. Among the improvement of these impedance networks, quasi-Z source (qZS) is reported by the researchers in the literature which has a simple and efficient structure as shown in Figure 3.1. This chapter presents new qZS DC-DC converter with restricted duty range operation and common ground between source to load. Continuous input current, reduced capacitor stress, high boost factor and low voltage stress across semiconductor devices are the salient features of this converter. The diode-assisted boost qZS converter is presented in [48] and shown in Figure 3.2. The converter boost factor is increased by $\frac{1}{1-D}$ compared to the traditional Z-source converter. A different topology based on SL called SL-qZS is proposed in [52], but it has a low boost factor. A new type of extended boost qZS is reported in [53] at the cost of more inductors and capacitors. Enhanced boost qZS integrated with diode assisted network proposed in [54] with maximum duty $D = 0.29$.

Many new high-gain inverter topologies based on the Z-source have recently been presented to improve the output waveform of ZSIs by adopting a very high modulation

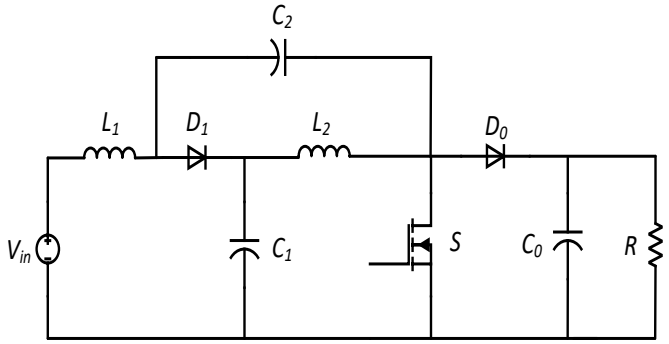

Figure 3.1: Typical structure of qZS DC-DC converter.

index. Enhance boost active switched Z-source network is reported in [55], for single phase AC load with low component count. Many new high-gain inverter topologies based on the Z-source have recently been presented to improve the output waveform of ZSIs by adopting a very high modulation index. Enhance boost active switched Z-source network is reported in [55], for single phase AC load with low component count. This chapter presents the qZS DC-DC converter with inverter operation. Compared to [53]-[54], it requires two less inductors, one less capacitor, and two additional power switches to enhance the voltage conversion ratio. In addition, the proposed converter has a continuous input current and shared common ground between the inverter bridge and source voltage.

3.2 Topological derivation of proposed converter-2 and its operation

Proposed converter is derived from extented boost network [48] as shown in Figure 3.2. The diode assisted qZS (DA-qZS) increses the boost factor by $\frac{1}{1-D}$. Furthermore, new modified switched boost based qZS is shown in Figure 3.3. The proposed converter is formed by replacing the network (C_3, L_3, C_2, D_2) with active switched boost (SB) network (C_3, D_3, D_4, S_1). The presence of capacitor C_3 in SB circuit in reference [56] increases the boost factor of qZS by $\frac{1}{1-2D}$. The proposed active switched qZS (AqZS) high voltage gain DC-DC converter is shown in Figure 3.4. It consists of five storing elements and two switches. The analysis of the converter is carried out in CCM mode, which has two modes of operation.

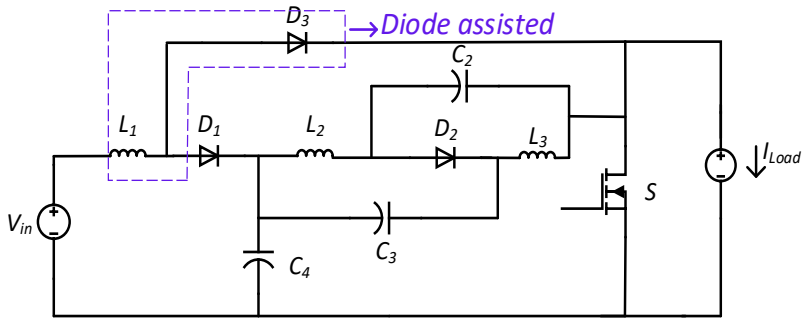

Figure 3.2: Diode assisted extented boost qZS DC-DC converter [48].

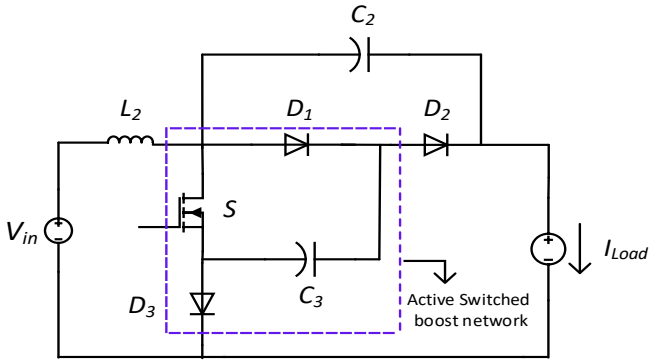

Figure 3.3: Active switched boost qZS DC-DC converter [56].

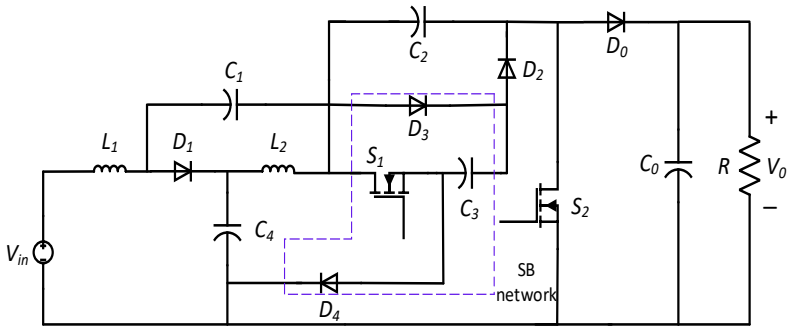

Figure 3.4: Active switched qZS high gain proposed converter-2.

3.2.1 Mode 1

This mode is brought into the circuit by applying the gate pulse to the both switches S_1 and S_2. The conducting devices are shown by solid red line and nonconducting by dashed line presented in Figure 3.5. Inductor L_1 is charge by source voltage V_{in}, capacitor C_1 and C_2. In the same way, L_2 is charged by capacitor C_3 and C_4. The output capacitor discharges its energy into load. The following equations hold in this mode.

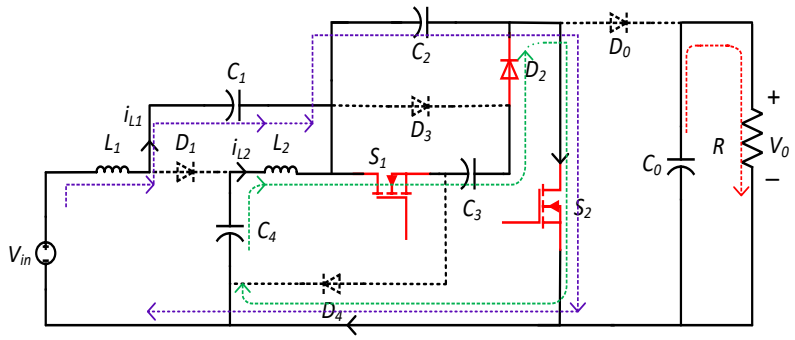

Figure 3.5: ON mode equivalent circuit.

$$v_{L1} = V_{in} + v_{C1} + v_{C2} \tag{3.1}$$

$$v_{L2} = v_{C3} + v_{C4} \tag{3.2}$$

$$v_{C3} = v_{C4} \tag{3.3}$$

$$i_{C1} = -i_{L1}, \quad i_{C4} = -i_{L2} \tag{3.4}$$

$$i_{C0} = -i_0, \quad i_{C2} + i_{C3} = -(i_{L1} + i_{L2}) \tag{3.5}$$

3.2.2 Mode 2

In this mode, both switches S_1 and S_2 are in the OFF state. Inductor L_1 releases its stored energy to charge capacitor C_4, while inductor L_2 releases energy to charge capacitors C_1 and C_3. The following equations apply in this mode:

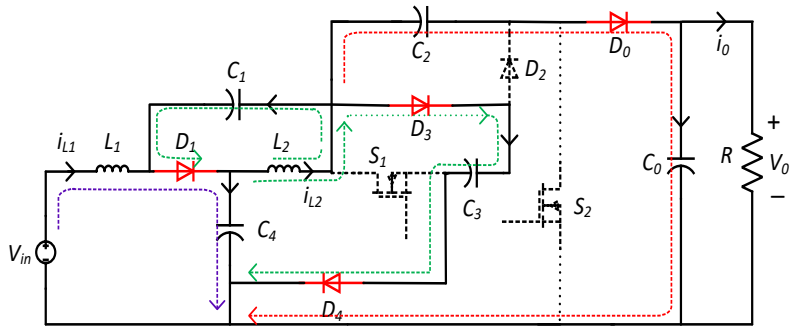

Figure 3.6: OFF mode equivalent circuit.

$$v_{L1} = V_{in} - v_{C4}, \tag{3.6}$$

$$v_{L1} = V_{in} + v_{C1} - v_{C3} \tag{3.7}$$

$$v_{L2} = -v_{C1} \tag{3.8}$$

$$v_{L2} = v_{C4} - v_{C3} \tag{3.9}$$

$$v_0 = v_{C2} + v_{C3} \tag{3.10}$$

$$i_{L2} - i_{L1} = i_{C1} - i_{C4} \tag{3.11}$$

$$i_{c2} + i_{C0} + i_0 = 0 \tag{3.12}$$

For calculation of average voltage across capacitors applying volt-second law across both inductors;

$$\int_0^{DT_s} v_{L1,L2}dt + \int_{DT_s}^{T_s} v_{L1,L2}dt = 0 \tag{3.13}$$

$$V_{C1} = \frac{2D}{1-4D}V_{in} \tag{3.14}$$

$$V_{C2} = V_{C3} = \frac{V_{C1}}{2D} \tag{3.15}$$

$$V_{C4} = V_{C3}(1-2D) \tag{3.16}$$

The voltage gain formula for the proposed qZS converter is given by in CCM mode;

$$B = \frac{V_0}{V_{in}} = \frac{2}{1-4D} \tag{3.17}$$

3.3 Design guidelines

The design of inductance (L) and capacitance (C) is based on the average current flow through the inductor and the average voltage across the capacitor. The inductance of input inductor L_1 is a series with source voltage. Hence, the input current is equal to the average inductor current for L_1.

$$I_{in} = I_{L1} = \frac{V_0^2}{V_{in}R} \tag{3.18}$$

Likewise, the current through inductor L_2 can be written by the application of Kirchhoff's current law (KCL) during both modes. Applying charge -balanace law across capacitor C_4 using eq. (3.4) and eq. (3.11).

$$-i_{L2}D + (i_{c1} - i_{L2} + i_{L1})(1-D) = 0 \tag{3.19}$$

After simplifying eq. (3.19)

$$i_{C1,mode2} = \frac{I_{L2} - I_{L1}(1-D)}{(1-D)} \tag{3.20}$$

Again, using the principle of charge balance law on capacitor C_1, which yields

$$-i_{L1}D + \left(\frac{I_{L2} - I_{L1}(1-D)}{(1-D)}\right)(1-D) = 0 \tag{3.21}$$

After simplifying following relation is obtained in qZS DC-DC converter,

$$I_{L1} = I_{L2} \tag{3.22}$$

3.3.1 Inductor design

During Mode 1, the design equations for both inductors can be written as follows:

$$L_1 = \left(\frac{V_{in} + V_{C1} + V_{C2}}{\Delta I_{L1}}\right) DT_s \tag{3.23}$$

$$L_2 = \left(\frac{V_{C3} + V_{C4}}{\Delta I_{L2}}\right) DT_s \tag{3.24}$$

3.3.2 Capacitor design

The design of the capacitance requires the current flow through the capacitors for a particular switching period and the percentage of ripple voltage. Here the 1% ripple percenatge is taken for the designing purpose. Input current equals to the capacitor current i_{C1} during Mode 1

$$C_1 \frac{\Delta V_{C1}}{DT_s} = I_{L1}, \implies C_1 = \frac{I_{L1} DT_s}{\Delta V_{C1}} \tag{3.25}$$

Calculation for capacitance C_2 can be expressed as following; using eq. (3.12) and applying charge balance law across C_2 gives

$$C_2 \frac{\Delta V_{C2}}{DT_s} = I_0, \implies C_2 = \frac{I_0 DT_s}{\Delta V_{C2}} \tag{3.26}$$

During Mode 1, current through capacitor C_3 is given as,

$$I_{C3} = I_{L1} + I_{L2} + \frac{I_0}{D} \tag{3.27}$$

$$C_3 \frac{\Delta V_{C3}}{DT_s} = (I_{L1} + I_{L2}) + \frac{I_0}{D}, \implies C_3 = \frac{[(I_{L1} + I_{L2})D + I_0]T_s}{\Delta V_{C3}} \tag{3.28}$$

Similarly during Mode 1 capacitance C_4 and C_0 calculation given by following expressions,

$$C_4 \frac{\Delta V_{C4}}{DT_s} = I_{L2}, \implies C_4 = \frac{I_{L2} DT_s}{\Delta V_{C4}} \tag{3.29}$$

$$C_0 \frac{\Delta V_{C0}}{DT_s} = I_0, \implies C_0 = \frac{DI_0 T_s}{\Delta V_{C0}} \tag{3.30}$$

From above all equations the capacitance value is for $C_1 = 46\ \mu F$, $C_2 = 6\ \mu F$, $C_3 = 30\ \mu F$, $C_4 = 20\ \mu F$ $C_0 = 10\ \mu F$ is obtained for load current $I_0 = 0.84\ A$. However for practical consideration used values for all the capacitors are $47\ \mu F$.

3.4 Voltage and current stress of semiconductor devices

The proposed converter utilizes various diodes and switches, which operate by the modes of operation. Diodes D_1, D_3, D_4 and D_0 are in the OFF state during Mode 1 and Diode D_2 along with both switches (S_1, S_2) are in the ON state. The OFF state of any device has voltage stress across it, while the ON state offers zero voltage across them. The following equations hold to determine the voltage stress across used devices during Mode 1.

$$v_{D1} = -(v_{c1} + v_{c2} + v_{c4}) \tag{3.31}$$

$$v_{D3} = v_{c4} - v_{L2}, \implies v_{D3} = -v_{c3} \tag{3.32}$$

$$v_{D4} = -v_{c3}, \quad v_{D_0} = -v_0 \tag{3.33}$$

Similarly, during Mode 2 Diode D_2 and both switches (S_1, S_2) have voltage stress across them. The following equations holds to calculate the voltage stress.

$$v_{D2} = -v_{c2} \tag{3.34}$$

$$v_{s1} - v_{c4} + v_{L2} = 0, \quad v_{S2} = -v_0 \tag{3.35}$$

The voltage stress across the switches and diodes is listed in Table 3.1. According to this table, the voltage stress on the Switch S_1 and the Diodes (D_2, D_3, D_4, D_0) is reduced to half of the output voltage. However, the voltage stress on the Switch S_2 and the Diode D_1 equals the output voltage. Average currents through the switches

Table 3.1: Voltage stress across devices

Devices	**Mode 1**	**Mode 2**
S_1	0	$\frac{1}{1-4D}V_{in}$
S_2	0	$\frac{2}{1-4D}V_{in}$
D_1	$\frac{2}{1-4D}V_{in}$	0
D_2	0	$\frac{1}{1-4D}V_{in}$
D_3	$\frac{1}{1-4D}V_{in}$	0
D_4	$\frac{1}{1-4D}V_{in}$	0
D_0	$\frac{2}{1-4D}V_{in}$	0

Table 3.2: Current stress of devices

Device	**Current stress**	**Switching period**
S_1	$\frac{(I_{L1}+I_{L2})D+I_0}{D}$	DT_s
S_2	$(I_{L1}+I_{L2})$	DT_s
D_1	$\frac{I_{L2}}{1-D}$	$(1-D)T_s$
D_2	$\frac{(I_{L1}+I_{L2})D+I_0}{D}$	DT_s
D_3	$\frac{(I_{L1}+I_{L2})D+I_0}{1-D}$	$(1-D)T_s$
D_4	$\frac{(I_{L1}+I_{L2})D+I_0}{1-D}$	$(1-D)T_s$
D_0	$\frac{I_0}{1-D}$	$(1-D)T_s$

and diodes are expressed during the device's conduction period. During Mode 1, the following equations hold to calculate the average current.

$$I_{S1} = I_{C3} = \left(I_{L1} + I_{L2} + \frac{I_0}{D}\right) \tag{3.36}$$

$$I_{S2} = I_{C2} + I_{C3} \tag{3.37}$$

$$I_{D2} = I_{C3} \tag{3.38}$$

Similarly, during Mode 2 following equations holds,

$$I_{D1} = I_{L1} + I_{C1} \tag{3.39}$$

$$I_{D3} = I_{D4} = I_{C3} \tag{3.40}$$

$$I_{D0} = I_{C2} \tag{3.41}$$

According to Table 3.2 Switch S_1 have more current than Switch S_2. Among intermediate Diodes (D_2, D_3, D_4), Diode D_2 have more current among them and output Diode D_0 have lower value of current.

3.5 Dynamic analysis of proposed converter

Dynamic behavior is necessary to analyze the converter using a small-signal model to determine stability. Inductors current $\hat{i_{L2}}$-$\hat{i_{L2}}$ and capacitor voltage $\hat{v_{c1}}$-$\hat{v_{c0}}$ are taken as state variables. The proposed converter is a seven-order system. Both stages provide a set of equations during each period. The state variables are described by small-signal disturbances, which can be given below:

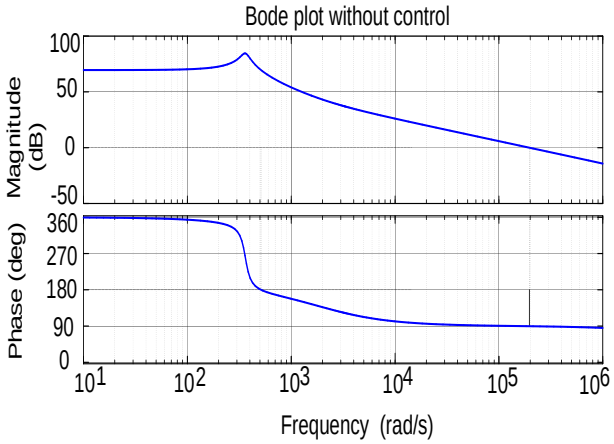

Figure 3.7: Bode plot without controller.

$$\left.\begin{aligned} i_{L1}(t) &= I_{L1} + \hat{i_{L1}}(t), \quad & i_{L2}(t) &= I_{L2} + \hat{i_{L2}}(t) \\ v_{C1}(t) &= V_{C1} + \hat{v_{c1}}(t), \quad & v_{C2}(t) &= V_{C2} + \hat{v_{c2}}(t) \\ v_{C3}(t) &= V_{C3} + \hat{v_{c3}}(t), \quad & v_{C4}(t) &= V_{C4} + \hat{v_{c4}}(t) \\ v_{C0}(t) &= V_{C0} + \hat{v_{c0}}(t), \quad & v_{in}(t) &= V_{in} + \hat{v_{in}}(t) \\ d(t) &= D + \hat{d}(t) \end{aligned}\right\} \tag{3.42}$$

Where I_{L1}, I_{L2}, V_{C1}, V_{C2}, V_{C3}, V_{C4}, V_{C0}, V_{in} and D are the DC quantity, $\hat{i_{L1}}(t)$, $\hat{i_{L2}}(t)$, $\hat{v_{c1}}(t)$, $\hat{v_{c2}}(t)$, $\hat{v_{c3}}(t)$, $\hat{v_{c4}}(t)$, $\hat{v_{c0}}(t)$, $\hat{v_{in}}(t)$ and $\hat{d}(t)$ are the small-signal disturbances. After

performing perturbation and linearization, the small-signal ac model of the proposed converter can be presented in matrix form.

$$\begin{bmatrix} \frac{d\hat{i_{L1}}}{dt} \\ \frac{d\hat{i_{L2}}}{dt} \\ \frac{d\hat{V_{c1}}}{dt} \\ \frac{d\hat{V_{c2}}}{dt} \\ \frac{d\hat{V_{c3}}}{dt} \\ \frac{d\hat{V_{c4}}}{dt} \\ \frac{d\hat{V_{c0}}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{DR_{C1}}{L_1} & 0 & \frac{D}{L_1} & 0 & \frac{D}{L_1} & -\frac{D'}{L_1} & 0 \\ 0 & 0 & 0 & 0 & \frac{D-D'}{L_2} & \frac{1}{L_2} & 0 \\ -\frac{D}{C_1} & 0 & -\frac{D'}{C_1R_{C1}} & 0 & \frac{D'}{C_1R_{C1}} & -\frac{D'}{C_1R_{C1}} & 0 \\ 0 & 0 & 0 & \frac{D-D'}{C_2R_{C2}} & \frac{D-D'}{C_2R_{C2}} & 0 & \frac{D'}{C_2R_{C2}} \\ D & 1 & \frac{D'}{C_3R_{C1}} & \frac{D-D'}{C_3R_{C2}} & -\frac{D'}{C_3R_{C1}} - \frac{1}{C_3R_{C2}} & 0 & \frac{D'}{C_3R_{C2}} \\ \frac{D'}{C_4} & -\frac{1}{C_4} & -\frac{D'}{C_4R_{C1}} & 0 & -\frac{D'}{C_4R_{C1}} & -\frac{1}{C_4R_{C1}} & 0 \\ 0 & 0 & 0 & -\frac{D'}{C_0R_{C2}} & -\frac{D'}{C_0R_{C2}} & 0 & -\frac{1}{R_{C0}} - \frac{D'}{C_0R_{C2}} \end{bmatrix} \begin{bmatrix} \hat{i_{L1}} \\ \hat{i_{L2}} \\ \hat{V_{c1}} \\ \hat{V_{c2}} \\ \hat{V_{c3}} \\ \hat{V_{c4}} \\ \hat{V_{c0}} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{V_{in}}$$

$$+ \begin{bmatrix} \frac{R_{C1}}{L_1} & 0 & \frac{1}{L_1} & 0 & \frac{1}{L_1} & \frac{1}{L_1} & 0 \\ 0 & 0 & 0 & 0 & \frac{2}{L_2} & 0 & 0 \\ -\frac{1}{C_1} & 0 & \frac{1}{C_1R_{C1}} & 0 & -\frac{1}{C_1R_{C1}} & \frac{1}{C_1R_{C1}} & 0 \\ 0 & 0 & 0 & 0 & \frac{C_2}{R_{C2}} & 0 & -\frac{C_2}{R_{C2}} \\ \frac{1}{C_3} & 0 & -\frac{1}{C_3R_{C1}} & -\frac{2}{C_3R_{C2}} & \frac{2}{C_3R_{C1}} & -\frac{1}{C_3R_{C1}} & -\frac{1}{C_3R_{C2}} \\ -\frac{I_{L1}}{C_4} & 0 & \frac{1}{C_4R_{C1}} & 0 & -\frac{1}{C_4R_{C1}} & -\frac{1}{C_4R_{C2}} & 0 \\ 0 & 0 & 0 & -\frac{1}{C_0R_{C2}} & -\frac{1}{C_0R_{C2}} & 0 & -\frac{1}{C_0R_{C2}} + \frac{1}{C_0R} \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \\ V_{C0} \end{bmatrix} \hat{d(t)} \tag{3.43}$$

$$\hat{v_0} = \begin{bmatrix} 0\,0\,0\,0\,0\,0\,1 \end{bmatrix} \begin{bmatrix} \hat{i_{L1}}\ \hat{i_{L2}}\ \hat{v_{c1}}\ \hat{v_{c2}}\ \hat{v_{c3}}\ \hat{v_{c4}}\ \hat{v_{c0}} \end{bmatrix}^T \tag{3.44}$$

$$G_{vd}(s) = \frac{\hat{V_0}(s)}{\hat{d}(s)} = \frac{-7.44\times10^{39}s^6 - 2.86\times10^{48}s^5 - 1.32\times10^{56}s^4 - 9.72\times10^{62}s^3 + 1.74\times10^{66}s^2 - 2.58\times10^{70}s + 4.65\times10^{73}}{3.42\times10^{35}s^7 + 3.81\times10^{43}s^6 + 1.07\times10^{51}s^5 + 5.34\times10^{57}s^4 + 3.8\times10^{59}s^3 + 1.42\times10^{65}s^2 + 9.3\times10^{66}s + 1.67\times10^{70}} \tag{3.45}$$

Control to output transfer function can be obtained by state-space averaging technique with the help of state space eq.'s (3.43) and eq. (3.44). The control to output transfer function represented in the frequency domain is given by eq. (3.45), which is calculated based on the parameters listed in Table 3.3, and the corresponding Bode plot is shown in Figure 3.7. According to Bode plot, gain margin (G.M.) and phase margin (P.M.) of the converter have negative value $-69.5\ dB$ and -90.4^o, therefore, system becomes unstable when operated in closed loop. Thus, it is necessary to improve the

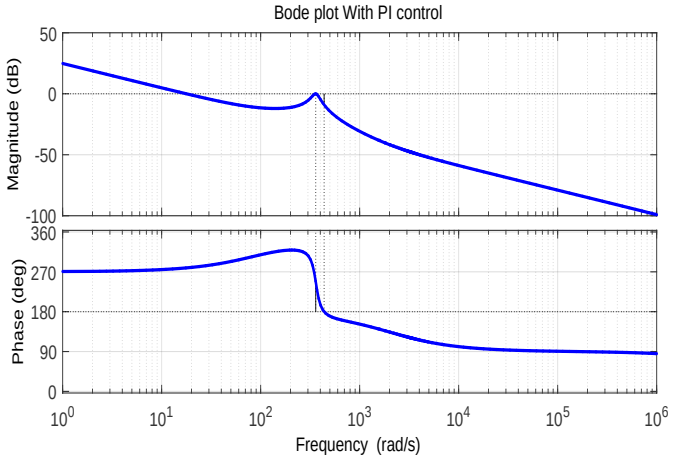

Figure 3.8: Bode Plot with PI controller.

stability of closed loop system. Hence, controller is needed for converter to improve the stability. To stabilize the control, a voltage control loop scheme is adopted. A PI control is adopted to regulate the output with where K_P=0.00005, and $K_I = 0.005$ to stabilize the control loop with phase margin 67.4^o. After placing controller, the Bode plot is shown in Figure 3.8.

3.6 Boost stage experimental validation

The proposed converter for the boost stage (DC stand-alone operation) is validated experimentally. The numerical value of storing elements is derived from the design equation presented in Section 3.3.1 and Section 3.3.2. The calculation of storing elements for the converter is discussed here. The design of storing element is calculated for $P_0 = 250\ W$ of load power keeping the load resistance $R = 350\ \Omega$, switching frequency f_s=30 kHz and input voltage fixed to 60 V. The duty cycle calculation for all these value is eq. (3.47).

$$P_0 = \frac{V_0^2}{R}, \implies V_0 = 300\ V \tag{3.46}$$

$$\frac{V_0}{V_{in}} = \frac{2}{1-4D}, \implies D = 0.15 \tag{3.47}$$

The calculation of both inductance can be done using eq. (3.23) and eq. (3.24).

$$L_1 = \left(\frac{V_{in}+V_{C1}+V_{C2}}{\Delta I_{L1}}\right) DT_s, \implies L_1 = \frac{255\times 0.35}{30k\times 0.15} = 2.0\ mH \tag{3.48}$$

$$L_2 = \left(\frac{V_{C3}+V_{C4}}{\Delta I_{L2}}\right) DT_s, \implies L_2 = \frac{255\times 0.15}{30k\times 0.15} = 2.0\ mH \tag{3.49}$$

Similarly, the calculation for capacitance is discussed using eq. (3.26) to eq. (3.30).

$$C_1 = \frac{I_{L1} D T_s}{\Delta V_{C1}}, \implies C_1 = \frac{4.2 \times 0.15}{0.02 \times 30k} = 24\ \mu F \tag{3.50}$$

$$C_2 = \frac{I_0 D T_s}{\Delta V_{C2}}, \implies C_2 = \frac{1.01}{0.02 \times 30k} = 16\ \mu F \tag{3.51}$$

$$C_3 = \frac{(I_{L1} + I_{L2})D + I_0) D T_s}{\Delta V_{C3}}, \implies C_3 = \frac{8.4 \times 0.15 + 1.01}{0.02 \times 30k} = 26\ \mu F \tag{3.52}$$

$$C_4 = \frac{I_{L2} D T_s}{\Delta V_{C4}}, \implies C_4 = \frac{4.2 \times 0.15}{0.02 \times 30k} = 25\ \mu F \tag{3.53}$$

$$C_0 = \frac{I_0 D T_s}{\Delta V_{C0}}, \implies C_0 = \frac{1.01 \times 0.15}{0.02 \times 30k} = 15\ \mu F \tag{3.54}$$

The specifiaction and used final value of storing elemets for proposed converter-2 is listed in Table 3.3. A scaled down laboratory prototype is developed to test the theo-

Table 3.3: Proposed converter-2 specification

S.No	**Parameter**	**Values**
1	Input Voltage V_{in}	60 V
2	DC output power P_0	250 W
2	Inductance L_1, L_2	2.2 mH
3	All capacitance C	47μF
4	Duty Cycle D	0.15
5	Switching Frequency f_s	30 kHz

retical analysis for the specifications as mentioned in Table 3.3. The both inductance (L_1 and L_2) are designed for reducing the ripple current about $< 15\%$. The components utilized for experimentation are listed in Table 3.4. The observed spikes in experimental voltage and current are attributed to switching effects, stray inductance, and parasitic capacitances. The proposed converter-2 with low source current ripple and low duty cycle with high voltage gain has been experimentally validated, and the measured results are shown in Figure 3.9. The measured value of input voltage V_{in}, output voltage V_0, and load current are 60 V, 295 V, and 0.84 A, respectively. The steady state feature of qZS high gain converter with low source current ripple is demonstrated in Figure 3.10 . The measured value of ripple current peak to peak is

Table 3.4: Device and components used in experiment

Component/Device	Part Number and Manufacturer
DC Source	H3010, Aplab
MOSFET	SiHFPS40N50L, Vishay
Diode	DPG60C400QB, IXYS STPS60SM200CW, STElectronics
Gate driver	HCPL3120 Avago Technology
Inductor	PCV-2-564-08L, Colicraft
Capacitor	ESU476M400AM5AA, Kemet
Control board	eZdsp F28335 DSP board, Texas

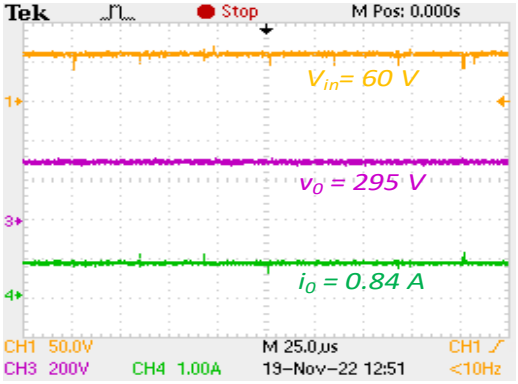

Figure 3.9: Measured input-output voltage and load current of proposed converter.

$\approx 0.7\ A$ or $\approx 15.5\%$ as per design guidelines for the both the inductor. The measured mean value of both inductor currents are 4.55 A for L_1, and 4.4 A for L_2 which is in the close agreement with eq. (3.22).

In the same way, the measured switch voltage stress is demonstrated in Figure 3.11. It is observed that Switch S_1 has voltage stress almost half of the output voltage V_0, whereas Switch S_2 is equal to the output voltage V_0. The measured value of voltage stress across Switch S_1 and S_2 is $\approx 152\ V$ and $\approx 295\ V$, respectively. Similarly, the voltage stress across used diodes is described in Figure 3.12 and Figure 3.13. The maximum voltage stress across Diodes D_1 and D_0 is $\approx 295\ V$, which is equal to the output voltage. Voltage stress across remaining Diodes (D_2, D_3, D_4) are equal and its

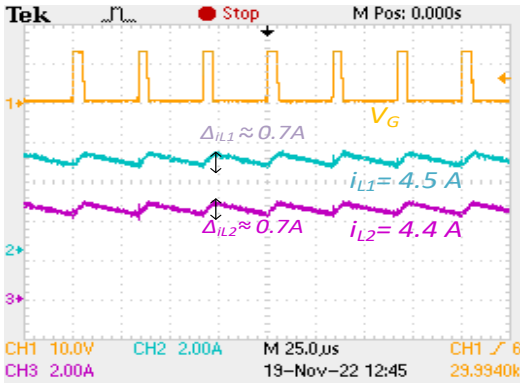

Figure 3.10: Measured source current $i_{in} = i_{L1}$ and inductor L_2 current waveforms.

values are $\approx 152\ V$. The measured stress across semiconductor devices confirms the theoretical analysis as shown in Table 3.1.

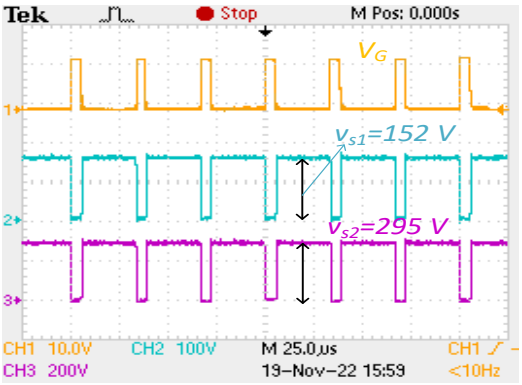

Figure 3.11: Measured voltage stress of both switch with gating pulse.

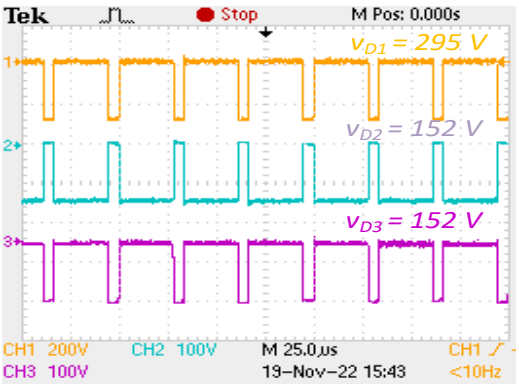

Figure 3.12: Measured voltage stress across diodes D_1, D_2 and D_3.

Finally, the mean voltage value across the capacitors is measured and depicted in Figure 3.14. From all the demonstrated waveforms, it is evident that the proposed converter achieves a high voltage gain for low values of the duty cycle with low volt-

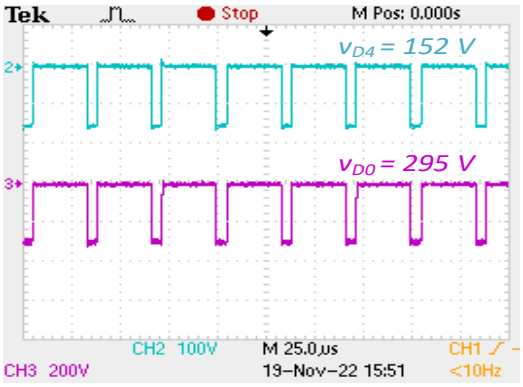

Figure 3.13: Measured voltage stress across diode D_4 and D_0.

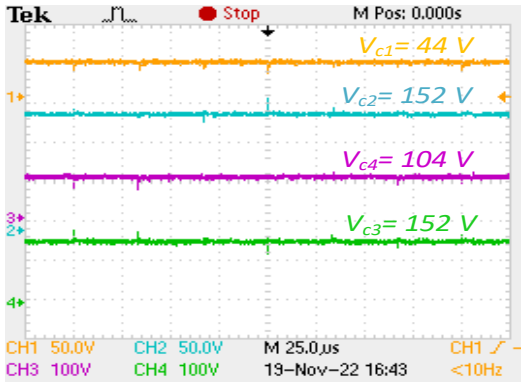

Figure 3.14: Measured mean value of voltage across capacitors.

age stress across capacitors. The measured efficiency of the proposed converter in standalone mode is found to be 91%, corresponding to a load power of 250 W.

3.6.1 Boost stage closed loop validation

The closed-loop validation using the PI controller is validated experimentally. This includes the input voltage and load current variations. The dynamic response of the converter with under load current variations from (350 $\Omega - 200\ \Omega$, vice versa) is demonstrated in Figure 3.15 and Figure 3.16 respectively, with input voltage fixed to ($V_{in} = 52\ V$). Under load current variations, output voltage settles with the controller, and it takes 5 ms to reach the reference set point. Similarly, the dynamic performance with fixed load resistance (300 Ω) and variation in input voltage from ($V_{in} = 52 - 65\ V$, vice versa) is verified, and the controller takes 22 ms to track the reference voltage as shown in Figure 3.17 and Figure 3.18, respectively. Hence, experimental demonstrations effectively showcased the dynamic performance of the qZS

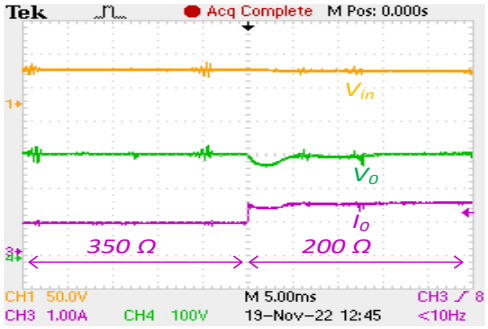

Figure 3.15: Closed loop response to increase in I_0.

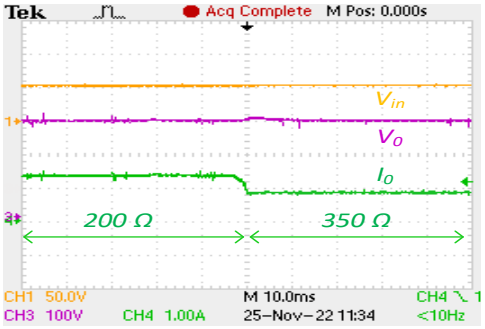

Figure 3.16: Closed loop response to decrease in I_0.

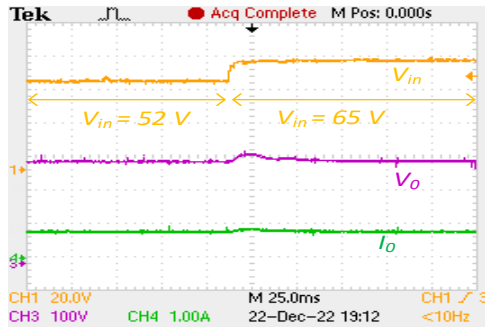

Figure 3.17: Closed loop response to increase in V_{in}.

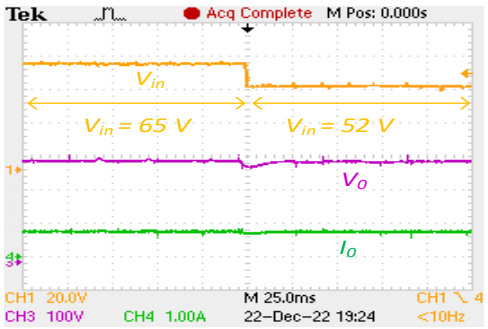

Figure 3.18: Closed loop response to decrease in V_{in}.

system with a controller during the boost stage. The tuned parameters of the PI controller facilitated precise tracking of the reference voltage.

3.7 Extension to hybrid system

For hybrid loads (AC and DC), the cascaded boost inverter requires an additional switch and a large DC link capacitor, resulting in a large-sized converter with a low-voltage input for the inverter. These converters are suitable for several applications, such as distribution and smart grids. Since both AC and DC loads are connected to the DC grid, different converters must supply them. To avoid different converters, a hybrid converter that includes both DC and AC converters is substituted in the DC grid. The proposed DC-DC converter can be extended for hybrid applications. This hybrid converter will act as a Z-source inverter and, therefore, will have all the features of Z-source, such as shoot-through (ST) protection, better THD, zero dead time requirement, power conversion, etc. ST protection makes the hybrid converter

more reliable. The proposed converter for hybrid applications is shown in Figure 3.19, and its operation is as follows:

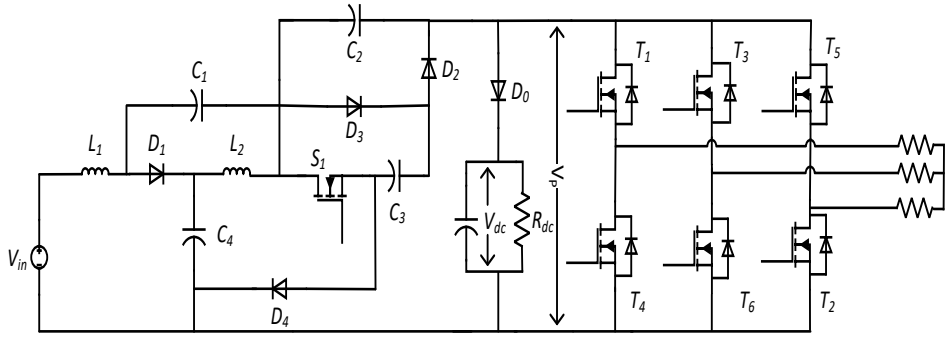

Figure 3.19: Proposed converter-2 for hybrid load.

3.7.1 Operating modes

The proposed converter can be used for hybrid load which comprised of three phase AC load connected in star and DC load resistance R_{dc}. The converter have following operating modes namely, shoot through, active or power transfer state.

Shoot through state

This state happens when switches of the same leg (T_1 and T_4) are turned ON simultaneously by a gate signal. The shoot through state is equal to the operating time DT_s for the proposed converter. In this state, Diode D_2 is forward biased, and the rest of the diodes are reversed biased. Charging of the inductor is accomplished by turning ON Switch S_1 and the same leg of inverter switches. The equivalent diagram of the shoot-through state is shown in Figure 3.20.

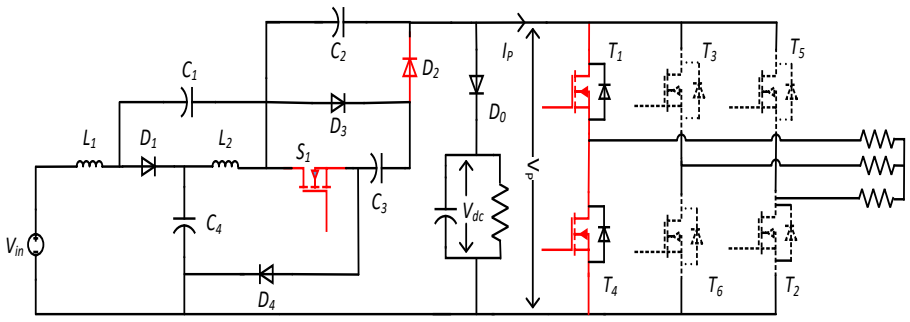

Figure 3.20: Shoot through state equivalent circuit.

Power transfer or Active state

In this state, two switches of different legs, either (T_1 and T_6) or (T_1 and T_2), are turned ON, and power flows through AC loads. During this state in the qZS network, except Diode D_2, all diodes are forward biased and Switch S_1 in OFF state. The conducting devices are depicted in Figure. 3.21.

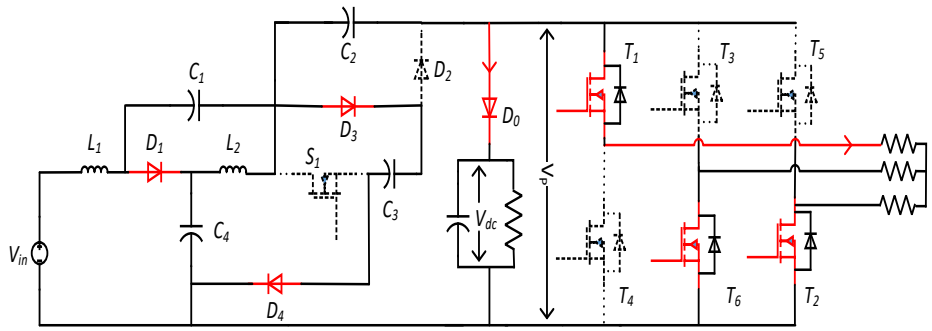

Figure 3.21: Active state equivalent circuit.

3.8 Steady state analysis

The DC link voltage V_P for the three-phase inverter is the boosted voltage (B) of the proposed converter-2. The DC link voltage can be written as;

$$V_P = \frac{2}{1-4D} V_{in}, \implies B = \frac{V_P}{V_{in}} = \frac{2}{1-4D} \tag{3.55}$$

For the three-phase inverter system, its peak ac output phase voltage can be defined as follows:

$$v_{ac} = \frac{M}{2} V_P, \implies G = \frac{M}{2} B \tag{3.56}$$

Here M=modulation index, and G= three phase AC gain The final value of AC gain (G) for the proposed qZS inverter is;

$$G = \frac{M}{4M-3} \tag{3.57}$$

For hybrid load total input power P_{in} is the summation of DC power (P_{dc}) and AC power (P_{ac}). Thus,

$$P_{in} = P_{dc} + P_{ac} \tag{3.58}$$

$$V_{in} I_{in} = V_{dc} I_{dc} + 3 V_{ac} I_{ac} \cos\theta \tag{3.59}$$

where V_{ac} and I_{ac} are the RMS value of ac phase volatge and current. The proposed converter input current is nothing inductor current of L_1. Hence the above expression can be written as;

$$I_{L1} = \frac{V_{dc}I_{dc} + 3V_{ac}I_{ac}\cos\theta}{V_{in}} \tag{3.60}$$

For supplying both load AC as well DC, The input current must be greater than zero and diode must be forward biased i.e;

$$i_{L,min} - i_{ac} > 0, \implies (I_L - \frac{\Delta I_L}{2}) - i_{ac} > 0 \tag{3.61}$$

Where i_{ac} is peak value of AC load current. From eq. (3.60) and eq. (3.61)

$$\left[\frac{V_{dc}I_{dc} + 3V_{ac}I_{ac}\cos\theta}{V_{in}} - \frac{V_{in}D}{2f_sL} - i_{ac}\right] > 0, \tag{3.62}$$

Replacing peak current ($i_{ac} = \sqrt{2} * I_{ac}$) and rearranging eq. (3.62),

$$I_{dc} > \left[\frac{I_{ac}(1-4D)}{\sqrt{2}} + \frac{(1-D)DV_{in}}{f_sL}\right] - \frac{3M}{\sqrt{2}}I_{ac}\cos\theta \tag{3.63}$$

3.9 Simulation and experimental validation

The proposed converter-2 for hybrid operation is simulated in MATLAB Simulink, and its validation is conducted experimentally. The specifications for the hybrid load are provided in Table 3.5. In the case of continuous conduction mode (CCM) with simultaneous DC and AC load, eq. (3.63) must be met to avoid unintended operation of the converter. The implementation of the shoot-through pulse (ST) pulses involves comparing a triangular carrier wave with a three-phase sinusoidal waveform and two constant values (equal to duty cycle) with equal and opposite magnitudes. The carrier wave frequency is 5 kHz. The ST pulses that enhance the qZS converter's voltage have a frequency of 10 kHz. This occurs due to the derivation of the ST through the comparison of two constant values that are contrary to each other. Although the duty cycle (D) and modulation index (M) are independently controlled, their range is limited. The conditions that must be met for the converter to function are:

$$M + D \leq 1 \tag{3.64}$$

Simulation results

The simulated waveform for hybrid load is presented in Figure 3.22. During the shoot-through period, the inductor is magnetized by DC input voltage, and the current is rising in nature. Simultaneously, the DC link voltage V_P is zero. Conversely, the DC link voltage manifests across the inverter leg during the active-state period. The three-phase output voltage waveform during inverter operation is shown in Figure 3.23. Figure 3.22 and Figure 3.23 shows the simulated waveform for both DC as well as AC voltage, which is equal to the $V_{dc} = 135\ V$ and $V_{ac} = 35\ V$, respectively.

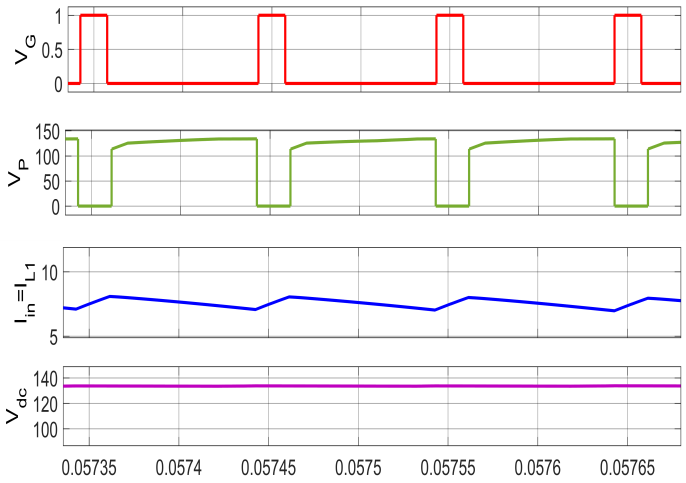

Figure 3.22: DC output and DC link voltage during hybrid operation.

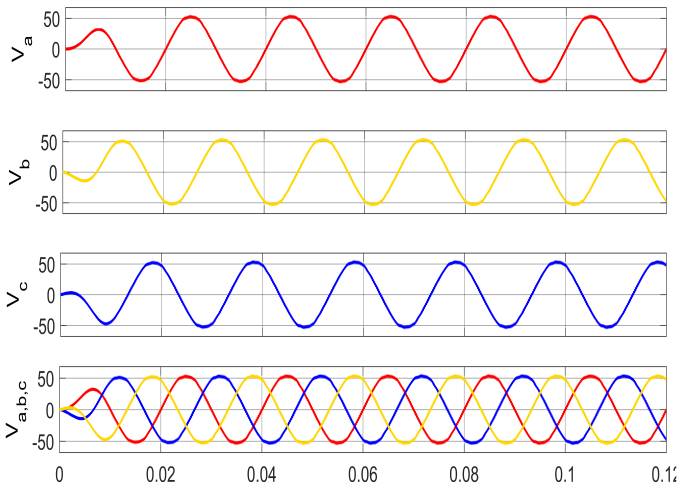

Figure 3.23: Three phase AC output voltage during hybrid operation.

3.9.1 Experimental results

To evaluate the performance during hybrid operation, the DC load is considered to be 150 Ω, and the AC load is 40 Ω per phase. The modulation index (M) is 0.8, and the duty (D) is kept at 0.15. An experiment is performed to validate the hybrid operation of the converter. The photograph of the developed converter during hybrid operations is shown in Figure 3.24. The specification of the converter during hybrid operation is listed in Table 3.5.

Table 3.5: Proposed qZS converter for hybrid operation

S.No	Parameter	Values
1	Input Voltage V_{in}	27 V
2	Total power P_o	200 W
3	DC output power P_{DC}	116 W
4	AC output power P_{AC}	84 W
5	Inductance L_1,L_2	2.2 mH
6	All capacitance C	47μF
7	AC Filter Inductance L_f	1.2 mH
8	AC Filter capacitance C_f	10μF
9	Carrier Frequency f_c	5 kHz

Results

Proposed converter-2 is extended for both DC and AC loads and is called a hybrid converter. The measured DC link voltage $V_P = 132\ V$ is fed to the inverter of qZS. The measured mean value of both inductors is $I_{L1} = I_{L2} = 8.4\ A$ and presented in Figure 3.25. The measured per phase AC output voltage $V_{ac,rms}$ is 33.4 V, shown in Figure 3.26. The total power during hybrid load is $P_{total} = 200\ W$. Out of total power, DC load shares $P_{dc} = 116\ W$ and AC load shares $P_{ac} = 84\ W$. The measured efficiency during hybrid operation is found to be 88%. The reduced efficiency observed during hybrid operation arises from using additional devices and the inherent parasitic effects

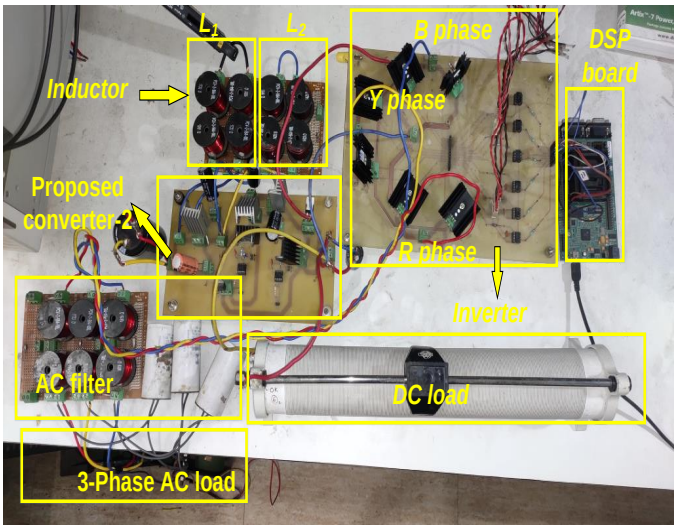

Figure 3.24: Experimental setup for qZS converter for hybrid operation

in all components used.

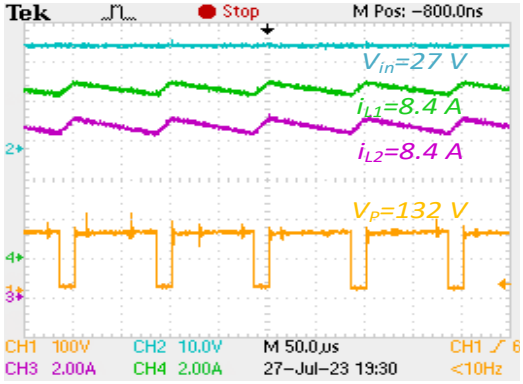

Figure 3.25: Measured inductors current and DC link V_P voltage.

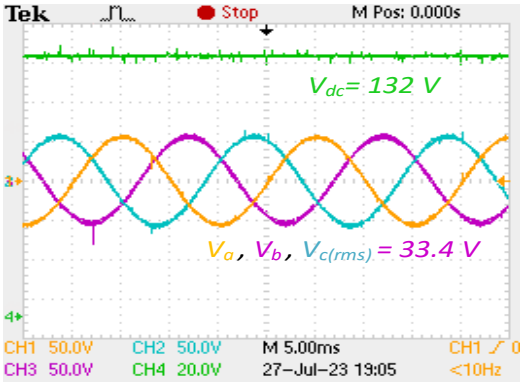

Figure 3.26: Measured DC voltage and AC voltage during hybrid operation.

3.10 Comparison with other existing topologies

To give a comprehensive comparison between the proposed converter-2 and other existing high voltage gain Z-source converters, Table 3.6 is provided. In the comparison, it is assumed that all the converters are operated as three-phase Z-source inverters. In the table, voltage gain (B), overall voltage gain (G) at the ac terminal, the total number of devices (TC), diodes, switches, and capacitor stress, inductors current, and input current ripple are presented. The calculation of capacitor stress, diode stress, switch stress and inductor current stress is demonstrated for the proposed qZS inverter.

Capacitor stress

Using eq. (3.14) to eq. (3.16) to determine the capacitor stress,

$$V_{C1} = \frac{2D}{1-4D}V_{in}, \implies \frac{V_{C1}}{V_{in}} = \frac{2D}{1-4D} = DB \tag{3.65}$$

$$V_{C2} = V_{C3} = \frac{1}{1-4D}V_{in}, \implies \frac{V_{C2,C3}}{V_{in}} = \frac{B}{2} \tag{3.66}$$

$$V_{C4} = \frac{1-2D}{1-4D}V_{in}, \implies \frac{V_{C4}}{V_{in}} = \frac{1-2D}{2}B \tag{3.67}$$

All capcitor stress is represented by $\frac{V_C}{V_{in}}$ in Table 3.6.

Diode and switch stress

Using Table 3.1 to represent the stress across diodes and switches. It can be represented by $\frac{V_D}{V_{in}}$ and $\frac{V_S}{V_{in}}$ in Table 3.6.

$$V_{D1} = V_{D0} = \frac{2}{1-4D}V_{in}, \implies \frac{V_{D1,D0}}{V_{in}} = B \tag{3.68}$$

$$V_{D1} = V_{D2} = V_{D4} = \frac{1}{1-4D}V_{in}, \implies \frac{V_D}{V_{in}} = \frac{B}{2} \tag{3.69}$$

$$V_S = \frac{1}{1-4D}V_{in}, \implies \frac{V_S}{V_{in}} = \frac{B}{2} \tag{3.70}$$

Inductor current stress

According to power balance theory at DC link

$$V_{in}I_{in} = (1-D)V_P I_P \tag{3.71}$$

where V_P and I_P are DC link voltage and current, respectively.

$$I_{in} = I_{L1} = (1-D)\frac{2}{1-4D} I_P, \implies \frac{I_L}{I_P} = (1-D)B \tag{3.72}$$

Table 3.6: Comparison of proposed converter-2 with existing topologies

Topology	***L***	***C***	***S***	***Di***	**TC**	***B***	$\mathbf{V_c/V_{in}}$	$\mathbf{V_D/V_{in}}$	$\mathbf{V_S/V_{in}}$	**G**	$\mathbf{I_L/I_P}$	$\mathbf{I_P}$	$\mathbf{\Delta I_{in}}$	**Operating efficiency**
Proposed	2	4	7	4	17	$\frac{2}{1-4D}$	$B/2, DB$ $\frac{1-2D}{2}B$	$B, B/2$	$B/2$	$\frac{M}{4M-3}$	$(1-D)B$	$\frac{(1-D)V_P}{R_l}$	ΔI_{L1}	88% @200 W
McASC-qZSI[57]	1	3	9	6	19	$\frac{1}{1-4D}$	B	B	B	$\frac{M}{2(4M-3)}$	$(1-D)B$	$\frac{(1-D)V_P}{R_l}$	ΔI_{L1}	91% @90 W
HP-ZSI[45]	4	3	6	6	19	$\frac{2(1+D)}{1-4D-D^2}$	$\frac{1-D}{2}B$ $\frac{1+D}{2}B$	$B, B/2$ $\frac{1-D}{1+D}B, \frac{D}{1+D}B$	NA	$\frac{M(2-M)}{6M-M^2-4}$	$\frac{1-D}{1+D}B$	$\frac{(1-D)V_P}{R_l}$	$(1-D)I_L$	91.5% @100 W
EB-ZSI[53]	4	4	5	6	19	$\frac{1}{1-4D+2D^2}$	$(1-D)^2B$ $(1-D)B$	B, DB $(1-D)B$	NA	$\frac{M}{2(2M^2-1)}$	$(1-D)B$ $(1-D)^2B$	$\frac{(1-D)V_P}{R_l}$	$(1-2D)I_{L3}-$ $-(1-D)I_P$	NA 200 W
EB-qZSI[54]	4	4	5	6	19	$\frac{1}{1-4D+2D^2}$	$(1-D)^2B, D(1-D)B$ $D(2-D)B$ $(1-3D+D^2)B$	B $3DB$ $(1-3D)B$	NA	$\frac{M}{2(2M^2-1)}$	$(1-D)B$ $(1-D)^2B$	$\frac{(1-D)V_P}{R_l}$	ΔI_{L1}	88% @1000 W
rASLB-qZSI[58]	3	3	6	7	19	$\frac{1+D}{1-4D+D^2}$	$DB, (1-D)B$ $DB, (1-D)B$	$B, (1-D)B$ $D\frac{2-D}{1+D}B, \frac{2-3D+D^2}{1+D}B$	NA	$\frac{M(2-M)}{2(M^2+2M-2)}$	$(1-D)B$ $(1-D)^2B$	$\frac{(1-D)V_P}{R_l}$	$\frac{D(1-D)B}{1+D}$	91.2% @890 W
SL-ZSI[59]	4	2	7	6	19	$\frac{1+D}{1-3D}$	$\frac{1-D}{1+D}B$	$B, \frac{1-D}{1+D}B$ $\frac{D}{1-D}B$	NA	$\frac{M(2-M)}{2(3M-2)}$	$\frac{1-D}{1+D}B$	$\frac{(1-D)V_P}{R_l}$	$(1-2D)I_L - I_P$	NA @3.9 kW
Hybrid ZSI[60]	4	6	3	6	19	$\frac{1}{1-4D}$	$B, DB, (1-2D)B$ $2DB, (1-3D)B$	B	NA	$\frac{M}{2(4M-3)}$	$(1-D)B$	$\frac{(1-D)V_P}{R_l}$	ΔI_{L1}	92% @100 W

Note1: In this table L=number of inductor, C=number of capacitor, S=number of switches, Di= number of diodes, TC= total count, B=boost factor, D=Duty cycle of converter, NA=not applicable, ΔI_{L1}= Ripple content in inductor L_1

Here I_P is the corresponding average DC-link current, I_P=$(1-D)\frac{V_P}{R_l}$ R_l is the simplified equivalent DC load of the ac-side circuit. In comparison to the voltage gain, it can be seen that the proposed converter has higher voltage gain as compared to the other existing, except high-performance Z-source inverter (HP-ZSI). For a graphical comparison of the voltage gain of the converters, Figure 3.27 is provided. Furthermore, the overall gain (G) versus modulation index (M) curves is also plotted in Figure 3.28. Similar to voltage gain, the overall voltage gain is also higher for the proposed converter except for HP-ZSI. However, the proposed converter has the lowest component count among all the topologies, which is an interesting improvement over existing topologies. The HP-ZSI also has a higher input current ripple as compared to the proposed converter. The proposed converter has lower stress across the capacitors as compared to McASC-qZSI and HP-ZSI. Therefore, the proposed converter is quite suitable for high gain. The proposed converter-2 can be extended for inverter applications to act as a Z-source inverter. The gain achieved by the proposed converter is quite high in the

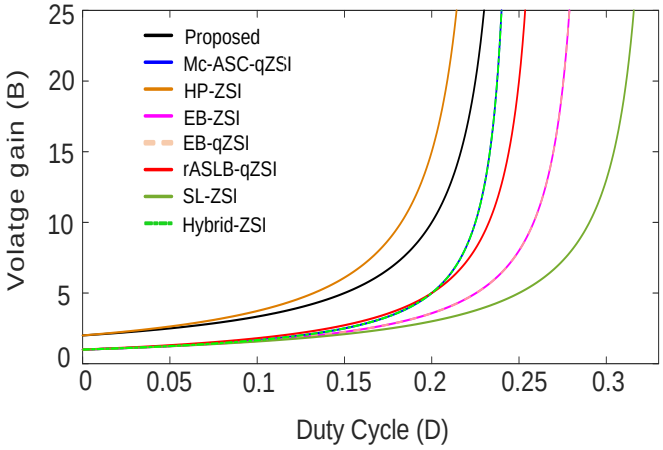

Figure 3.27: Boost factor comparison.

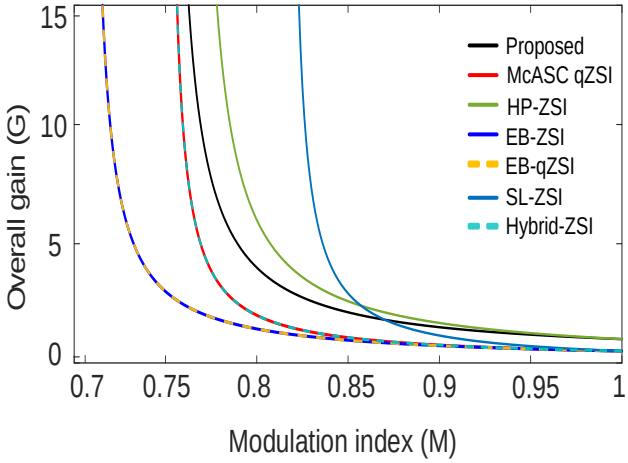

Figure 3.28: Overall gain considering inverter extension.

lower duty cycle range; therefore, the inverter can be operated at a higher modulation index, which improves the output voltage magnitude and waveshape.

3.11 Conclusion

This chapter provides an active switch-based qZS high voltage gain converter for hybrid loads. The concept of the capacitor-diode network is utilized to modify and incorporate it into the inverter. The topology modification permits the converter's operation with a low-duty cycle. Upon analyzing the boosting operation, it is found that the experimental results are in agreement with the simulation and analytical results. Compared with existing converters, the proposed topology has greater potential in terms of overall

gain and capacitor stress. However, the proposed qZS utilizes more storage elements. In addition, the input inductor is connected in series with the source voltage. More current is drawn from the source side to accomplish the high voltage gain, which directly influences the rating of inductors. The motivation for the following chapter is to reduce the number of passive elements and inductor current stress and maintain higher voltage gain.