4

CHAPTER

DIODE ASSISTED SWITCHED LC QUASI-Z-SOURCE SERIES-PARALLEL HYBRID CONVERTERS WITH MULTI AC AND SINGLE DC OUTPUTS

4.1 Introduction

In recent times, the idea of microgrid having both AC and DC system is emerging fast which can serve both; 1) the AC load demands at different voltage levels and 2) the DC load demand which is increasing day by day with use of laptops, electric vehicle chargers, mobiles etc. This type of microgrid where both DC bus line and AC bus lines coexist is called hybrid microgrid (HMGS). The HMGS provides reliable, low-cost and improved local resilience, which improves the regional electric grid's operation and stability. For hybrid microgrids with modern applications such as hybrid electric vehicles and futuristic houses having both AC and DC loads, the conventional single output converters cannot fully meet the simultaneous requirements of different types of voltage outputs. Moreover, the muti-output converters discussed in the previous chapters are also not suitable for hybrid microgrid as they are able to supply only AC voltages. Therefore, to fulfil these requirements the hybrid multi output converters (HMOCs) are emerging as a promising solution due to their ability to generate multiple AC and DC outputs simultaneously. Various topologies have been evolved for hybrid converters based on voltage source inverters. However, there are many drawbacks associated with these topologies such as they have voltage buck capability only, shoot-through problem, lower efficiency due to large number of conversion stages. To cope up the above-mentioned problems of conventional HMOCs and to obtain multiple AC along with DC outputs, diode assisted switched LC quasi-Z-source series parallel hybrid converters (QSPHCs) are proposed in this chapter.

The proposed QSPHCs are capable of providing simultaneous multiple single phase AC outputs at different voltage levels along with one DC output. The topologies of the *q*-ZS based inverters presented in previous chapters have been used with some modification to achieve an additional DC output. Thus, in the proposed hybrid converters, a controllable DC supply is achieved in parallel with various regulated single-phase AC output units in both series

and parallel mode topologies. The detailed circuit analysis and mathematical modelling of proposed QSPHC topologies are presented and validation of the steady state and dynamic performances are accomplished by simulation results.

4.2 Proposed QSPHCs with Single Phase Multiple AC and Single DC outputs

Figure 4.1 shows the circuit diagram of the proposed QSPHCs with multiple single phase AC and one DC outputs. Figure 4.1(a) and 4.1(b) shows a parallel and series version of

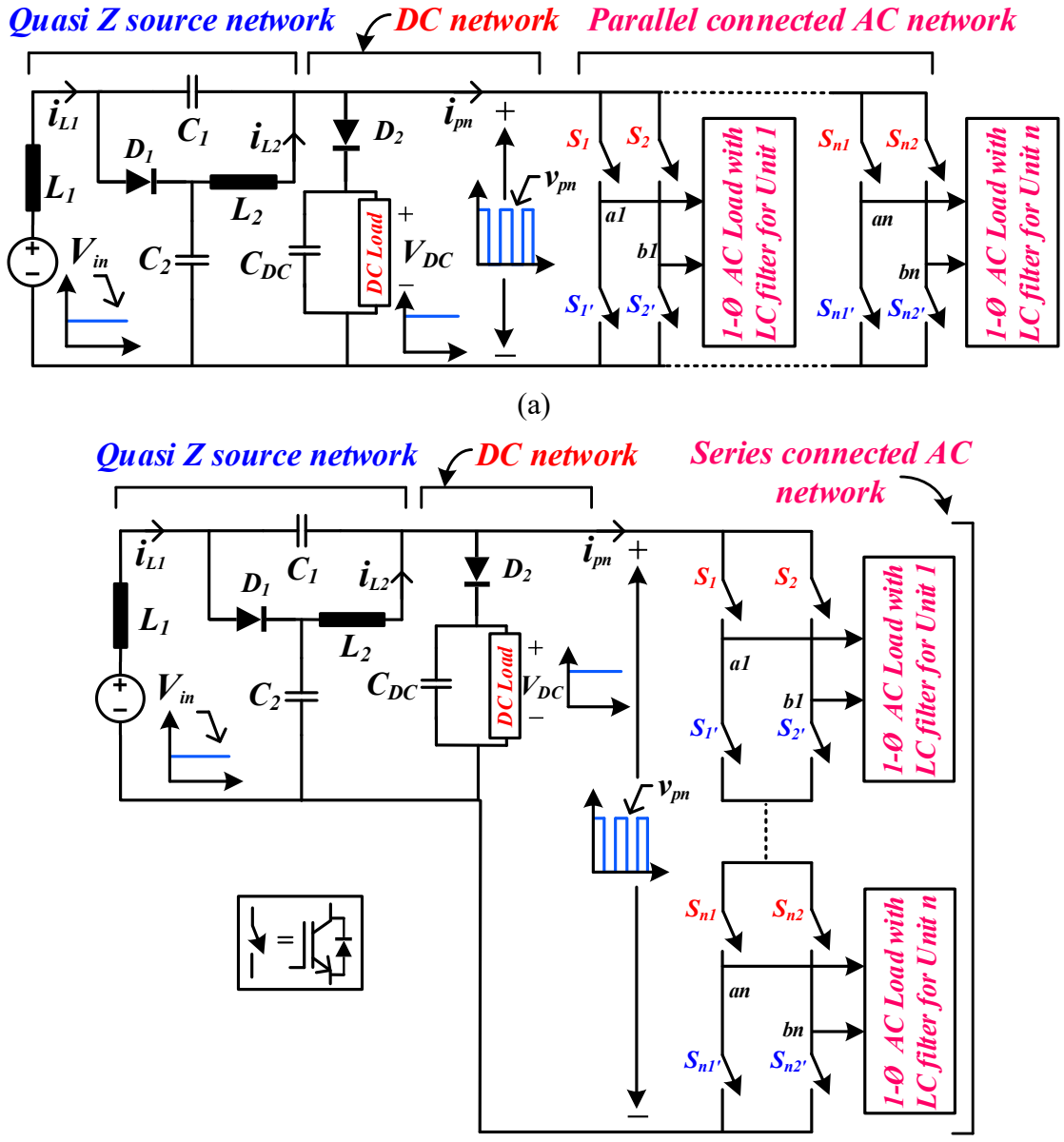


Figure 4.1: Circuit diagram of the proposed (a) parallel and (b) series version of the single-phase series-parallel multi outputs converters.

the proposed QSPHCs respectively, which consist of a switched LC impedance based quasi-Z-source network, a DC network to achieve the DC output, and *n* number of single-phase AC inverters connected in the parallel and series. To achieve the DC network, a circuit modification is done in both the versions (i.e. series and parallel) by inserting a parallel branch consisting of a capacitor (C_{DC}) assisted with a series diode (D_2) across the switch nodes of the quasi-Z-source network of the proposed QSPHCs. By this circuit modification, the switch node voltage will be translated as the output DC supply. The proposed parallel version of converters is capable of supplying *n* number of single-phase AC outputs with constant voltage and variable load currents along with one simultaneous boost DC output. Similarly, the series version of converter gives *n* number of single-phase AC outputs with constant load currents with simultaneous boost DC output. It is to mention here that the proposed single-phase series-parallel topologies are verified for two AC output units ($n = 2$).

4.3 Circuit Operation

In a conventional voltage source inverter (VSI), there is only power interval of operation. The power interval occurs when a non-zero voltage appears at the output of inverter bridge and supplied to the load. Sometimes, due to some mal-operation in switching signals, there may be condition of shoot through when upper and lower switches of same leg of the inverter bridge become ON to produce a zero voltage condition across the load. This condition may cause deadly short circuit and thus a problem in VSI. However, in quasi-Z-source inverter, a shoot-through condition (short-circuit of inverter switches) is purposefully introduced that provides extra control parameter. By doing so, it becomes able to give the boost operation too, whereas, in conventional VSI, only buck output voltage is possible. Here, the operation of the proposed QSPHCs are the same as the traditional quasi-Z-source inverters having two intervals i.e. shoot-through (ST) and power intervals, thus giving AC with addition DC output.

4.3.1 Shoot-Through (ST) Interval

Figures 4.2(a) and (b) show the circuit diagram of the proposed parallel and series version hybrid converters, respectively Figure 4.2 (c) shows their equivalent circuits during the ST interval. To explain the circuit behaviors, all the AC output units are replaced with short circuit switches as shown in Figure 4.2(c). During the ST interval, all the switches of the proposed series-parallel converters are ON at the same time and hence the switch node voltage V_{pn} across them is equal to zero. Diodes D_1 and D_2 are reverse biased and hence currents through them are zero. Inductor L_1 is charged by capacitor C_1 and input source voltage V_{in}. Inductor L_2 is charged by the capacitor C_2 and DC filter capacitor C_{dc} is discharged through the DC load [97]-[101]. Therefore, by applying KVL in Figure 4.2(c), the voltages across L_1 and L_2 are given as

$$L_1 \frac{di_{L1}}{dt} = V_{L1} = V_{in} + V_{c1} \tag{4.1}$$

$$L_2 \frac{di_{L2}}{dt} = V_{L2} = V_{c2} \tag{4.2}$$

where V_{in} is input DC voltage, V_{c1} and V_{c2} are voltage across capacitors C_1 and C_2.

Since, during the ST interval, all the switches are ON at the same time, the switch node voltage (V_{pn}) is equal to zero.

$$V_{pn} = 0 \tag{4.3}$$

The diodes D_1 and D_2 are reverse biased in this interval due to the higher voltage of the inductors. Hence, the voltage across and the current through D_1 and D_2 are

$$V_{D1} = V_{D2} = V_{c1} + V_{c2} \tag{4.4}$$

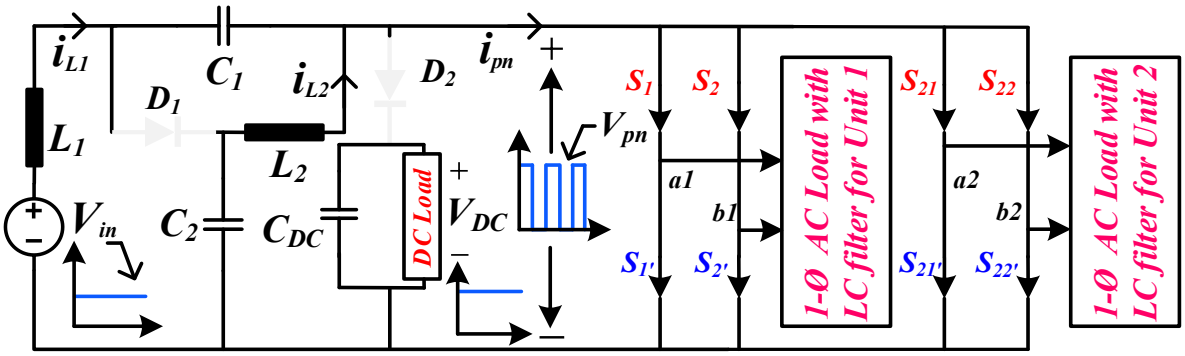
$$i_{D1} \text{ and } i_{D2} = 0 \tag{4.5}$$

where V_{D1} and V_{D2} are the voltages across and i_{D1} and i_{D2} are the current through the diodes D_1 and D_2 respectively.

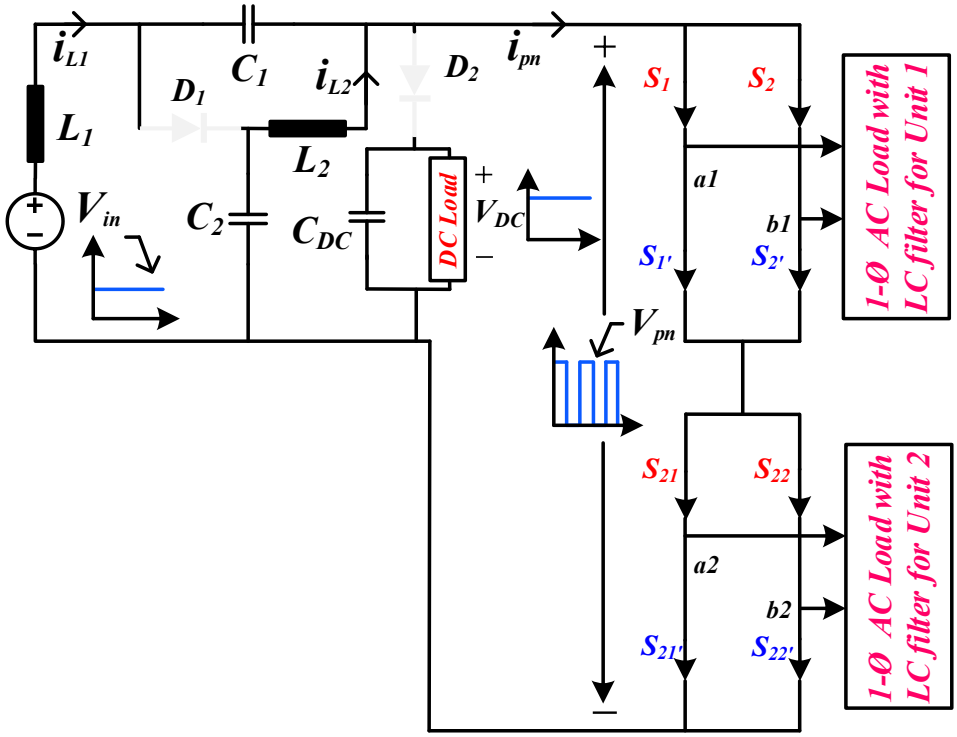
Now, by applying KCL in Figure 4.2(c), the capacitor currents are given as

$$C_1 \frac{dV_{c1}}{dt} = i_{C1} = -i_{L1}, \tag{4.6}$$

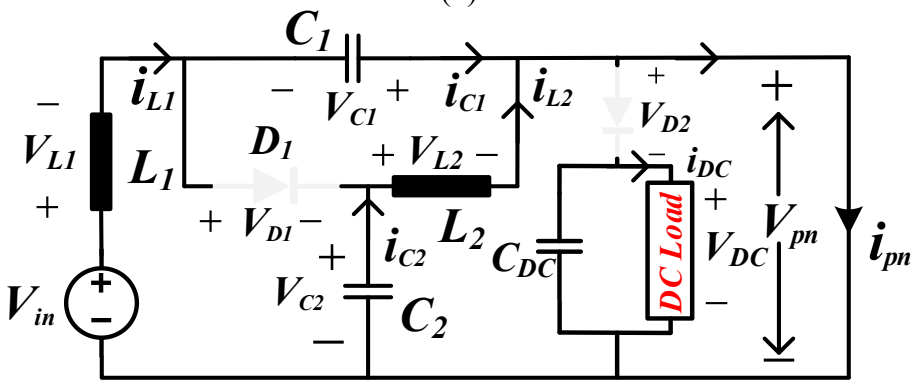
$$C_2 \frac{dV_{c2}}{dt} = i_{C2} = -i_{L2}, \tag{4.7}$$



(a)



(b)



(c)

Figure 4.2: Circuit diagram of the proposed (a) parallel, (b) series version and (c) equivalent circuit diagram during the ST interval of the single-phase hybrid multi-outputs converters.

During this interval, the diode D_2 is reverse biased and hence the DC filter capacitor C_{DC} discharges through the resistive DC load (R_{DC}). The expression for DC current (i_{DC}) is

$$C_{\mathrm{DC}} \frac{dV_{\mathrm{CDC}}}{dt} = -i_{DC} = -\frac{V_{DC}}{R_{DC}}, \tag{4.8}$$

where i_{C1}, i_{C2}, i_{L1}, i_{L2} and i_{DC} are the current through the capacitors, inductors and DC network.

4.3.2 Power Interval

The equivalent circuits of parallel and series version of the proposed QSPHCs are shown in Figures 4.3(a) and (b), respectively. To illustrate the circuit behaviour during the power interval, the circuit is simplified by replacing the single-phase inverters by an inverted current source with potential V_{pn}, as shown in Figure 4.3(c). During the power interval, the diodes D_1 and D_2 are forward biased and hence the voltages across them are zero. The capacitors C_1 and C_2 is charged by energy released from the inductors L_1 and L_2, respectively. During this interval, not all the switches are turned ON at the same time and the AC output units behave like a traditional voltage source inverter [102]-[106]. Therefore, by applying KVL in Figure 4.3(c), the voltage across inductors L_1 and L_2 are

$$L_1 \frac{di_{L1}}{dt} = V_{L1} = V_{in} - V_{c2} \tag{4.9}$$

$$L_2 \frac{di_{L2}}{dt} = V_{L2} = -V_{c1} \tag{4.10}$$

Since during the power interval, the AC output units behave like traditional VSIs, the V_{pn} is not zero. The switch node voltage in this case is the summation of V_{c1} and V_{c2}, which gives

$$V_{pn} = V_{c1} + V_{c2} \tag{4.11}$$

The diode voltages and currents in this interval are given as

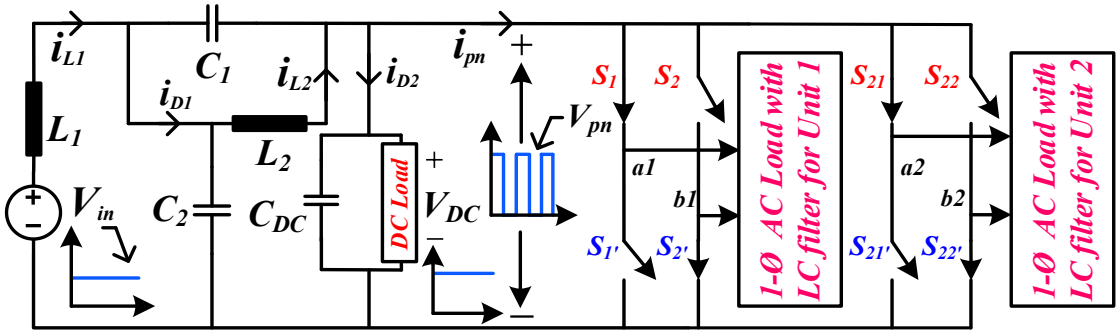
$$V_{D1} = V_{D2} = 0 \tag{4.12}$$

$$i_{D1} = i_{L1} + i_{D2} - i_{pn} \quad \text{and} \quad i_{D2} = i_{CDC} + i_{DC} \tag{4.13}$$

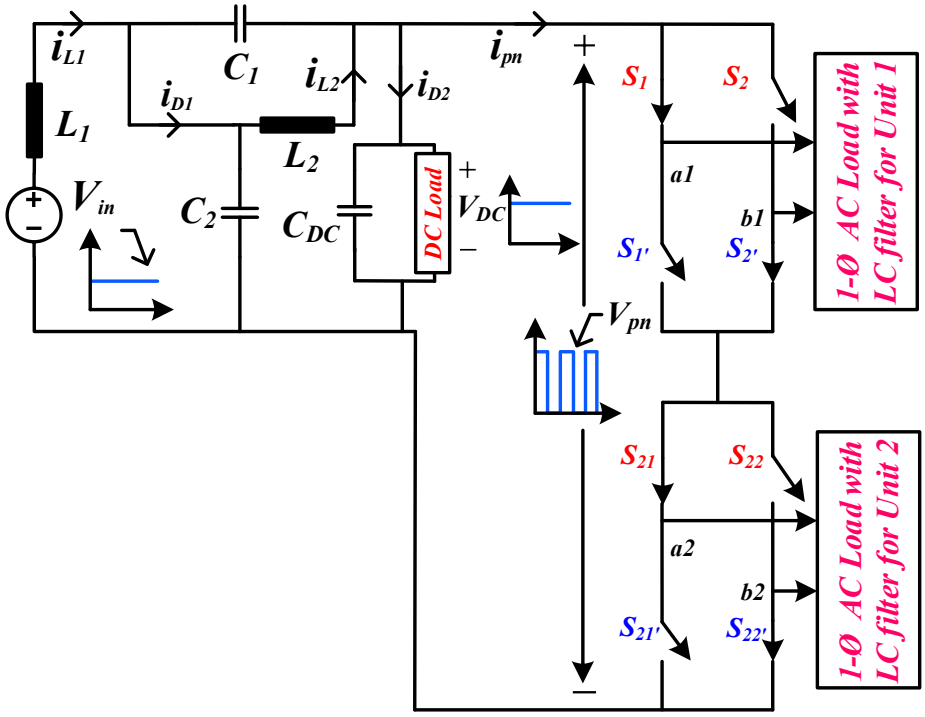
Applying KCL in Figure 4.3(c), the current through the capacitors C_1 and C_2 are given as

$$C_1 \frac{dV_{C1}}{dt} = i_{C1} = i_{L1} - i_{D1} \tag{4.14}$$

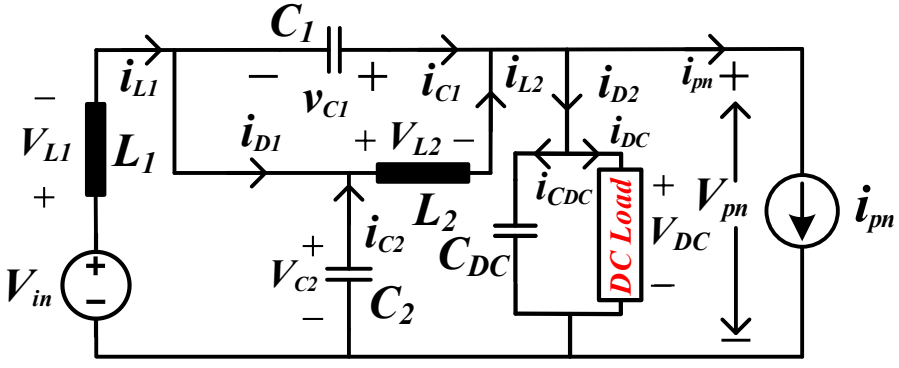
$$C_2 \frac{dV_{C2}}{dt} = i_{C2} = i_{L2} - i_{D1} \tag{4.15}$$



(a)



(b)



(c)

Figure 4.3: Circuit diagram of the proposed (a) parallel, (b) series version and (c) equivalent circuit diagram during power interval of the single-phase hybrid multi outputs converters.

Considering the average voltage across the inductors and average current through the capacitors zero under the steady-state condition and subsequently using flux balance principle on inductors L_1 and L_2, from (4.1) -(4.2) and (4.9) -(4.10) the followings are obtained

$$L_1 \frac{di_{L1}}{dt} = V_{L1} = d\ (V_{in} + V_{c1}) + (1- d)\ (V_{in} - V_{c2}) = 0 \tag{4.16}$$

$$L_2 \frac{di_{L2}}{dt} = V_{L2} = d\ (V_{c2}) + (1- d)\ (-V_{c1}) = 0 \tag{4.17}$$

Solving (4.16) and (4.17), the following expressions of V_{c1} and V_{c2} are obtained.

$$V_{c1} = \frac{d}{(1-2d)} V_{in} \text{ and } V_{c2} = \frac{(1-d)}{(1-2d)} V_{in} \tag{4.18}$$

By using charge balance principle on (4.6) -(4.7) and (4.14) -(4.15) the following are obtained.

$$C_1 \frac{dV_{c1}}{dt} = i_{C1} = d\ (-i_{L1}) + (1- d)\ (i_{L1} - i_{D1}) = 0 \tag{4.19}$$

$$C_2 \frac{dV_{c2}}{dt} = i_{C2} = d\ (-i_{L2}) + (1- d)\ (i_{L2} - i_{D1}) = 0 \tag{4.20}$$

Solving the (4.19) and (4.20), the following expressions of i_{L1} and i_{L2} are obtained

$$i_{L1} = \frac{(1-d)}{(1-2d)} i_{D1} \text{ and } i_{L2} = \frac{(1-d)}{(1-2d)} i_{D1} \tag{4.21}$$

The peak switch node voltage across the inverters $\hat{V}_{pn}$ is

$$\hat{V}_{pn} = V_{c1} + V_{c2} \tag{4.22}$$

4.3.3 DC Voltage Gain

Solving (4.18) and (4.22), the peak switch node voltage of the proposed converters is given as

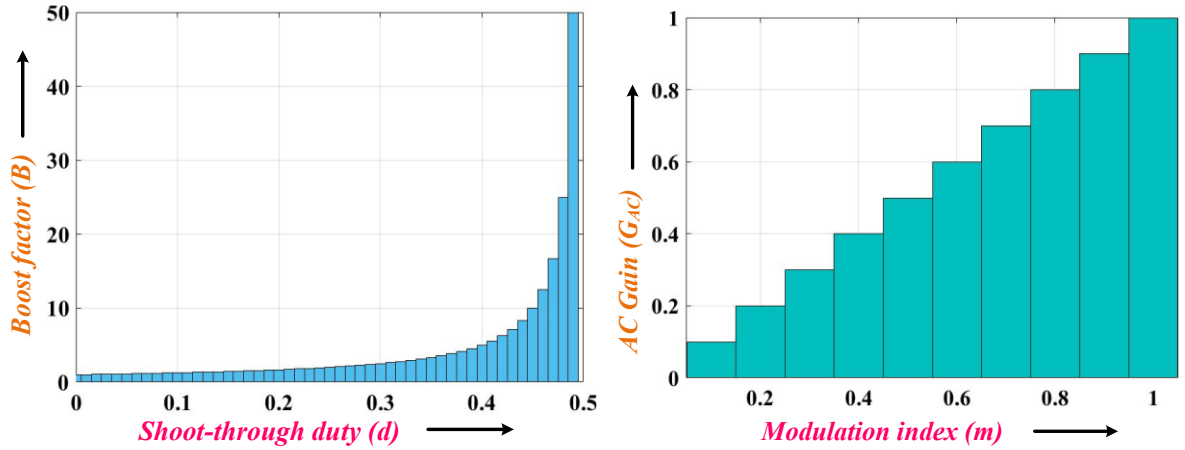
$$\hat{V}_{pn} = \frac{d}{(1-2d)} V_{in} + \frac{(1-d)}{(1-2d)} V_{in} \tag{4.23}$$

$$\hat{V}_{pn} = \frac{1}{(1-2d)} V_{in} \tag{4.24}$$

$$\left.\begin{aligned} \hat{V}_{pn} &= B\ V_{in} \\ \frac{\hat{V}_{pn}}{V_{in}} &= GDC = B \end{aligned}\right\} \tag{4.25}$$

In (4.24), the term $\frac{1}{(1-2d)}$ is known as the boost factor (B) and in (4.25) the ratio $\frac{\hat{V}_{pn}}{V_{in}}$ is known as the DC voltage gain (G_{DC}) of the proposed converters.

As the ST duty d increases, the denominator term $(1-2d)$ decreases. Consequently, $\hat{V}_{pn}$ increases. Since, $\hat{V}_{pn}$ is directly proportional to B, hence B also increases which is shown in Figure 4.4(a).



(a) (b)

Figure 4.4: The graph of (a) boost factor (B) versus ST duty d, and (b) AC gain (G_{AC}) versus modulation index (m) of the proposed converters.

4.3.4 Derivation of AC Voltage Gain

From (4.24), the peak fundamental component of the AC voltage outputs is given as

$$\hat{V}_{(AC)pk} = m\frac{1}{(1-2d)}V_{in} \tag{4.26}$$

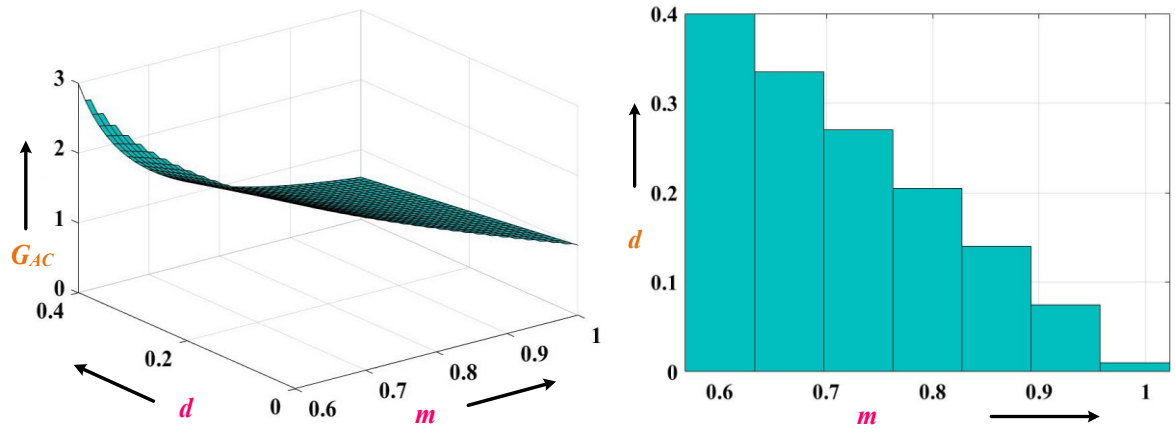
From (4.25) and (4.26),

$$\hat{V}_{(AC)pk} = mBV_{in} \tag{4.27}$$

$$\hat{V}_{(AC)pk} = m\hat{V}_{pn} \tag{4.28}$$

$$\frac{\hat{V}_{(AC)pk}}{\hat{V}_{pn}} = G_{AC} = m \tag{4.29}$$

From (4.29), the ratio of peak AC voltage $\hat{V}_{(AC)pk}$ to switch $\hat{V}_{pn}$ is known as AC voltage gain (G_{AC}), which is directly proportional to the modulation index m. Therefore, as m increases, G_{AC} also increases in a linear manner, which can be seen from Figure 4.4(b). Figure 4.5(a) shows the three dimensional view of the proposed converters with G_{AC}, d and m. In (4.27), as d and m increases, G_{AC} also increases. At $d = 0.4$ and $m = 0.6$, the $G_{AC} = 3$ at constant V_{in}.



(a) (b)

Figure 4.5: The graph of (a) G_{AC} versus d and m, and (b) operating region of the proposed converters.

The duty ratio of the ST mode is limited to (1–m) for hybrid converters inverters (i.e. $m + d$)≤ 1. As a result, the suggested converters have a maximum DC–AC inversion voltage gain (G_{AC}), achieved by putting d = (1–m) in (4.26).

$$\frac{\hat{V}_{(AC)pk}}{V_{in}} = G_{AC} = \frac{m}{(2m-1)} \tag{4.30}$$

$$\text{Since, } m + d \leq 1 \quad \Rightarrow \quad d = (1-m) \tag{4.31}$$

The term ($m + d \leq 1$), represents the operating region of the proposed converters, which is shown in Figure 4.5(b). At m = 0.6 the value of d obtained form (4.31) is 0.4, which can be verified from Figure 4.5(b).

4.4 Mathematical Expression for AC and DC Power

The following subsections represent the mathematical expression for AC and DC power for parallel and series versions with two inverter units (n = 2).

4.4.1 AC and DC Power for the Parallel Version Converters

In parallel version of the proposed converters, both the AC output units are connected in parallel with the quasi-Z-source network. Therefore, the output of the quasi-Z-source network (i.e. switch node voltage V_{pn}) is the input for the inverter units and this is same for both the units. In voltage control, the peak AC voltage ($\hat{V}_{(AC1)pk}$ and $\hat{V}_{(AC2)pk}$) of inverter units

1 and 2 are same for the same reference AC peak voltage, V_{ref} and balanced AC load. For different V_{ref}, $\hat{V}_{(AC1)pk}$ and $\hat{V}_{(AC2)pk}$ are different. Thus from (4.26), the peak AC voltage of inverter units 1 and 2 for same reference V_{ref} is given as

$$\hat{V}_{(AC1)pk} = \hat{V}_{(AC2)pk} = \frac{m}{(1-2d)} V_{in} \tag{4.32}$$

The rms AC output voltages of inverter units 1 and 2 at same value of V_{ref} is expressed as

$$V_{(\text{AC1})\text{rms}} = V_{(\text{AC2})\text{rms}} = \frac{m}{\sqrt{2}(1-2d)} V_{in} \tag{4.33}$$

The single-phase AC power output ($P_{1\text{-}\emptyset}$) of inverter units 1 and 2 is expressed as

$$P_{(1-\emptyset)} = 2\frac{V^2(\text{AC})\text{rms}}{R_{\text{AC}}} \tag{4.34}$$

The single-phase AC power output ($P_{1\text{-}\emptyset}$) of inverter unit 1 and 2 from (4.33) and (4.34) is

$$P_{(1-\emptyset)} = \frac{m^2\, V^2 in}{R_{\text{AC}}(1-2d)^2} \tag{4.35}$$

From (4.24) and (4.35), the $P_{(1-\emptyset)}$ for both the units in term of B at same V_{ref} is given as

$$P_{(1-\emptyset)} = \frac{m^2\, B^2\, V^2 in}{R_{\text{AC}}} \tag{4.36}$$

Similarly, the $P_{(1-\emptyset)}$ for both the units at different V_{ref} is given as

$$P_{(1-\emptyset)} = \frac{(m_1{}^2 + m_2{}^2)\, B^2\, V^2 in}{R_{\text{AC}}} \tag{4.37}$$

where m_1 and m_2 are the modulation indices of the inverter units 1 and 2, respectively and R_{AC} is the AC load resistance.

The DC output power P_{DC} of the proposed converter in parallel version is given by

$$P_{\text{DC}} = \frac{V^2\text{DC}}{R_{\text{DC}}} \quad \Rightarrow \frac{V^2 in}{R_{\text{DC}}(1-2d)^2} \tag{4.38}$$

where R_{DC} is the DC load resistance. From (4.37), it can be seen that $P_{(1-\emptyset)}$ depends on m and d both, whereas the DC output power P_{DC} depends on d only.

4.4.2 AC and DC Power for the Series Version Converters

In the proposed series version converters, AC output units 1 and 2 are connected in

series. The switch node voltage (V_{pn}) across both the AC output units are equally divided (i.e. $V_{pn}/2$ for each unit) for the balanced AC load. Therefore, the peak AC output voltage of inverter units 1 and 2 are same for equal reference voltage (V_{ref}) and are given by

$$\hat{V}_{(AC1)pk} = \hat{V}_{(AC2)pk} = \frac{m}{2(1-2d)} V_{in} \tag{4.39}$$

The rms AC output voltage of inverter units 1 and 2 at same reference voltage are given as

$$V_{(AC1)rms} = V_{(AC2)rms} = \frac{m}{2\sqrt{2}(1-2d)} V_{in} \tag{4.40}$$

The single-phase AC power output ($P_{1\text{-}\emptyset}$) of output units 1 and 2 at the same V_{ref} is express as

$$P_{(1-\emptyset)} = 2\frac{V^2{}_{(AC)rms}}{R_{AC}} \tag{4.41}$$

From (4.40) and (4.41), $P_{(1\text{-}\emptyset)}$ for both the inverter units are given by

$$P_{(1-\emptyset)} = \frac{m^2\, V^2{}_{in}}{8(1-2d)^2 R_{AC}} \tag{4.42}$$

Since the term $\frac{1}{(1-2d)}$ is equal to the boost factor (B) of the converters, hence from (4.42)

$$P_{(1-\emptyset)} = \frac{m^2\, B^2\, V^2{}_{in}}{8R_{AC}} \tag{4.42}$$

The DC output power P_{DC} of the series version converter is same as that of parallel version and depends on d as given in (4.38). Therefore, as d increases, P_{DC} also increases and vice-versa. However, P_{AC} can be varied by varying the m.

4.5 Voltage and Current Stresses

The voltage and current stresses of each component of the proposed converters are given in Table 4.1. In the case of parallel version, if number of AC output units increases, the current stress on L_1, L_2 and D_1 increase, since these elements depends upon the currents i_{in} i_{pn}. As the dc-link voltage V_{pn} is dependent only on constant ST duty d, therefore V_{pn} remains constant consequently voltage stress on capacitors (C_1 and C_2) and diodes (D_1 and D_2) will remain constant with increase in the units. However, in series version, as the number of inverter

unit increases, V_{pn} also increases to get the desired output voltage and therefore the voltage stresses on capacitors and diodes increase, however the current stresses remain constant.

TABLE 4.1. Voltage and Current Stresses of the of the Component

Parameters	Voltage Stresses	Parameters	Current Stresses
C_1	$\frac{(d)\,V_{in}}{(1-2d)}$	L_1	i_{in}
C_2	$\frac{(1-d)\,V_{in}}{(1-2d)}$	L_2	$\frac{(1-d)\,i_{pn}}{(1-2d)}$
C_{DC}	$\frac{V_{in}}{(1-2d)}$	D_1	$\frac{i_{pn}}{(1-2d)}$
D_1 , D_2	$\frac{V_{in}}{(1-2d)}$	D_2	$\frac{i_{DC}}{(1-d)}$

4.6 Passive Components Design

In switched LC quasi-Z-source networks of proposed QSPHCs, the inductors and capacitors are designed to keep the inductors' ripple current and capacitors' ripple voltage with in the safe limit. Thus, form (4.1) and (4.2), for the proposed converters, the inductors and capacitors are designed as follow:

$$L_1 = \frac{(V_{L1})*dt}{di_{L1}} \tag{4.44}$$

$$\Rightarrow L_1 = \frac{(V_{in}+V_{c1})*d}{\%\Delta i_{L1}*i_{L1}*f_s} \tag{4.45}$$

Similarly, the expression for inductor L_2 is

$$L_2 = \frac{(V_{L2})*d}{\%\Delta i_{L2}*i_{L2}*f_s} \tag{4.46}$$

From (4.6) and (4.7), the expression for capacitors C_1 and C_2 are given as

$$C_1 = \frac{i_{C1}*d}{\%\Delta V_{C1}*V_{C1}*f_s} \tag{4.47}$$

$$C_2 = \frac{i_{C2}*d}{\%\Delta V_{C2}*V_{C2}*f_s} \tag{4.48}$$

where V_{L1} and V_{L2} are the voltage across the inductors L_1 and L_2 and i_{L1} and i_{L2} are the current through the inductors L_1 and L_2. During ST interval (d), the term Δi_{L1} and Δi_{L2} indicate the percentage ripple current in inductors L_1 and L_2. Similarly, V_{C1} and V_{C2} represent the voltage across the capacitors C_1 and C_2 and i_{C1} and i_{C2} are the currents flowing through the capacitors C_1 and C_2. ΔV_{C1} and ΔV_{C2} represent the percentage ripple voltage in capacitors C_1 and C_2. f_s is the switching frequency of the proposed converters.

The typical values of Δi_{L1} and Δi_{L2} lie in the range of 10-20% of the inductors currents i_{L1} and i_{L2}. Allowing Δi_{L1} and Δi_{L2} to rise is undesirable since they increase the value of inductors and semiconductor switching devices peak currents, as well as their size and cost. As a result, when compared to the i_{L1} and i_{L2}, the inductor current ripples ($\Delta i_{L1}$and Δi_{L2}) are typically small. Similarly, the range of the voltage ripple (ΔV_{C1} and ΔV_{C2}) lie in the range of 1-5% of the capacitors voltages V_{C1} and V_{C2}.

From (4.1), (4.2), (4.18) and power balance equation ($V_{in} i_{in} = P_0, i_{in} = i_{L1}$) the corresponding voltage and current expression of the proposed converters are

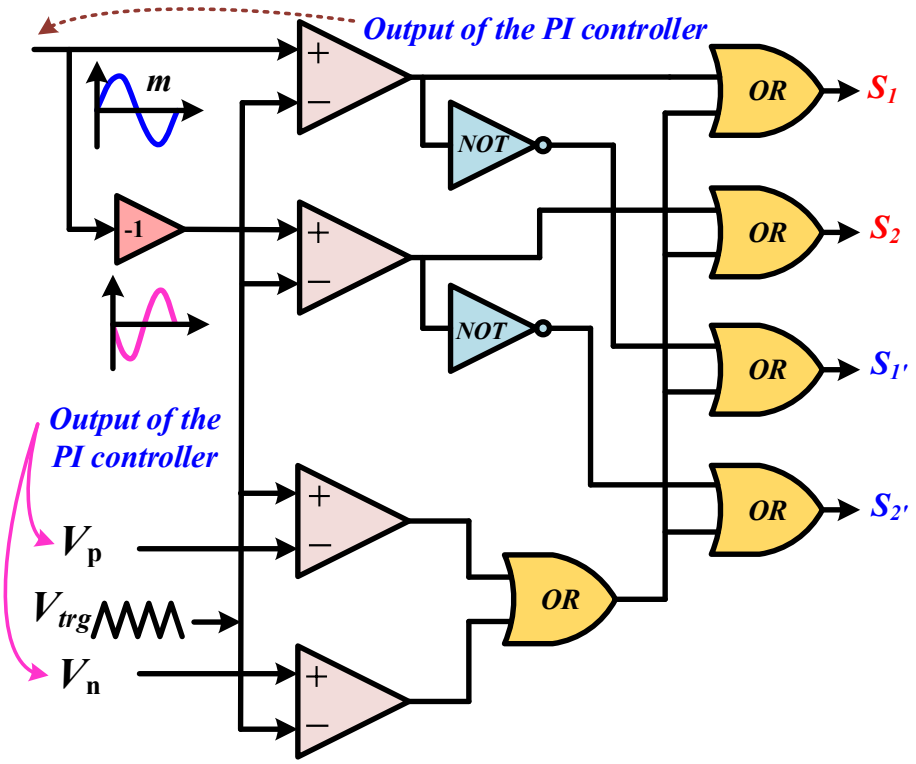
$$\left.\begin{aligned} V_{L1} &= V_{L2} = \frac{(1-d)}{(1-2d)} V_{in} \\ i_{L1} &= i_{L2} = \frac{P_0}{V_{in}} \\ V_{C1} &= \frac{(d)}{(1-2d)} V_{in} \\ V_{C2} &= \frac{(1-d)}{(1-2d)} V_{in} \\ i_{C1} &= i_{C2} = \frac{P_0}{V_{in}} \end{aligned}\right\} \tag{4.49}$$

where P_0 is the output power of the proposed converters. By substituting (4.49) in (4.45), (4.46), (4.47) and (4.48), the inductance and capacitance values are obtained as follows:

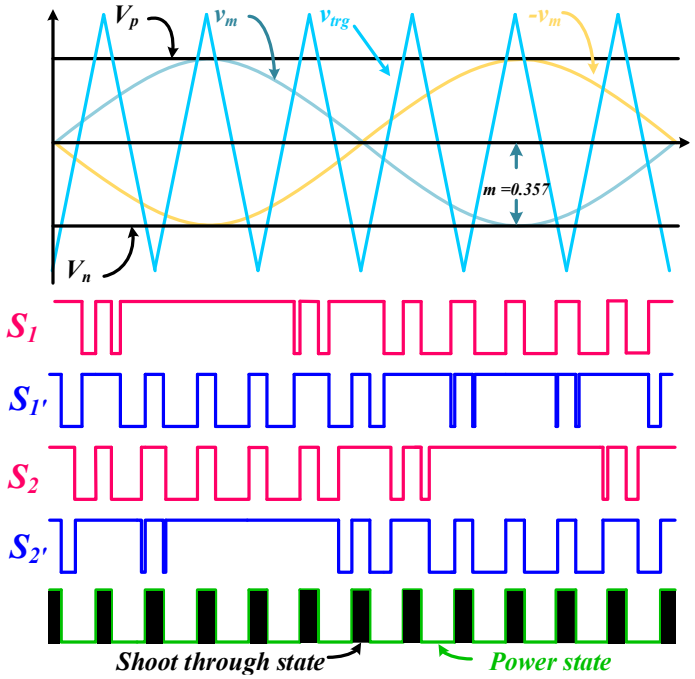
$$\left.\begin{aligned} L_1 &= \frac{d*(1-d)*V^2{}_{in}}{\%\Delta i_{L1}*P_o*f_s*(1-2d)} \\ L_2 &= \frac{d*(1-d)*V^2{}_{in}}{\%\Delta i_{L2}*P_o*f_s*(1-2d)} \\ C_1 &= \frac{P_o*(1-2d)}{\%\Delta V_{C1}*V^2{}_{in}*f_s} \\ C_2 &= \frac{P_o*(1-2d)*d}{\%\Delta V_{C2}*(1-d)*V^2{}_{in}*f_s} \end{aligned}\right\} \tag{4.50}$$

4.7 Hybrid Pulse Width Modulation (HPWM) Technique

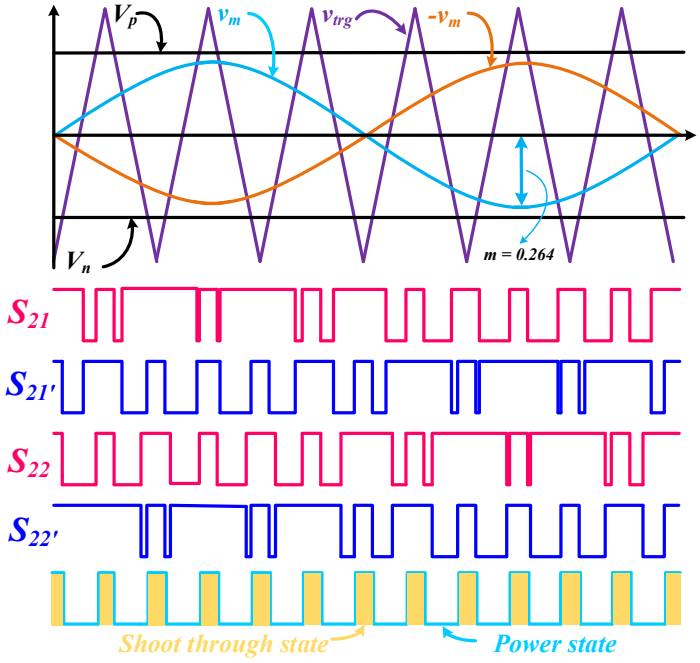
To control the outputs of the proposed converters, hybrid pulse width modulation (HPWM) technique is used. One switching cycle contain both ST and power interval in HPWM [107]-[112]. Figure 4.6(a) shows the schematic diagram of HPWM control logic circuit for the proposed converters. The HPWM control technique is realized using comparator, OR and NOT gates. In this equivalent model, two-reference sinusoidal signals of opposite phases (v_m and -v_m) are used having a maximum amplitude of m. The two sinusoidal signals are compared with the high frequency triangular carrier waveform v_{trg} and the resultant signals are used to drive the top and bottom switches of leg a and leg b of the proposed converters. For generating ST signal two constant DC voltages, V_p (positive DC) and V_n (negative DC) are compared with the carrier v_{trg}. The ST signals are generated when v_{trg} is greater or less than the V_p (positive DC) and V_n (negative DC). In this way, the inverter switches S_1–$S_{1'}$, S_2–$S_{2'}$, S_{21}–$S_{21'}$ and S_{22}–$S_{22'}$ are controlled by the same PWM signals.



(a)



(b)



(c)

Figure 4.6: Hybrid modulation scheme for proposed converters when both converters are at different V_{ref} (a) Schematic diagram of modulation scheme, (b) and (c) PWM pulses of inverter unit 1 and 2 during parallel version operation with V_{ref} = 125 and 100 V, respectively.

Figures 4.6(b) and (c) show the PWM signal of the proposed QSPHCs during parallel operation, when units 1 and 2 have different reference voltages, V_{ref1} = 125 V and V_{ref2} =100 V with modulation index m_1 = 0.357 and m_2 = 0.246 and d = 0.33 (Figure 4.11(a)).

4.8 Close-Loop Implementation of the Proposed Converters

Figure 4.7 shows the complete closed loop control scheme (both AC and DC output control) of QSPHCs. The sensed single-phase AC output voltage from the proposed converter is considered as V_α. To get V_β, V_α is delayed by 90° to generate components similar to Clarke transformation in a three-phase system. The components V_α and V_β further undergo Park's transformation to yield stationary V_d and V_q components and compared with the reference *dq* voltages $V_{d(ref)}$ and $V_{q(ref)}$. By comparing V_d and V_q with $V_{d(ref)}$ and $V_{q(ref)}$, an error signal is generated and then the error signal is passed through a PI controller. The output of the PI controller gives further undergo inverse park's transformation to yield the sinusoidal modulating signal *m*. Further, to control the DC output voltage, (V_{DC}) is sensed and compared with the reference DC voltage $V_{DC(ref)}$ and the resultant output is passed through the PI controller, which results in positive constant DC voltage V_p. The V_p is multiplied with -1 to get the negative constant DC voltage V_n. Finally, modulating signal *m*, V_p and V_n are compared with the triangular carrier wave to generate the switching signals.

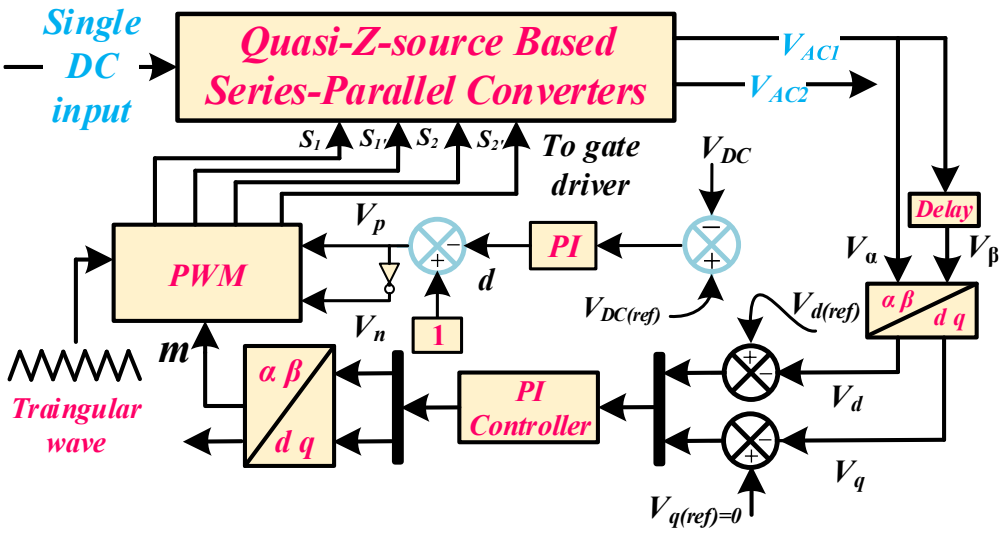


Figure 4.7: closed loop control scheme.

4.9 Verification of the Proposed Converters

Figure 4.8 shows the overall concept of the proposed converters' scheme, which can be

connected to independent load or grid. It consists a quasi-Z-source network, a DC network and series-parallel connected *n* number of AC output units. The simulation of the proposed converters is done using MATLAB 2017a software. At a switching frequency of 10 kHz and a line frequency of 50 Hz, Table 4.2 lists the values of passive elements employed in the proposed converters in the simulation studies. The steady-state and dynamic analysis are done in the following subsections.

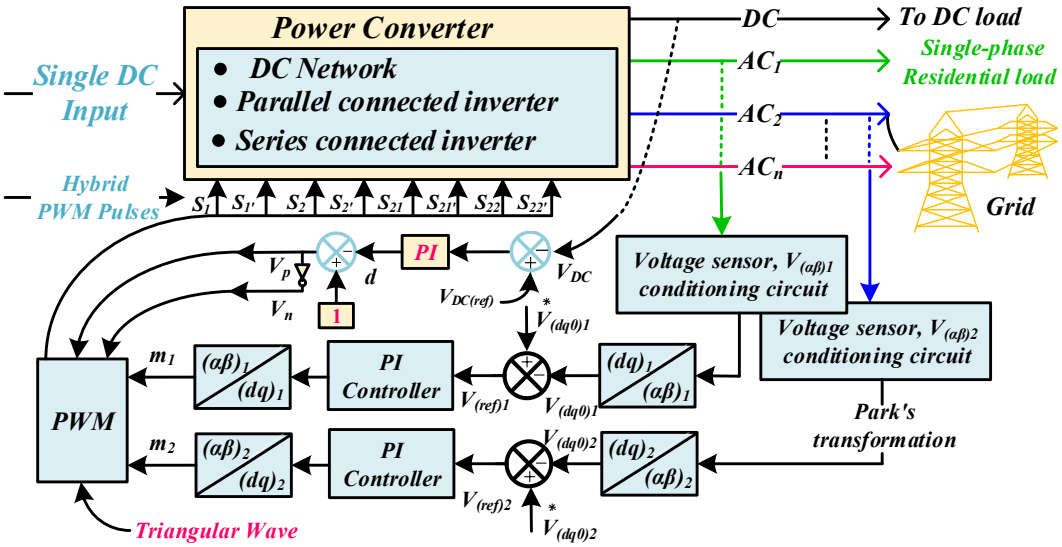


Figure 4.8: Overall concept for the proposed converters.

TABLE 4.2

LIST OF PARAMETERS WITH THEIR ATTRIBUTES

Parameters	Attributes
Inductors	$L_1 = L_1 = 5$ mH
Capacitance	$C_1 = C_2 = C_3 = 470$ µF
AC and DC load resistance	$R_{AC} = 20$ Ω, $R_{DC} = 100$ Ω
Fundamental Frequency	50 Hz
Filter inductors and Capacitors	$L_f = 2$ mH and $C_f = 10$ µF

4.9.1 Simulation of the Proposed Parallel Version Converters (Dual AC with Single Boost DC Outputs)

In this chapter, the proposed parallel version is justified for 2.225 kW with AC (P_{AC} = 781 W) and DC power (P_{DC} = 1444 W), while the input voltage V_{in} = 130 V.

4.9.1.1 Steady-State Results at Same Reference AC Voltage (V_{ref} = 125 V)

Figure 4.9 and Figure 4.10 show the steady-state results of the proposed converters during parallel version, while the DC and AC reference peak voltages are V_{dcref} = 380 V, V_{ref} = 125 V, and input voltage V_{in} = 130 V. Figure 4.9(a) shows the input voltage V_{in} = 130 V, switch node voltage V_{pn} = 380 V and inductor currents i_{L1} and i_{L2} = 17.2 A, which is also equal to the input current (i_{in}). During the ST interval V_{pn} = 0 V and inductors L_1 and L_2 are charged and subsequently start discharging during power interval, when V_{pn} = 380 V. Figure 4.9 (b) shows V_{in} = 130 V, capacitors voltage V_{C1} = 125 V and V_{C2} = 255 V and voltage across the diode (V_{D1} = -380 V). During the ST interval, the diodes D_1 and D_2 are open circuited and hence voltage

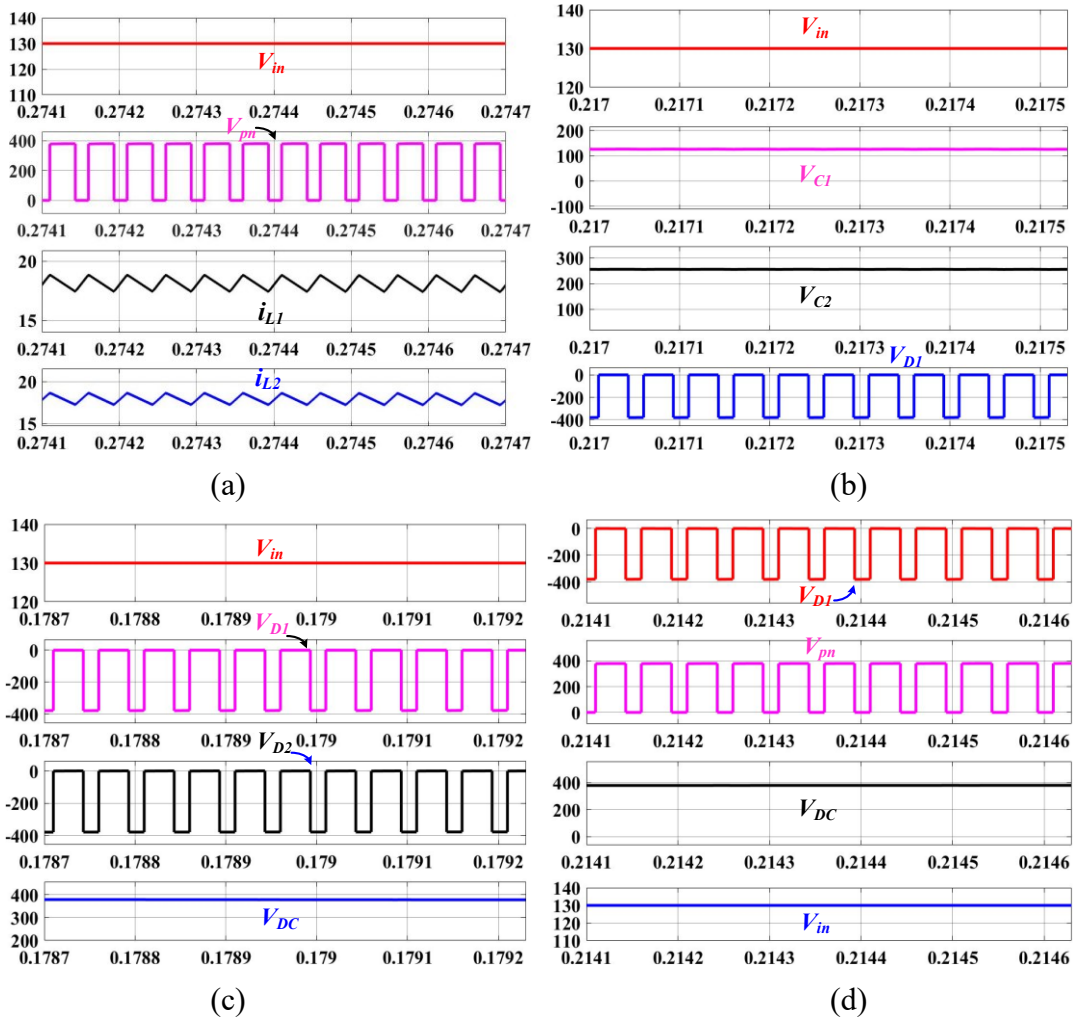


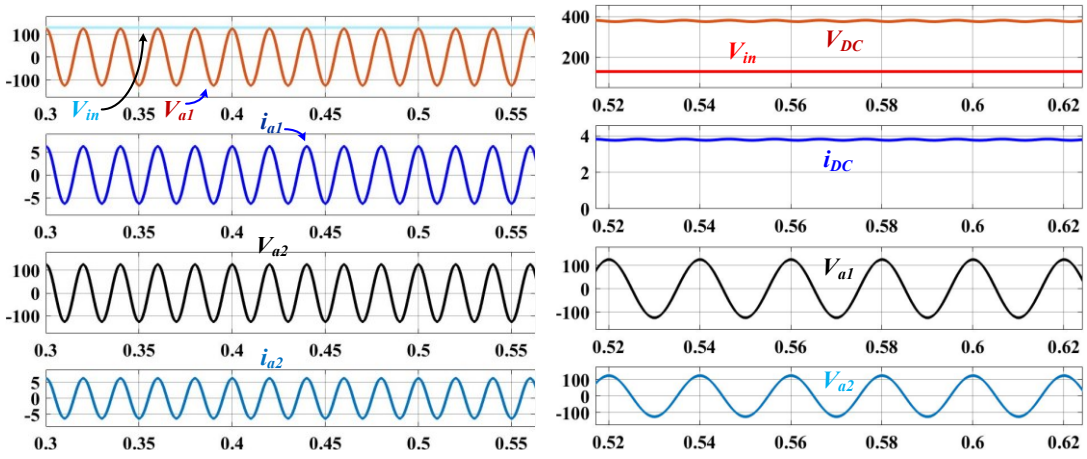
Figure 4.9: Steady-state results of the parallel version at V_{dcref} = 380 V and V_{ref} = 125 V, (a) input voltage (V_{in}), dc-link voltage (V_{pn}) and inductors current, (b) capacitor voltages with input and diode voltage, (c) diode voltages (V_{D1} and V_{D1}) with V_{in} and DC output voltage (V_{DC}), (d) diode voltage (V_{D1}), V_{pn}, V_{DC} and input voltage V_{in}.

across D_1, $V_{D1} = V_{C1} + V_{C2}$. During the power interval, D_1 and D_2 are short circuited and hence voltage across them $V_{D1} = V_{D2} = 0$ V. Figure 4.9(c) shows $V_{in} = 130$ V, $V_{D1} = V_{D2} = -380$ V and DC output voltage $V_{DC} = 380$ V. Figure 4.9(d) shows voltage across (D_1), switch node voltage V_{pn}, $V_{DC} = 380$ V and $V_{in} = 130$ V. In the ST interval, when all the switches of both the inverters are turned ON, the switch node voltage $V_{pn} = 0$ V and D_1 is reverse biased and hence $V_{D1} = -380$ V. The diode D_1 is forward biased in power interval and hence $V_{D1} = 0$ V and $V_{pn} = 380$ V, which can be verified from (4.3), (4.4), (4.11) and (4.12).

Figure 4.10 (a) shows V_{in}, switch node voltage units 1 and 2 and current i_{D2} of the diode D_2. Since both the inverter units are connected in parallel, hence the outputs of the quasi-Z-source network V_{pn} is same for both the units and are equal to 380 V. Figure 4.10 (b) shows $V_{in} = 130$ V, $V_{pn} = 380$ V and DC output voltage and current $V_{DC} = 380$ V and $i_{DC} = 3.8$ A) as the $R_{DC} = 100$ Ω. Figure 4.10 (c) shows $V_{in} = 130$ V and phase *a* voltages and currents of inverter units 1 and 2. At the reference voltage $V_{ref} = 125$ V, the peak-to-peak (pk-pk) voltage and current magnitudes of units 1 and 2 are 250 V and 12.5 A pk-pk as the $R_{AC} = 20$ Ω. Figure 4.10(d) shows $V_{in} = 130$ V, DC output voltage and current along with phase *a* voltage of units 1 and 2, which gives the DC power output $P_{DC} = 1444$ W.

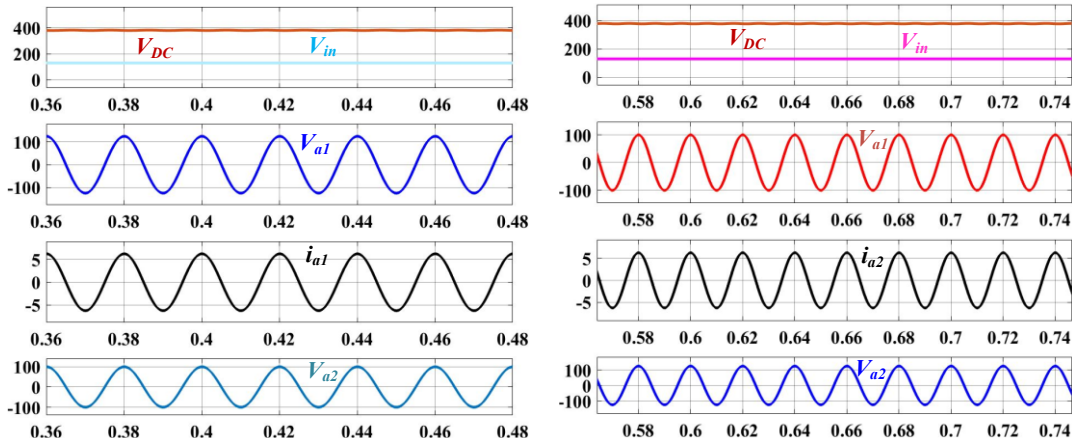
4.9.1.2 Steady-State Results at Different Reference Voltage (V_{ref})

Figure 4.11(a) shows $V_{in} = 130$ V, $V_{DC} = 380$ V, phase *a* voltage and current of inverter unit 1 and phase *a* voltage of unit 2 at $V_{ref1} = 125$ V and $V_{ref2} = 100$ V. Figure 4.11(b) shows the same results with reversed reference voltages i.e. $V_{ref1} = 100$ V and $V_{ref2} = 125$ V. In the parallel version, by changing the reference voltage (V_{ref}), both the units are operated at different powers and thus can be used for different power applications. The 380 V DC obtained here can be used in the DC distribution system or load.



(c) (d)

Figure 4.10: Steady state results of the parallel version at $V_{\text{dcref}} = 380$ and $V_{\text{ref}} = 125$ V, (a) V_{in}, dc-link voltages (V_{pn} and V_{pn1}) and diode current, (b) V_{in}, V_{pn} and DC output voltage and current (V_{DC} and i_{DC}), (c) phase *a* voltages and currents of units 1 and 2 with V_{in}, (d) V_{in}, V_{DC}, i_{DC} and phase *a* voltages of units 1 and 2.



(a) (b)

Figure 4.11: Input voltage V_{in}, DC output voltage V_{DC}, phase *a* voltages of units 1 and 2, and (a) of the parallel version, (a) phase *a* current of units 1 with $V_{\text{ref1}} = 125$ and $V_{\text{ref2}} = 100$ (b) phase *a* current of units 1 with $V_{\text{ref1}} = 100$ and $V_{\text{ref2}} = 125$.

Figures 4.12(a) and (b) show the PWM signals for leg *a* and *b* of inverter units 1 and 2 for the reference voltages $V_{\text{ref1}} = 125$ and $V_{\text{ref2}} = 100$. In the ST interval, the switches of inverter units 1 and 2; S_1–$S_{1'}$, S_2–$S_{2'}$, S_{21}–$S_{21'}$ and S_{22}– $S_{22'}$ are turned ON at the same time which results in zero switch node voltage ($V_{\text{pn}} = 0$ V) and it is equal to 380 V in power interval as the inverters work as normal VSIs. An arrow in Figure 4.12(a) [113]-[117], represents the ST interval of inverter unit 1.

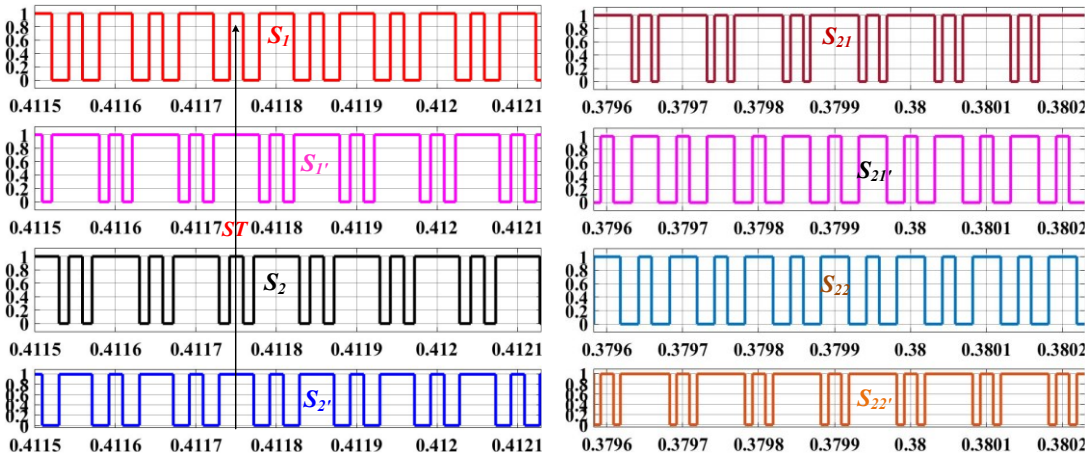


Figure 4.12: PWM signals in parallel version, (a) and (b) PWM pulses of leg *a* and *b* of inverter units 1 and 2, respectively.

4.9.1.3 Dynamic Results at the Same Reference Voltage (V_{dcref} = 380 and V_{ref} = 125 V)

Figure 4.13(a) shows the step-up AC load current dynamics in unit 1 with input voltage V_{in}, DC output voltage (V_{DC}), V_{in} and phase *a* voltage of Unit 1 and unit 2. As the AC load current of unit 1 increases from 12.5-25 A (pk-pk), the corresponding Unit 1 voltage slightly decreases and then restores to its original position without affecting unit 2 voltage and V_{DC}. Similarly, Figure 4.13(b) shows the step-down AC load current dynamics of unit 2. As the AC load current of unit 2 decreases from 25-12.5 A (pk-pk), the corresponding voltage slightly increases and then restores to its original position within a short time. However, unit 1 voltage and V_{DC} remain unaffected. Figures 4.13(c) and (d) show the step-up and step-down dynamics in DC load current. As the DC load (i_{DC}) increases from 3.8-7.6 A, the DC output voltage (V_{DC} = 380 V) first slightly decreases and then settles to its original position within a short time and vice-versa. However, phase *a* voltage (V_{a1}) and current (i_{a1}) of unit 1 and V_{a2} of unit 2 have voltage of 250 V and current magnitude of 12.5 A (pk-pk) remain unchanged. This indicates that the system is having good dynamics behaviour.

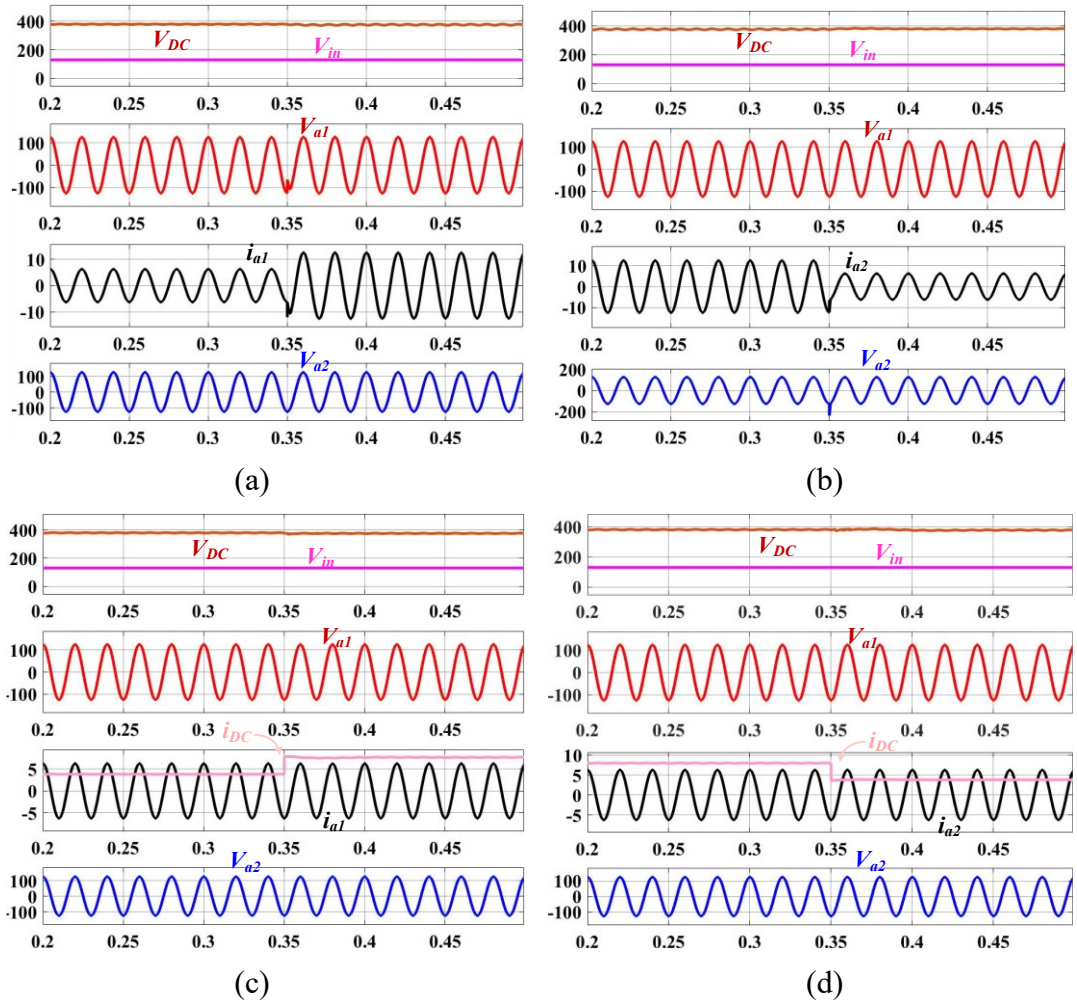


Figure 4.13: Dynamic performance in the parallel version, (a) step-up dynamics in unit 1 with unit 2, V_{DC} and V_{in}, (b) step-down dynamics in unit 2 with unit 1, V_{DC} and V_{in}, (c) step-up and (d) down dynamics in DC network with unit 1, 2 and V_{in} while V_{dcref} = 380 and V_{ref} = 125 V.

Figure 4.14(a) shows the dynamic performance with step up change in DC load current and AC load current in unit 1 simultaneously. As R_{DC} and R_{AC} load resistances change from 100 Ω to 50 Ω and 20 Ω to 10 Ω, respectively, the DC and AC load current correspondingly changes from 3.8 A to 7.6 A and 12.5 A to 25 A (pk-pk). However, the DC output voltage (380 V) and phase *a* voltage (V_{a1} = 250 V) slightly increases and settles to its original value within a short time (one cycle). Similarly, Figure 4.14(b) shows the step-down dynamics in the DC load and unit 2 load simultaneously, as R_{DC} and R_{AC} changes from 50 Ω to 100 Ω and 10 Ω to 20 Ω. The i_{DC} and i_{a2} changes from 7.6 A to 3.8 A and 25 A to 12.5 A (pk-pk). However, in Figure 4.14(a) inverter unit 2 and Figure 4.14(b) unit 1 remain unaffected.

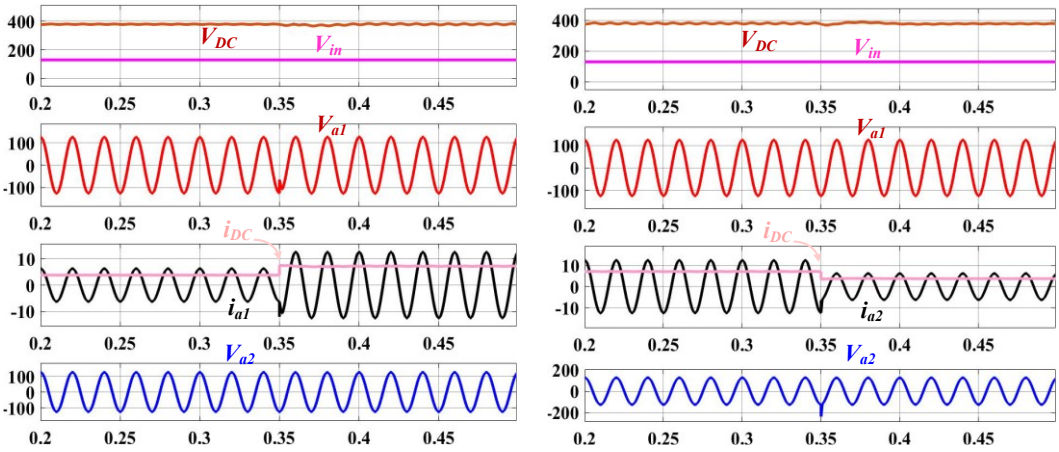


Figure 4.14: Dynamic performance (a) step-up dynamics in DC load and unit 1 load(b) step-down dynamic in DC load and unit 2 load with respect to unit 1 and V_{in} while V_{dcref} = 380 and V_{ref} = 125 V in parallel version of the proposed converters.

4.9.1.4 Dynamic Results with Different Reference Voltage (V_{ref1} = 125 and V_{ref2} = 100 V)

Figures 4.15(a) and (b) show the step-up and step-down load change dynamics in unit 1, respectively with different reference peak AC voltages (V_{ref1} = 125 V and V_{ref2} = 100 V). As the load current i_{a1} increases (Figures 4.15(a)) from 12.5 A to 25 A (pk-pk) or decreases (Figures 4.15(b)) from 25 A to 12.5 A (pk-pk), the corresponding voltage V_{a1} slightly changes and then restores to its original position within a short time. However, the DC output voltage (V_{DC} = 380 V), phase *a* voltage of unit 2 (V_{a2} = 200 V pk-pk) and V_{in} = 130 V remain unchanged. This indicates that the system is stable against load change and has good dynamic response. Similarly, Figures 4.15(c) and (d) show the step-up and step-down load change dynamics in phase *a* voltage of inverter unit 2. As the load current i_{a2} changes from 10-20 A, the corresponding voltage V_{a2} first slightly decreases and then restores to its original value within a short time and vice-versa. However, other parameters remain unaffected.

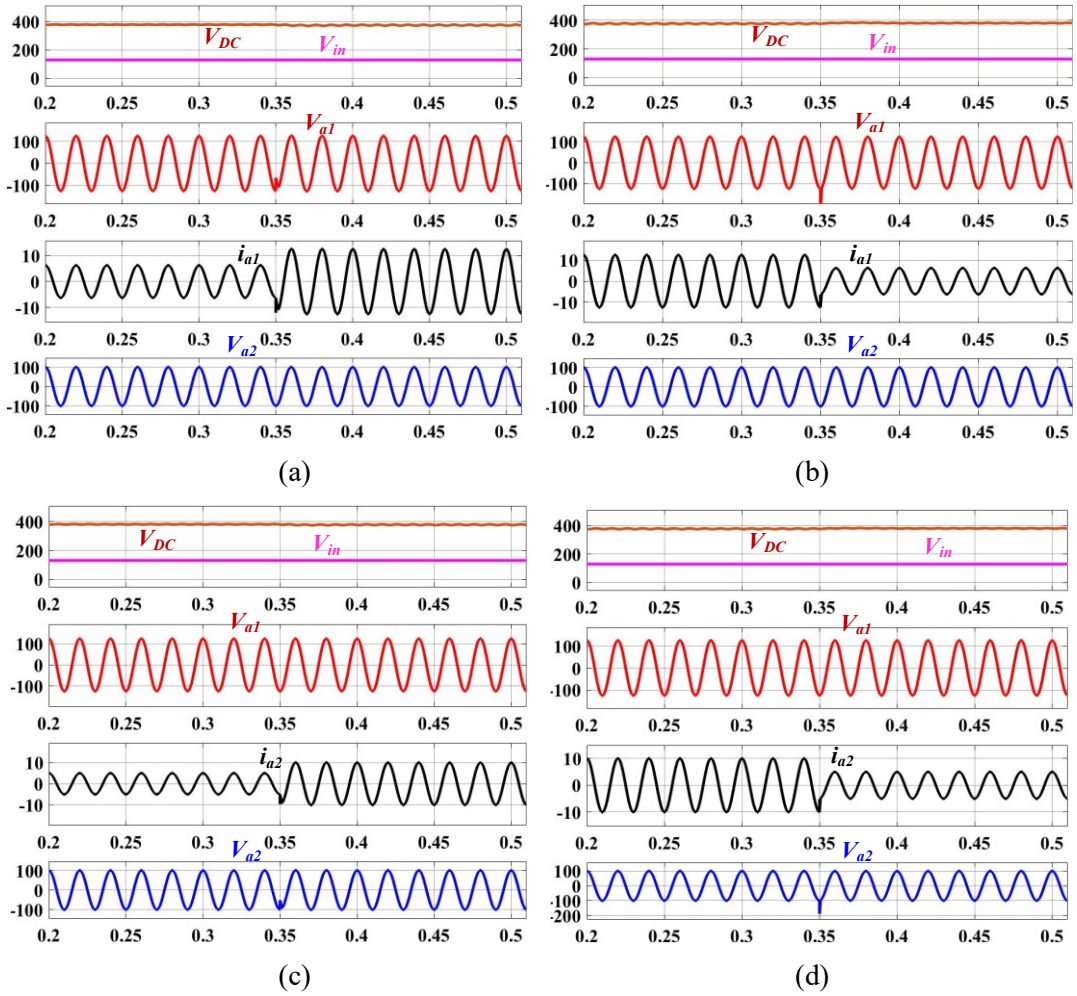


Figure 4.15: Show the (a) step-up and (b) step-down dynamics in unit 1 w.r.t. DC network, V_{in} and unit 2, (c) step-up and (d) step-down dynamics in unit 2 w.r.t. DC network, V_{in} and unit 1, while both the units are at different V_{ref}.

4.9.1.5 Dynamic Results with Buck-Boost and Different Frequency Operation

Figures 4.16(a) and (b) show the buck-boost operation with step-up and step-down dynamics in units 1 and 2, while V_{ref1} = 125 V (peak), 50 Hz, V_{ref2} = 200 V (peak), 60 Hz, and V_{dcref} = 500 V. The rms voltage of the units 1 and 2 are 88.39 and 141.42 V. Since the output rms voltage V_{rms1} = 88.39 V of unit 1 is less than the input voltage V_{in} =130 V, hence unit 1 shows voltage buck property with a frequency of 50 Hz. The output rms voltage V_{rms2} = 141.42 V of unit 2 is more than the input voltage V_{in} = 130 V, hence unit 2 shows voltage boost property with a frequency of 60 Hz. In this way, the proposed parallel version converter can perform buck-boost operations at different voltages and frequencies with boosted DC output voltage of 500 V. In addition, step-up dynamics are performed in units 1 and 2 to check the dynamic

behavior in both buck as well as boost mode. In Figure 14.6(a), as the load current increases, the corresponding voltage (V_{a1} = 250 V) slightly decreases and then settles to its original value. However, V_{a2}, V_{DC} and V_{in} remain constant at 400 V (pk-pk), 500 V and 130 V. Similarly, it is done for Figure 14.6(b) also.

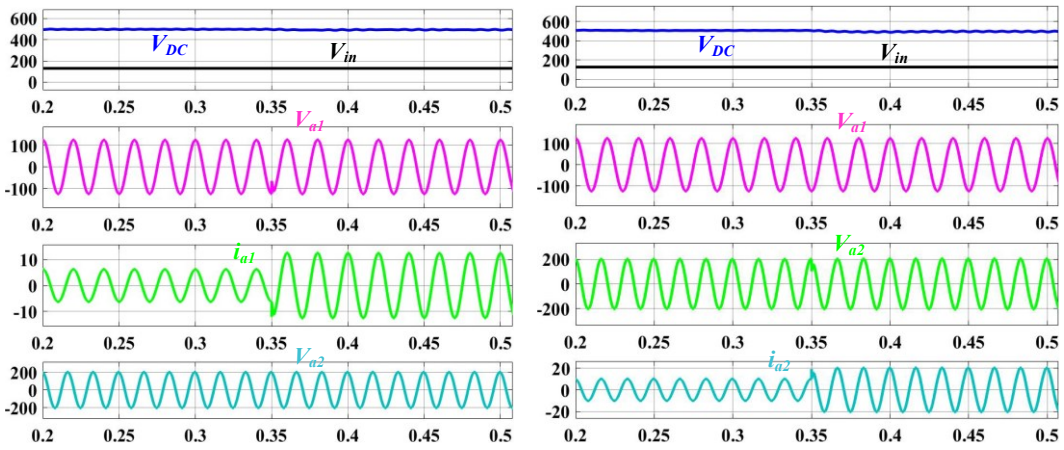


Figure 4.16: Buck-boost operation along with load change dynamics of AC output units in parallel version with V_{dcref} = 500, V_{refl} = 125 V, 50 Hz and V_{ref2} = 200 V, 60 Hz (a) Step-up dynamics in unit 1 (b) Step-down dynamic in unit 2. (unit 1 showing voltage buck property and with unit 2 showing voltage boost property)

4.9.2 Simulation of the Proposed Series Version of QSPHCs (Dual AC with Single Boost DC Outputs)

The proposed series version is justified for 2.036 kW with DC power P_{DC} = 1056 W and AC power P_{AC} = 981 W, while the input voltage V_{in} = 130 V.

Figure 4.17 shows the steady-state results of the proposed converters during series version, while the DC and AC reference voltages are V_{dcref} = 325 and V_{ref} = 140 V respectively. Figure 4.17 (a) shows the input voltage V_{in} = 130 V, switch node voltage V_{pn} = 325 V and inductors current i_{L1} and i_{L2} = 15.67 A, which are also equal to the input current (i_{in}). During the ST interval V_{pn} = 0 V and inductors L_1 and L_2 are in charging state. The inductors L_1 and L_2 start discharging during power interval and V_{pn} = 325 V. Since i_{L1} = i_{L2}, the charging and discharging nature of L_1 and L_2 are same. Figure 4.17(b) shows V_{in} = 130 V, capacitors voltage V_{C1} = 100 V and V_{C2} = 225 V and voltage across the diode (V_{D1} = -325 V).

During the ST interval, the diodes D_1 and D_2 are reversed biased and hence the voltage V_{D1} is expressed as $V_{D1} = V_{C1} + V_{C2}$. During the power interval, D_1 and D_2 are forward biased and hence voltage across them $V_{D1} = V_{D2} = 0$ V. Figure 4.17(c) shows $V_{in} = 130$ V, boost DC output $V_{DC} = 325$ V, $V_{pn} = 325$ V and voltage across diode $V_{D1} = V_{D2} = -325$ V. In the ST interval, $V_{pn} = 0$ V and the diodes are reversed biased having voltages $V_{D1} = V_{D2} = -325$ V. During the power interval, the diodes are forward biased and hence $V_{D1} = V_{D2} = 0$ V and $V_{pn} = 325$ V. Figure 4.17(d) shows phase *a* voltages of units 1 and 2 along with DC output voltage 325 V, dc load current 3.25 A. The voltage magnitude of units 1 and 2 are same and equal to 280 V (pk-pk) as they have same reference voltages 140 V.

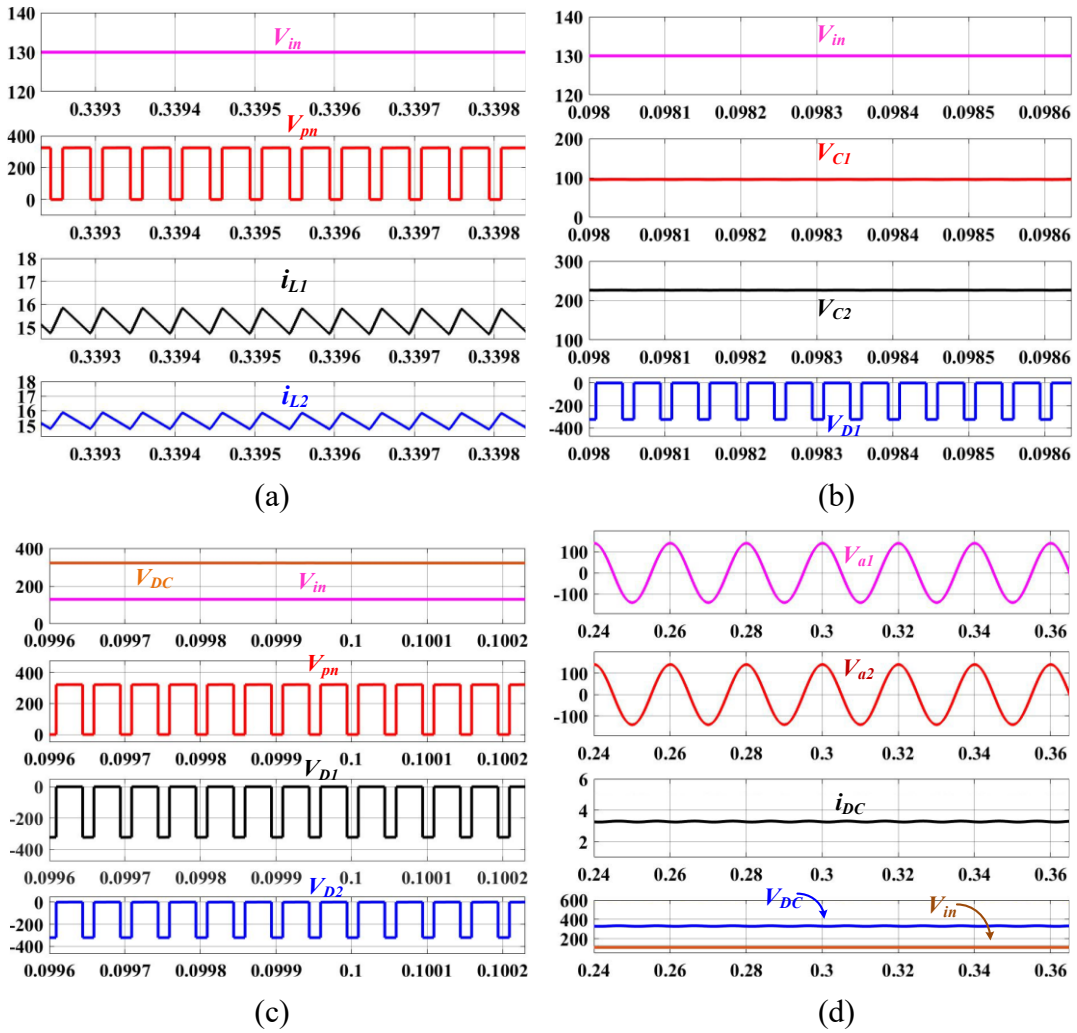


Figure 4.17: Steady state results of the series version at $V_{dcref} = 325$ V and $V_{ref} = 140$ V, (a) input voltage (V_{in}), dc-link voltage (V_{pn}) and inductors current, (b) capacitor voltages with input and diode voltage, (c) diode voltages (V_{D1} and V_{D2}) with V_{in}, V_{DC} and V_{pn}, (d) phase *a* voltages of unit 1 and 2, V_{DC} and i_{DC} with V_{in}.

4.9.2.1 Dynamic Response of Series Version by Changing the Reference Voltage

Figure 4.18 depicts the dynamic behaviour of the proposed series version converters with input voltage V_{in} = 130 V, AC and DC load resistance R_{AC} = 20 Ω and R_{DC} =100 Ω respectively. Initially, he DC and AC reference (V_{ref}) voltages are 325 V and 140 V, respectively. When V_{ref} is changed from 140 to 100 V, both inverter units respond as shown in Figure 4.18(a). The peak-peak voltage magnitude of phase *a* of units 1 and 2 changes from 280 to 200 V, resulting in a phase a current change from 14 A to 10 A (pk-pk) for both the units. Figure 4.18(b) depicts the response, when V_{ref} is increased from 100 V to 140 V. The phase *a* voltages of units 1 and 2 follow the reference voltage and eventually becomes equal to 280 V (pk-pk), with a current of 14 A. During this operation, the DC output (V_{DC}) and input voltage (V_{in}) remain constant at 325 V and 130 V, respectively. The proposed inverters settle to a new reference value in a very short time, indicating that the system is having good dynamic behaviour.

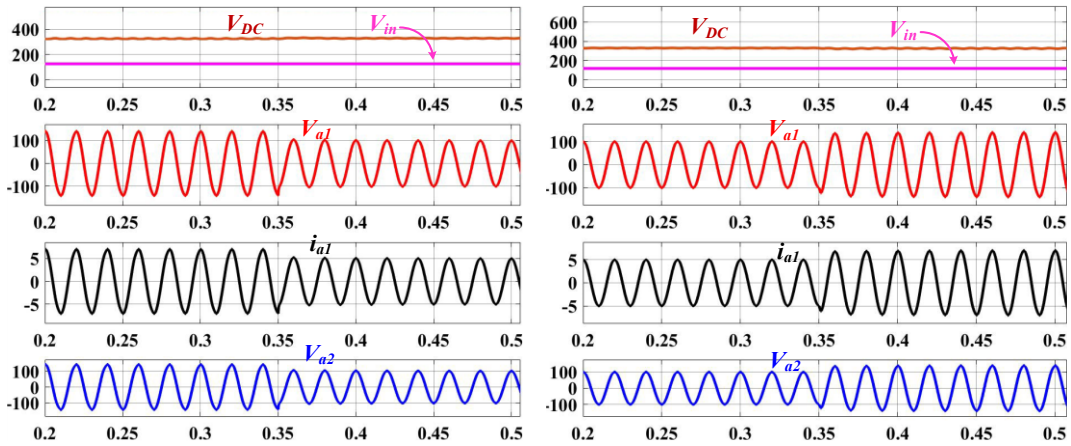


Figure 4.18: Shows the dynamic results during series version of the proposed converters (a) V_{in}, V_{DC} and phase *a* voltages and currents of inverter unit 1 and 2 when V_{ref} changes from 140 to 100 V and (b) when V_{ref} changes from 100 to 140 V.

4.10 Conclusion

This chapter presents single-phase quasi-Z-source series parallel hybrid converters (QSPHCs) with single boost DC outputs and multiple AC output with both buck and boost

properties. The proposed converters are achieved by replacing the quasi-Z-source inverter switch with *n* number of series-parallel connected inverters. In addition, a capacitor and diode combination is included in the circuit to achieve the DC output. The proposed parallel version is able to supply *n* number of single-phase AC outputs with variable load currents and one DC boost outputs. It is able to give voltage outputs not only with different magnitudes but with different frequencies also as per the requirements. Similarly, the series version of converters is capable of suppling *n* number of AC and single boost DC outputs with constant load currents. The simulation results, the proposed parallel version is justified for 2.225 kW with AC load of 781 W and DC load of 1444 W. Similarly, the proposed series version is justified for 2.036 kW with DC load of 1056 W and AC load of 981 W. In both the series and parallel mode, the simulations results verify the performed of converters for two single phase AC output units and one DC output. The proposed QSPHCs good dynamic response in case of load change as well as voltage reference change for DC output or the AC output units. Thus, the proposed hybrid converters provide reliable solution for supplying more than one flexible AC/AC load demand simultaneously using any extra adopter or voltage regulator.