CHAPTER 6

Interleaved Hybrid Converter for AC and DC Outputs

6.1 Introduction

In recent times, DC loads are gradually increasing along with existing AC loads in modern residential systems which enables a requirement of hybrid AC and DC system. Although the proposed converters (TSHGC, HGIBC and SLC-ZSIs) can be used for hybrid systems, they can only supply either AC or DC loads in their present form, which results in increase in volume and decrease in power density of the overall system. To take care of these issues, this chapter presents an interleaved hybrid converter (IHC) for a hybrid AC/DC system to supply AC and DC loads simultaneously through a single power converter. The IHC is developed from the switching concept of HGIBC and SLC-ZSIs. The operation and verification of IHC are given in the subsequent sections of this chapter.

6.2 Interleaved Hybrid Converter

Fig. 6.1 shows an IHC for simultaneous AC and DC outputs [119]. The IHC has five switches (S_a and $S_1 - S_4$), two diodes (D_a and D_b), two DC capacitors (C and C_o) and two interleaved inductors (L_1 and L_2). Further, it has DC resistive load (R_{dc}) and AC resistive load (R_{ac}) along with a second-order low pass filter (L_f and C_f). As shown in Fig. 6.1, the IHC has AC and DC outputs (V_{ac} and V_{dc}) from a single DC input voltage (V_{in}). The salient features of IHC are as follows.

- It has two operating conditions $D + M \leq 1$ and $D + M \geq 1$, unlike CHCs.
- Due to the two operating conditions, it has wider ranges of D and M which results in AC and DC outputs at desired values.
- It has continuous input current with less ripple due to interleaved inductors at the input side.
- The IHC also has better electromagnetic interference immunity due to its inherent shoot-through protection capability similar to SLC-ZSIs

The AC and DC outputs of IHC can be independently controlled because of two operating conditions, unlike CHCs. The IHC gives high voltage gain DC output and reduced harmonic

distortion in AC output due to wider ranges of D and M. Moreover, the IHC has three operating modes in the two operating conditions; (1) Mode 1 ($D + D_{st} < 1$), (2) Mode 2 ($D + D_{st} = 1$) and (3) Mode 3 ($D + D_{st} > 1$). Due to the three operating modes, the IHC has three different AC and DC voltage gains.

Although the IHC has two operating conditions, this chapter investigates the performance of IHC in the operating condition, $D + M \geq 1$ only. For analyzing the operation of IHC easily, the switches ($S_1 - S_4$) in HB circuit of IHC are denoted by an equivalent switch S_b as shown in Fig. 6.1. The power flow of IHC is controlled by shoot-through unipolar SPWM which is derived from the switching logic of HGIBC and SLC-ZSIs. The voltage between the points S and T (as shown in Fig. 6.1) v_{inv} is the voltage appearing across HB circuit and i_{inv} is current drawn by HB circuit of IHC. The AC output of IHC is decided by three states; power, shoot-through, and zero states similar to SLC-ZSIs. The three states are existed due to ON/OFF state of S_b. It means that ON state of S_b gives STS and OFF state of S_b gives PS/ZS of IHC. The equivalent circuits of IHC during three states are shown in Fig. 6.2. It is assumed that D is the steady-state duty ratio of S_a and D_{st} is the steady-state shoot-through duty ratio of S_b.

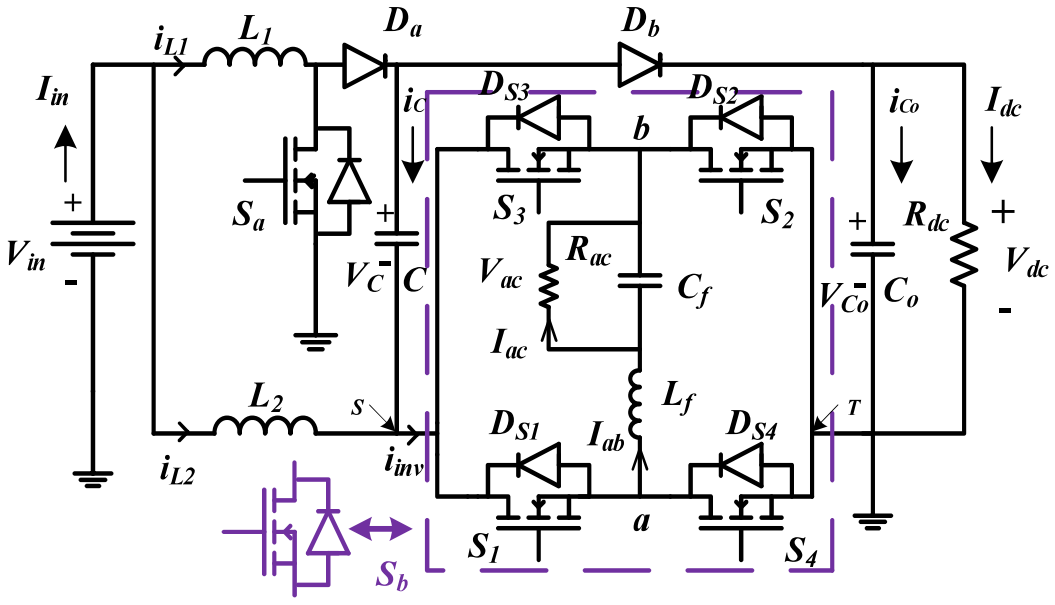


Fig. 6.1. An interleaved hybrid converter for AC and DC outputs.

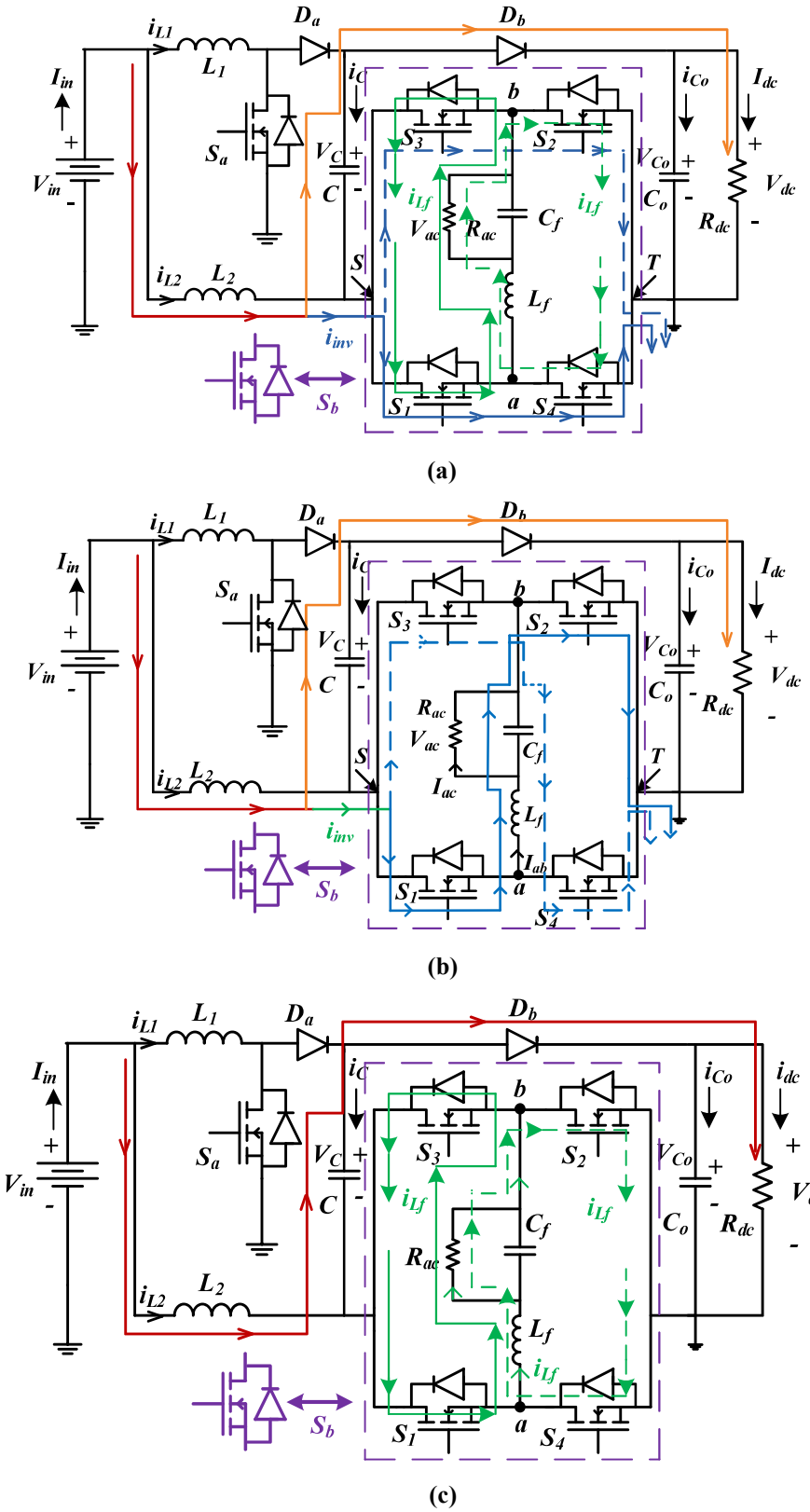


Fig. 6.2. Equivalent circuits of IHC **(a)** during shoot-through state **(b)** during power state **(c)** during zero state.

Fig. 6.2(a) shows an equivalent circuit of IHC during STS. The STS (ON state of S_b) occurs due to turn-on of either $S_1$and S_4 or S_2 and S_3 at the same time similar to SLC-ZSIs. The STS is inserted into the ZS without disturbing the PS. During the STS, no power is transferred to AC load. Fig. 6.2(b) shows an equivalent circuit of IHC during PS. The PS (OFF state of S_b) occurs due to turn-on of $S_1$and S_2 in a positive half cycle and turn-on of S_3 and S_4 in a negative half cycle of AC output. During the PS, power is transferred to AC load from V_{in}. Fig. 6.2(c) shows an equivalent circuit of IHC during ZS. In the ZS (OFF state of S_b), anti-parallel diodes ($D_{S1} - D_{S4}$) of switches ($S_1 - S_4$) start conducting along with switches to freewheel AC filter inductor current through AC load. Further, no power is transferred to AC load from V_{in}.

6.3 Operation of IHC

The IHC has three operating modes when S_a is operated along with S_b (i.e., $S_1 - S_4$). It is important to mention that the three operating modes of IHC give simultaneous AC and DC outputs with the operating condition $D + M \geq 1$. The detailed operation of IHC in the three operating modes is explained in the subsequent sections.

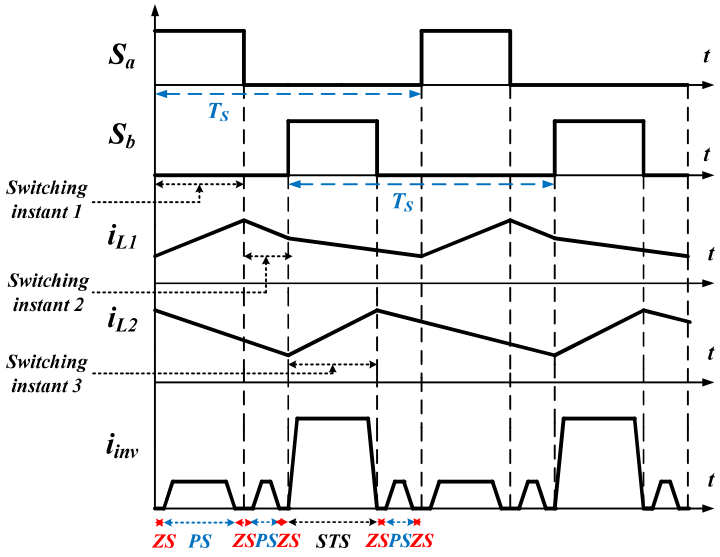


Fig. 6.3. Operating waveforms of IHC during mode 1 operation.

6.3.1 Mode 1 Operation of IHC

Fig. 6.3 shows operating waveforms of IHC during mode 1 operation. In this mode, the IHC has a summation of D and D_{st} is less than 1, i.e., $D + D_{st} < 1$. The inductor currents ($i_{L1}$and i_{L2}) and current drawn by HB switches (i_{inv}) are shown in Fig. 6.3 along with gating pulses (G_{sa} and G_{Sb}) of S_a and S_b. It can be noticed from Fig. 6.3 that the IHC has three switching instants during mode 1 operation.

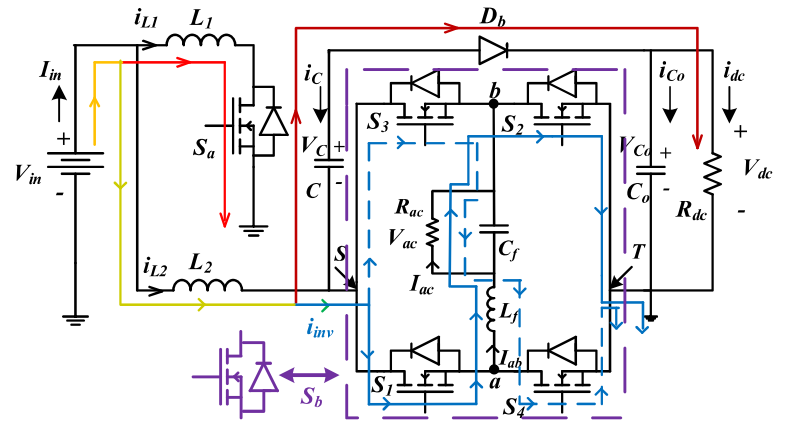
(a) Switching Instant 1 of Mode 1 Operation

Switching instant 1 exists when S_a is ON and S_b is OFF. As stated earlier that when S_b is OFF, the IHC operates either in PS or ZS. It can be observed from Fig. 6.3 that i_{inv} has finite value during PS and zero value during ZS. The equivalent circuits of IHC at this switching instant are shown in Fig. 6.4. At this instant, L_1 starts charging from V_{in} and the stored energy of L_2 starts discharging into C_o through C and AC load. Meanwhile, D_a is reverse biased and D_b is forward biased. It is important to mention that switches (S_1 and S_2) start conducting in positive half cycle and switches (S_3 and S_4) start conducting in a negative half cycle of AC output during PS. The power flow diagram of IHC during PS is shown in Fig. 6.4(a). During ZS, S_1 and D_{S3} or S_2 and D_{S4} start conducting in a positive half cycle, S_3 and D_{S1} or S_4 and D_{S2} start conducting in negative half cycle of AC output voltage. The power flow diagram of IHC during ZS is shown in Fig. 6.4(b).

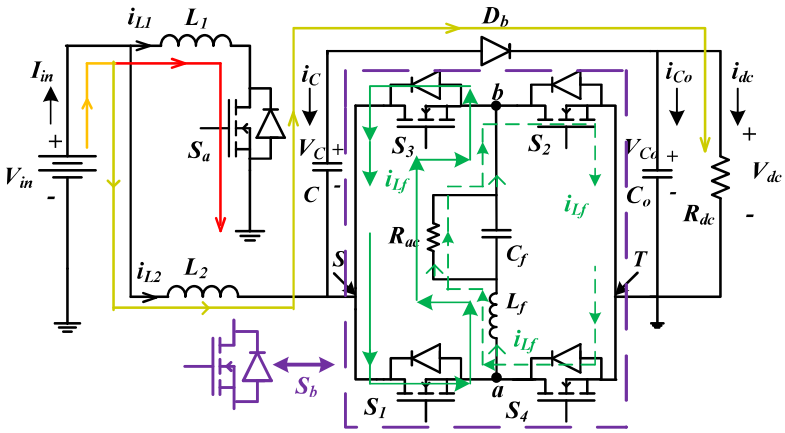
The corresponding KCL and KVL equations of IHC during PS at switching instant 1 are given in (6.1).

$$\left.\begin{aligned} v_{L1} &= v_{in} \\ v_{L2} &= v_{in} + v_C - v_{dc} \\ C\frac{dv_C}{dt} &= -i_{L2} + i_{inv} \\ C_o\frac{dv_{dc}}{dt} &= i_{L2} - i_{inv} - i_{dc} \\ i_{inv} &= i_C + i_{L2} \end{aligned}\right\} \tag{6.1}$$

Similarly, the corresponding KCL and KVL equations of IHC during ZS at switching instant 2 are given in (6.2).



(a)



(b)

Fig. 6.4. Equivalent circuits of IHC when S_a is ON and S_b is OFF **(a)** during PS **(b)** during ZS.

$$\left.\begin{aligned} v_{L1} &= v_{in} \\ v_{L2} &= v_{in} + v_C - v_{dc} \\ C\frac{dv_C}{dt} &= -i_{L2} \\ C_o\frac{dv_{dc}}{dt} &= i_{L2} - i_{dc} \\ i_{inv} &= 0 \end{aligned}\right\} \tag{6.2}$$

(b) Switching Instant 2 of Mode 1 Operation

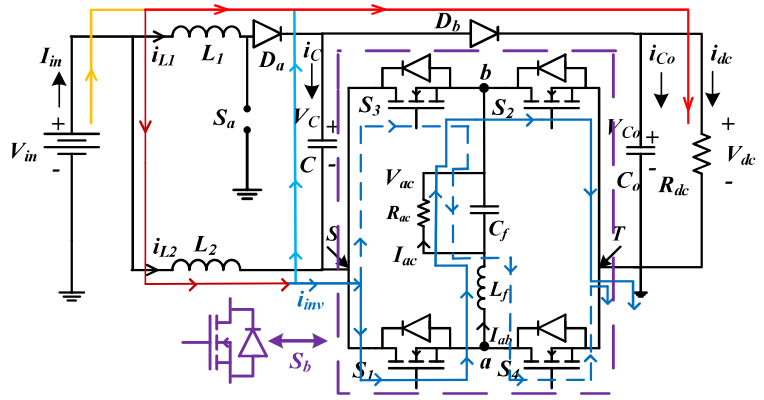
Switching instant 2 exists when both S_a and S_b are OFF. The stored energy of L_1 is transferred to C_o through D_a and D_b whereas L_2 is still in discharging mode. As S_b is OFF, the IHC operates either in ZS or PS. It can be observed from Fig. 6.3 that i_{inv} has zero value during ZS and finite value during PS. Fig. 6.5 shows equivalent circuits of IHC in this switching state. At this switching instant, the power flow diagram of IHC during PS is shown in Fig. 6.5(a) and power flow diagram of IHC during ZS is shown in Fig. 6.5(b).

The corresponding KCL and KVL expressions of IHC during PS at switching instant 2 are given in (6.3).

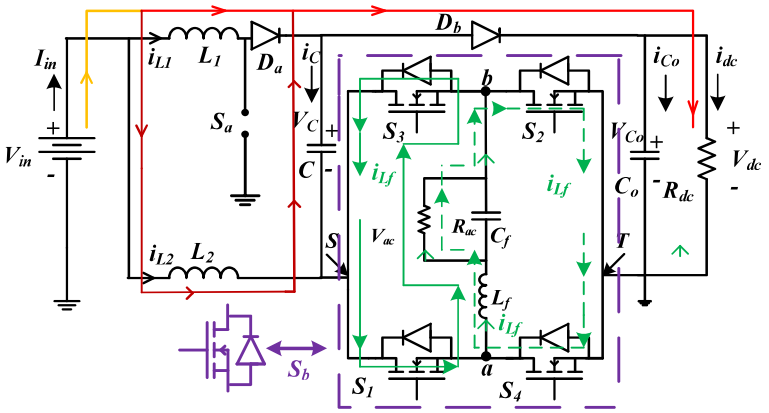
$$\left.\begin{aligned} v_{L1} &= v_{in} - v_{dc} \\ v_{L2} &= v_{in} + v_C - v_{dc} \\ C\frac{dv_C}{dt} &= -i_{L2} + i_{inv} \\ C_o\frac{dv_{dc}}{dt} &= i_{L1} + i_{L2} - i_{inv} - i_{dc} \\ i_{inv} &= i_C + i_{L2} \end{aligned}\right\} \tag{6.3}$$

The corresponding KCL and KVL expressions of IHC during ZS at switching instant 2 are given in (6.4).

$$\left.\begin{aligned} v_{L1} &= v_{in} - v_{dc} \\ v_{L2} &= v_{in} + v_C - v_{dc} \\ C\frac{dv_C}{dt} &= -i_{L2} \\ C_o\frac{dv_{dc}}{dt} &= i_{L1} + i_{L2} - i_{dc} \\ i_{inv} &= 0 \end{aligned}\right\} \tag{6.4}$$



(a)



(b)

Fig. 6.5. Equivalent circuits of IHC when both S_a and S_b are OFF **(a)** during PS **(b)** during ZS.

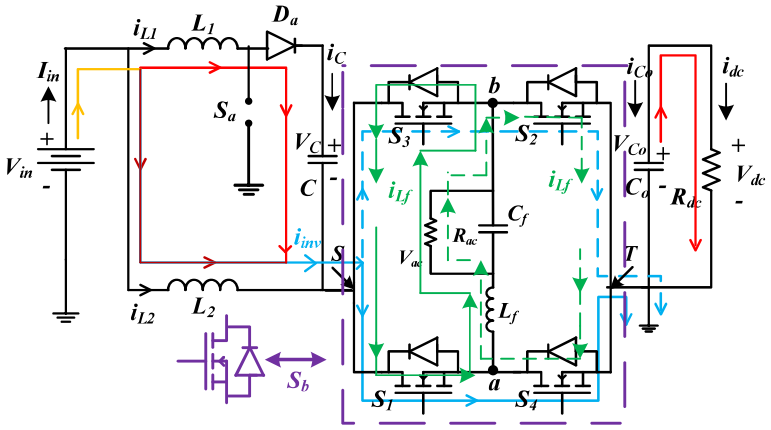


Fig. 6.6. Equivalent circuit of IHC when S_a is OFF and S_b is ON.

(c) Switching Instant 3 of Mode 1 Operation

Switching instant 3 exists when S_a is OFF and S_b is ON. It can be observed from Fig. 6.3 that the IHC operates in STS at this switching instant of mode 1 operation. As shown in Fig. 6.3, i_{inv} has finite value and greater than values of I_{inv} in switching instants 1 and 2. The power flow diagram of IHC at this switching instant is shown in Fig. 6.6. During this switching instant, the combined energy of L_1 and C start discharging and L_2 start charging. Meanwhile, D_a is forward biased and D_b is reverse biased. Also, the stored energy of C_o is discharged into DC load R_{dc}. The corresponding KCL and KVL equations of IHC during STS at switching instant 3 are given in (6.5).

$$\left.\begin{aligned} v_{L1} &= v_{in} - v_C \\ v_{L2} &= v_{in} \\ C\frac{dv_C}{dt} &= i_{L1} \\ C_o\frac{dv_{dc}}{dt} &= -i_{dc} \\ i_{inv} &= i_{L1} + i_{L2} \end{aligned}\right\} \tag{6.5}$$

6.3.2 Mode 2 Operation of IHC

Fig. 6.7 shows operating waveforms of IHC for mode 2 operation. Further, the summation of D and D_{st} is equal to 1, i.e., $D + D_{st} = 1$. It can be observed from Fig. 6.7 that the IHC has two switching instants during mode 2 operation. The currents i_{L1}, i_{L2}, and i_{inv} are shown in Fig. 6.7 along with gating pulses of S_a and S_b of IHC. In this mode, I_{L1} has a rising slope when S_a is ON and I_{L2} has a rising slope when S_b is ON.

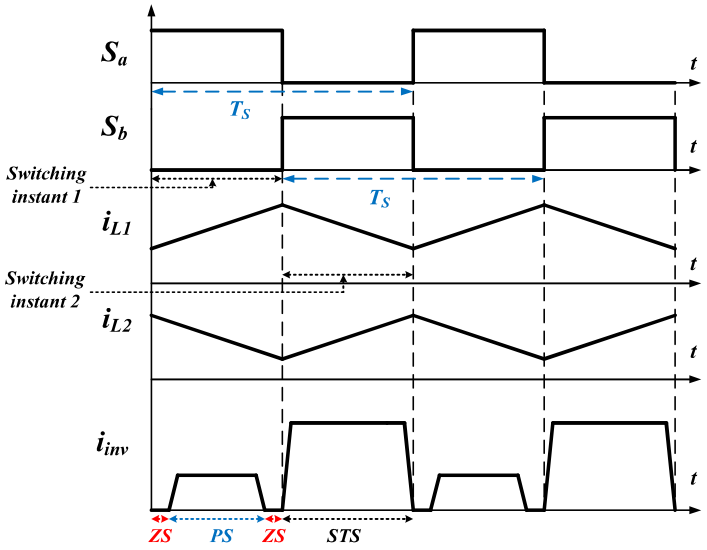


Fig. 6.7. Operating waveforms of IHC during mode 2 operation.

(a) Switching Instant 1 of Mode 2 Operation

At this switching instant, S_a is ON and S_b is OFF. It can be observed from Fig. 6.7 that the IHC operates either in PS and ZS at switching instant 1. As shown in Fig. 6.7, i_{inv} has zero value in ZS and finite value in PS. The equivalent circuits of IHC at this switching instant are shown in Fig. 6.4. Further, the operation of IHC at this switching instant is same as that of switching instant 1 of the mode 1 operation.

(b) Switching Instant 2 of Mode 2 Operation

At this switching instant, S_a is OFF and S_b is ON. The operation of IHC at this switching instant is same as that of switching instant 3 of the mode 1 operation.

6.3.3 Mode 3 Operation of IHC

Fig. 6.8 shows operating waveforms of IHC during mode 3 operation. Further, the summation of D and D_{st} is greater than 1, i.e., $D + D_{st} > 1$. It can be observed from Fig. 6.8 that the IHC has three switching instants during mode 3 operation. The inductor currents (i_{L1} and i_{L2}) and current by HB circuit (i_{inv}) are shown in Fig. 6.8 along with gating pulses of S_a and S_b.

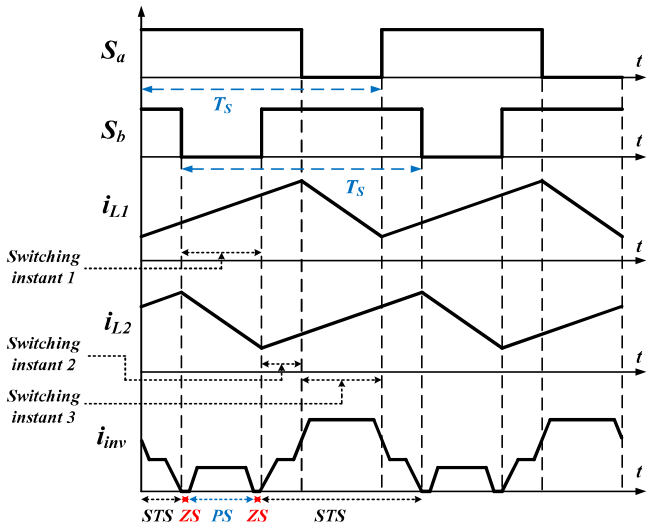


Fig. 6.8. Operating waveforms of IHC during mode 3 operation.

(a) Switching Instant 1 of Mode 3 Operation

At this switching instant, S_a is ON and S_b is OFF. The operation of IHC at this switching instant is same as that of switching instant 1 of the mode 1 operation.

(b) Switching Instant 2 of Mode 3 Operation

At this switching instant, both S_a and S_b are ON. The power flow diagram of IHC at this switching instant is shown in Fig. 6.9. It can be observed from Fig. 6.9 that both diodes (D_a and D_b) are reverse biased. At this switching instant, the two inductors start charging from the V_{in} whereas C is in standstill position.

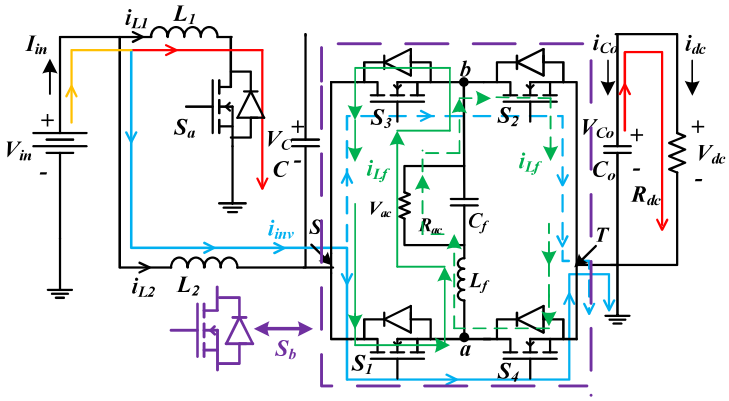


Fig. 6.9. Equivalent circuit of IHC when both S_a and S_b are ON.

The corresponding KCL and KVL expressions of IHC at this switching instant are given in (6.6).

$$\left.\begin{aligned} v_{L1} &= v_{in} \\ v_{L2} &= v_{in} \\ C\frac{dv_C}{dt} &= 0 \\ C_o\frac{dv_{dc}}{dt} &= -i_{dc} \\ i_{inv} &= i_{L2} \end{aligned}\right\} \tag{6.6}$$

(c) Switching Instant 3 of Mode 3 Operation

At this switching instant, S_a is OFF and S_b is ON. The operation of IHC in this switching instant is also same as that of switching instant 3 of the mode 1 operation.

6.3.4 Steady-State Voltage and Power Expressions of IHC

As discussed above, the AC and DC outputs of IHC are controlled by D, M and D_{st}. The steady-state AC and DC voltage gains of IHC in the three operating modes are determined by applying volt-second balance principle to inductors.

The obtained steady-state AC and DC voltage gains of IHC in the mode 1 operation are given in (6.7).

$$\left.\begin{aligned} \frac{V_{dc}}{V_{in}} &= \frac{1}{1-D-D_{st}+DD_{st}} \\ \frac{V_{ac(pk)}}{V_{in}} &= \frac{M\,(1-D)}{1-D-D_{st}+DD_{st}} \end{aligned}\right\} \tag{6.7}$$

The obtained steady-state AC and DC voltage gains of IHC in the mode 2 operation are given in (6.8).

$$\left.\begin{aligned} \frac{V_{dc}}{V_{in}} &= \frac{1}{DD_{st}} \\ \frac{V_{ac(pk)}}{V_{in}} &= \frac{M}{D} \end{aligned}\right\} \tag{6.8}$$

The obtained steady-state AC and DC voltage gains of IHC in the mode 3 operation are given in (6.9).

$$\left.\begin{aligned} \frac{V_{dc}}{V_{in}} &= \frac{2-D-D_{st}}{(1-D)(1-D_{st})} \\ \frac{V_{ac(pk)}}{V_{in}} &= \frac{M}{1-D_{st}} \end{aligned}\right\} \tag{6.9}$$

As per the AC and DC voltage gains, the AC and DC output powers of IHC in the three operating modes can be determined from the equations given in (6.10).

$$\left.\begin{aligned} P_{dc} &= \frac{{V_{dc}}^2}{R_{dc}} \\ P_{ac} &= \frac{{V_{ac(pk)}}^2}{2R_{ac}} \end{aligned}\right\} \tag{6.10}$$

where P_{ac} and P_{dc} are AC and DC output powers, R_{ac} and R_{dc} are AC and DC load resistances, V_{dc} is the DC output voltage, and $V_{ac(pk)}$ is the fundamental peak AC output voltage of IHC. The AC and DC output voltages of IHC in the three operating modes are different and controlled by the values of D, M and D_{st}.

Table 6.1. Maximum voltage stress on the elements ($C, Di.$ and $Sw.$) of IHC in the three operating modes

	Mode 1	**Mode 2**	**Mode 3**
V_C	$\frac{D}{1-D-D_{st}+DD_{st}}V_{in}$	$\frac{1}{(1-D)}V_{in}$	$\frac{1}{(1-D)}V_{in}$
V_{C_o}	$\frac{1}{1-D-D_{st}+DD_{st}}V_{in}$	$\frac{1}{DD_{st}}V_{in}$	$\frac{2-D-D_{st}}{(1-D)(1-D_{st})}V_{in}$
V_{D_1}	$\frac{1}{1-D-D_{st}+DD_{st}}V_{in}$	$\frac{1}{DD_{st}}V_{in}$	$\frac{2-D-D_{st}}{(1-D)(1-D_{st})}V_{in}$
V_{D_2}	$\frac{1-D}{1-D-D_{st}+DD_{st}}V_{in}$	$\frac{1}{(1-D_{st})}V_{in}$	$\frac{1}{(1-D_{st})}V_{in}$
V_{S_1}	$\frac{1}{1-D-D_{st}+DD_{st}}V_{in}$	$\frac{1}{(1-D)}V_{in}$	$\frac{1}{(1-D)}V_{in}$
V_{S_2}	$\frac{1-D}{1-D-D_{st}+DD_{st}}V_{in}$	$\frac{1}{(1-D_{st})}V_{in}$	$\frac{1}{(1-D_{st})}V_{in}$

6.3.5 Design of Passive Elements of IHC

For the CCM operation of IHC, the minimum values of passive elements of IHC in the three operating modes can be determined from the inequalities given in (6.11).

$$\left.\begin{aligned} L_1 &\geq \frac{V_{in}T_sR_{dc}D(1-D)}{x_{L1}\%\,V_{dc}} \\ L_2 &\geq \frac{(V_{in}-(1-D)V_{DC})R_{dc}T_sD(1-D)M}{x_{L2}\%\,D_{st}V_{dc}} \\ C &\geq \frac{D_{st}V_{dc}T_s(1-D-D_{st}+DD_{st})}{x_C\%\,R_{dc}(1-D)MV_{in}} \\ C_o &\geq \frac{DT_s(D_{st}R_{dc}-M(1-D))}{x_{Co}\%\,R_{dc}(1-D)M} \end{aligned}\right\} \tag{6.11}$$

where D, M and D_{st} are same as discussed previously, T_s is the switching period, V_{in} is the input voltage and V_{dc} is the output DC voltage of IHC. Moreover, $x_{L1}\%$ and $x_{L2}\%$ are

percentage of inductor current ripples, $x_C\%$ and $x_{Co}\%$ are percentage of capacitor voltage ripples.

The percentage ripples in inductor currents and capacitor voltages of IHC in the three operating can be determined from the equations given in (6.12).

$$\left.\begin{aligned} x_{L1}\% &= \frac{V_{L1}DT_S}{L_1 I_{L1}} \\ x_{L2}\% &= \frac{V_{L2}DT_S}{L_2 I_{L2}} \\ x_C\% &= \frac{I_C DT_S}{CV_C} \\ x_{Co}\% &= \frac{I_{Co}DT_S}{C_o V_{Co}} \end{aligned}\right\} \tag{6.12}$$

where V_{L1} and V_{L2} are voltages across L_1 and L_2; I_{L1} and I_{L2} are currents flowing through L_1 and L_2; V_C and V_{C_o} are voltages across C and C_o; I_C and I_{Co} are currents flowing through C and C_o of IHC.

Further, the design criteria of second-order low-pass filter consisting of C_f and L_f which gives sinusoidal AC output across load terminals is discussed here. The cutoff frequency (f_c) of low-pass filter should be chosen one decade below the switching frequency of IHC to obtain a 40-dB attenuation for the voltage components at switching frequency and unity gain at frequency of AC output. As per the above statements and assuming some value of C_f, value of L_f can be determined from the equation given in (6.13).

$$L_f = \frac{1}{(2\pi f_c)^2 C_f} \tag{6.13}$$

6.3.6 Shoot-Through SPWM Technique of IHC

A shoot-through SPWM technique has been derived from the unipolar SPWM technique to control the power flow of IHC which is similar to the SPWM technique of SLC-ZSIs [115]-[117]. The switching logic of IHC is also implemented in the FPGA based digital domain for generating gating pulses of IHC and its equivalent analog representation is shown in Fig. 6.10. For generating gating pulses, four reference signals are used which are modulating signal $V_m(t)$, constant signals (V_{c_Sa} and V_{c_Sb}) and carrier signal $V_{tr}(t)$. The peak of $V_m(t)$ determines M which decides magnitude AC output voltage. Further, the frequency of $V_m(t)$ determines the frequency of AC output. The values of V_{c_Sa} and V_{c_Sb} determine D of S_a and

D_{st} of HB switches ($S_1 - S_4$). The $V_{tr}(t)$ is a high-frequency carrier signal which determines the switching frequency of IHC. The STS is placed alternatively within the ZS without disturbing the PS of IHC. Hence, the alternate insertion of STS during positive and negative half-cycles of AC output may reduce switching losses and improve the reliability of IHC. Although the SPWM technique of IHC is similar to the SPWM of SLC-ZSIs, it gives independent control of AC and DC outputs of IHC. The relationship among $D, V_{c\_sa}, V_{tr}(t)$ and $M, V_m(t), V_{tr}(t)$ are given in (6.14).

$$\left.\begin{aligned} D &= \frac{V_{c\_sa}}{V_{tr}} \\ M &= \frac{V_m}{V_{tr}} \end{aligned}\right\} D + M \geq 1 \tag{6.14}$$

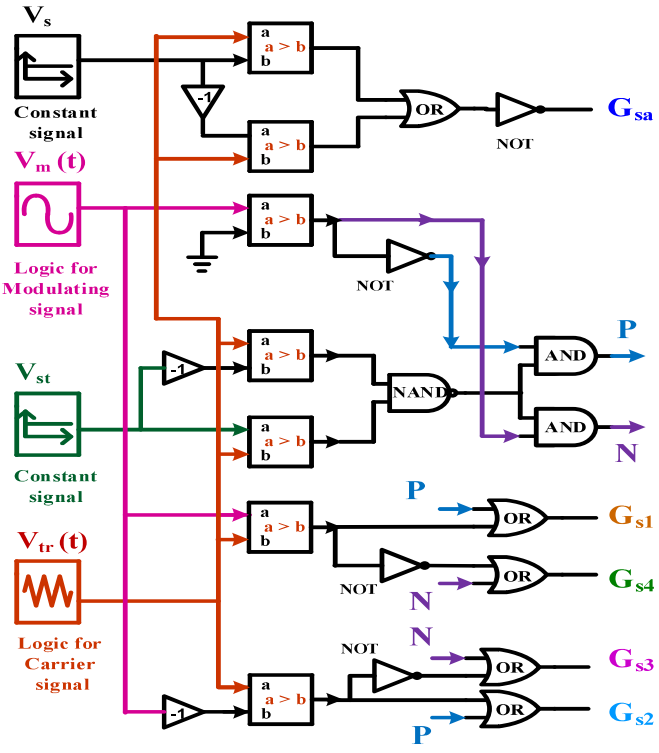


Fig. 6.10. Analog representation of shoot-through SPWM switching logic of IHC.

6.4 Verification of IHC

The performance of IHC is verified through simulation and experimental results under resistive loading. Although the IHC is capable of operating at two operating conditions $D + M \geq 1$ and $D + M \leq 1$, its performance is verified at the $D + M \geq 1$ only in this chapter for the operating conditions given in Table 6.2.

Table 6.2. Operating conditions and list of parameters for the validation of IHC

Parameters		Attributes
Input voltage,V_{in}		48 V
Output Power	P_{dc}	400 W
	P_{ac}	100 W
Inductors	L_1	1.12 mH
	L_2	1.12 mH
Intermediate capacitor,C		470 µF
Output capacitor, C_O		220 µF
AC filter inductor, L_f		2 mH
AC filter capacitor, C_f		10 µF
Line frequency, f_{line}		50 Hz
Switching frequency, f_s		10 Hz

6.4.1 Simulation Results of IHC

The performance of IHC is verified through simulation results in the three operating modes of $D + M \geq 1$ for the chosen operating conditions. As stated earlier that D_{st}, D and M are control parameters for achieving AC and DC outputs of IHC. By maintaining $D + M \geq 1$ of IHC, different values of D_{st}, D and M are considered in the three operating modes which are given in the subsequent sections. Further, in the simulation results, Y-axis has voltage/current values having units "V" or "A" and X-axis has time values having a unit "s"

6.4.1.1 Simulation Results of IHC during Mode 1 Operation

The simulation results of IHC during mode 1 operation ($D + D_{st} < 1$) are shown in Fig. 6.11 at $D_{st} = 0.2$, $D = 0.7$ and $M = 0.8$. Fig. 6.11(a) shows voltage across C, $V_C = 140$ V, output DC voltage $V_{dc} = 200$ V and fundamental AC output voltage $V_{ac}(rms) = 33.94$ V for input voltage $V_{in} = 48$ V. Further, the voltage across C_o, V_{Co} is as same as V_{dc}. It can be observed from Fig. 6.11(a) that V_C and V_{dc} have double line frequency ($2f_{line}$) ripples. The ripples are appeared due to presence of a double line frequency component of single-phase power. However, these ripples can be minimized by using higher values of energy storage elements. Fig. 6.11(b) shows AC load current $I_{ac}(rms) = 2.94$ A and Fig. 6.11(c) shows DC load current $I_{dc} = 2$ A along with V_{dc}, V_{ac} and V_{in}. It can be noticed from Fig. 6.11(c) that I_{ac} has good sinusoidal waveshape with reduced harmonic distortion because of high value of M and

in phase with V_{ac} due to resistive load. Fig. 6.11(d) shows maximum voltage and currents experienced by the active switches of IHC.

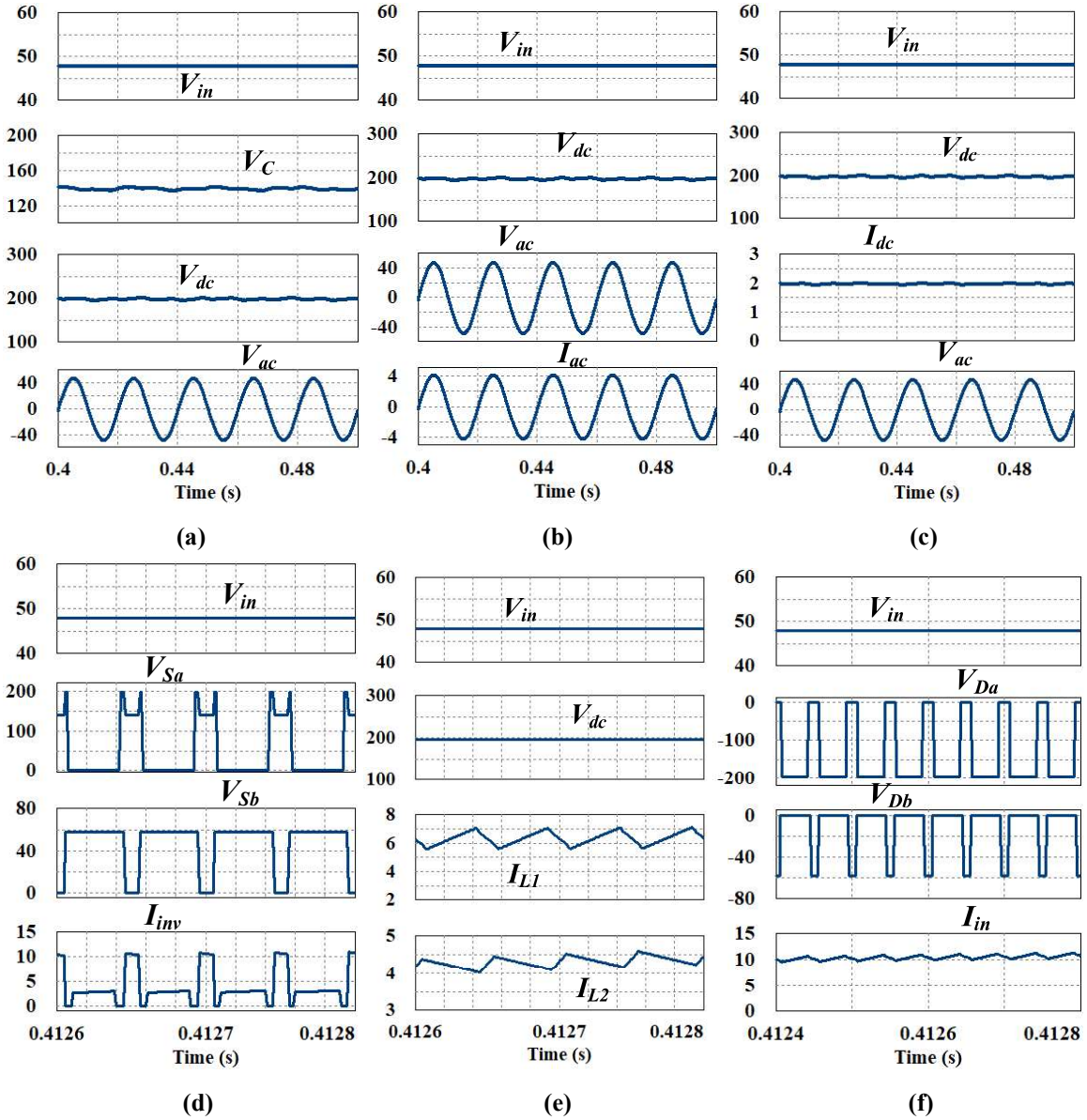


Fig. 6:11. Simulation results of IHC during mode 1 operation **(a)** V_{in}, V_C, V_{dc} and V_{ac} **(b)** V_{in}, V_{dc}, V_{ac} and I_{ac} **(c)** V_{in}, V_{dc}, I_{dc} and V_{ac} **(d)** V_{in}, V_{Sa}, V_{Sb} and I_{inv} **(e)** V_{in}, V_{dc}, I_{L1} and I_{L2} **(f)** V_{in}, V_{Da}, V_{Db} and I_{in}. **[Y-axis has voltage/current values, having units "V" or "A"]**

It can be noticed from Fig. 6.11(d) that peak current drawn by HB circuit is $I_{inv} = 10.62$ A, voltage appeared across HB is $V_{Sb} = 60$ V and maximum voltage stress experienced by S_a is $V_{Sa} = 200$ V. Further, the current I_{inv} has three different magnitudes because of power, shoot-through and zero states of HB switches. Fig. 6.11(e) shows average currents flowing

through inductors ($L_1$and L_2) as $I_{L1} = 6.61$ A and $I_{L2} = 3.75$ A along with V_{dc} and V_{in}. Fig. 6.11(f) shows voltages experienced by diodes (D_a and D_b) as $V_{Da} = -200$ V and $V_{Db} = -60$ V along with the input current of IHC, $I_{in} = 10.42$ A and V_{in}. It can be observed from Fig. 6.11(e) that the inductor currents have opposite slopes which gives low ripple input current (as shown in Fig. 6.11(f)).

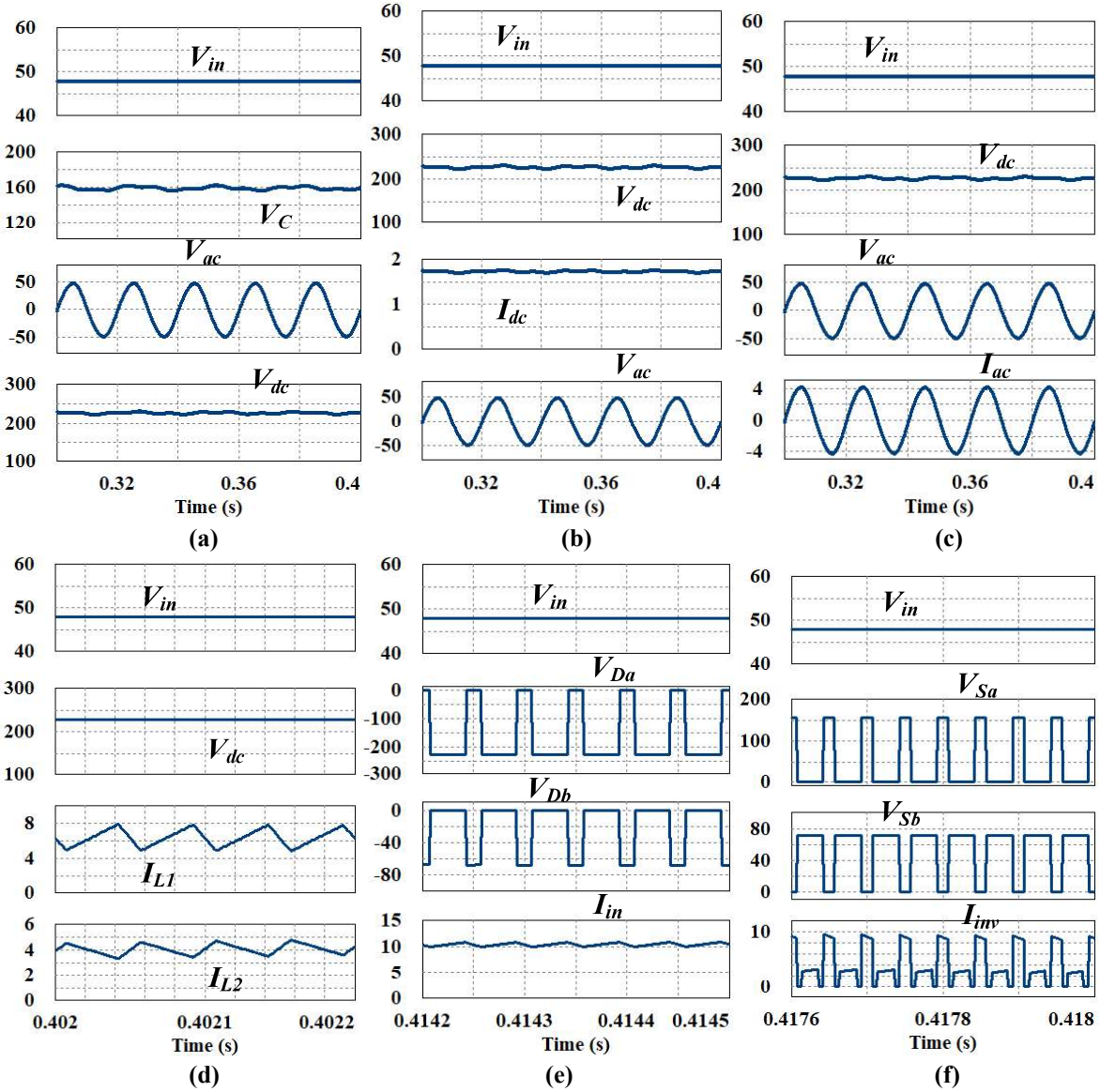


Fig. 6:12. Simulation results of IHC during mode 2 operation **(a)** V_{in}, V_C, V_{ac} and V_{dc} **(b)** V_{in}, V_{dc}, I_{dc} and V_{ac} **(c)** V_{in}, V_{dc}, V_{ac} and I_{ac} **(d)** V_{in}, V_{dc}, I_{L1} and I_{L2} **(e)** V_{in}, V_{Da}, V_{Db} and I_{in} **(f)** V_{in}, V_{Sa}, V_{Sb} and I_{inv}. **[Y-axis has voltage/current values, having units "V" or "A"]**

6.4.1.2 Simulation Results of IHC during Mode 2 Operation

The simulation results of IHC during mode 2 operation ($D + D_{st} = 1$) are shown in Fig. 6.12 at $D_{st} = 0.3$, $D = 0.7$ and $M = 0.7$. It can be observed from Fig. 6.12(a) that voltage across C, $V_C = 160$ V, output DC voltage $V_{dc} = 228.27$ V and fundamental AC output voltage $V_{ac}(rms) = 33.94$ V for $V_{in} = 48$ V. Fig. 6.12(b) shows output DC load current $I_{dc} = 1.75$ A and Fig. 6.12(c) shows AC load current $I_{ac}(rms) = 2.95$ A along with V_{dc}, V_{ac}, and V_{in}. Fig. 6.12(d) shows average currents flowing through the inductors (L_1 and L_2) as $I_{L1} = 5.83$ A and $I_{L2} = 4.6$ A along with V_{dc} and V_{in}. Due to the interleaving nature, the input current is divided between the two inductors and having minimum ripple. Fig. 6.12(e) shows voltages appeared across the diodes (D_a and D_b) are $V_{Da} = -228.57$ V and $V_{Db} = -68.57$ V along with $I_{in} = 10.42$ A and V_{in}. Fig. 6.12(f) shows the peak current drawn by HB circuit of IHC is $I_{inv} = 10.8$ A, maximum voltage appeared across HB circuit is $V_{Sb} = 68.57$ V and maximum voltage stress experienced by S_a is $V_{Sa} = 160$ V.

6.4.1.3 Simulation Results of IHC during Mode 3 Operation

The simulation results of IHC during mode 3 operation ($D + D_{st} > 1$) are shown in Fig. 6.13 at $D_{st} = 0.4$, $D = 0.7$ and $M = 0.6$. Fig. 6.13(a) shows voltage across C, $V_C = 160$ V, output DC voltage $V_{dc} = 240$ V and fundamental AC output voltage $V_{ac}(rms) = 33.94$ V for $V_{in} = 48$ V. Further, the voltage across C_o is as same as V_{dc}. It can be observed from Fig. 6.13(a) that capacitor voltages have double line frequency ripples due to presence of a double line frequency component in the input power of single-phase system. Fig. 6.13(b) shows AC load current $I_{ac}(rms) = 2.95$ A and Fig. 6.13(c) shows DC load current $I_{dc} = 1.66$ A along with V_{dc}, V_{ac}, and V_{in}. Fig. 6.13(d) shows maximum voltage stresses across the diodes are $V_{Da} = -240$ V and $V_{Db} = -80$ V along with $I_{in} = 10.42$ A. Fig. 6.13(e) shows peak current flowing through HB switches of IHC as $I_{inv} = 11.13$ A, maximum voltage stress experienced by HB switches as $V_{Sb} = 80$ V and maximum voltage stress across S_a as $V_{Sa} = 160$ V. Further, the current I_{inv} has three different magnitudes during power, shoot-through, and zero states of IHC. Fig. 6.13(f) shows average currents flowing through the inductors are $I_{L1} = 5.64$ A and $I_{L2} = 4.87$ A along with V_{dc} and V_{in}.

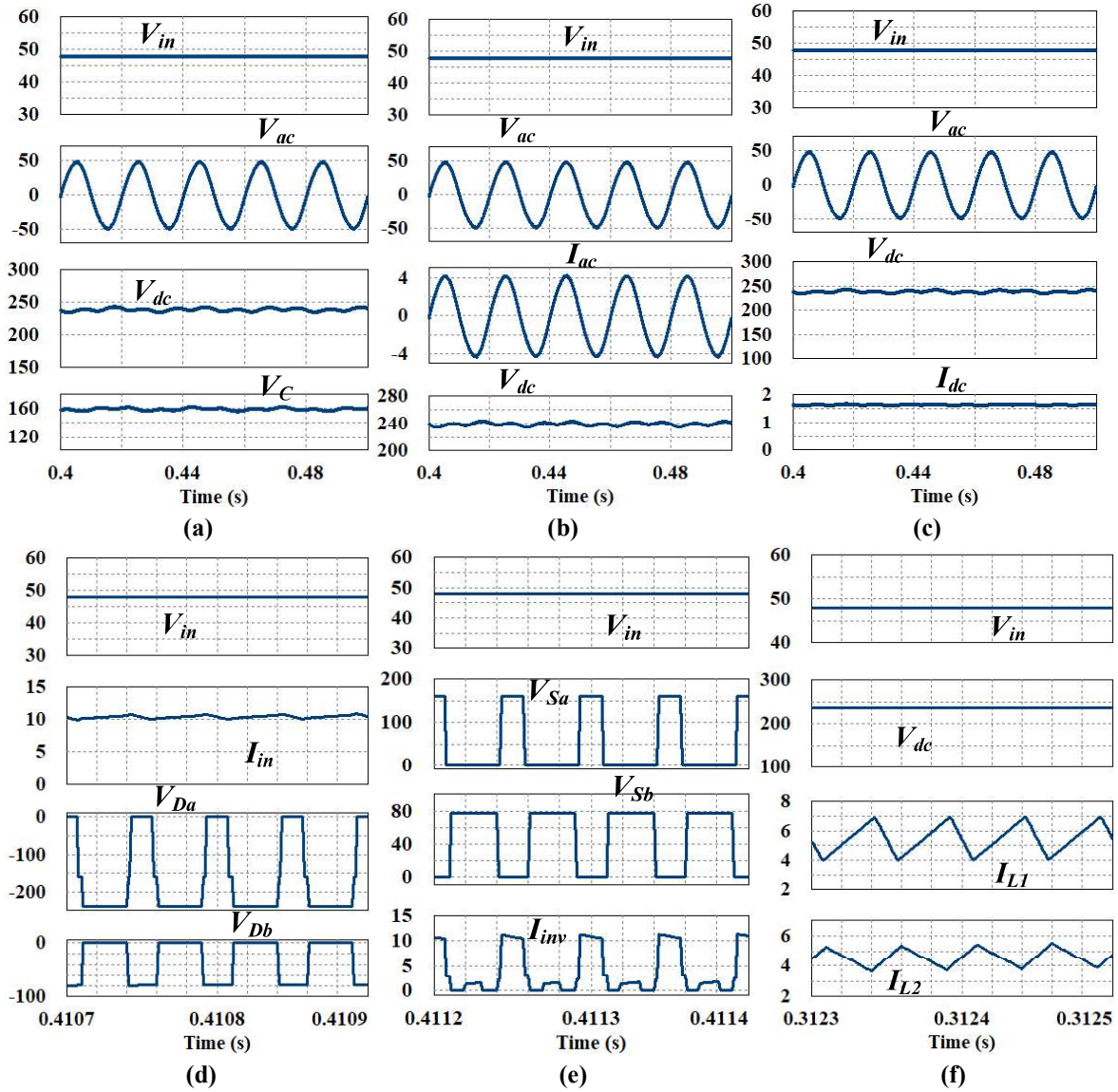


Fig. 6:13. Simulation results of IHC during mode 3 operation **(a)** V_{in}, V_{ac}, V_{dc} and V_C **(b)** V_{in}, V_{ac}, I_{ac} and V_{dc} **(c)** V_{in}, V_{ac}, V_{dc} and I_{dc} **(d)** V_{in}, I_{in}, V_{Da} and V_{Db} **(e)** V_{in}, V_{Sa}, V_{Sb} and I_{inv} **(f)** V_{in}, V_{dc}, I_{L1} and I_{L2}. **[Y-axis has voltage/current values, having units "V" or "A"]**

6.4.2 Experimental Results of IHC

The performance of IHC is verified through a laboratory prototype as same as that of the simulation studies of IHC. Fig. 6.14 shows a photograph of the experimental set-up of IHC.

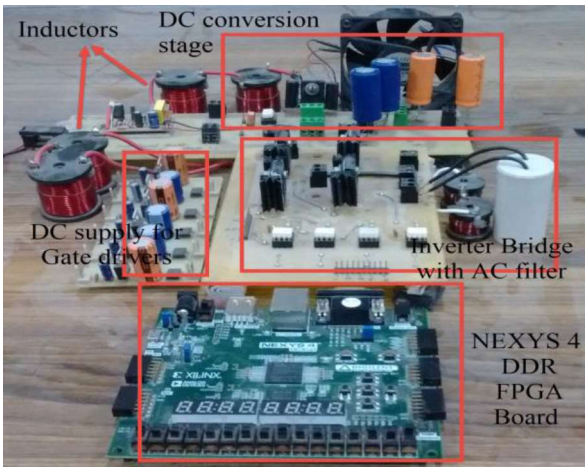


Fig. 6.14. A photograph of the experimental set-up of IHC.

6.4.2.1 Experimental Results of IHC during Mode 1 Operation

The experimental results of IHC during mode 1 operation ($D + D_{st} < 1$) are shown in Figs. 6.15 and 6.16. at $D_{st} = 0.2$, $D = 0.7$ and $M = 0.8$. Fig. 6.15(a) shows voltage across C, $V_C =$ 133.7 V, output DC voltage $V_{dc} = 191.4$ V and fundamental AC output voltage $V_{ac}(rms) =$ 31.8 V for $V_{in} = 48$ V. Further, voltage across C_o, V_{Co} is as same as V_{dc}. It can be observed from Fig. 6.15(a) that V_C and V_{dc} contain double line frequency ($2f_{line}$) ripples. The ripples are due to presence of low-frequency components in the current drawn by HB circuit from the input DC source. However, these ripples can be minimized by using higher values of passive elements. Fig. 6.15(b) shows AC output voltage $V_{ab}(rms) = 41.3$ V without filtering and Fig. 6.15(c) shows AC load current $I_{ac}(rms) = 2.65$ A along with V_{dc}, V_{ac} and V_{in}. It can be noticed from Fig. 6.15(c) that I_{ac} has good sinusoidal waveshape with reduced distortion. For analyzing distortion in I_{ac}, a harmonic spectrum of I_{ac} is shown in Fig. 6.15(d). The THD of I_{ac} is found to be 1.6%. Fig. 6.16(a) shows output DC load current $I_{dc} = 1.94$ A along with V_{dc}, V_{ac} and V_{in}. Fig. 6.16(b) shows average currents flowing through $L_1$and L_2 are $I_{L1} = 6.69$ A and $I_{L2} = 3.63$ A along with V_{dc} and V_{in}. It can be determined from Fig. 6.16(b) that percentage high-frequency ripple in I_{L1} as 29.8% and in I_{L2} as 19.4%. Fig. 6.16(c) shows maximum voltage stresses experienced by D_a and D_b are $V_{Da} = -192.6$ V and $V_{Db} = -60.2$ V along with $I_{in} = 10.34$ A and V_{in}. Fig. 6.16(d) shows current drawn by HB switches $I_{inv}(pk) = 10.3$ A, voltage appearing across HB circuit of IHC $V_{Sb} = 60.1$ V and maximum voltage stress experienced by S_a, $V_{Sa} = 193.1$ V. It can be

noticed from Fig. 6.16(d) that the current I_{inv} has three different magnitudes due to the presence of power, shoot-through, and zero states of IHC.

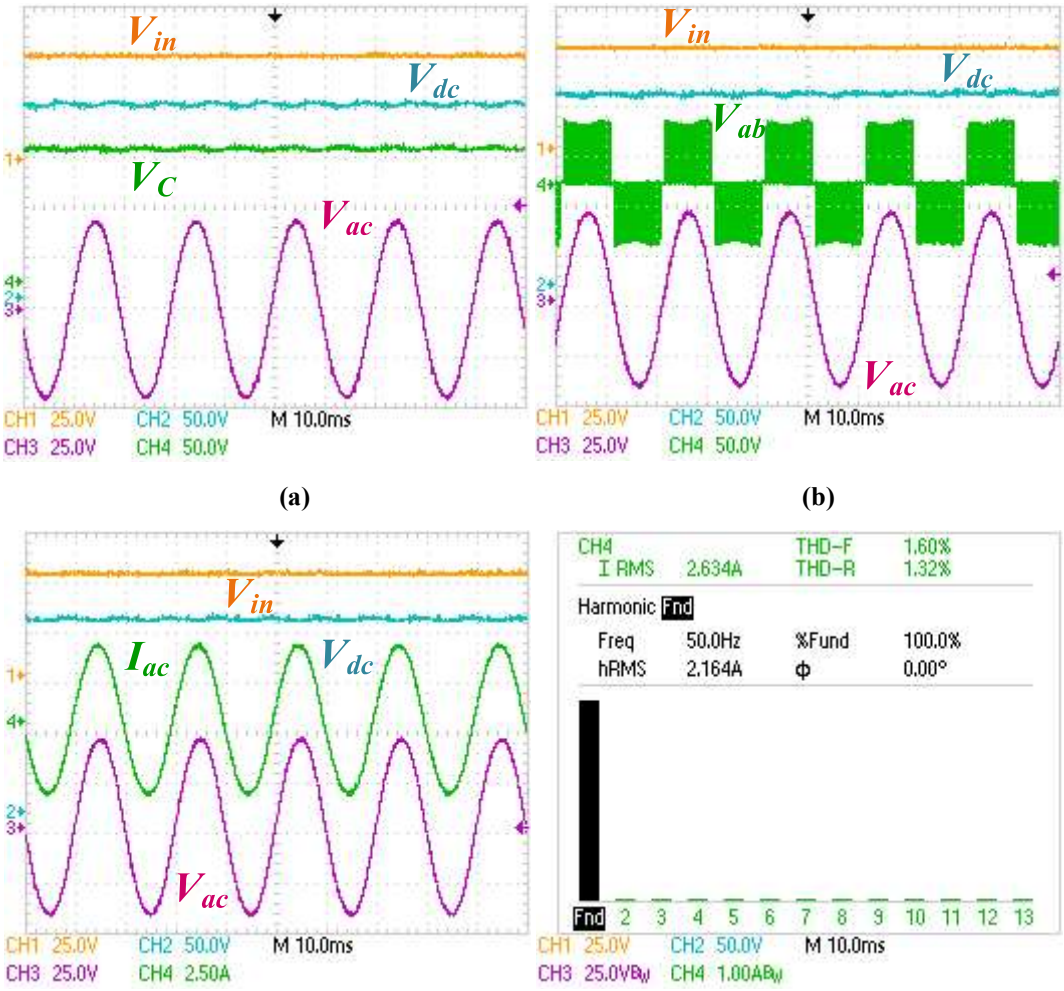


Fig. 6.15. Experimental results of IHC during mode 1 operation **(a)** V_C, V_{dc}, V_{ac} and V_{in} **(b)** V_{ab}, V_{dc}, V_{ac} and V_{in} **(c)** I_{ac}, V_{dc}, V_{ac} and V_{in} **(d)** harmonic spectrum of I_{ac}.

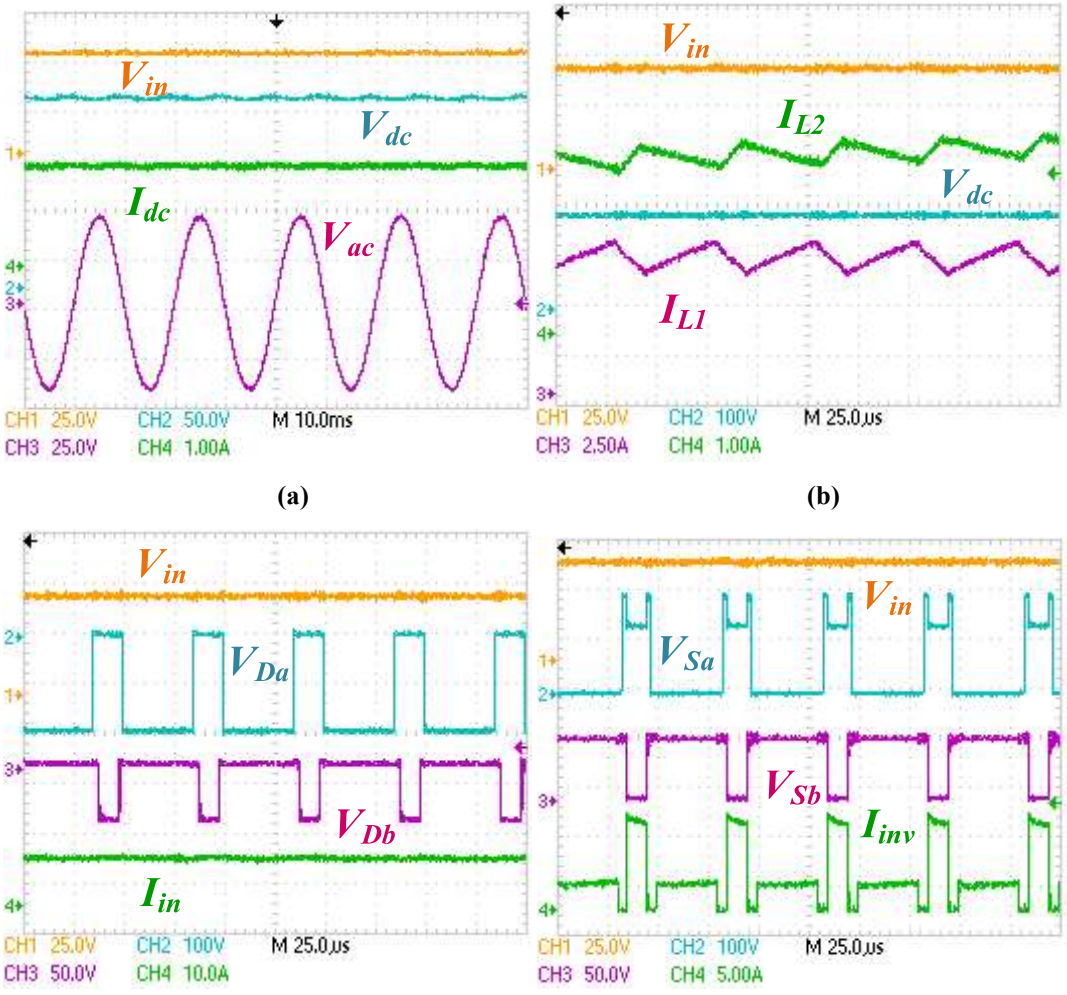


Fig. 6.16. Experimental results of IHC during mode 1 operation consisting of voltage and current stresses on the elements **(a)** I_{dc}, V_{dc}, V_{ac} and V_{in} **(b)** I_{L1}, I_{L2}, V_{dc} and V_{in} **(c)** V_{Da}, V_{Db}, I_{in} and V_{in} **(d)** V_{Sa}, V_{Sb}, I_{inv} and V_{in}.

6.4.2.2 Experimental Results of IHC during Mode 2 Operation

The experimental results of IHC during mode 2 operation ($D + D_{st} = 1$) are shown in Figs. 6.17 and 6.18 at $D_{st} = 0.3$, $D = 0.7$ and $M = 0.7$. It can be observed from Fig. 6.17(a) that voltage across C, $V_C = 149.7$ V, output DC voltage $V_{dc} = 211$ V and fundamental AC output voltage $V_{ac}(rms) = 31.3$ V for $V_{in} = 48$ V. Fig. 6.17(b) shows AC output voltage $V_{ab}(rms) = 43.7$ V without filtering and Fig. 6.17(c) shows AC load current $I_{ac}(rms) = 2.32$ A along with V_{dc}, V_{ac}, and V_{in}. Fig. 6.17(d) shows a harmonic spectrum of I_{ac}. The THD of I_{ac} is found to be 1.78%. Fig. 6.18(a) shows output DC load current $I_{dc} = 1.79$ A along with V_{dc}, V_{ac}, and V_{in}. Fig. 6.18(b) shows maximum voltage stresses appeared across D_a and

D_b are $V_{Da} = -218$ V and $V_{Db} = -65$ V along with $I_{in} = 10.6$ A and V_{in}. Fig. 6.18(c) shows average currents flowing through L_1 and L_2 are $I_{L1} = 5.81$ A and $I_{L2} = 4.76$ A along with V_{dc} and V_{in}. It can be determined from Fig. 6.18(c) that percentage high-frequency ripple in I_{L1} as 27.4% and in I_{L2} as 23.3% of their mean values. Fig. 6.18(d) shows current drawn by HB circuit $I_{inv}(pk) = 10.8$ A, maximum voltage appeared across HB circuit of IHC $V_{Sb} =$ 67.2 V and maximum voltage stress experienced by S_a, $V_{Sa} = 159.3$ V. It can be noticed from Fig. 6.18(d) that the current I_{inv} has different magnitudes because of power, shoot-through, and zero states of IHC.

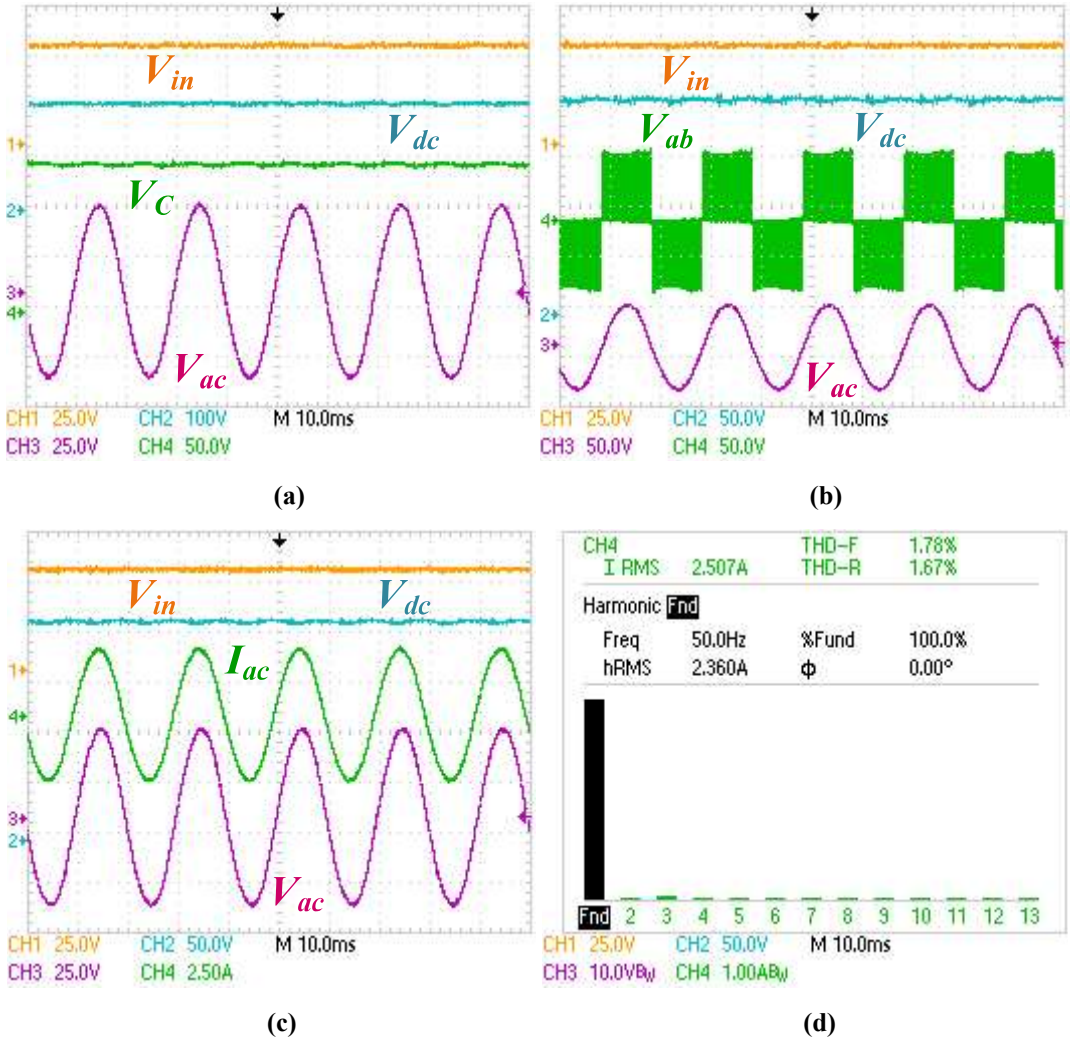


Fig. 6.17. Experimental results of IHC during mode 2 operation **(a)** V_C, V_{dc}, V_{ac} and V_{in} **(b)** V_{ab}, V_{dc}, V_{ac} and V_{in} **(c)** I_{ac}, V_{dc}, V_{ac} and V_{in} **(d)** harmonic spectrum of I_{ac}.

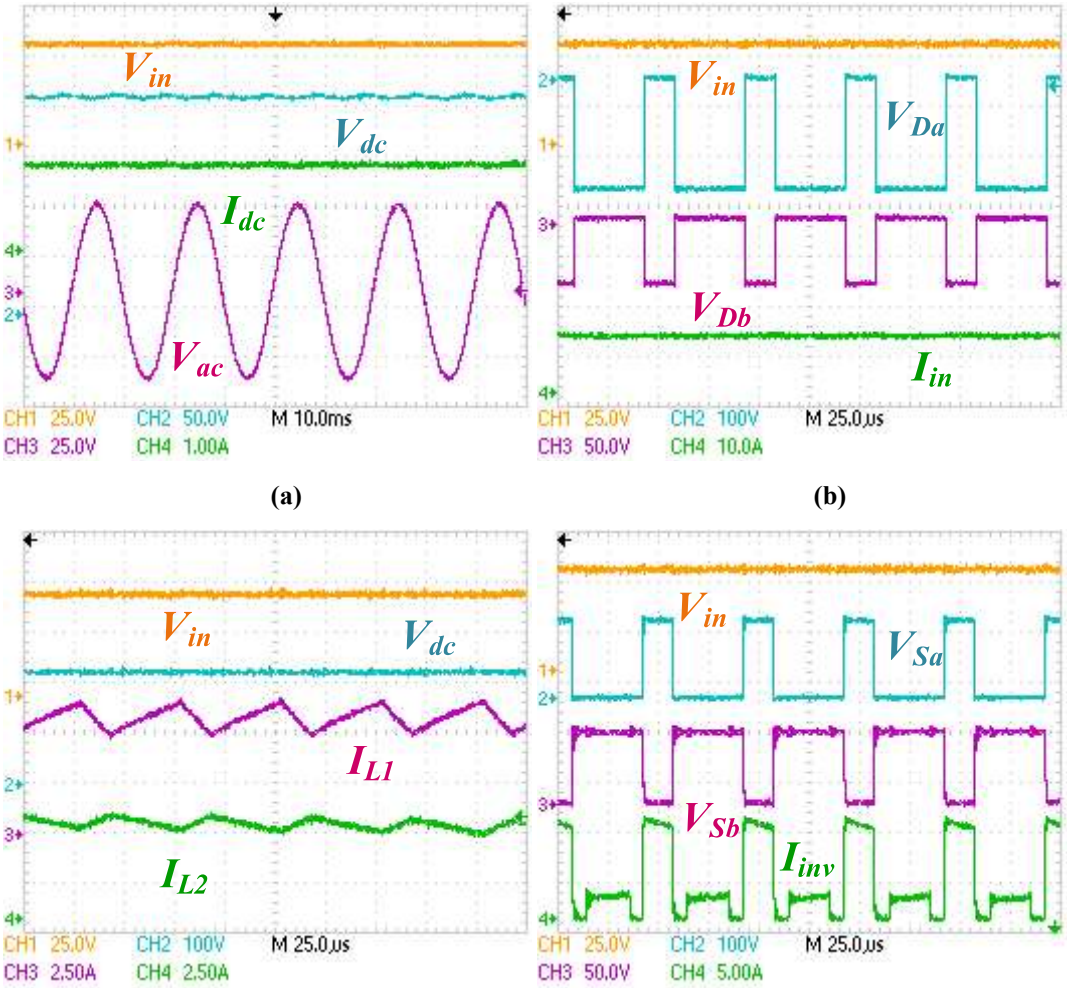


Fig. 6.18. Experimental results of IHC during mode 2 operation consisting of voltage and current stresses on the elements **(a)** I_{dc}, V_{dc}, V_{ac} and V_{in} **(b)** V_{Da}, V_{Db}, I_{in} and V_{in} **(c)** I_{L1}, I_{L2}, V_{dc} and V_{in} **(d)** V_{Sa}, V_{Sb}, I_{inv} and V_{in}.

6.4.2.3 Experimental Results of IHC during Mode 3 Operation

The experimental results of IHC during mode 3 operation ($D + D_{st} > 1$) are shown in Figs. 6.19 and 6.20 at $D_{st} = 0.4$, $D = 0.7$ and $M = 0.6$. Fig. 6.19(a) shows voltage across C, $V_C =$ 152.8 V, output DC voltage $V_{dc} = 226.4$ V and fundamental AC output voltage $V_{ac}(rms) =$ 31.8 V for $V_{in} = 48$ V. The voltage across C_o is as same as V_{dc}. It can be observed from Fig. 6.19(a) that the capacitor voltages have double line frequency ripples due to presence of a double line frequency component in the input power of single-phase system. Fig. 6.19(b) shows AC output voltage $V_{ab}(rms) = 46.34$ V without filtering and Fig. 6.19(c) shows AC load current $I_{ac}(rms) = 2.39$ A along with V_{dc}, V_{ac} and V_{in}. Fig. 6.19(d) shows a harmonic

spectrum of I_{ac}. It can be noticed from Fig. 6.19(d) that THD of I_{ac} is 2.35%. Fig. 6.20(a) shows average currents flowing through the inductors are $I_{L1} = 5.51$ A and $I_{L2} = 4.79$ A along with V_{dc} and V_{in}. It can be determined from Fig. 6.20(a) that percentage high-frequency ripple in I_{L1} as 33.7% and in I_{L2} as 34.1% of its average values. Fig. 6.20(b) shows maximum voltage stresses across the diodes are $V_{Da} = -228.2$ V and $V_{Db} = -81.7$ V along with $I_{in} = 10.3$ A. Fig. 6.20(c) shows output DC load current $I_{dc} = 1.63$ A along with V_{dc}, V_{ac}, and V_{in}. Fig. 6.20(d) shows $I_{inv}(pk) = 10.2$ A, $V_{Sb} = 81.9$ V and maximum voltage stress across S_a, $V_{Sa} = 161.2$ V. Further, I_{inv} has three different magnitudes because of power, shoot-through, and zero states of IHC.

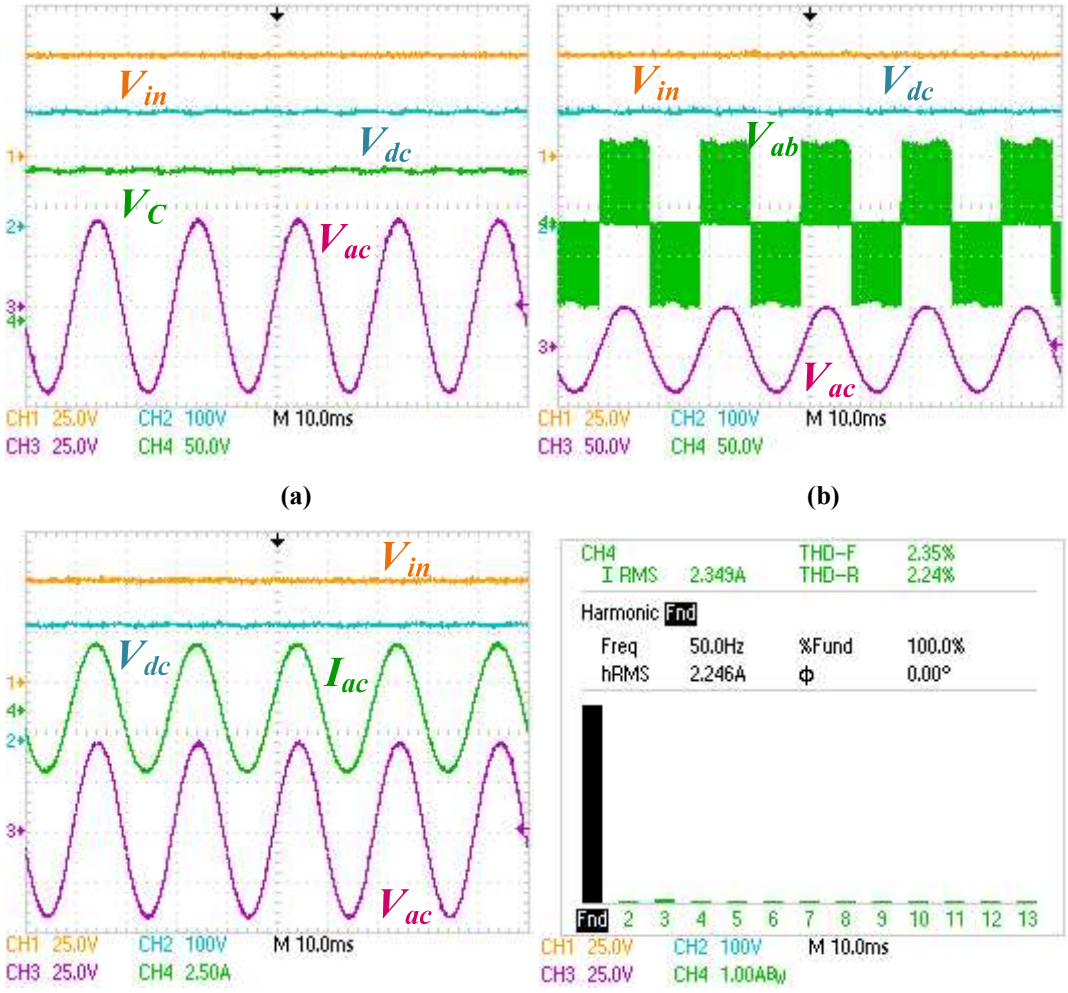


Fig. 6.19. Experimental results of IHC during mode 3 operation **(a)** V_C, V_{dc}, V_{ac} and V_{in} **(b)** V_{ab}, V_{dc}, V_{ac} and V_{in} **(c)** I_{ac}, V_{dc}, V_{ac} and V_{in} **(d)** harmonic spectrum of I_{ac}.

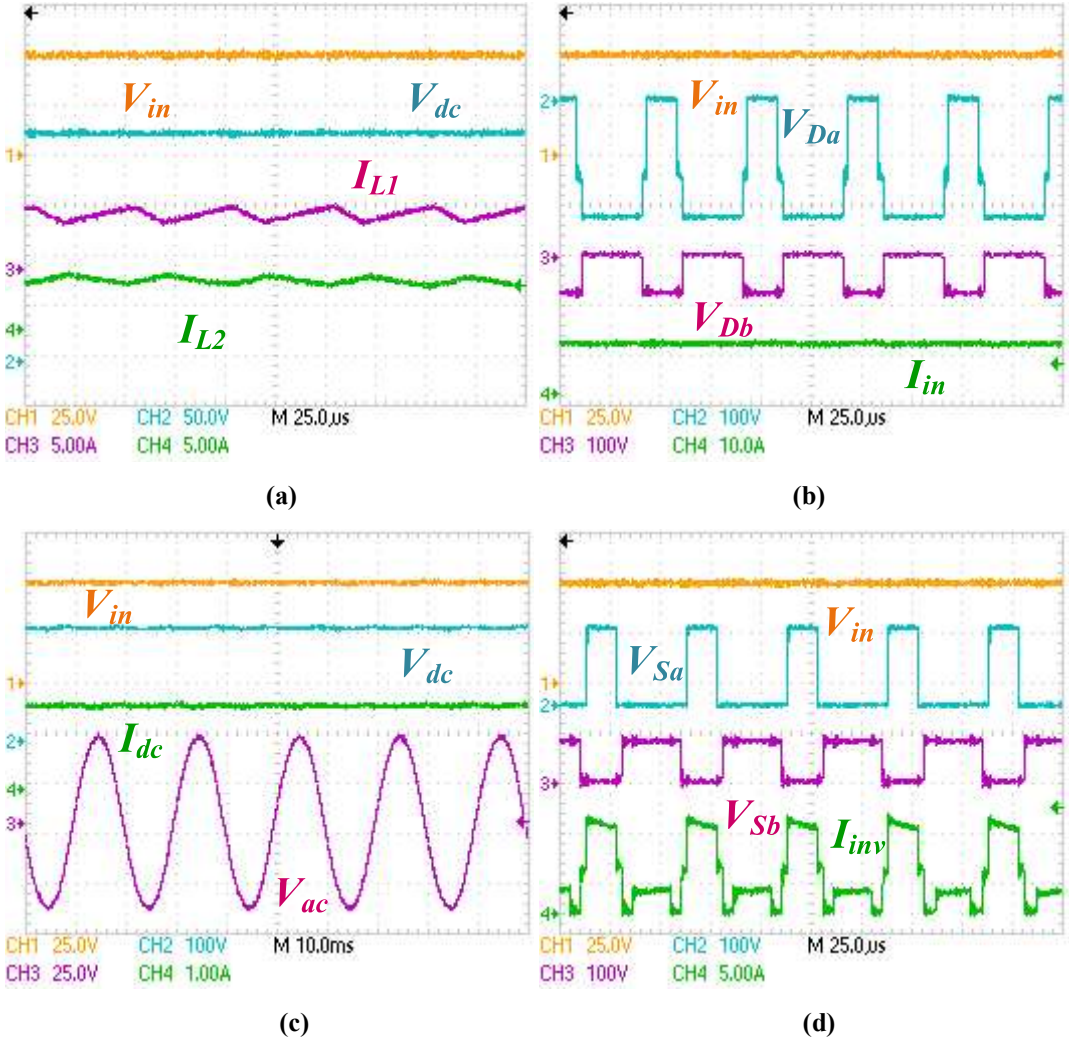
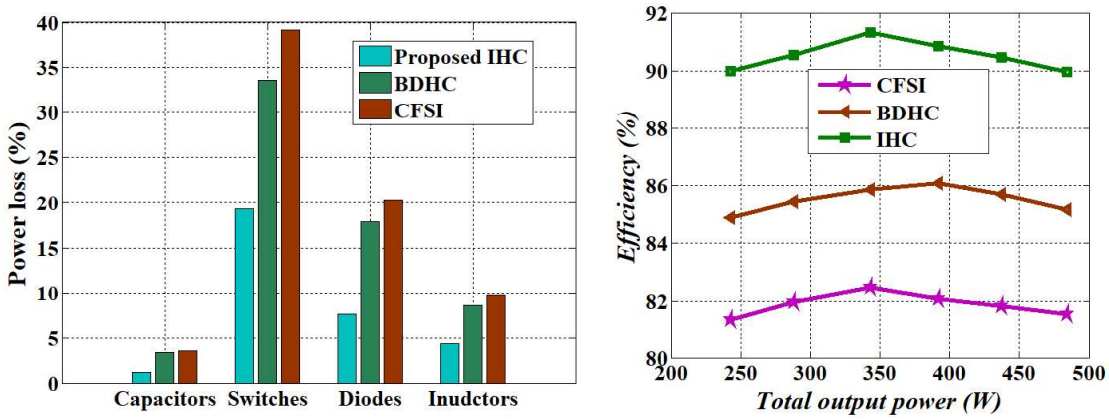


Fig. 6.20. Experimental results of IHC during mode 3 operation consisting of voltage and current stresses on the elements **(a)** I_{L1}, I_{L2}, V_{dc} and V_{in} **(b)** V_{Da}, V_{Db}, I_{in} and V_{in} **(c)** I_{dc}, V_{dc}, V_{ac} and V_{in} **(d)** V_{Sa}, V_{Sb}, I_{inv} and V_{in}.

6.4.3 Power Losses in the Elements and Efficiency Variation of IHC as Compared to BDHC and CFSI

It is important to mention here that power loss calculations and efficiency variation of the IHC are carried out during mode 1 operation only as shown in Fig. 6.21. As per the discussed power loss calculations in previous chapters, power losses in the elements of IHC are determined at a rated power in comparison to two CHCs (BDHC and CFSI). The determined power losses are shown in Fig. 6.21 along with their efficiency variation at different loading conditions. It can be noticed from Fig. 6.21(a) that power losses in the elements of IHC are less as compared to two CHCs. Further, efficiency variation of the IHC at different loading conditions is carried out in comparison to BDHC and CFSI as shown in Fig. 6.21(b). It can

be observed from Fig. 6.21(b) that the maximum efficiency of IHC is 91.32%, the maximum efficiency of BDHC is 86.08% and maximum efficiency of CFSI is 82.45%. It is clear from Fig. 6.21 that the IHC has better efficiency as compared to BDHC and CFSI for under the same operating conditions. Moreover, the efficiency of IHC can be improved by avoiding lengthy wires and by designing a proper PCB layout.



(a) (b)

Fig. 6.21. Power loss distribution among the elements and efficiency variation of IHC as compared to BDHC and CFSI **(a)** power losses in the elements of IHC, BDHC and CFSI **(b)** efficiency variation of IHC in comparison to BDHC and CFSI.

6.5 Summary

An interleaved hybrid converter (IHC) is presented in this chapter, which gives simultaneous AC and DC outputs for a hybrid AC/DC system. The IHC is developed from the switching concept of the HGIBC and SLC-ZSIs. It has operating conditions $D + M \leq 1$ and $D + M \geq 1$, unlike CHCs. Due to the two operating conditions, it has wider ranges of D and M which results in DC output with high voltage gain and AC output with reduced harmonic distortion. As the IHC is developed from HGIBC and SLC-ZSIs, it also has three modes of operations in the two operating conditions and better electromagnetic interference immunity. The IHC is capable of giving different AC and DC voltage gains in the three modes of operations. Due to its interleaving nature, input and output currents have low ripples using lesser values of energy storage elements. Hence, the IHC has improved power density. Also, it can use lower current rating devices for higher power applications which results in economical prototype design. Detailed mathematical modeling of the IHC is carried out and steady-state voltage gains are determined at the operating condition $D + M \geq 1$. Moreover, simulation and

experimental results have been given to verify the performance of IHC. The power loss distribution among elements and efficiency analysis of IHC is carried-out to show its effectiveness in comparison to BDHC and CFSI at same operating conditions.