CHAPTER-5

Conclusion and Future Scope of Research

Figure 5.1 Thesis chapter outlines

This thesis presented a comprehensive study on the device-circuit co-design approach for novel FinFET-based devices, aimed at enhancing neuromorphic computing and non-volatile memory technologies. The primary contributions of this work are summarized in **Figure 5.1**. Our research introduced three major advancements, each addressing critical challenges in its respective domain. Firstly, a 3-D JAM FeFinFET at a 3-nm technology node was proposed as a synaptic weight device for neuromorphic applications. Secondly, a novel 1T-1R non-volatile memory cell was introduced, leveraging a memristive variant of the ferroelectric field-effect transistor for data storage. This architecture enabled non-destructive readout while achieving improved read performance at low operating voltages. Third, the need for power-efficient STT-MRAM and MTJ-based non-volatile logic devices was addressed by designing a novel asymmetric FinFET-based access device at a 3-nm node. The proposed architecture exhibited reduced gate and write-line capacitance, ensuring improved

integration density and energy efficiency. Furthermore, these contributions collectively advanced the design and integration of next-generation memory and neuromorphic computing devices while maintaining compatibility with standard CMOS fabrication processes.

5.1 Chapter-wise Conclusion

The introduction of the thesis was presented in ***Chapter 1***, which provided an overview of neuromorphic computing, emphasizing the critical role of synaptic devices in mimicking biological neural networks. It presented a comprehensive literature review covering two major types of non-volatile memory: ferroelectric memory and spin-based memory (specifically MTJ-based memory). The review began with a basic overview of ferroelectric memory, including its non-volatile nature, hysteresis behavior, and CMOS compatibility, which made it a promising candidate for energy-efficient and scalable neuromorphic systems. It then delved into the use of FinFET-based architectures for designing synaptic devices, as opposed to traditional planar CMOS designs. The advantages of FinFET structures, including superior electrostatic control, reduced leakage, and scalability for advanced technology nodes, made them highly suitable for neuromorphic applications. Furthermore, the literature review included an analysis of existing JL FET devices that had been explored for synaptic applications. These studies highlighted the potential benefits of junctionless architectures in achieving low-power and high-efficiency in synaptic behavior. Furthermore, this chapter explored various device and circuit co-design approaches that had been proposed to enhance the performance of the STT-MRAM memory bit cell. Different techniques, including modifications at the device level (such as optimizing access transistors) and circuit-level innovations, were discussed in the context of improving write efficiency, reducing power consumption, and achieving faster switching speeds. Particular emphasis was placed on the design of

asymmetric FinFET devices, which had been shown to enhance the performance of STT-MRAM by optimizing asymmetric current characteristics. Finally, the chapter concluded with the problem statement, establishing the foundation for the research contributions presented in the subsequent chapters. The insights gained from this comprehensive review highlighted the need for novel device architectures and process integration strategies to advance the fields of neuromorphic computing and non-volatile memory technologies.

Chapter 2 presented a 3D SOI-based JAM FeFinFET, along with its fabrication process flow at the 3-nm technology node, designed for synaptic weight applications in neuromorphic computing. The device was evaluated through numerical simulations using the Sentaurus TCAD simulator, demonstrating its feasibility and performance. The proposed JAM FeFinFET was fully compatible with the standard SOI FinFET manufacturing process, allowing seamless integration with the fabrication flow of p-FinFETs. Through a well-calibrated TCAD simulation setup, it was analyzed that the device exhibited non-volatile conductance characteristics and history-dependent memory behavior under asymmetric biasing conditions. Compared to previously developed synaptic devices, the proposed architecture achieved a broader range of history-dependent conductance while significantly lowering power consumption, making it highly suitable for energy-efficient neuromorphic computing applications. Additionally, the JAM FeFinFET demonstrated a memory window of 1.30 V and exhibited a 76% improvement in the non-volatile conductance range in the ON state compared to conventional junctionless and ferroelectric FinFET devices. These findings established the proposed device as a promising candidate for next-generation neuromorphic hardware.

Chapter 3 introduced a novel MFeFET designed for a 1T-1R non-volatile memory

cell with non-destructive read capability. The proposed MFeFET transformed a conventional FeFinFET to function as a memristor by optimizing its fin dimensions and threshold voltage behavior. These refinements enabled the device to sustain a high drain current at zero gate voltage. Through a well-calibrated TCAD simulation framework, the device was demonstrated to achieve a memory window of 1.30 V, along with negative high and low threshold voltages that allowed read operations without disturbing the stored data. A 1T-1MFeFET memory cell was proposed, offering improved reliability, endurance, energy efficiency, and compatibility with FEOL processes. This 1T-1MFeFET memory cell has distinct read and write paths, eliminating the common issue of destructive read operations seen in conventional FeFET-based memory cells. System-level performance evaluation using NVSim benchmarked the MFeFET-based memory against STT-MRAM, revealing a 50% reduction in read latency, making it a highly efficient solution for next-generation non-volatile memory applications. These findings suggested that the MFeFET could play a crucial role in high-performance memory systems.

Chapter 4 was the final contribution of this thesis, focusing on the development of a novel asymmetric FinFET-based access device designed to enhance the performance of STT-MRAM. The proposed device was developed at the 3-nm node and employed a selective fin-trimming technique during the RMG process. This innovative fabrication approach did not require additional mask designs, making it highly compatible with standard CMOS manufacturing. Using 3D TCAD simulations, the study demonstrated that the proposed device achieved up to 26% asymmetry in current characteristics, meeting the requirements of STT-MRAM circuits. Additionally, the design exhibited a 30% reduction in gate capacitance compared to previously reported asymmetric devices, leading to lower power consumption and

improved integration density. These findings established the proposed architecture as a promising candidate for future STT-MRAM and logic-in-memory applications.

5.2 Future Scope of Research

The future scope of research based on the work presented in this thesis includes several promising directions. The scope of ***Chapter 2*** offered significant potential for advancing neuromorphic computing and low-power memory applications. Several key areas can be explored to further enhance proposed capabilities and practical implementation:

- ***Experimental Validation and Fabrication***: While this study relies on TCAD-based simulations, the next step involves experimental fabrication and characterization of the JAM FeFinFET to validate its performance. Real-world testing will help in refining the design and assessing process variations.
- ***Spiking Neural Networks***: The JAM FeFinFET could be further explored for SNN. This would involve designing circuits that leverage the device's synaptic plasticity.
- ***Optimization for Low-Power Applications***: Further research can focus on optimizing the device structure and material properties to reduce power consumption while maintaining a stable, non-volatile conductance range. This will be critical for energy-efficient neuromorphic processors.
- ***Hybrid Memory Applications***: Integrating the JAM FeFinFET with MTJ devices could enable hybrid memory solutions. This could lead to the development of low-power, high-speed memory and logic devices.
- ***Crossbar Arrays***: Expanding the use of JAM FeFinFET in crossbar arrays for in-memory computing could be explored. This would involve designing scalable and energy-efficient crossbar architectures that leverage the device's non-volatile

conductance and history-dependent behavior.

- ***Neuromorphic Systems-on-Chip (SoCs)***: Future research could focus on integrating the JAM FinFET into neuromorphic SoCs that combine memory, logic, and sensing functionalities. This would involve developing heterogeneous integration techniques to combine the device with sensors, processors, and communication modules.

The proposed MFeFET-based 1T-1R memory presented in ***Chapter 3*** offers significant advancements in non-volatile memory technology. However, further research is necessary to enhance its practical implementation and explore new applications. The following areas outline the future scope of this work:

- ***Endurance and retention Studies***: One of the primary concerns with FeFET-based memory is the endurance and retention of stored data. Previous works have shown that optimizing the ferroelectric layer thickness and doping profiles can mitigate degradation effects and enhance long-term reliability. Further research is required to investigate fatigue effects, charge trapping, and ferroelectric aging.
- ***Scaling to Advanced Technology Nodes***: As semiconductor technology progresses beyond the 3-nm node, exploring the feasibility of scaling the proposed MFeFET-based memory while maintaining process compatibility will be a vital area of research.
- ***Peripheral Circuit Design***: Optimizing peripheral circuitry, including sense amplifiers, and write drivers can further enhance the performance and efficiency of the 1T-1R memory architecture.

By addressing these research directions, the proposed MFeFET-based memory cell has the potential to become a key enabling technology for next-generation non-volatile memory,

neuromorphic computing.

The scope of ***Chapter 4*** is focused on the use of asymmetric FinFET devices in non-volatile memory, logic-in-memory, and device-circuit co-design for low-power computing. The following areas outline the future scope of this research:

- ***Energy-Efficient Write Operations:*** The asymmetric FinFET structure aims to optimize write current efficiency for STT-MRAM. Future studies should focus on refining the device geometry and material properties to further reduce power consumption while maintaining high-speed operation.
- ***Integration with Advanced Memory Architectures:*** The proposed device can be extended to hybrid memory architectures by combining it with other non-volatile memory technologies such as FeFET, RRAM, or PCM. Exploring its role in multi-bit storage and computing-in-memory paradigms could enhance its applicability.
- ***Device-Circuit Co-Design for Low-Power Computing:*** Future research should explore the co-optimization of asymmetric FinFETs with peripheral circuits, such as sense amplifiers and write drivers, to enable energy-efficient and high-density memory arrays. Circuit-level simulations incorporating these access devices can provide insights into their performance in real-world applications.
- ***Low-Power Write Circuits***: Future work could focus on designing low-power write circuits using the proposed asymmetric FinFET for STT-MRAM applications. This would involve developing novel circuit topologies that leverage the device's asymmetric current flow to reduce write energy and write latency.
- ***Non-Volatile Logic Circuits***: The device could be used to design non-volatile logic circuits for instant-on computing. This would involve integrating the asymmetric

FinFET into sequential logic circuits for zero-standby-power operation.

Through the exploration of these avenues, the foundational work presented in this thesis may be expanded and implemented across a comprehensive array of advanced, cutting-edge technologies, thereby contributing significantly to the progress of non-volatile memory and neuromorphic computing.