DEVICE MODELING AND LOGIC CIRCUITS DESIGN FOR SPIN-BASED COMPUTING

Thesis submitted in the partial fulfillment for the Award of Degree

Doctor of Philosophy

By

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It is certified that the work contained in the thesis intitled "***Device Modeling and Logic Circuits Design for Spin-Based Computing***" by "***Jagadish***" has been carried out under my supervision and that this work has not been submitted elsewhere for a degree.

It is further certified that the student has fulfilled all the requirements of Comprehensive Examination, Candidacy, and SOTA for the award of Ph.D. Degree.

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I, *"JAGADISH"*, certify that the work embodied in this thesis is my own bona fide work and carried out by me under the supervision of ***DR. SHIVAM VERMA*** *from* ***2020*** to ***2024*** at the ***Department of Electronics Engineering, Indian Institute of Technology (BHU), Varanasi.*** The matter embodied in this thesis has not been submitted for the award of any other degree/diploma elsewhere. I declare that I have faithfully acknowledged and accredited to the research communities wherever their works have been cited in the accomplished of this thesis. I further declare that I have not intentionally copied any other's work, paragraphs, text, data, results, *etc.*, reported in journals, books, magazines, reports, dissertations, theses, *etc.*, or available at websites and have not included them in this thesis or cited as my own work.

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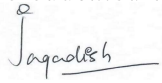

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LIST OF ABBREVIATIONS

Abbreviation	Details
CMOS	Complementary Metal-Oxide-Semiconductor
STT	Spin Transfer Torque
MTJ	Magnetic Tunnel Junction
TMR	Tunnel Magnetoresistance
TMC	Tunnel Magnetocapacitance
SPICE	Simulation Program with Integrated Circuit Emphasis
NEGF	Non-Equilibrium Green's Function
AWT	Auto-Write Termination
OOMMF	Object Oriented Micromagnetic Framework
HSPICE	Hewlett Simulation Program with Integrated Circuit Emphasis
TCL	Tool Command Language
GMR	Giant Magnetoresistance
FM	Ferromagnetic
NM	Nonferromagnetic
p	Parallel
AP	Anti-Parallel
MRAM	Magnetoresistive Random-Access Memory
LiM	Logic-in-Memory
NM	Non-magnetic
PL	Pinned Layer
FL	Free Layer
SHE	Spin Hall Effect
SOT	Spin-orbit Torque
VCMA	Voltage-Controlled Magnetic Anisotropy
DOS	Density of State
iMTJ	In-Plane MTJ
pMTJ	Perpendicular-plane MTJ
NV	Non-volatile
MA	Magnetic Anisotropy
IMA	In-Plane Magnetic Anisotropy
PMA	Perpendicular-plane Magnetic Anisotropy
MR	Magnetoresistance
SAF	Synthetic Antiferromagnetic
LLGS	Landau-Lifshitz-Gilbert-Slonczewski
NUCD	Non-Uniform Current Density
SA	Sense Amplifier
nMOS	N-Type Metal-Oxide-Semiconductor
PCSA	Pre-Charge Sense Amplifier
FLT	Field-Like Torque

LIST OF SYMBOLS

Symbol	Abbreviation
R_{P}	Parallel Resistance of MTJ
R_{AP}	Anti-parallel Resistance of MTJ
C_{P}	Parallel Capacitance of MTJ
C_{AP}	Anti-parallel Capacitance of MTJ
α	Damping Coefficient
RA	Resistance-Area Product
P	Spin Polarization Factor of the FM
γ	Gyromagnetic Ratio
M	Magnetization of an FM layer
I_S	Spin-polarized Current
t_C	Critical Thickness of Free Layer
I_W	Write Current
I_C	Critical Current
E_F	Fermi Energy Level
S	Surface area of MTJ
J	Current Density
$N_{\uparrow}$	Up-spin Electrons at the Fermi energy
$N_{\downarrow}$	Down-spin Electrons at the Fermi energy
$\mathrm{E_b}$	Energy Berrier Height
t_{FL}	Thickness of Free Layer
M_S	Saturation Magnetization
V_{dd}	Power supply Voltage
$V_{1/2}$	Half bias Voltage
T	Temperature
k_B	Boltzmann's Constant
$\tau\vert\vert$	In-plane Torque
$\tau\perp$	out-of-plane Torque

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