CHAPTER 3

High Gain Interleaved Boost Converter

3.1 Introduction

Chapter 2 presents a TSHGC which can be used as a front-end DC-DC converter for two-stage AC residential distribution system. Although the TSHGC has high voltage gain with continuous input current and reduced elements, it has a floating output ground and requires a high value of input inductance for low input current ripple. Also, the TSHGC has moderate voltage stresses on power semiconductor devices. To take care of the issues of TSHGC, a high gain interleaved boost converter (HGIBC) is presented in this chapter. The HGIBC is capable of giving different voltage gains in three operating regions ($0 \leq D \leq 0.5$, $0.5 \leq D \leq 1$ and $0 \leq D \leq 1$) based on two switching logics; 180° phase-shifted and complementary switching. Detailed mathematical analysis of the HGIBC is carried out in the three regions to analyze its operation and to obtain steady-state parameters. As the HGIBC is a non-isolated interleaved converter, some reported non-isolated high gain interleaved converters are considered for a reasonable comparison; in terms of number elements, voltage gain, current and voltage stresses on the elements. The performance of HGIBC is verified through simulation and experimental results.

3.2 High Gain Interleaved Boost Converter

Fig. 3.1 shows a circuit diagram of HGIBC [113]. The HGIBC is developed by interleaving the two CBCs. It can be observed from Fig. 3.1 that HGIBC has two switches ($S_1$and S_2), two diodes ($D_1$and D_2) and two capacitors (C and C_o) along with two parallelly connected inductors (L_1 and L_2) at input side. As shown in Fig. 3.1, input and output voltage ground terminals of HGIBC have a common ground. The operation of HGIBC is investigated based on two switching logics; 180° phase-shifted and complementary switching. The HGIBC has three operating regions: (1) operating region 1 ($0 \leq D < 0.5$), (2) operating region 2 ($0.5 \leq D < 1$) and (3) operating region 3 ($0 \leq D < 1$), where D is duty ratio of HGIBC. Further, the HGIBC has some salient features which are outlined as follows.

- It is capable of giving different voltage gains in the three operating regions with reduced elements as compared to some reported high gain converters. Also, it has a high voltage gain at lower values of D.
- The HGIBC has different current/voltage stresses on its elements in the three regions which leads to cost-effective device selection for a particular application according to the voltage-gain requirement.
- As it has a common ground for the input and output ground terminals, common-mode voltage problems can be resolved and differential voltage sensing/measuring devices can be avoided.
- As it is in interleaving nature, it gives low ripple in input current and output voltage with reduced energy storage elements.
- It has better power density due to the lesser number of elements and reduced energy storage elements.
- Moreover, the HGIBC can be used for multi-input power conversion from the low voltage DC sources.

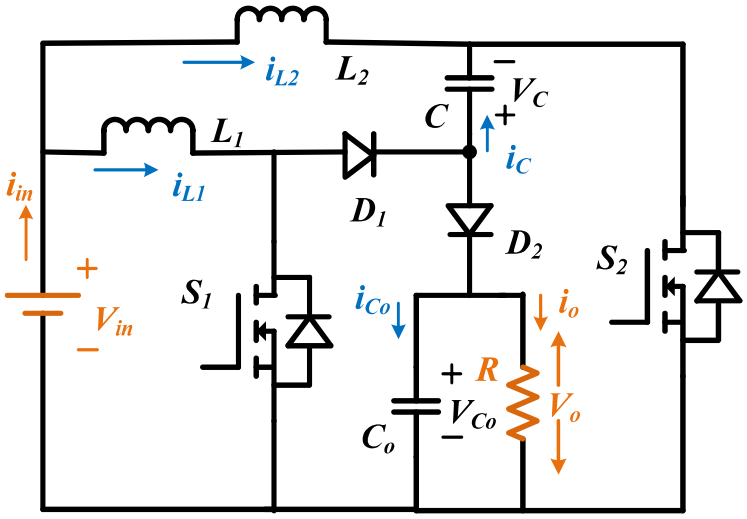


Fig. 3.1. High gain interleaved boost converter (HGIBC).

3.2.1 Operation of HGIBC

The operation of HGIBC is explained in three operating regions based on two developed switching logics. The operating waveforms and mathematical relations of HGIBC are given in the subsequent sections.

3.2.1.1 Operation of HGIBC in the Operating Region 1 ($0 \leq D \leq 0.5$)

The operating waveforms of HGIBC in the operating region, $0 \leq D \leq 0.5$ are shown in Fig. 3.2. The two switches are switched at 180° phase-shifted to each other in this region. It can be observed from Fig. 3.2 that the HGIBC operates at four switching states (state I, state II, state III, and state IV) during a switching period T_S. Moreover, HGIBC has the same behaviour in states II and IV.

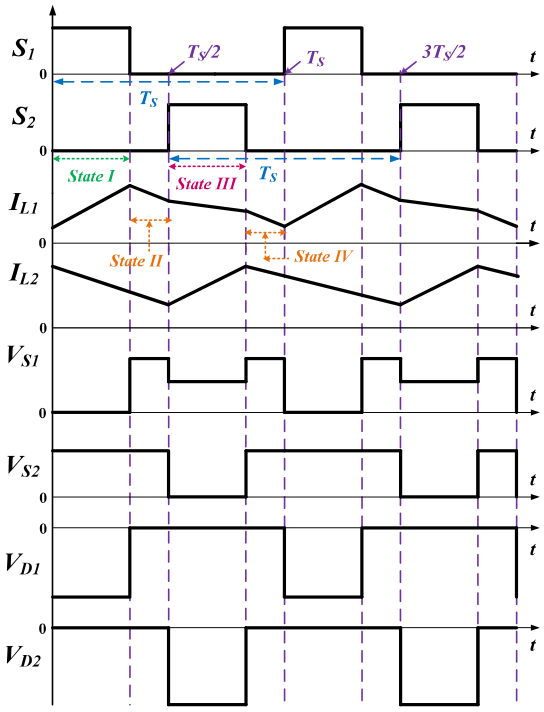


Fig. 3.2. Operating waveforms of HGIBC in the operating region 1 ($0 \leq D \leq 0.5$).

a) Switching State I (S_1 ON and S_2 OFF) of the Operating Region 1

The equivalent circuit of HGIBC at S_1 ON and S_2 OFF is shown in Fig. 3.3(a). During this state, inductor L_1 stores energy, inductor L_2 discharges its stored energy into C_o and R through C and D_2. Meanwhile, diode D_1 is reverse biased. The corresponding KCL and KVL equations of HGIBC at this switching state are given in Table 3.1.

b) Switching States II and IV (S_1 OFF and S_2 OFF) of the Operating Region 1

The equivalent circuit of HGIBC at S_1 OFF and S_2 OFF is shown in Fig. 3.3(b). During this state, L_1 discharges its stored energy into the load along with stored energy of L_2. Meanwhile,

D_1 and D_2 are forward biased and C is still in discharging mode. The corresponding KCL and KVL expressions of HGIBC at this switching state are also given in Table 3.1.

c) Switching State III (S_1 OFF and S_2 ON) of the Operating Region 1

The equivalent circuit of HGIBC at S_1 OFF and S_2 ON is shown in Fig. 3.3(c). At this switching state, L_2 stores energy from V_{in} and L_1 discharges its stored energy into C. Further, the stored energy of C_o discharges into R. Meanwhile, D_1 is forward biased and D_2 is reverse biased. The obtained KCL and KVL expressions of HGIBC at this switching state are given in Table 3.1.

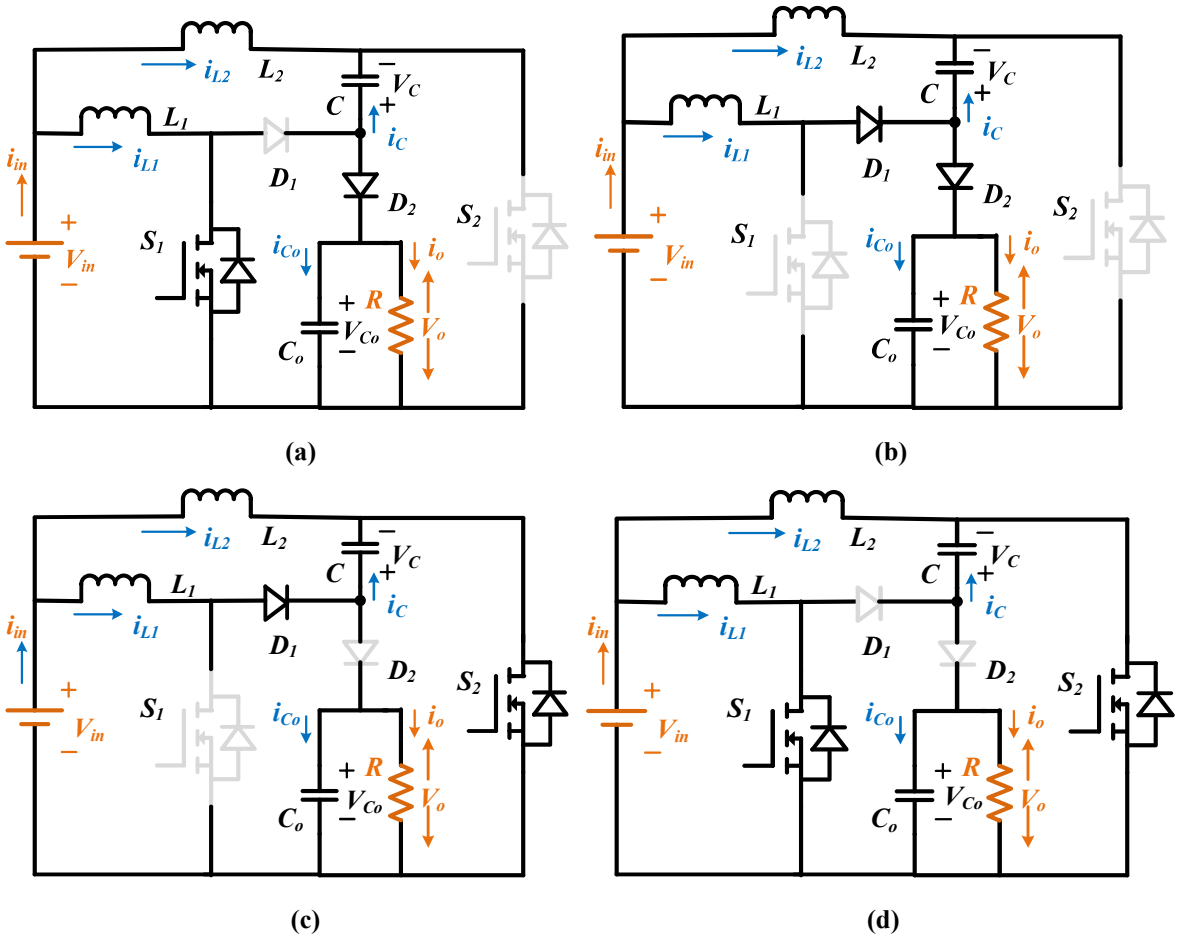


Fig. 3.3. Equivalent circuits of HGIBC at different switching states **(a)** S_1ON and S_2 OFF **(b)** S_1OFF and S_2 OFF **(c)** S_1OFF and S_2 ON **(d)** S_1ON and S_2 ON.

Table 3.1. KCL and KVL equations of HGIBC at different switching states.

	S_1 ON and S_2 ON	S_1 ON and S_2 OFF	S_1 OFF and S_2 ON	S_1 OFF and S_2 ON
v_{L1}	v_{in}	v_{in}	$v_{in} - v_C$	$v_{in} - v_{Co}$
v_{L2}	v_{in}	$v_{in} + v_C - v_{Co}$	v_{in}	$v_{in} + v_C - v_{Co}$
i_C	0	$-i_{L2}$	i_{L1}	$-i_{L2}$
i_{Co}	$-i_o$	$i_{L2} - i_o$	$-i_o$	$i_{L1} + i_{L2} - i_o$
v_{S1}	0	0	v_C	v_{Co}
i_{S1}	i_{L1}	i_{L1}	0	0
v_{S2}	0	$v_{Co} - v_C$	0	$v_{Co} - v_C$
i_{S2}	i_{L2}	0	$i_{L1} + i_{L2}$	0
v_{D1}	$-v_C$	$-v_{Co}$	0	0
i_{D1}	0	0	i_{L1}	i_{L1}
v_{D2}	$v_C - v_{Co}$	0	$v_C - v_{Co}$	0
i_{D2}	0	i_{L2}	0	$i_{L1} + i_{L2}$

By applying volt-second balance principle to inductors and charge-second balance principle to capacitors over the switching period T_S, the obtained steady-state equations of HGIBC in the operating region 1 are given in (3.1).

$$\left.\begin{array}{c} V_C = \frac{DV_{in}}{(1-D)^2} \\ V_o = V_{Co} = \frac{V_{in}}{(1-D)^2} \\ I_{L1} = (1-D)I_{in} \\ I_{L2} = DI_{in} \\ I_o = (1-D)^2 I_{in} \end{array}\right\} \quad (3.1)$$

3.2.1.2 Operation of HGIBC in Operating Region 2 ($0.5 \leq D \leq 1$)

The operating waveforms of HGIBC in the operating region, $0.5 \leq D \leq 1$ are shown in Fig. 3.4. In this operating region, the two switches are also switched at 180^o phase-shifted to each other. It can be observed from Fig. 3.4 that the HGIBC also operates at four switching states (state I, state II, state III and state IV) in this operating region. Further, the HGIBC has the same behaviour in states I and III.

a) Switching States I and III (S_1 ON and S_2 ON) of Operating Region 2

The equivalent circuit of HGIBC at S_1 ON and S_2 ON is shown in Fig. 3.3(d). In this switching state, both inductors are charged from V_{in} and two diodes are reverse biased. The stored energy of C_o is transferred to R and C is neither charging nor discharging in this state. The corresponding KCL and KVL equations of HGIBC at this switching state are given in Table 3.1.

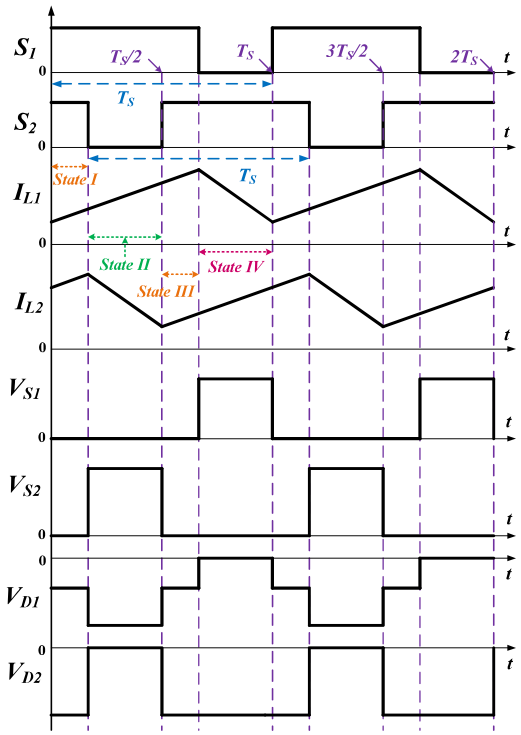


Fig. 3.4. Operating waveforms of HGIBC in the operating region 2 ($0.5 \leq D \leq 1$).

b) Switching State II (S_1 ON and S_2 OFF) of Operating Region 2

The equivalent circuit of HGIBC at S_1 ON and S_2 ON is shown in Fig. 3.3(a). The operation of HGIBC at this switching state is the same as that of switching state I of the operating region 1.

c) Switching State IV (S_1 OFF and S_2 ON) of Operating Region 2

The equivalent circuit of HGIBC at S_1 OFF and S_2 ON is shown in Fig. 3.3(c). Moreover, the operation of HGIBC at this switching state is the same as that of switching state III of the operating region 1.

After applying volt-second balance principle to inductors and charge-second balance principle to capacitors over T_S, the obtained steady-state equations of HGIBC in the operating region 2 are given in (3.2).

$$\left.\begin{aligned} V_C &= \frac{V_{in}}{(1-D)} \\ V_o = V_{Co} &= \frac{2V_{in}}{(1-D)} \\ I_{L1} = I_{L2} &= \frac{I_{in}}{2} \\ I_o &= (1-D)I_L \end{aligned}\right\} \tag{3.2}$$

3.2.1.3 Operation of HGIBC in Operating Region 3 ($0 \leq D \leq 1$)

The operating waveforms of HGIBC in the operating region, $0 \leq D \leq 1$ are shown in Fig. 3.5. In this region, the two switches are switched at complementary to each other. It can be observed from Fig. 3.5 that the HGIBC operates at two switching states (state I and state II) only over T_S, unlike the operating regions 1 and 2.

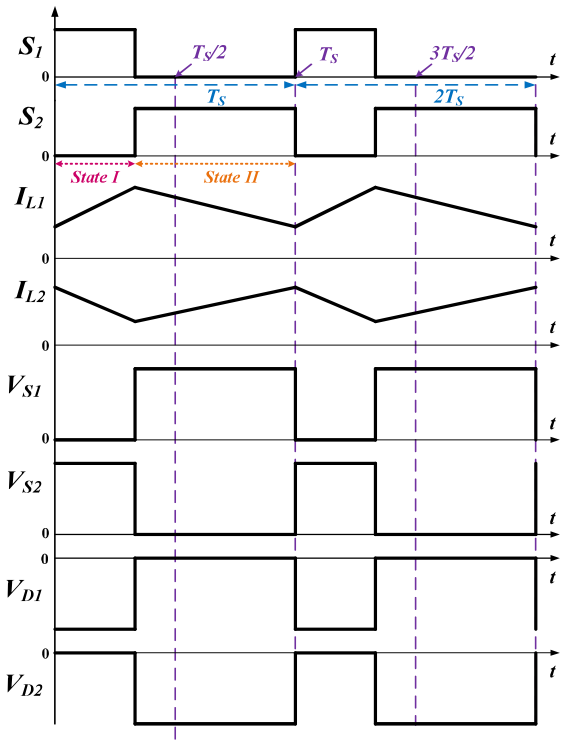


Fig. 3.5. Operating waveforms of HGIBC in the operating region 3 ($0 \leq D \leq 1$).

a) Switching State I (S_1 ON and S_2 OFF) of the Operating Region 3

The operation of HGIBC at this switching state is the same as that of switching state I of the operating region 1.

b) Switching State II (S_1 OFF and S_2 ON) of the Operating Region 3

The operation of HGIBC at this switching state is also the same as that of switching state III of the operating region 1.

After applying volt-second balance principle to inductors and charge-second balance principle to capacitors over T_S, the obtained steady-state equations of HGIBC in the operating region 3 are given in (3.3).

$$\left.\begin{aligned} V_C &= \frac{V_{in}}{(1-D)} \\ V_o = V_{Co} &= \frac{V_{in}}{D(1-D)} \\ I_{L1} &= DI_{in} \\ I_{L2} &= (1-D)I_{in} \\ I_o &= D(1-D)I_{in} \end{aligned}\right\} \tag{3.3}$$

3.2.2 Maximum Current and Voltage Stresses on the Elements of HGIBC

The current and voltage stresses on the elements of HGIBC in the three operating regions are determined and given in Table 3.2. For the operating region $0 \leq D \leq 0.5$, maximum current and voltage stresses on the elements of HGIBC normalized (by I_{in} and V_{in}) and are plotted with respect to D as shown in Fig. 3.6. It can be observed from Fig. 3.6(a) that C has lower voltage stress and devices (S_1 and D_1) have higher voltage stress among the elements (C, $Di.$, and $Sw.$) of HGIBC. Fig. 3.6(b) shows normalized maximum current stress on the elements ($Di.$, L, and $Sw.$) of HGIBC. It can be noticed from Fig. 3.6(b) that devices (D_2 and S_2) have higher current stress as compared to other elements ($Di.$, L, and $Sw.$) of HGIBC.

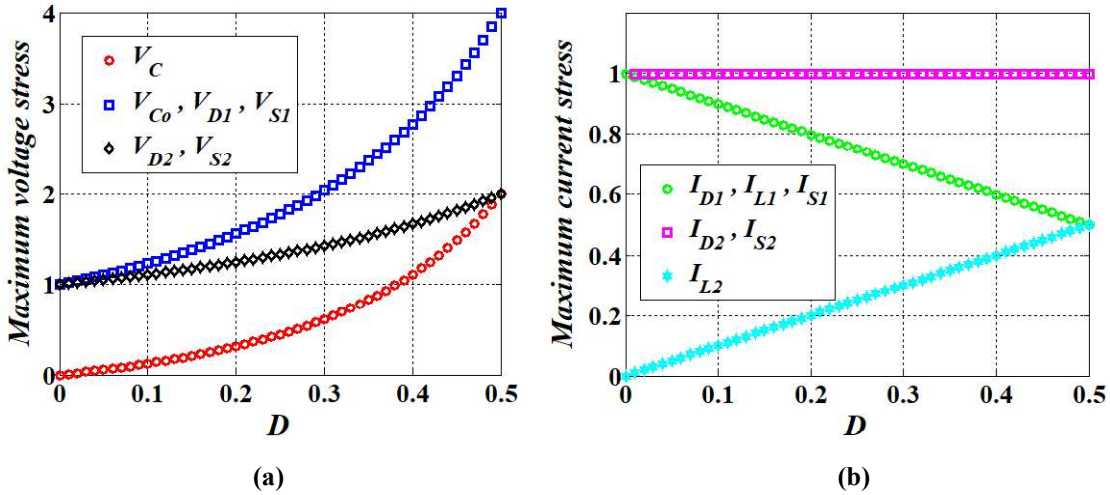
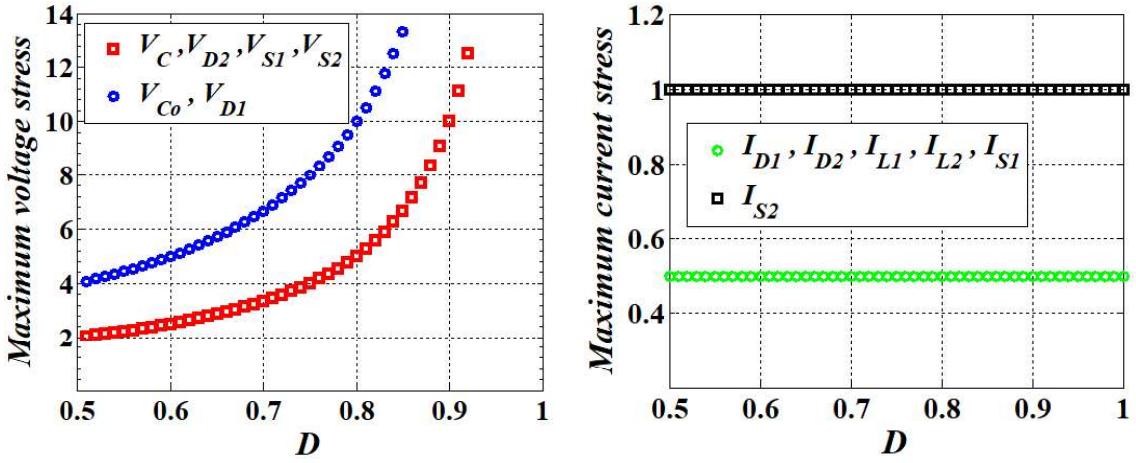


Fig. 3.6. Normalized maximum current and voltage stresses on the elements of HGIBC in the operating region 1 ($0 \leq D \leq 0.5$) **(a)** voltage stress on the elements (C, $Di.$, and $Sw.$) of HGIBC **(b)** current stress on the elements ($Di.$, L, and $Sw.$) of HGIBC.

Table 3.2. Maximum current and voltage stresses on the elements of HGIBC in the three operating regions.

	$\mathbf{0 \leq D \leq 0.5}$	$\mathbf{0.5 \leq D \leq 1}$	$\mathbf{0 \leq D \leq 1}$
$\boldsymbol{V_C}$	$\frac{D}{(1-D)^2}V_{in}$	$\frac{1}{(1-D)}V_{in}$	$\frac{1}{(1-D)}V_{in}$
$\boldsymbol{V_{C_o}}$	$\frac{1}{(1-D)^2}V_{in}$	$\frac{2}{(1-D)}V_{in}$	$\frac{1}{D(1-D)}V_{in}$
$\boldsymbol{V_{S_1}}$	$\frac{1+D}{(1-D)^2}V_{in}$	$\frac{1}{(1-D)}V_{in}$	$\frac{1}{(1-D)}V_{in}$
$\boldsymbol{V_{S_2}}$	$\frac{1}{(1-D)}V_{in}$	$\frac{1}{(1-D)}V_{in}$	$\frac{1}{D}V_{in}$
$\boldsymbol{V_{D_1}}$	$\frac{1}{(1-D)^2}V_{in}$	$\frac{1}{(1-D)}V_{in}$	$\frac{1}{D(1-D)}V_{in}$
$\boldsymbol{V_{D_2}}$	$\frac{1}{(1-D)}V_{in}$	$\frac{2}{(1-D)}V_{in}$	$\frac{1}{D}V_{in}$
$\boldsymbol{I_{L_1}}$	$(1-D)I_{in}$	$\frac{I_{in}}{2}$	DI_{in}
$\boldsymbol{I_{L_2}}$	DI_{in}	$\frac{I_{in}}{2}$	$(1-D)I_{in}$
$\boldsymbol{I_{D_1}}$	$(1-D)I_{in}$	$\frac{I_{in}}{2}$	DI_{in}
$\boldsymbol{I_{D_2}}$	I_{in}	$\frac{I_{in}}{2}$	I_{in}
$\boldsymbol{I_{S_1}}$	$(1-D)I_{in}$	$\frac{I_{in}}{2}$	DI_{in}
$\boldsymbol{I_{S_2}}$	I_{in}	I_{in}	I_{in}

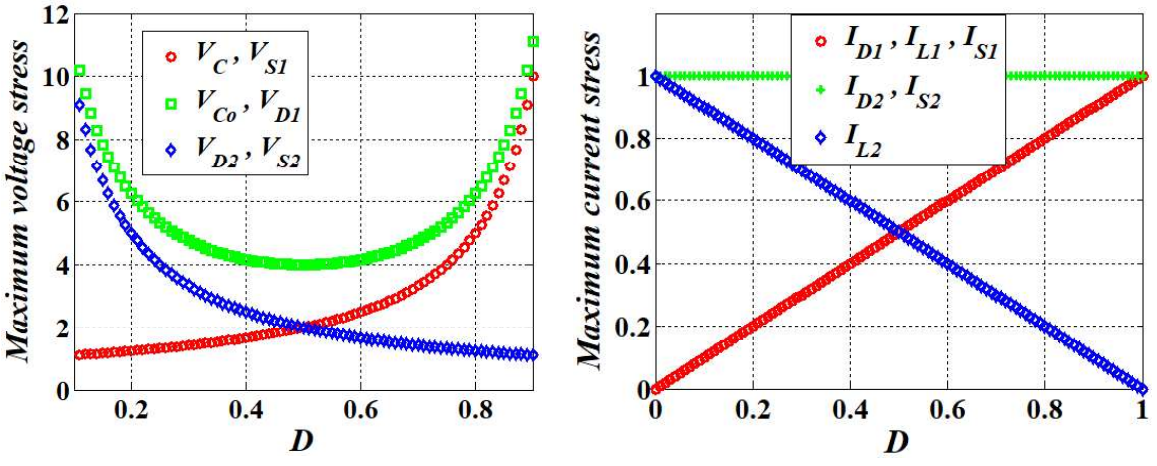
For the operating region $0.5 \leq D \leq 1$, the normalized maximum current and voltage stresses on the elements of HGIBC are also plotted with respect to D and are shown in Fig. 3.7. It can be observed from Fig. 3.7(a) that devices (D_1 and S_1) have higher voltage stress and devices (C, D_2 and S_2) have lower voltage stress. Fig. 3.7(b) shows normalized maximum current stress on the elements ($Di.$, L, and $Sw.$) of HGIBC. It can be noticed from Fig. 3.7(b) that devices (D_2 and S_2) have higher current stress as compared to other elements of HGIBC. Moreover, current stress on the elements (L_1, D_1 and S_1) decreases as D increases and current stress on L_2 increases as D increases.



(a) **(b)**

Fig. 3.7. Normalized maximum current and voltage stresses on the elements of HGIBC in the operating region 2 ($0.5 \leq D \leq 1$) **(a)** voltage stress on the elements (C, $Di.$, and $Sw.$) of HGIBC **(b)** current stress on the elements ($Di.$, L, and $Sw.$) of HGIBC.

Fig. 3.8 shows normalized maximum current and voltage stresses on the elements of HGIBC in the operating region $0 \leq D \leq 1$. It can be noticed from Fig. 3.8(a) that devices (S_1 and D_1) have higher voltage stress in comparison to other elements of HGIBC. Moreover, V_{Co} and V_{D1} decreases as D increases from 0 to 0.5 and increases as D increases from 0.5 to 1. As D increases, V_C and V_{S1} increases, and V_{D2} and V_{S2} decreases. It can be observed from Fig. 3.8(b) that devices (D_2 and S_2) have higher current stress in comparison to other elements of HGIBC. As D increases, current stress on L_2 decreases and current stress on devices (L_1, D_1 and S_1) increases.



(a) **(b)**

Fig. 3.8. Normalized maximum current and voltage stresses on the elements of HGIBC in the operating region 3 ($0 \leq D \leq 1$) **(a)** voltage stress on the elements (C, $Di.$, and $Sw.$) of HGIBC **(b)** current stress on the elements ($Di.$, L, and $Sw.$) of HGIBC.

3.2.3 Design of Passive Elements of HGIBC

For CCM operation of HGIBC, passive elements can be designed from the inequalities given in (3.4) by assuming percentage of inductor current ripples ($x_{L1}\%$ and $x_{L2}\%$) and capacitor voltage ripples ($x_C\%$ and $x_{Co}\%$).

$$\left.\begin{aligned} L_1 &\geq \frac{V_{L1}DT_s}{x_{L1}\%I_{L1}} \\ L_2 &\geq \frac{V_{L2}DT_s}{x_{L2}\%I_{L2}} \\ C &\geq \frac{I_CDT_s}{x_C\%V_C} \\ C_o &\geq \frac{I_{Co}DT_s}{x_{Co}\%V_{Co}} \end{aligned}\right\} \tag{3.4}$$

where V_{L1} and V_{L2} are voltages across L_1 and L_2, I_C and I_{Co} are currents flowing through C and C_o, D is the duty ratio and T_S is the switching period of HGIBC. Moreover, capacitor currents and inductor voltages can be considered from Table 3.1 for designing passive elements in the three operating regions of HGIBC. Further, ripple in inductor currents and capacitor voltages are determined as below.

The ripple in inductor currents (ΔI_L) of HGIBC can be calculated from the following expression.

$$\Delta I_L = \int_0^{DT_s} \frac{di_L}{dt}\,dt \tag{3.5}$$

By using (3.5), the obtained ripples in two inductor currents of HGIBC are given in (3.6).

$$\left.\begin{aligned} \Delta I_{L1} &= \frac{V_{L1}}{L_1}DT_s \\ \Delta I_{L2} &= \frac{V_{L2}}{L_2}DT_s \end{aligned}\right\} \tag{3.6}$$

where V_{L1} and V_{L2} are voltages across L_1 and L_2 during ON-time of switches.

The ripple in capacitor voltages (ΔV_C) of HGIBC can be determined from the following expression.

$$\Delta V_C = \int_0^{DT_s} \frac{dV_C}{dt}\,dt \tag{3.7}$$

By using (3.7), the obtained ripples in two capacitor voltages of HGIBC are given in (3.8).

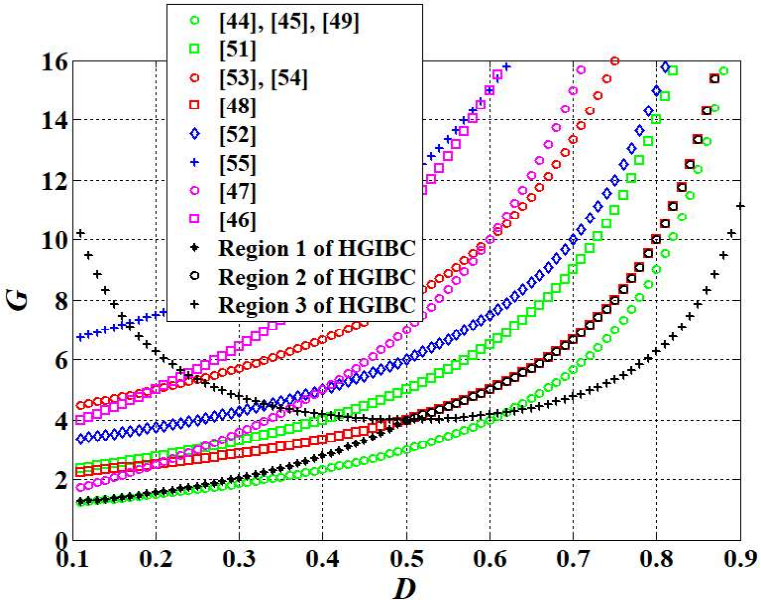
$$\left.\begin{aligned} \Delta V_C &= \frac{I_C}{C}DT_s \\ \Delta V_{Co} &= \frac{I_{Co}}{C_o}DT_s \end{aligned}\right\} \tag{3.8}$$

where I_C and I_{Co} are currents through C and C_o during ON-time of the switches.

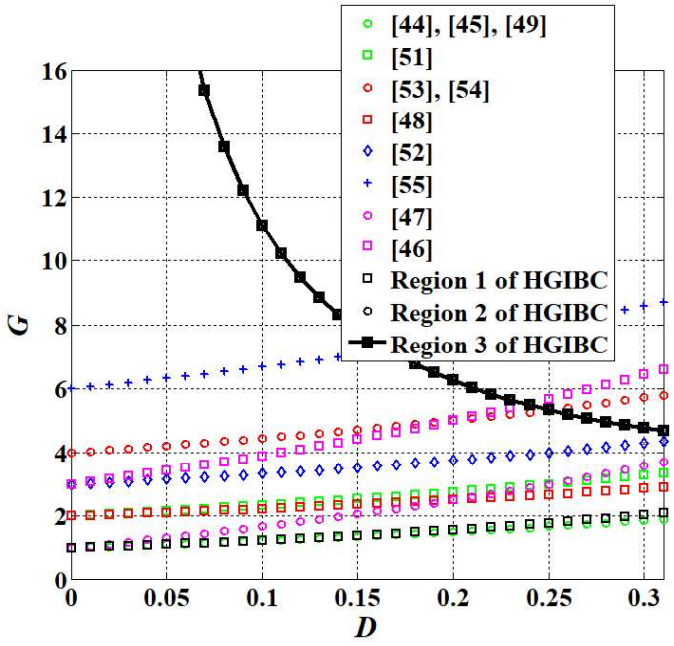
3.3 Comparison Between HGIBC and Some Reported High Gain DC-DC Converters

As the HGIBC is non-isolated topology, some reported non-isolated high gain converters [44]-[55] are only considered for a reasonable comparison. The comparison is made in terms of a number of elements, voltage gain, nature of input current and output voltage of the reported converters as compared to HGIBC, and is given in Table 3.3. Further, a discussion on the pros and cons of HGIBC is made in comparison to reported converters and given in Table 3.4. It can be observed from Table 3.3 that the HGIBC has lesser number of elements and has three different voltage gains as compared to reported converters [46]-[55]. Also, the HGIBC has continuous input current with less ripple and common ground between input and output voltage ground terminals. The voltage gains of HGIBC in comparison to reported converters are plotted with respect to D and are shown in Fig. 3.9. It can be noticed from Fig. 3.9(a) that the HGIBC has higher voltage gain in comparison to reported converters for $D \leq 0.25$. Although converters reported in [46], [47], [53] and [54]; have higher voltage gain for $D \geq 0.25$ in comparison to HGIBC, they have a higher number of elements. Further, the normalized total maximum voltage stress on the elements ($Sw.$, $Di.$ and C) of HGIBC and converters reported in [46]-[55] are determined and given in Table 3.5. The normalized total maximum voltage stress on the elements are plotted with respect to D and is shown in Fig. 3.10. It can be observed from Fig. 3.10(a) that the HGIBC has lesser total switch voltage stress as compared to converters reported in [46]-[55] for $D \geq 0.5$. Although converters reported in [46]-[55] have lesser switch voltage stress in comparison to HGIBC for $D \leq 0.22$, they have a higher number of elements. Fig. 3.10(b) shows normalized total diode maximum voltage stress of HGIBC as compared to reported converters [46]-[55]. It can be noticed from Fig. 3.10(b) that the converters reported in [46], [47], [53]-[55] have higher diode voltage stress as compared to HGIBC and remaining reported converters for $D \geq 0.22$. Also, the HGIBC has lesser diode voltage stress in comparison to converters reported in [46]-[55] for $D \geq 0.65$. Fig. 3.10(c) shows normalized total capacitor maximum voltage stress of HGIBC as compared to reported converters [46]-[55]. It can be observed from Fig. 3.10(c) that the HGIBC and converter reported in [49] have lesser capacitor voltage stress as compared to converters reported in ([46]-[48] and [51]-[55]) for $D \geq 0.5$. Also, converter reported in [55] has higher capacitor voltage stress as compared to converters reported in [46]-[54] at low values of D. Hence, it can be concluded from Fig. 3.10 that the HGIBC has different voltage

stresses on the elements for various values of D as compared to some reported converters. As the cost of the devices depends on the current and voltage stresses, cost-effective device selection of the HGIBC can be made according to the gain requirement for a particular application.



(a)



(b)

Fig. 3.9. Voltage gain variation of HGIBC with respect to D in comparison to some reported high gain DC-DC converters **(a)** normal view of voltage gain plot **(b)** zoomed view of voltage gain plot.

Table 3.3. Comparison between HGIBC and some reported high gain converters.

Converters	$Sw.$	$Di.$	L	C	Total Elements	Voltage Gain $(\frac{V_o}{V_{in}})$	Input Current	Output Voltage
Fig. 3(a), [44]	3	6	2	7	18	$\frac{1+D}{1-D}$	Continuous with low ripple	Floating output
Fig. 1, [45]	1	3	2	3	9	$\frac{1+D}{(1-D)}$	Continuous with more ripple	Common ground
Fig. 9, [46]	2	9	4	3	18	$\frac{3+5D}{1-D}$	Continuous with more ripple	Floating ground
Fig. 1, [47]	3	12	6	1	22	$\frac{1+5D}{1-D}$	Continuous with more ripple	Floating ground
Fig. 1, [48]	2	3	2	3	10	$\frac{2}{1-D}$	Continuous with low ripple	Floating and inverting output
Fig. 1, [49]	2	2	2	2	8	$\frac{1+D}{1-D}$	Continuous with more ripple	Floating ground
Fig. 2, [51]	3	3	3	3	12	$\frac{2+D}{1-D}$	Continuous with low ripple	Floating ground
Fig. 1, [52]	2	3	2	3	10	$\frac{3}{1-D}$	Continuous with low ripple	Common ground
Fig. 3, [53]	2	4	2	4	12	$\frac{4}{1-D}$	Continuous with low ripple	Floating ground
Fig. 3, [54]	2	4	2	5	13	$\frac{4}{1-D}$	Continuous with low ripple	Floating ground
Fig. 5(d), [55]	2	6	2	6	16	$\frac{6}{1-D}$	Continuous with low ripple	Floating ground
Proposed HGIBC	2	2	2	2	8	$\frac{1}{(1-D)^2}$ $\frac{2}{1-D}$ $\frac{1}{D(1-D)}$	Continuous with low ripple	Common ground

Note: C = capacitor, $Di.$ = diode, L = inductor, $Sw.$ = switch

Table 3.4. Discussion on the pros and cons of HGIBC and reported converters.

	Pros	Cons
Fig. 3(a), [44]	✓ Lower voltage stresses on the power devices ✓ Continuous input current with lower boost inductor ✓ Various operating regions ✓ Extendibility is possible	× Moderate voltage-gain × A higher number of components × Floating output
Fig. 1, [45]	✓ less number of components ✓ Common ground	× Moderate voltage gain × Input current has more ripple
Fig. 9, [46]	✓ High voltage gain ✓ Lower voltage/current stresses on the power devices ✓ Extendibility is possible	× A higher number of components × Four bulky inductors × Continuous input current with more ripple × Floating ground
Fig. 1, [47]	✓ High voltage gain ✓ Lower voltage/current stresses on the power devices ✓ Extendibility is possible	× A higher number of components × Six bulky inductors × Continuous input current with more ripple × Floating ground
Fig. 1, [48]	✓ High voltage gain ✓ Less number of components ✓ Continuous input current with less ripple ✓ Different input current ripple in two operating duty regions	× Floating ground and inverting output × The two duty regions have the same gain
Fig. 1, [49]	✓ Lesser number of components ✓ Lower voltage/current stresses ✓ Robust control is required	× Moderate voltage gain × Floating ground × Continuous input current with more ripple
Fig. 1, [50]	✓ Lower ripple in input current and output voltage ✓ Minimum phase system ✓ Common ground	× Moderate gain × Four active switches × Low efficiency
Fig. 2, [51]	✓ High voltage gain ✓ Lower ripple in input current ✓ Lesser voltage stress on power semiconductor devices	× Floating ground × Three active switches and three bulky inductors × Low efficiency
Fig. 1, [52]	✓ High voltage gain ✓ Continuous input current with less ripple ✓ Multiple input operation ✓ Common ground ✓ Extendibility is possible	× A current balancing control scheme is required among the input inductors × Non-minimum phase behaviour
Fig. 3, [53]	✓ High voltage gain ✓ Continuous input current with less ripple ✓ Lesser voltage stress on active switches	× Floating ground × A higher number of components × Operating constraint, $D \geq 0.5$
Fig. 3, [54]	✓ High voltage gain ✓ Continuous input current with less ripple ✓ Lesser voltage stress on capacitors	× Floating ground × A higher number of elements × Low efficiency
Fig. 5(d), [55]	✓ High voltage gain ✓ Continuous input current with less ripple ✓ Lesser voltage stress on switches and passive components	× Floating ground × A higher number of components × Operating constraint, $D \geq 0.5$
HGIBC	✓ Various operating regions ✓ High voltage-gain with lesser number of components ✓ Lower voltage/current stresses ✓ Continuous input current with less ripple ✓ Common ground	× Non-minimum phase behaviour × A current balancing control scheme is required among the input inductors

Table 3.5. Normalized total maximum voltage stress on the elements ($Sw.$, $Di.$, and C) of HGIBC and reported converters.

Converters	$\frac{V_S}{V_{in}}$	$\frac{V_D}{V_{in}}$	$\frac{V_C}{V_{in}}$
Fig. 9, [46]	$\frac{2(1+D)}{1-D}$	$\frac{8(1+D)}{1-D}$	$\frac{5+7D}{1-D}$
Fig. 1, [47]	$\frac{3+5D}{1-D}$	$\frac{6+8D}{1-D}$	$\frac{1+5D}{1-D}$
Fig. 1, [48]	$\frac{2}{1-D}$	$\frac{3}{1-D}$	$\frac{3}{1-D}$
Fig. 1, [49]	$\frac{2}{1-D}$	$\frac{2}{1-D}$	$\frac{2}{1-D}$
Fig. 2, [51]	$\frac{3}{1-D}$	$\frac{4}{1-D}$	$\frac{4}{1-D}$
Fig. 3, [53]	$\frac{2}{1-D}$	$\frac{8}{1-D}$	$\frac{6}{1-D}$
Fig. 3, [54]	$\frac{2}{1-D}$	$\frac{8}{1-D}$	$\frac{4}{1-D}$
Fig. 5(d), [55]	$\frac{2}{1-D}$	$\frac{12}{1-D}$	$\frac{12}{1-D}$
Proposed HGIBC	$\frac{2-D}{(1-D)^2}$ $\frac{2}{(1-D)}$ $\frac{1}{D(1-D)}$	$\frac{2-D}{(1-D)^2}$ $\frac{3}{(1-D)}$ $\frac{2-D}{D(1-D)}$	$\frac{1+D}{(1-D)^2}$ $\frac{3}{(1-D)}$ $\frac{1+D}{D(1-D)}$

Table 3.6. Common operating conditions and list of parameters for the validation of HGIBC in the three operating regions.

Parameter	**Value**
Input voltage (V_{in})	24 V
Output power (P_o)	100 W
Switching frequency (f_s)	10 kHz
Inductor (L_1)	1120 uH
Inductor (L_2)	1120 uH
Capacitor (C)	47 uF
Capacitor (C_o)	100 uF

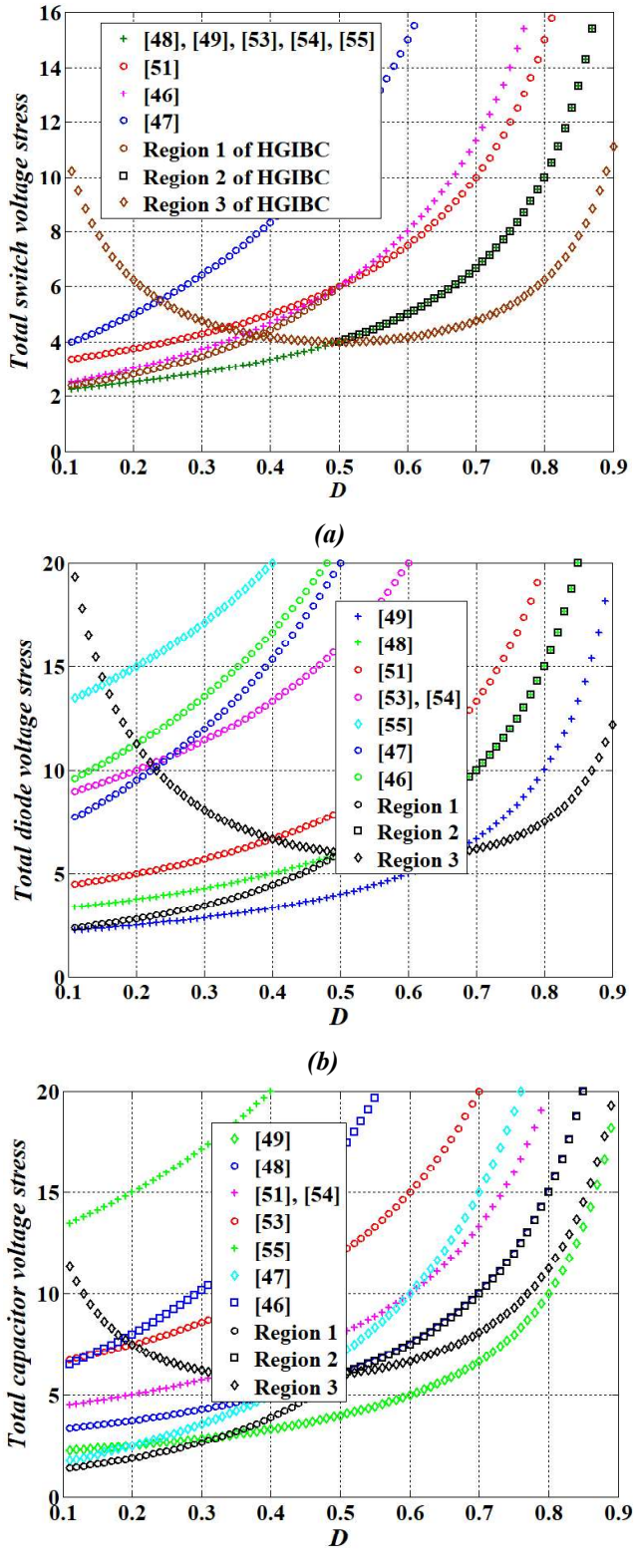


Fig. 3.10. Normalized total maximum voltage stress on the elements ($Sw.$, $Di.$, and C) of HGIBC and some reported converters with respect to D **(a)** total maximum switch voltage stress **(b)** total maximum diode voltage stress **(c)** total maximum capacitor voltage stress

3.4 Verification of HGIBC

The performance of HGIBC is verified through simulation and experimental results for the operating conditions given in Table 3.6. Further, different values of D are considered in the three operating regions of HGIBC for its verification under the same operating conditions.

3.4.1 Simulation Results of HGIBC

For the simulation studies, the considered duty ratios in the three operating regions are; $D = 0.4$ for the operating region 1, $D = 0.6$ for the operating region 2 and $D = 0.3$ for the operating region 3, respectively. The simulation results of HGIBC in the three regions are given in the subsequent sections. Moreover, Y-axis in the simulation results consists of voltage/current values having units "V" or "A" and X-axis consists of time values having a unit "s".

3.4.1.1 Simulation Results of HGIBC in Operating Region 1 ($0 \leq D \leq 0.5$)

The simulation results of HGIBC at $D = 0.4$ in the operating region $0 \leq D \leq 0.5$ are shown in Fig. 3.11. It can be noticed from Fig. 3.11(a) that voltages across capacitors are $V_C = 26.66$ V and $V_{Co} = 66.63$ V for input voltage $V_{in} = 24$ V. Moreover, the output voltage V_o is as same as V_{Co} which is shown in Fig. 3.11(b) along with load current $I_o = 1.49$ A and V_{in}. Fig. 3.11(c) shows average current flowing through L_1 as $I_{L1} = 2.55$ A along with V_{in} and gating signal V_{GS1} of S_1. It can be observed from Fig. 3.11(c) that I_{L1} has two different discharging slopes as discussed in section 3.2. Fig. 3.11(d) shows average current flowing through L_2 as $I_{L2} = 1.65$ A along with gating signal V_{GS2} of S_2 and V_{in}. The average input current, I_{in} drawn by HGIBC is a summation of I_{L1} and I_{L2}. Figs. 3.11(e) and 3.11(f) show voltages experienced by power semiconductor devices. It can be observed from Fig. 3.11(e) that maximum voltage stress across switches are $V_{S1} = 67.05$ V and $V_{S2} = 41.03$ V along with V_{in}. Moreover, V_{S1} has two values of voltage stress during OFF state of S_1. The maximum voltage stress across diodes are $V_{D1} = -66.86$ V and $V_{D2} = -40.99$ V are shown in Fig. 3.11(f) along with V_{in}. The devices (S_1 and D_1) have the same maximum voltage stress and equal to the output voltage of HGIBC. The devices (S_2 and D_2) experience lesser voltage stress as compared to S_1 and D_1.

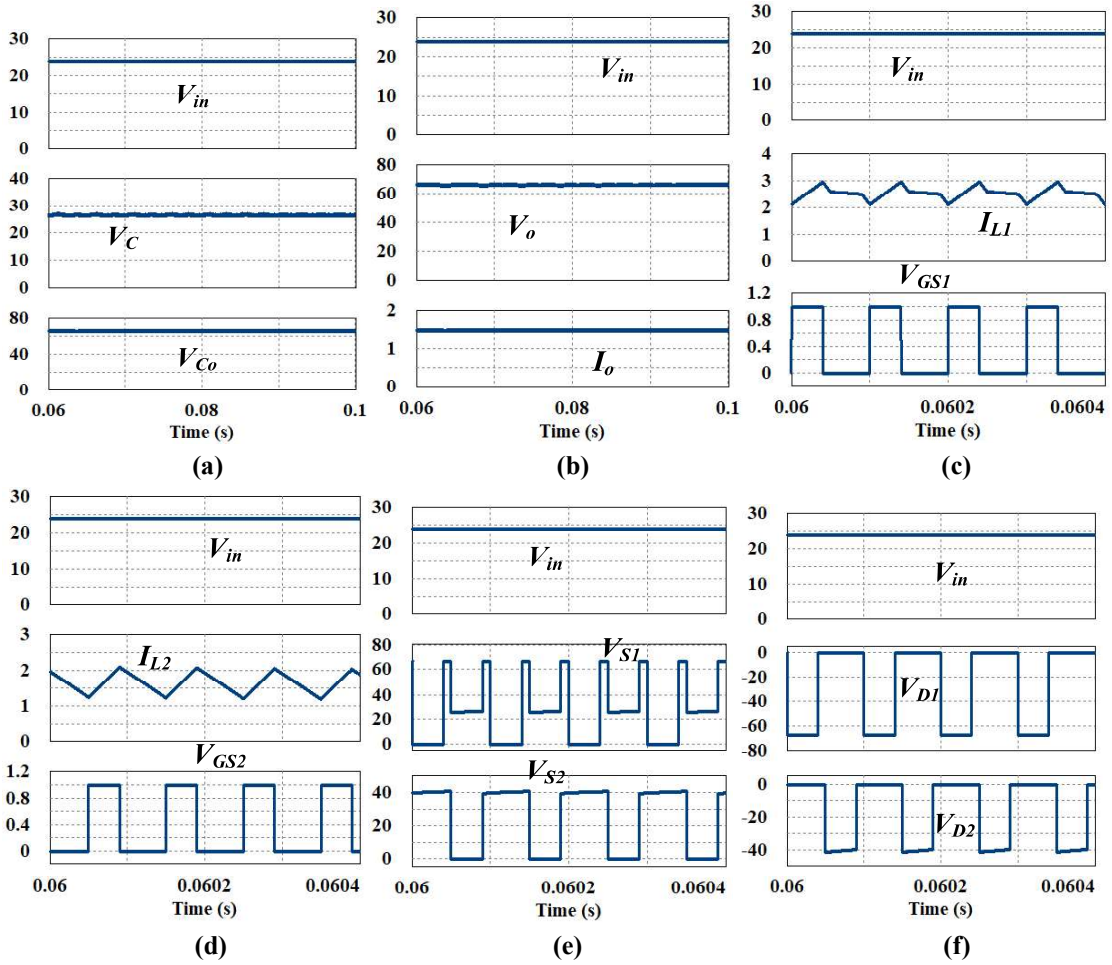


Fig. 3.11. Simulation results of HGIBC at $D = 0.4$ in the operating region 1 ($0 \leq D \leq 0.5$) **(a)** V_C, and V_{Co} for V_{in} **(b)** V_o, I_o, and V_{in} **(c)** I_{L1}, V_{GS_1}, and V_{in} **(d)** I_{L2}, V_{GS_2}, and V_{in} **(e)** V_{S1}, V_{S2}, and V_{in} **(f)** V_{D1}, V_{D2}, and V_{in}. **[Y-axis has voltage/current values, having units "V" or "A"]**

3.4.1.2 Simulation Results of HGIBC in Operating Region 2 ($0.5 \leq D \leq 1$)

The simulation results of HGIBC at $D = 0.6$ in the operating region $0.5 \leq D \leq 1$ are shown in Fig. 3.12. It can be noticed from Fig. 3.12(a) that voltages across capacitors are $V_C = 60$ V and $V_{Co} = 120$ V for $V_{in} = 24$ V. Further, V_C has more ripple as compared to V_{Co}. However, ripple in V_C can be minimized by increasing its capacitance value. Fig. 3.12(b) shows output voltage $V_o = 120$ V and load current $I_o = 0.832$ A along with V_{in}. It can be observed from Fig. 3.12(b) that value of V_o is same as that of V_{Co}. Fig. 3.12(c) shows average current flowing through L_1 as $I_{L1} = 2.28$ A along with V_{GS1} and V_{in}. It can be observed from Fig. 3.12(c) that I_{L1} has raising slope when S_1 is ON and has falling slope when S_1 is OFF. Fig. 3.12(d) shows current flowing through L_2 as $I_{L2} = 2.43$ A along with V_{GS2} and V_{in}. Figs. 3.12(e) and 3.12(f)

show voltages appeared across power semiconductor devices. It can be observed from Fig. 3.12(e) that maximum voltage stress experienced by switches are $V_{S1} = 60$ V and $V_{S2} = 60$ V along with V_{in}. The maximum voltage stress experienced by diodes are $V_{D1} = -120$ V and $V_{D2} = -60$ V can be noticed from Fig. 3.12(f) along with V_{in}. Moreover, V_{D1} has two values of voltage stress during its OFF state.

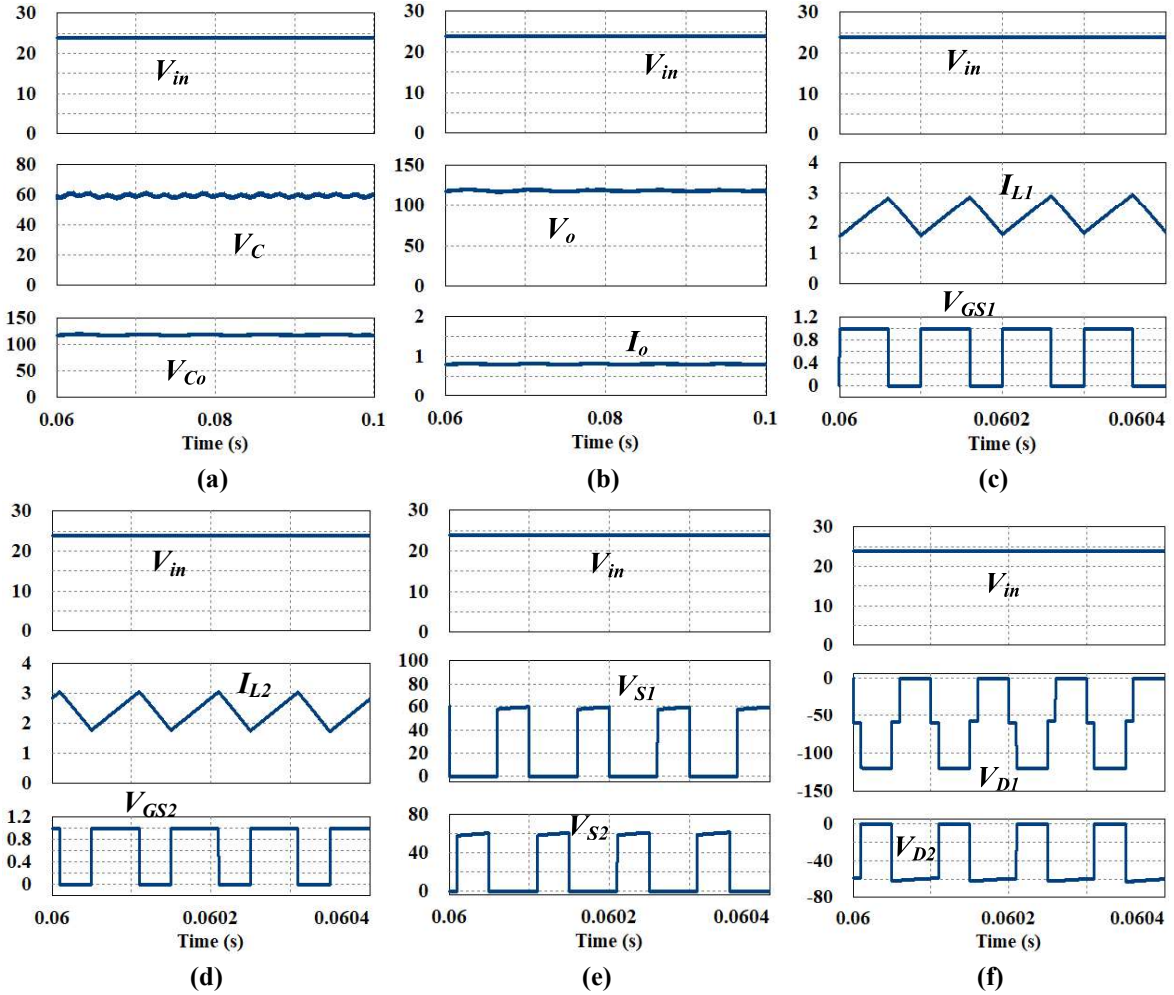


Fig. 3.12. Simulation results of HGIBC at $D = 0.6$ in the operating region 2 ($0.5 \leq D \leq 1$) **(a)** V_C, and V_{Co} for V_{in} **(b)** V_o, I_o, and V_{in} **(c)** I_{L1}, V_{GS_1}, and V_{in} **(d)** I_{L2}, V_{GS_2}, and V_{in} **(e)** V_{S1}, V_{S2}, and V_{in} **(f)** V_{D1}, V_{D2}, and V_{in}. **[Y-axis has voltage/current values, having units "V" or "A"]**

3.4.1.3 Simulation Results of HGIBC in Operating Region 3 ($0 \leq D \leq 1$)

The simulation results of HGIBC at $D = 0.3$ in the operating region $0 \leq D \leq 1$ are shown in Fig. 3.13. It can be noticed from Fig. 3.13(a) that voltages across capacitors are $V_C = 34.2$ V and $V_{Co} = 114.2$ V for $V_{in} = 24$ V. Fig. 3.13(b) shows output voltage $V_o = 114.29$ V and

load current $I_o = 0.87$ A along with V_{in}. Also, V_o is same as that of V_{Co}. Fig. 3.13(c) shows the average current flowing through L_1 as $I_{L1} = 1.57$ A along with V_{GS1} and V_{in}. It can be observed from Fig. 3.13(c) that L_1 starts charging when S_1 is ON and starts discharging when S_1 is OFF as same as in the other two operating regions. Fig. 3.13(d) shows the average current flowing through L_2 as $I_{L2} = 3.23$ A along with V_{GS2} and V_{in}. It can be observed from Fig. 3.13(e) that maximum voltage stress experienced by switches are $V_{S1} = 33.87$ V and $V_{S2} = 81.7$ V. Fig. 3.13(f) shows maximum voltage stress appeared across diodes are $V_{D1} = -115.9$ V and $V_{D2} = -81.7$. It can be concluded from Figs. 3.13(e) and 3.13(f) that D_1 has higher voltage stress and S_1 has lower voltage stress among power semiconductor devices.

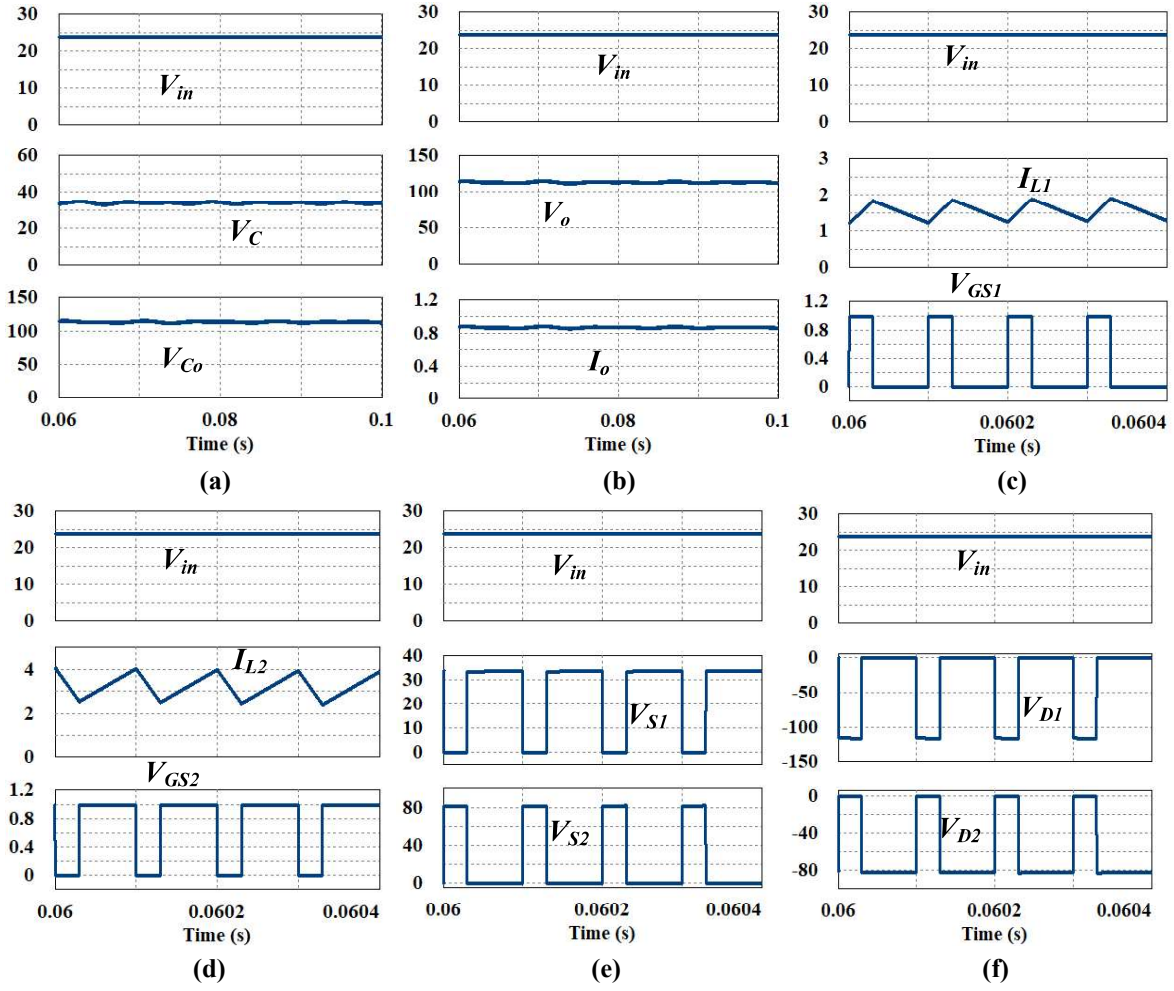


Fig. 3.13. Simulation results of HGIBC at $D = 0.3$ in the operating region 3 ($0 \leq D \leq 1$) **(a)** V_C, and V_{Co} for V_{in} **(b)** V_o, I_o, and V_{in} **(c)** I_{L1}, V_{GS_1}, and V_{in} **(d)** I_{L2}, V_{GS_2}, and V_{in} **(e)** V_{S1}, V_{S2}, and V_{in} **(f)** V_{D1}, V_{D2}, and V_{in}. **[Y-axis has voltage/current values, having units "V" or "A"]**

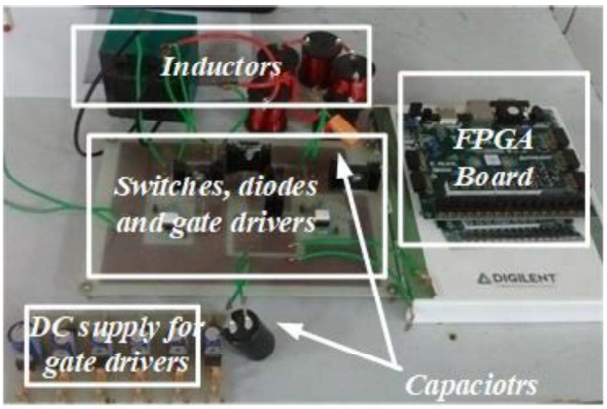


Fig. 3.14. A photograph of the experimental set-up of HGIBC.

3.4.2 Experimental Results of HGIBC

A laboratory prototype is developed to verify the performance of HGIBC in the three operating regions at different values of D. For experimentation, considered values of D for simulation are also used. Fig. 3.14 shows a photograph of the experimental set-up of HGIBC.

3.4.2.1 Experimental Results of HGIBC in Operating Region 1 ($0 \leq D \leq 0.5$)

The experimental results of HGIBC at $D = 0.4$ in the operating region $0 \leq D \leq 0.5$ are shown in Fig. 3.15. It can be noticed from Fig. 3.15(a) that voltages across capacitors are $V_C = 24.6$ V and $V_{Co} = 63.3$ V for $V_{in} = 24$ V. Fig. 3.15(b) shows output voltage $V_o = 63.3$ V and load current $I_o = 1.44$ A along with V_{in}. It can be observed from Fig. 3.15(c) that average current flowing through L_1 as $I_{L1} = 2.55$ A along with V_{GS1} and V_{in}. Further, I_{L1} has two discharging profiles during OFF-state of S_1. Fig. 3.15(d) shows the average current flowing through L_2 as $I_{L2} = 1.69$ A along with V_{GS2} and V_{in}. It can be noticed from Fig. 3.15(e) that maximum voltage stress experienced by switches are $V_{S1} = 64.3$ V and $V_{S2} = 41.2$ V along with V_{in}. Moreover, S_1 has two different values of voltage stress during its OFF-state because of two discharging profiles of I_{L1}. Fig. 3.15(f) shows maximum voltage stress appeared across diodes as $V_{D1} = -64.66$ V and $V_{D2} = -40.2$ V for V_{in}.

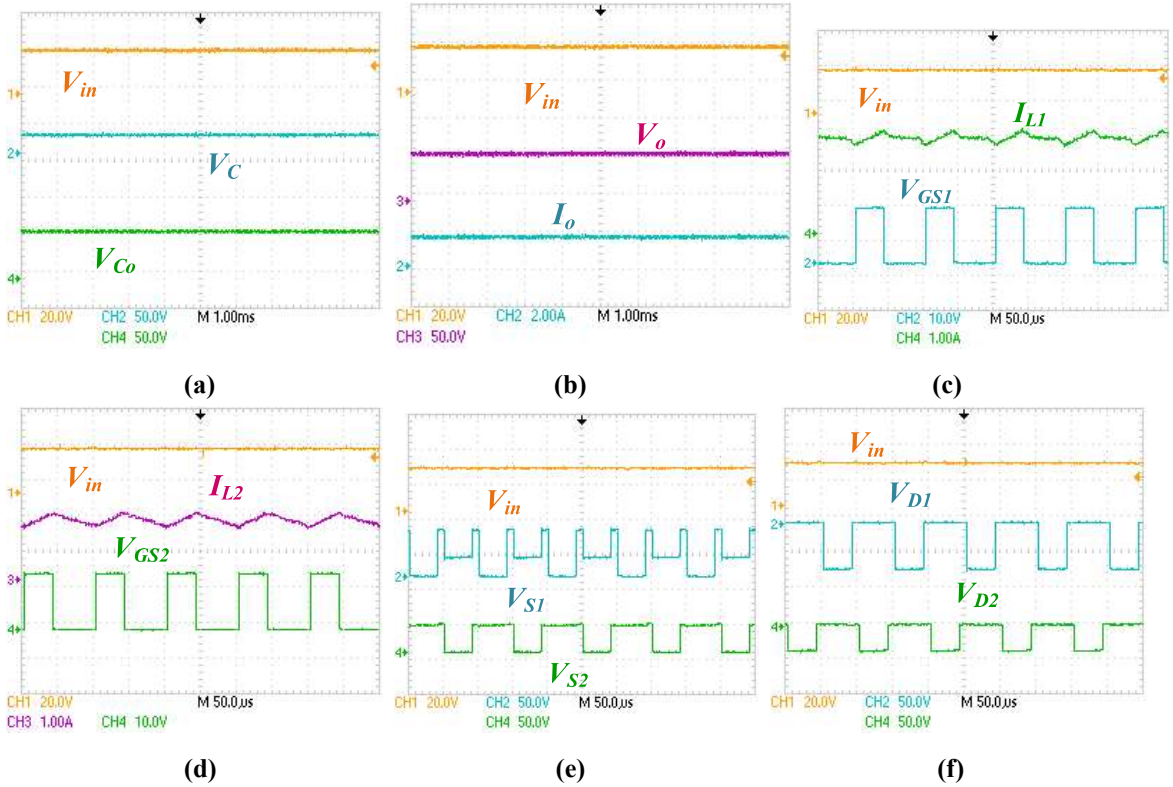


Fig. 3.15. Experimental results of HGIBC at $D = 0.4$ in the operation region 1 ($0 \leq D \leq 0.5$) **(a)** V_C, and V_{Co} for V_{in} **(b)** V_o, I_o, and V_{in} **(c)** I_{L1}, V_{GS_1}, and V_{in} **(d)** I_{L2}, V_{GS_2}, and V_{in} **(e)** V_{S1}, V_{S2}, and V_{in} **(f)** V_{D1}, V_{D2}, and V_{in}.

3.4.2.2 Experimental Results of HGIBC in Operating Region 2 ($0.5 \leq D \leq 1$)

Fig. 3.16 shows experimental results of HGIBC at $D = 0.6$ in the operating region $0.5 \leq D \leq 1$. It can be observed from Fig. 3.16(a) that voltages across capacitors are $V_C = 59.1$ V and $V_{Co} = 116$ V for $V_{in} = 24$ V. Fig. 3.16(b) shows output voltage $V_o = 116$ V and load current $I_o = 0.81$ A along with V_{in}. It can be noticed from Fig. 3.16(c) that average current flowing through L_1 as $I_{L1} = 2.14$ A along with V_{GS1} and V_{in}. Fig. 3.16(d) shows average current flowing through L_2 as $I_{L2} = 2.16$ A along with V_{GS2} and V_{in}. Figs. 3.16(e) and 3.16(f) show voltages appeared across power semiconductor devices. It can be observed from Fig. 3.16(e) that maximum voltage stress across switches are $V_{S1} = 59.2$ V and $V_{S2} = 59.1$ V along with V_{in}. The maximum voltage stress across diodes are $V_{D1} = -117$ V and $V_{D2} = -59.1$ V can be noticed from Fig. 3.16(f). Moreover, V_{D1} has two different values of voltage stress during its reverse-biased condition.

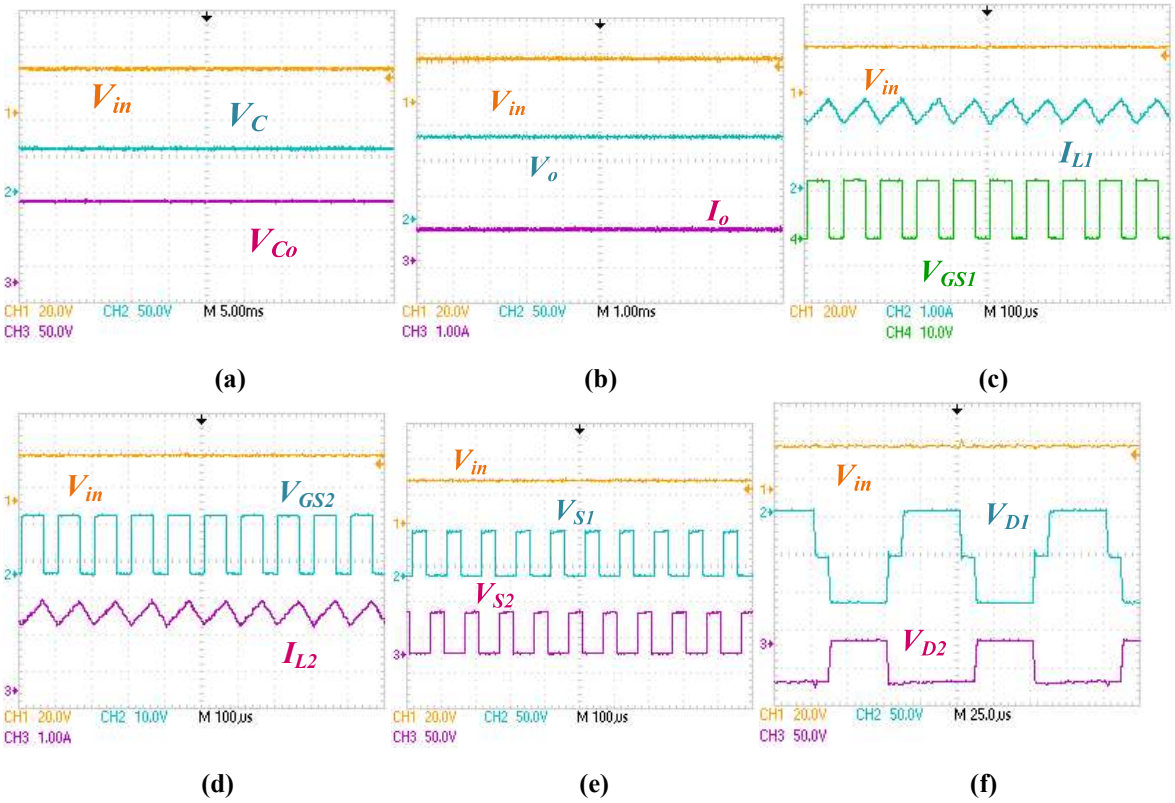


Fig. 3.16: Experimental results of HGIBC at $D = 0.6$ in the operating region 2 ($0.5 \leq D \leq 1$) **(a)** V_C, and V_{Co} for V_{in} **(b)** V_o, I_o, and V_{in} **(c)** I_{L1}, V_{GS_1}, and V_{in} **(d)** I_{L2}, V_{GS_2}, and V_{in} **(e)** V_{S1}, V_{S2}, and V_{in} **(f)** V_{D1}, V_{D2}, and V_{in}.

3.4.2.3 Experimental Results of HGIBC in Operating region 3 ($0 \leq D \leq 1$)

The experimental results of HGIBC at $D = 0.3$ in the operating region $0 \leq D \leq 1$ are shown in Fig. 3.17. It can be noticed from Fig. 3.17(a) that capacitor voltages are $V_C = 31.2$ V and $V_{Co} = 109$ V for $V_{in} = 24$ V. Fig. 3.17(b) shows output voltage $V_o = 109.1$ V and load current $I_o = 0.87$ A along with V_{in}. It can be observed from Fig. 3.17(c) that average current flowing through L_1 as $I_{L1} = 1.35$ A along with V_{GS1} and V_{in}. The average current flowing through L_2 as $I_{L2} = 3.01$ A can be found in Fig. 3.17(d) along with V_{GS2} and V_{in}. Figs. 3.17(e) and 3.17(f) show voltages appeared across power semiconductor devices. It can be observed from Fig. 3.17(e) that maximum voltage stress experienced by switches are $V_{S1} = 31.8$ V and $V_{S2} = 79.4$ V along with V_{in}. Fig. 3.17(c) shows maximum voltages across diodes are $V_{D1} = -109.8$ V and $V_{D2} = -79.2$ V along with V_{in}.

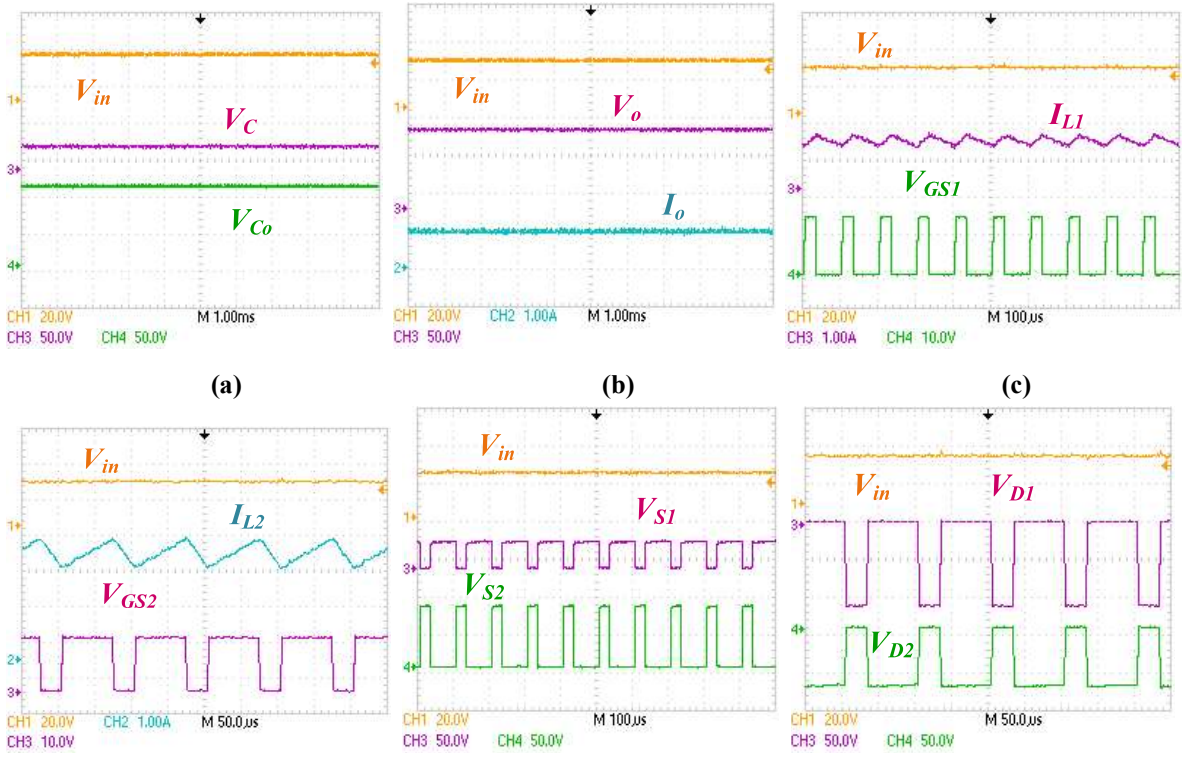


Fig. 3.17: Experimental results of HGIBC at $D = 0.3$ in the operating region 3 ($0 \leq D \leq 1$) **(a)** V_C, and V_{Co} for V_{in} **(b)** V_o, I_o, and V_{in} **(c)** I_{L1}, V_{GS_1}, and V_{in} **(d)** I_{L2}, V_{GS_2}, and V_{in} **(e)** V_{S1}, V_{S2}, and V_{in} **(f)** V_{D1}, V_{D2}, and V_{in}.

3.4.3 Power Loss Calculations and Variation in Efficiency of HGIBC

The power loss calculations of HGIBC are consisted of: conduction and switching losses of switches, conduction and reverse recovery (switching) losses of diodes, losses due to DCR of inductors and losses due to ESR of capacitors [106]-[112].

(a) Power Losses in Switches of HGIBC

The conduction losses in switches (S_1 and S_2) of HGIBC, P_{S_cond} can be calculated using (3.9).

$$P_{S\_cond} = {I_{S1,rms}}^2 * r_{DS(on),S1} + {I_{S2,rms}}^2 * r_{DS(on),S2} \tag{3.9}$$

The required RMS currents for calculating P_{S_cond} can be determined using (3.10).

$$\left.\begin{aligned} I_{S1\_rms} &= \left(\frac{1}{T_s}\int_0^{T_s}(i_{S1})dt\right)^{\frac{1}{2}} \\ I_{S2\_rms} &= \left(\frac{1}{T_s}\int_0^{T_s}(i_{S2})dt\right)^{\frac{1}{2}} \end{aligned}\right\} \tag{3.10}$$

As the HGIBC is working in three operating regions, currents through switches are also different and can be considered from Table 3.1 for calculation of RMS switch currents. Also, $r_{DS(on)}$ of switches can be known from the manufacturer's datasheet of switches.

The switching losses in switches (S_1 and S_2) of HGIBC, P_{S_switc} are obtained using (3.11).

$$P_{S\_switc} = \left[\frac{1}{2} * I_{S1,avg} * V_{S1} * \left(T_{on,S1} + T_{off,S1}\right) * f_s\right] + \left[\frac{1}{2} * I_{S2,avg} * V_{S2} * \left(T_{on,S2} + T_{off,S2}\right) * f_s\right] \quad (3.11)$$

The required currents and voltages for calculating P_{S_switc} of HGIBC in the three operating regions can be obtained from Tables 3.1 and 3.2. However, voltage and current expressions of HGIBC in the operating region 1 are given in (3.12).

$$\left.\begin{aligned} V_{S1} &= \frac{1+D}{(1-D)^2} V_{in} \\ V_{S2} &= \frac{1}{(1-D)} V_{in} \\ I_{S1} &= D I_{L_1} \\ I_{S2} &= D(I_{L_1} + I_{L_2}) \end{aligned}\right\} \quad (3.12)$$

(b) Power Losses in Diodes of HGIBC

The conduction losses in diodes (D_1 and D_2) of HGIBC, P_{D_cond} can be determined using (3.13).

$$P_{D\_cond} = \left[\left(I_{D1,avg} * V_{F,D_1}\right) + \left(I_{D1,rms}{}^2 * r_{F,D_1}\right)\right] + \left[\left(I_{D2,avg} * V_{F,D_2}\right) + \left(I_{D2,rms}{}^2 * r_{F,D_2}\right)\right] \quad (3.13)$$

For calculating P_{D_cond} of HGIBC in the three operating regions, the required RMS and average currents of diodes can be obtained from Table 3.1 and (3.14). Further, r_{F,D_1}, r_{F,D_2}, V_{F,D_1} and V_{F,D_2} can be known from the manufacturer's datasheet of diodes.

$$\left.\begin{aligned} I_{D1\_rms} &= \left(\frac{1}{T_s}\int_0^{T_s}(i_{D1})dt\right)^{\frac{1}{2}} \\ I_{D2\_rms} &= \left(\frac{1}{T_s}\int_0^{T_s}(i_{D2})dt\right)^{\frac{1}{2}} \\ I_{D1\_avg} &= \frac{1}{T_s}\int_0^{T_s}(i_{D1})dt \\ I_{D2\_avg} &= \frac{1}{T_s}\int_0^{T_s}(i_{D2})dt \end{aligned}\right\} \quad (3.14)$$

The diode switching losses (reverse recovery losses) of HGIBC, P_{D_switc} are determined using (3.15).

$$P_{D\_switc} = \left[\frac{1}{2} * (T_{RR} * I_{RR}) * V_{D1} * f_s\right] + \left[\frac{1}{2} * (T_{RR} * I_{RR}) * V_{D2} * f_s\right] \quad (3.15)$$

The required voltages (V_{D1} and V_{D2}) for calculating P_{D_switc} can be considered from Table 3.2. However, V_{D1} and V_{D2} of HGIBC in the operating region 1 are given in (3.16).

$$\left.\begin{aligned} V_{D1} &= \frac{1}{(1-D)^2} V_{in} \\ V_{D2} &= \frac{1}{(1-D)} V_{in} \end{aligned}\right\} \quad (3.16)$$

Further, reverse recovery time (T_{RR}) and reverse recovery current (I_{RR}) of diodes can be known from the manufacturer's datasheet of diodes and f_s is the switching frequency of HGIBC.

(c) Power Losses in Capacitors of HGIBC

The power losses in capacitors (C and C_o) of HGIBC, P_C are calculated using (3.17).

$$P_C = \left({I_{C,rms}}^2 * r_{ESR,C}\right) + \left({I_{C_o,rms}}^2 * r_{ESR,C_o}\right) \quad (3.17)$$

where $r_{ESR,C}$ and r_{ESR,C_o} are ESRs of capacitors.

The required RMS currents for calculating P_C can be determined using (3.18).

$$\left.\begin{aligned} I_{C\_rms} &= \left(\frac{1}{T_s}\int_0^{T_s} i_C dt\right)^{\frac{1}{2}} \\ I_{C_o\_rms} &= \left(\frac{1}{T_s}\int_0^{T_s} i_{C_o} dt\right)^{\frac{1}{2}} \end{aligned}\right\} \quad (3.18)$$

The HGIBC has different capacitor currents in the three operating regions and can be considered from Table 3.1 for capacitor RMS currents.

(d) Power Losses in Inductors of HGIBC

The power losses in inductors (L_1 and L_2) of HGIBC, P_L are determined using (3.19).

$$P_L = \left({I_{L1,rms}}^2 * r_{DCR,L_1}\right) + \left({I_{L2,rms}}^2 * r_{DCR,L_2}\right) \quad (3.19)$$

where $r_{DCR,L1}$ and r_{DCR,L_2} are DCRs of inductors.

The required RMS currents for calculating P_L can be obtained using (3.20).

$$\left.\begin{aligned} I_{L1\_rms} &= \left(\frac{1}{T_s}\int_0^{T_s} i_{L1} dt\right)^{\frac{1}{2}} \\ I_{L2\_rms} &= \left(\frac{1}{T_s}\int_0^{T_s} i_{L2} dt\right)^{\frac{1}{2}} \end{aligned}\right\} \quad (3.20)$$

The HGIBC has various inductor current profiles in the operating three regions and can be found from Table 3.1 for calculating inductor RMS currents.

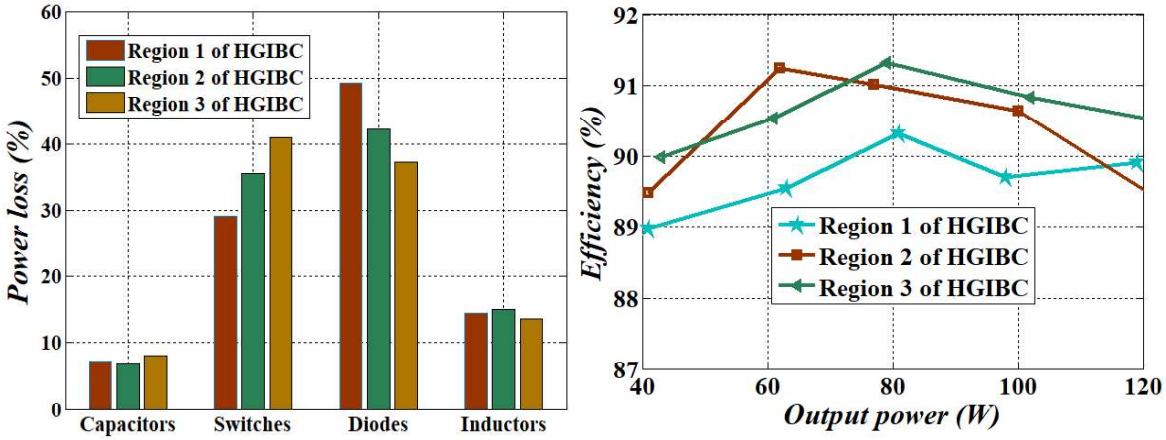


Fig. 3.18. Power loss distribution among the elements and variation in efficiency of HGIBC in the three operating regions **(a)** power loss distribution in the elements of HGIBC at rated power **(b)** efficiency variation under different loading conditions.

Based on the above power loss calculations, power losses in the elements of HGIBC in the three operating regions are determined at rated power by considering non-idealities: (1) $r_{ESR,C} = 40$ mΩ and $r_{ESR,Co} = 70$ mΩ, (2) ON-state voltage and resistance of switches $V_{DS(on)} = 1.1$ V and $r_{DS(on)} = 0.15$ Ω, (3) $r_{DCR,L1} = r_{DCR,L2} = 360$ mΩ and (4) forward voltage drop and resistance of diodes $V_F = 0.8$ V and $r_F = 0.1$ Ω. The determined power losses in the elements of HGIBC in the three operating regions are shown in Fig. 3.18(a) as a percentage of total power losses at rated power. It can be observed from Fig. 3.18(a) that diode power losses in the operating region 3 are lesser than the operating regions 1 and 2. Further, switch power losses in the operating region 1 are lesser than the operating regions 2 and 3. Fig. 3.18(b) shows the efficiency variation of HGIBC at different loading conditions in the three operating regions. It can be observed from Fig. 3.18(b) that the HGIBC has maximum efficiencies as 90.34% at 81 W in the operating region 1, 91.24% at 62 W in the operating region 2 and 91.32% at 79 W in the operating region 3.

3.5 Summary

This chapter has been investigated the three operating regions ($0 \leq D \leq 0.5$, $0.5 \leq D \leq 1$ and $0 \leq D \leq 1$) of HGIBC. The three regions have various voltage gains because of two switching logics, 180° phase-shifted and complementary switching. It can be observed from mathematical modeling that the HGIBC has different current and voltage stresses on the elements. Moreover, a comparison among the HGIBC and some reported high gain DC-DC converters is carried out in terms of number of elements and voltage gain. It can be observed from comparison that HGIBC has lesser number of elements and high gain at low values of D as compared to reported converters. Although there is a small difference in simulation and experimental values due to non-idealities of elements and measurement errors, it can be taken care of by proper design of PCB layout and avoiding lengthy wires. Further, power loss distribution and efficiency variation of HGIBC are carried out to verify its effectiveness in the three operating regions. It can be concluded from the above discussions that the HGIBC is well suited for two-stage AC system as a front-end DC-DC converter in comparison to reported converters. However, a DC-AC converter is required along with HGIBC when low voltage DC sources supply AC loads/grid of two-stage system. Hence, this arrangement leads to an increase in volume and a decrease in the reliability of the overall system. To take care of these issues, chapter 4 presents a high-gain DC-AC converter based on Z-source and switched-inductor-capacitor concepts.