Chapter 4

Quasi Z-source USMC with Reduced Inductor Current Ripple and CMV

4.1 Introduction

The maximum voltage gain of the USMC is 0.866, and to operate USMC, it should need to have a load phase angle that should lie within $\phi_o = (-\frac{\pi}{6}, \frac{\pi}{6})$. In addition, should provide dead time to H bridge switches to avoid overlapping two switch turn-on conditions. With these restrictions, USMC has not yet gained popularity in the industry applications. The impedance network is integrated with the USMC to improve the voltage transfer ratio more than unity. This can be done by two approaches, one is placing an impedance network between three-phase input and CSR, and the other is keeping an impedance network between CSR and VSI. The second approach, integration between CSR and VSI, is preferable due to the requirement of fewer components. This arrangement also acts as a protection circuit to reduce DC-link voltage spikes, which are eliminated by a braking capacitor and dissipating resistor in the conventional USMC [93]. This impedance network can improve the voltage gain, load power factor operating range and avoid the H bridge switches overlapping problem. In [94] the Z-source impedance network was introduced in the matrix converter (ZSMC). The voltage boosting was achieved by inserting a shoot-through (ST) period in a switching period [95–97]. Further this idea was extended to USMC (ZS-USMC).However,

ZS-USMC suffers from poor input current quality and requires high rating capacitors. To mitigate these issues, a quasi Z-source (QZS) is integrated with USMC (QZS-USMC) [73, 98–101] without disturbing the advantages of ZS-USMC. Compared to other high gain converters mentioned in [34, 102], QZS-USMC requires less number of passive elements (only two inductors and two capacitors). Reducing the filter requirement is an additional advantage of this converter. A new USMC topology is reported by shifting Quasi Z-source impedance (QZSI) to the supply side [35, 103, 104]. This allows QZSI to boost the output voltage and act like an input filter. However, the addition of three more bidirectional switches increased computational complexity. Also, it needs four extra capacitors, four inductors, and high rating semiconductor devices on the rectifier side, along with inverter switches. Considering the above limitations, inserting the QZS network at the DC link side is better. Increasing the output voltage also leads to a rise in common mode voltage (CMV). Therefore, it is crucial to address and minimize this increased CMV. The reduction of CMV through a modification in the modulation strategy for ZS-USMC is discussed in [105, 106], yet the inductor current ripple needs to be considered.

This chapter proposes the space vector modulation switching strategy to reduce the peak to peak common mode voltage along with the minimization of inductor current ripple in QZS-USMC.

4.2 SVM for QZS-USMC

Figure 4.1 shows the QZS-USMC, which has three stages, CSR, QZS and VSI. CSR is connected to a 3-phase supply, and has three unidirectional switches and 12 diodes. The SVM for CSR is divided into six equal sectors consisting of six active space vectors $[I_{ab}, I_{ac}, I_{bc}, I_{ba}, I_{ca}, I_{cb}]$ and three zero vectors $[I_{aa}, I_{cc}, I_{bb}]$ as shown in Figure 4.2(a). Here I_{ab} means the current starts from supply phase 'a' and returns through supply phase 'b'. Reference current vector I_{ref} drawn from the supply is formed with the help of two adjacent active vectors in each sector. The duty ratios of the active vectors are given by equation (4.1).

$$d_{iab} = m_i sin(\frac{\pi}{3} - \alpha), \quad d_{iac} = m_i sin(\alpha) \tag{4.1}$$

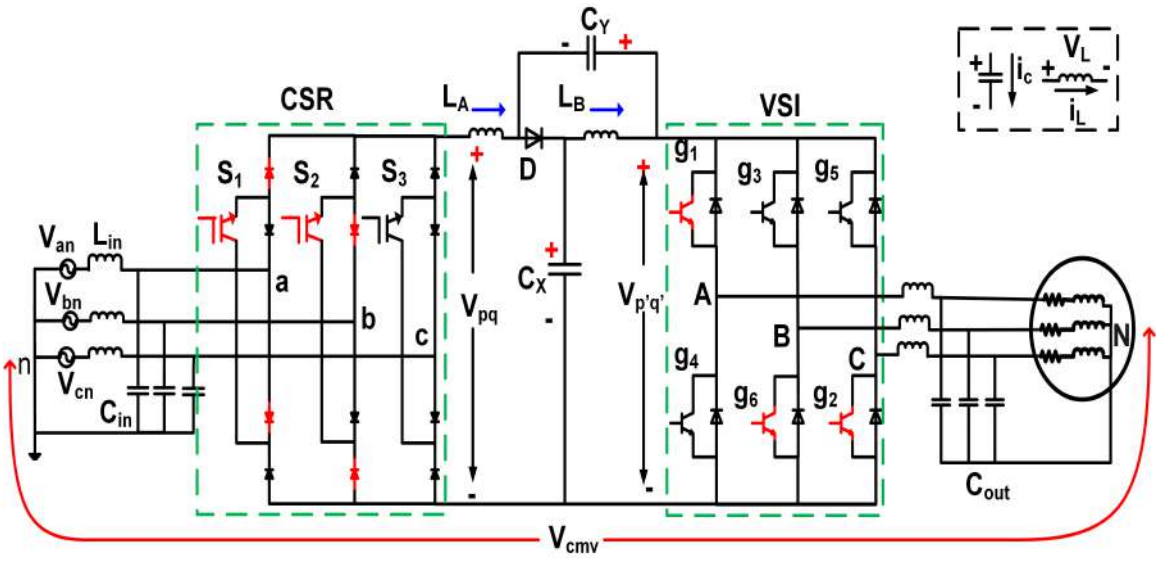

Figure 4.1: Three phase AC-AC Quasi Z-source ultra sparse matrix converter (QZS-USMC)

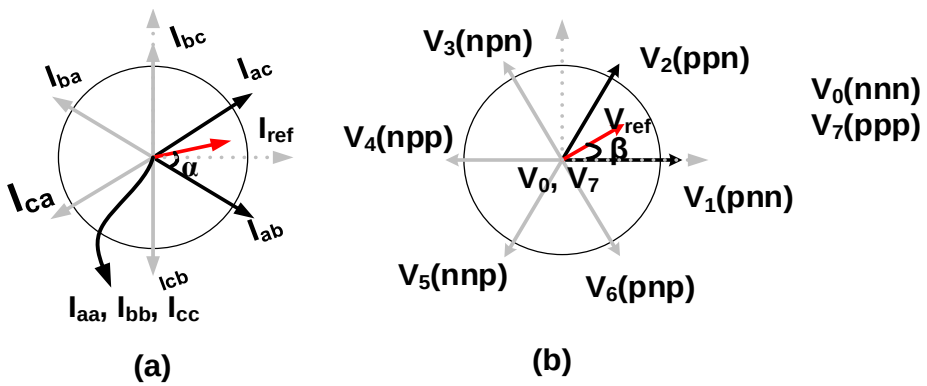

Figure 4.2: Space vector diagrams for (a) current source rectifier, and (b) voltage source inverter

Here m_i $(= \frac{I_{ref}}{I_i})$ is the CSR modulation index, α is the angle between the active vector and reference vector, I_i is the supply current and d_{iab}, d_{iac} are duty ratios of the active vectors i_{ab}, i_{ac} $|i_{ab}| = |i_{ac}| = I_i$. The output of the CSR is a pulsating DC voltage with a peak value equal to line-to-line peak voltage. The average DC voltage V_{pq} for QZS-USMC is

$$V_{pq} = \frac{3}{2} \times \hat{V}_m \times m_i \tag{4.2}$$

Here $\hat{V}_m$ is the maximum phase input voltage. m_i is a unity to achieve maximum DC voltage.

From Figure 4.2(b), the VSI involves six equal sectors, with each sector can be modelled by four active vectors out of six $[V_1, V_2, V_3, V_4, V_5, V_6]$, instead of two active vectors and zero vectors $[V_0, V_7]$ combination [107]. The reference output voltage vector

is constructed with the four adjacent active vectors. Duty ratios for the VSI stage in sector 1 are given by equation (4.3).

$$\begin{aligned} V_{ref} &= d_{v1}V_1 + d_{v2}V_2 + d_{v3}V_3 + d_{v_6}V_6 \\ d_{v1} &= m_v sin(\frac{\pi}{3} - \beta), \quad d_{v2} = m_v sin(\beta) \\ d_{v3} &= d_{v6} = d_{v0} = 1 - d_{v1} - d_{v2}, \quad m_v = \frac{\sqrt{3}V_{ref}}{V_{p'q'}} \end{aligned} \tag{4.3}$$

From Figure 4.1, QZS is inserted between CSR and VSI to get QZS-USMC. The voltage boosting is achieved by inserting the shoot-through (d_{st}) time within a switching period. To implement the switching sequence, synchronization between the CSR switching sequence and the VSI switching sequence is compulsory. This is achieved by multiplying current and voltage vector duty ratios together. For instance, if CSR and VSI are in Sector 1, then $d_{iab} \times d_{v1}$ corresponds to the I_{ab} state in the CSR and V_1 state of the VSI. Duty ratios for sector 1 of the QZS-USMC are given by equation (4.4).

$$\begin{aligned} d_1 &= d_{iab}d_{v1}, \quad d_2 = d_{iab}d_{v2} \\ d_3 &= d_{iac}d_{v2}, \quad d_4 = d_{iac}d_{v1} \\ d_0 &= 1 - d_1 - d_2 - d_3 - d_4 - d_{st} \\ m &= m_i \times m_v, \quad m + d_{st} \leq 1 \end{aligned} \tag{4.4}$$

Here, V_{pq} is a source for the QZS network. The QZS-USMC is operated in two modes: 1) Non-shoot-through (NST) mode and 2) shoot-through (ST) mode. The equivalent circuit for NST mode is shown in Figure 4.3. The diode (D) is forward-biased during this mode. Inductor L_A discharges through capacitor C_X, and inductor L_B discharges through C_Y. Expressions of current through the inductor and voltage across capacitors are given by equation (4.5).

$$\begin{aligned} C_X\frac{dV_{CX}}{dt} &= i_{LA} - i_0, \quad C_Y\frac{dV_{CY}}{dt} = i_{LB} - i_0 \\ L_A\frac{di_{LA}}{dt} &= V_{pq} - V_{CX}, \quad L_B\frac{di_{LB}}{dt} = -V_{CY} \end{aligned} \tag{4.5}$$

Where i_{LA}, i_{LB} are currents through inductor L_A, L_B respectively, i_0 is the impedance network output current, V_{CX} and V_{CY} are voltages across capacitors C_X, C_Y respectively. For the ST mode, any one leg of the inverter is shorted. Hence, diode D is reverse biased, as shown in Figure 4.4. During this mode, inductor L_A is energized by capacitor V_{CY} and V_{pq}. Likewise, inductor L_B is energized by capacitor V_{CX}. To make the calculation simple let $L_A = L_B = L$ and $C_X = C_Y = C$ in the equation (4.6).

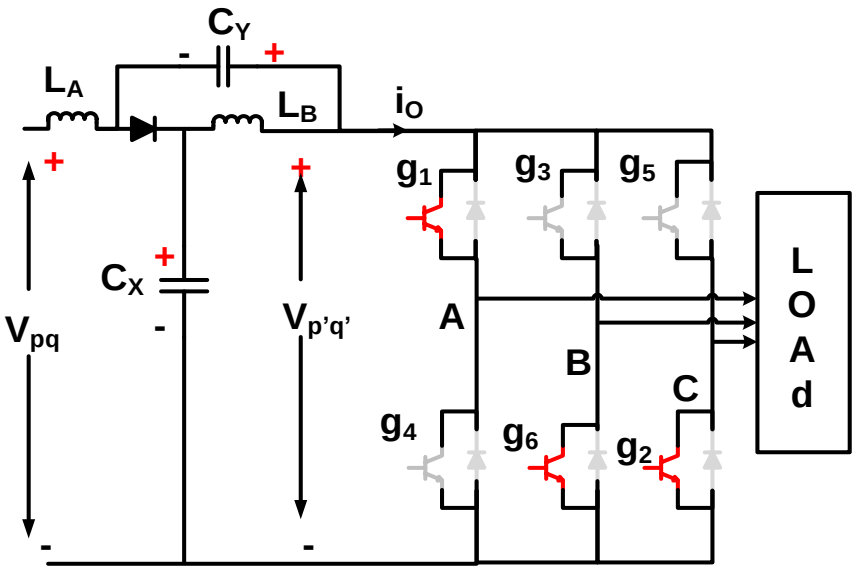

Figure 4.3: Equivalent circuit diagram for non shoot-through state (NST)

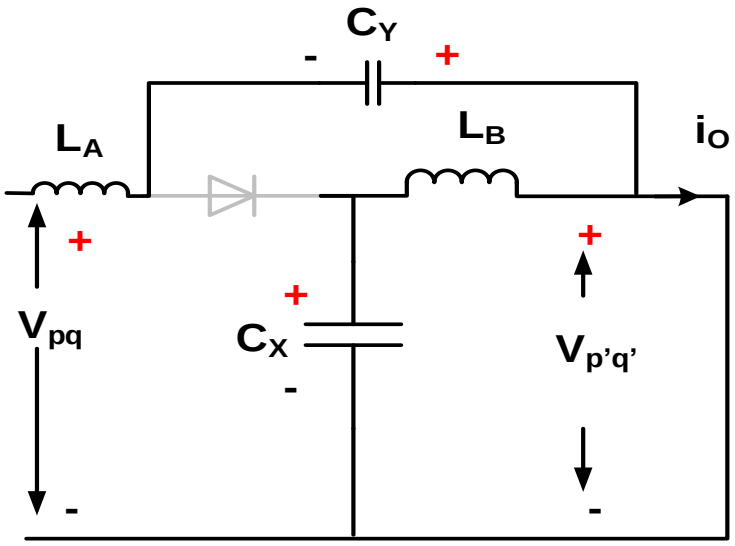

Figure 4.4: Equivalent circuit diagram for shoot-through state (ST)

$$\begin{aligned} C_X\frac{dV_{CX}}{dt} &= -i_{LB}, \quad C_Y\frac{dV_{CY}}{dt} = -i_{LA} \\ L_A\frac{di_{LA}}{dt} &= V_{pq} + V_{CY}, \quad L_B\frac{di_{LB}}{dt} = V_{CX} \end{aligned} \tag{4.6}$$

Using inductor energy balance equation and capacitor charge balance equation in one cycle, equation (4.7) is derived, where d_{st} is the duty ratio of the shoot-through state. Figure 4.5 shows the switching sequence for the conventional QZS-USMC.

$$V_{p'q'} = \frac{1}{1-2d_{st}}V_{pq} \tag{4.7}$$

The $V_{p'q'}$ is the boosted dc-link voltage. The boosting factor is

$$B = \frac{V_{p'q'}}{V_{pq}} = \frac{1}{1 - 2d_{st}} \tag{4.8}$$

The VSI per phase peak output voltage is

$$\hat{V}_{AN} = \frac{m_v V_{p'q'}}{\sqrt{3}} \tag{4.9}$$

Using equations (4.3), (4.4), (4.7), (4.8), and (4.9) the maximum phase output voltage

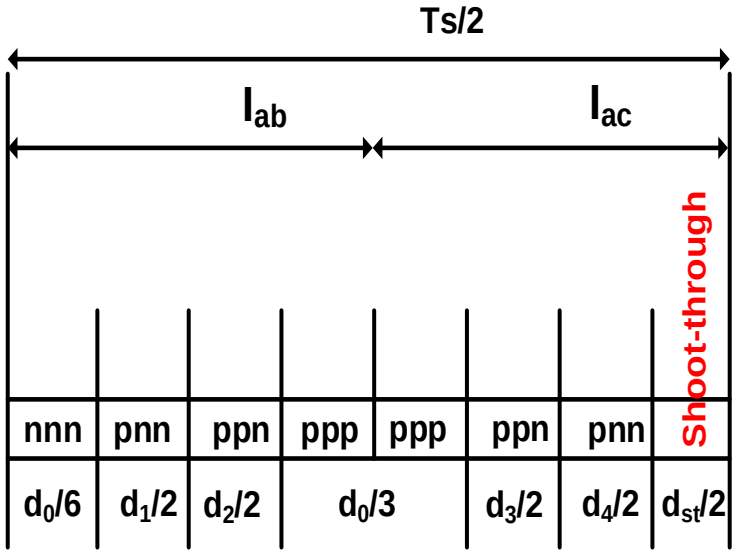

Figure 4.5: Switching sequence of the conventional switching strategy for half cycle $\frac{T_s}{2}$

of the QZS-USMC is

$$\hat{V}_{AN} = \frac{\sqrt{3}}{2} \frac{m\hat{V}_{im}}{1 - 2d_{st}} \tag{4.10}$$

4.3 Proposed switching strategy

In a conventional switching strategy, ST mode is placed in the middle of the sequence, as shown in Figure 4.5. During NST mode, both inductors are de-energized, and both capacitors are charged. Hence, the inductor current falls during this mode. In the same way, during ST mode, the inductor current builds up, and capacitors are discharged, so the inductor current rises. So from Figure 4.5 during $\frac{d_1+d_2+d_3+d_4+d_0}{2}$ time period inductor current decreases and during $\frac{d_{st}}{2}$ time period inductor current increases. Keeping the entire ST mode in one place has two main disadvantages: 1. The duration of rising inductor current and falling inductor current is longer, leading to high ripple content in

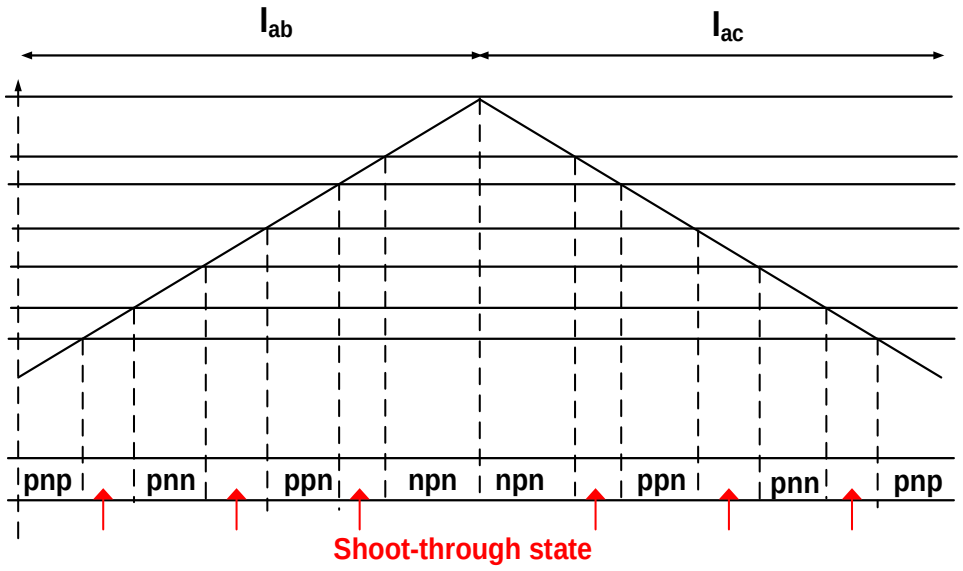

Figure 4.6: Inductor current waveform with six unequal shoot-through duty durations

the converter, as indicated by Δi_L. The entire ST period is applied to only one phase, thereby increasing harmonics on the load side. Therefore, the placement of the ST mode strongly influences the inductor current behaviour. The proposed modulation divides the entire ST mode duration into six unequal parts without changing the total shoot-through period to keep the same boosting factor (B). Figure 4.6 shows the proposed switching sequence, in which both the NST and ST modes are kept side by side to reduce ripple current in the inductor. The arrangement of the proposed modulation scheme is shown in Figure 4.7. The total ST duration is divided into $T_a, T_b, T_c, T_d, T_e, T_f$ From equations (4.5) and (4.7) current through inductor during NST mode is

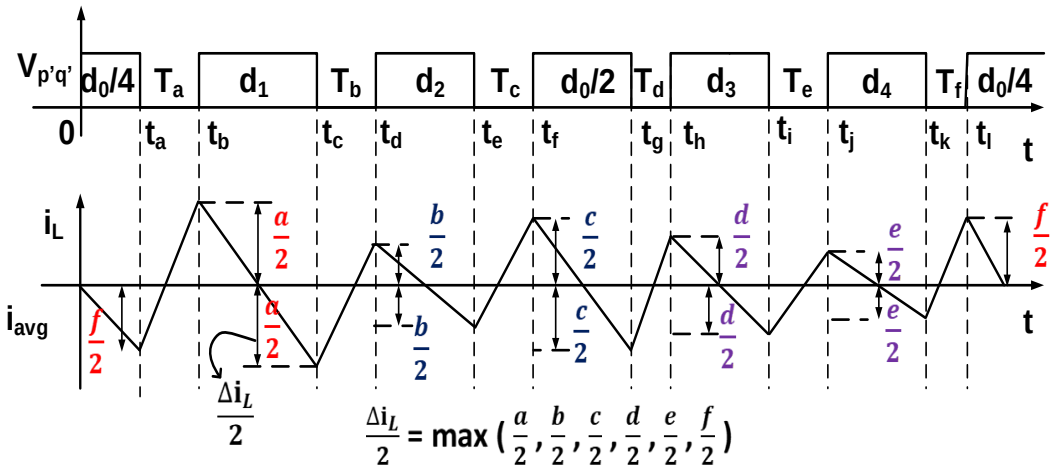

Figure 4.7: Inductor current waveform with six unequal shoot-through duty durations

$$\frac{di_{LA}}{dt} = \frac{V_{pq} - V_{CX}}{L_A} \quad = \frac{-d_{st}}{L} V_{p'q'} \tag{4.11}$$

From equation (4.6) and (4.7) inductor current during ST mode is

$$\frac{di_{LA}}{dt} = \frac{1 - d_{st}}{L} V_{p'q'} \tag{4.12}$$

From the above equations instantaneous inductor currents i_{t_a} and i_{t_b} at times t_a, t_b can be represented as

$$\begin{aligned} i_{t_a} &= i_{avg} - \frac{(d_{st})V_{p'q'}}{L}(t_a), \quad t_a = \frac{d_0}{4} \\ i_{t_b} &= i_{t_a} + \frac{(1 - d_{st})V_{p'q'}}{L}(t_b - t_a), \quad t_b = T_a + t_a \end{aligned} \tag{4.13}$$

where i_{avg} is the average inductor current. Similarly, remaining instantaneous inductor currents are calculated at different instants (t_c - t_l). The maximum ripple in the inductor current can be written as

$$\begin{aligned} \Delta i_L = 2max(&|i(t_a) - i_L|, |i(t_b) - i_L|, |i(t_c) - i_L|, |i(t_d) - i_L|, |i(t_e) - i_L|, |i(t_f) - i_L|, |i(t_g) - i_L|, \\ &|i(t_h) - i_L|, |i(t_i) - i_L|, |i(t_j) - i_L|, |i(t_k) - i_L|, |i(t_l) - i_L|) \end{aligned} \tag{4.14}$$

From Figure 4.7 and equation (4.13) instantaneous inductor current satisfies the equation (4.15).

$$\begin{aligned} |i_{t_b} - i_{avg}| + |i_{t_c} - i_{avg}| = a, \quad |i_{t_d} - i_{avg}| + |i_{t_e} - i_{avg}| = b \\ |i_{t_f} - i_{avg}| + |i_{t_g} - i_{avg}| = c, \quad |i_{t_h} - i_{avg}| + |i_{t_i} - i_{avg}| = d \\ |i_{t_j} - i_{avg}| + |i_{t_k} - i_{avg}| = e, \quad |i_{t_a} - i_{avg}| + |i_{t_l} - i_{avg}| = f \end{aligned} \tag{4.15}$$

Here a, b, c, d, e, f indicate the falling inductor current during NST mode corresponding to durations $d_1, d_2, \frac{d_0}{2}, d_3, d_4$ and $\frac{d_0}{2}$ respectively. Combining equations (4.14) and (4.15)

$$\Delta i_L \geq 2max(\frac{a}{2}, \frac{b}{2}, \frac{c}{2}, \frac{d}{2}, \frac{e}{2}, \frac{f}{2}) \tag{4.16}$$

when $|i(t_b) - i_L| = |i(t_c) - i_L| = \frac{a}{2}, |i(t_d) - i_L| = |i(t_e) - i_L| = \frac{b}{2}, |i(t_f) - i_L| = |i(t_g) - i_L| = \frac{c}{2}, |i(t_h) - i_L| = |i(t_i) - i_L| = \frac{d}{2}, and |i(t_j) - i_L| = |i(t_k) - i_L| = \frac{e}{2}$, then inductor ripple current reaches to its minimum value.

$$\Delta i_{Lmin} = max(a, b, c, d, e, f) \tag{4.17}$$

So, to get the minimum ripple current the total shoot-through durations $T_a, T_b, T_c, T_d, T_e, T_f$ from Figure 4.7, the rising inductor current ripple at T_a is

$$\Delta i_{T_a} = \frac{f}{2} + \frac{a}{2} \tag{4.18}$$

Similarly, inductor current ripple at other durations T_b, T_c, T_d, T_e, T_f are given by (4.19)

$$\begin{aligned} \Delta i_{T_b} &= \frac{a}{2} + \frac{b}{2} \\ \Delta i_{T_c} &= \frac{b}{2} + \frac{c}{2}, \quad \Delta i_{T_d} = \frac{c}{2} + \frac{d}{2}, \\ \Delta i_{T_e} &= \frac{d}{2} + \frac{e}{2} \quad and \quad \Delta i_{T_f} = \frac{e}{2} + \frac{f}{2} \end{aligned} \tag{4.19}$$

The fall in inductor current during NST mode is equal to the rise in inductor current during ST mode. So the corresponding shoot-through time period T_a can be calculated as

$$T_a = \frac{\frac{a}{2} + \frac{f}{2}}{a + b + c + d + e + f} T_{st} \quad T_{st} = d_{st} T_s \tag{4.20}$$

a, b, c, d, e, f is proportional to time interval of NST states $d_1, d_2, \frac{d_0}{2}, d_3, d_4, \frac{d_0}{2}$ and these are described as equation (4.21)

$$a : b : c : d : e : f = d_1 : d_2 : \frac{d_0}{2} : d_3 : d_4 : \frac{d_0}{2} \tag{4.21}$$

Let,

$$k = \frac{d_{st}}{2(1 - d_{st})} \quad then \quad T_a = k(d_1 + \frac{d_0}{2}) \tag{4.22}$$

Like wise the other shoot-through periods can be rearranged as given by equation (4.23).

$$\begin{aligned} T_b &= k(d_1 + d_2), \quad T_c = k(d_2 + \frac{d_0}{2}) \\ T_d &= k(\frac{d_0}{2} + d_3), \quad T_e = k(d_3 + d_4) \\ T_f &= k(d_4 + \frac{d_0}{2}) \end{aligned} \tag{4.23}$$

By substituting equations (4.1)-(4.4), (4.11)-(4.13), (4.22) and (4.23) into (4.14), $|i_{ta}| - |i_{tl}|$ can be summarised in Table 4.1, where $K_1 = \frac{d_{st}}{6Lf_s(1-2d_{st})} \hat{V_{im}}$. From the Table 4.1, current ripple of the QZS impedance network inductor depends on α, β, and shoot-through duty ratio (d_{st}). The variation of the inductor current ripple by changing α, β at $d_{st} = 0.25$ is shown in Figure 4.8.

4.4 Design guidelines

The proposed switching strategy is designed for switching frequency f_s and shoot-through duty ratio d_{st} in one cycle. From equations (4.6) and (4.7) voltage across

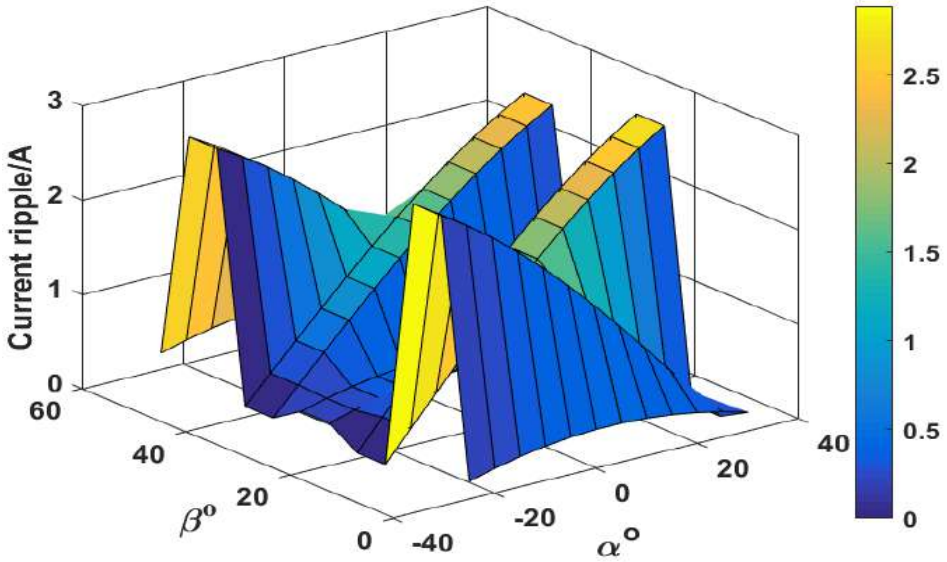

Figure 4.8: Inductor ripple current by varying current vector position (α) and voltage vector position (β)

inductor L_A is

$$V_{L_A} = \frac{1 - d_{st}}{1 - 2d_{st}} V_{pq} \tag{4.24}$$

And, during shoot-through state voltage across inductor is $V_{L_A} = L\frac{di_L}{dt}$. So,

$$L = \frac{(1 - d_{st})d_{st}}{(1 - 2d_{st})\Delta i_L} V_{pq} * T_s \tag{4.25}$$

Here Δi_L is the percentage ripple current in the inductor current. In the same manner, for the required percentage voltage ripple (ΔV_{CX}) in the capacitor voltage, the capacitance value is given by equation (4.26).

$$C_X = \frac{i_0(1 - d_{st})(d_{st})T_s}{(1 - 2d_{st})\Delta V_{CX}} \tag{4.26}$$

4.5 CMV calculation

The CMV is the voltage difference between the load neutral point (N) and supply neutral point (n). From Figure 4.1, for a balanced load, CMV is calculated by averaging the output voltages v_{An}, v_{Bn}, v_{Cn}.

$$v_{Nn} = v_{CMV} = \frac{v_{An} + v_{Bn} + v_{Cn}}{3} \tag{4.27}$$

Here v_{Nn} is the common mode voltage. So, CMV depends on the instantaneous values of three phase load voltages. CMV also depends on the switching states of the CSR

Table 4.1: Inductor ripple current for the proposed method

$\|i_{ta}\|$	$\|K_1[1 - d_{st} - mcos(\beta - \frac{pi}{6})]\|$
$\|i_{tb}\|$	$\|K_1[2m \times sin(\frac{pi}{3} - \alpha)sin(\frac{pi}{3} - \beta)]\|$
$\|i_{tc}\|$	$\|K_1[2m \times sin(\frac{pi}{3} - \alpha)sin(\frac{pi}{3} - \beta)]\|$
$\|i_{td}\|$	$\|K_1[2m \times sin(\frac{pi}{3} - \alpha)sin(\beta)]\|$
$\|i_{te}\|$	$\|K_1[2m \times sin(\frac{pi}{3} - \alpha)sin(\beta)]\|$
$\|i_{tf}\|$	$\|K_1[1 - d_{st} - mcos(\beta - \frac{pi}{6})]\|$
$\|i_{tg}\|$	$\|K_1[1 - d_{st} - mcos(\beta - \frac{pi}{6})]\|$
$\|i_{th}\|$	$\|K_1[2m \times sin(\frac{pi}{3} + \alpha)sin(\beta)]\|$
$\|i_{ti}\|$	$\|K_1[2m \times sin(\frac{pi}{3} + \alpha)sin(\beta)]\|$
$\|i_{tj}\|$	$\|K_1[2m \times sin(\frac{pi}{3} + \alpha)sin(\frac{pi}{3} - \beta)]\|$
$\|i_{tk}\|$	$\|K_1[2m \times sin(\frac{pi}{3} + \alpha)sin(\frac{pi}{3} - \beta)]\|$
$\|i_{tl}\|$	$\|K_1[1 - d_{st} - mcos(\beta - \frac{pi}{6})]\|$

and VSI. For example, it is assumed that S_1, S_2 in the CSR and g_1, g_2, g_6 in the VSI are ON and all remaining switches are OFF as shown in Figure 4.1. Under this condition

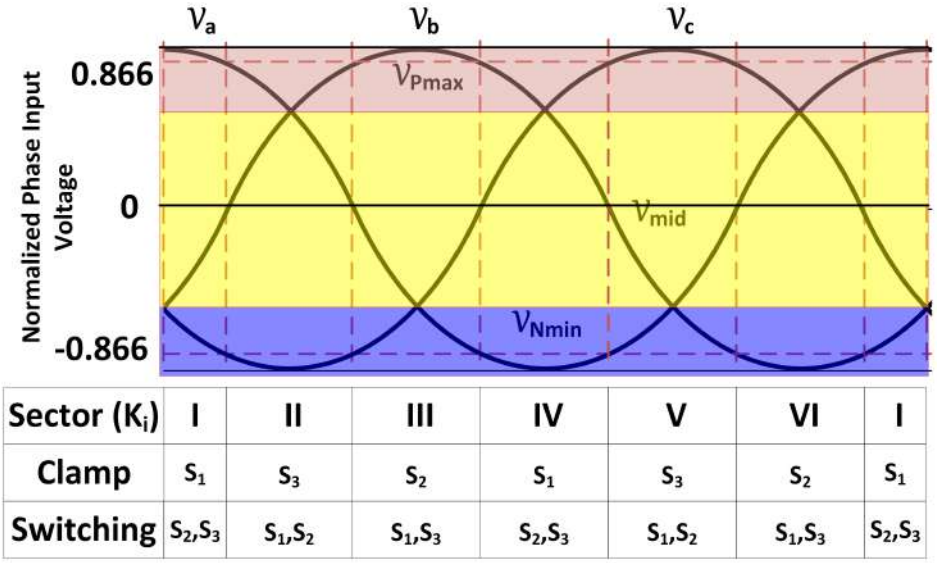

Figure 4.9: Current source rectifier sectors and switching transitions by varying the 3 phase input supply

output voltages can be calculated as

$$v_{An} = v_b + V_{p'q'}, \quad v_{Bn} = v_{Cn} = v_b \tag{4.28}$$

From equations (4.27), (4.28) CMV can be calculated as

$$v_{Nn} = \frac{3v_b + V_{p'q'}}{3} \tag{4.29}$$

Similarly for all sectors the maximum and minimum of the CMV can be calculated as

$$\begin{aligned} v_{Nn_{max}} &= \frac{max(3v_{mid} + V_{p'q'})}{3} (K_i = 2, 4, 6) \\ v_{Nn_{min}} &= \frac{min(3v_{mid} + V_{p'q'})}{3} (K_i = 1, 3, 5) \end{aligned} \tag{4.30}$$

Here v_{mid} is the supply voltage under the yellow shaded area of Figure 4.9. It is positive for $(K_i = 2, 4, 6)$ and negative for $(K_i = 1, 3, 5)$. Similarly, CMV for all combinations of CSR and VSI switching sectors are listed in Table 4.2 [73]. From Table 4.2, the maximum peak CMV is obtained in zero states of CSR or VSI, equal to $V_{p'q'}$. In the proposed switching strategy, the input current vector is synthesized by two active vectors, and four active vectors synthesize the output voltage vector to reduce the peak CMV. The maximum peak CMV of the proposed switching strategy is $\frac{2V_{p'q'}}{3}$. From the analysis of Section 4.3 and Section 4.5, the proposed method has lower inductor current ripple and CMV than the conventional method. Further effectiveness of the proposed method is validated through MATLAB simulation and experimental prototype.

Table 4.2: CMV for CSR and VSI switching states

CSR sector	VSI switching states	CMV	peak of the CMV
1, 3, 5	V_1, V_3, V_5	$\frac{3v_{mid}+V_{p'q'}}{3}$	$\frac{V_{p'q'}}{3}$
	V_2, V_4, V_6	$\frac{3v_{mid}+2V_{p'q'}}{3}$	$\frac{2V_{p'q'}}{3}$
	V_0	v_{mid}	$\frac{-\sqrt{3}\hat{V}_{im}}{2}$
	V_7	$\frac{3v_{mid}+3V_{p'q'}}{3}$	$V_{p'q'}$
	ST	v_{mid}	$\frac{-\sqrt{3}\hat{V}_{im}}{2}$
2, 4, 6	V_1, V_3, V_5	$\frac{3v_{min}+V_{p'q'}}{3}$	$\frac{-\sqrt{3}\hat{V}_{im}}{2} + \frac{V_{p'q'}}{3}$
	V_2, V_4, V_6	$\frac{3V_{min}+V_{p'q'}}{3}$	$\frac{-\sqrt{3}\hat{V}_{im}}{2} + \frac{V_{p'q'}}{3}$
	V_0	v_{min}	$-\hat{V}_{im}$
	V_7	$v_{min} + V_{p'q'}$	$\frac{-\sqrt{3}\hat{V}_{im}}{2} + V_{p'q'}$
	ST	v_{min}	$-\hat{V}_{im}$

Table 4.3: Parameters for the simulation

S. no	*Name of the parameter*	*Value*
1	Input supply voltage (peak)	120 V
2	Input supply frequency	50 Hz
3	d_{st}	0.25
4	QZSI Inductors, capacitors	1.5 mH, 120 uF
5	Output frequency	100 Hz
6	Power Rating	1 KW
7	Output filter	0.564 mH
9	Input filter (L_{in}, C_{in})	2 mH, 36 uF
10	Switching frequency	5 kHz

4.6 Simulation results

The proposed modulation scheme is analyzed using MATLAB SIMULINK software with 120 V peak voltage ($\hat{V}_{im}$), 50 Hz supply for 1 KW power converter. The ratings of the remaining components are listed in Table 4.3. From Figure 4.10, rectified voltage V_{pq} is pulsed in nature with a maximum of 208 V and a minimum of 104 V. The measured average value of V_{pq} is 178 V. This rectified voltage is the source for the QZS network. During the shoot-through state, both terminals p' and q' are short-circuited, so the voltage across these terminals is zero, and the inductor magnetizes during this period. For the Non-shoot-through state, active vectors are applied in VSI, which builds up the voltage across the p', q'terminals and inductor demagnetizes as shown in Figure 4.11. By selecting the shoot-through period as 0.25, the QZS network boosted V_{pq} value to 2 times. For the modulation index 0.7, the overall boosting factor is 1.212. By choosing the above parameters, the 3-phase load side maximum output voltage is 250 V. Fig.4.10 compares the conventional and proposed switching strategies. For the time $t \leq 0.05$, waveforms are for the conventional method, and for time $t > 0.05$ sec, the proposed modulation was implemented. The top waveform shows the CSR averaged output voltage of both methods, which is the same. The second waveform is the 3-phase load line voltage, which is the same for both modulations. The third waveform of Figure 4.10 shows the QZS output voltage $V_{p'q'}$, which is also measured the same in both cases. The last waveform indicates the current through inductor i_{L_A}, which has more ripple in the conventional compared to the proposed method. The previous method placed the total shoot-through time at one place and had a peak-to-

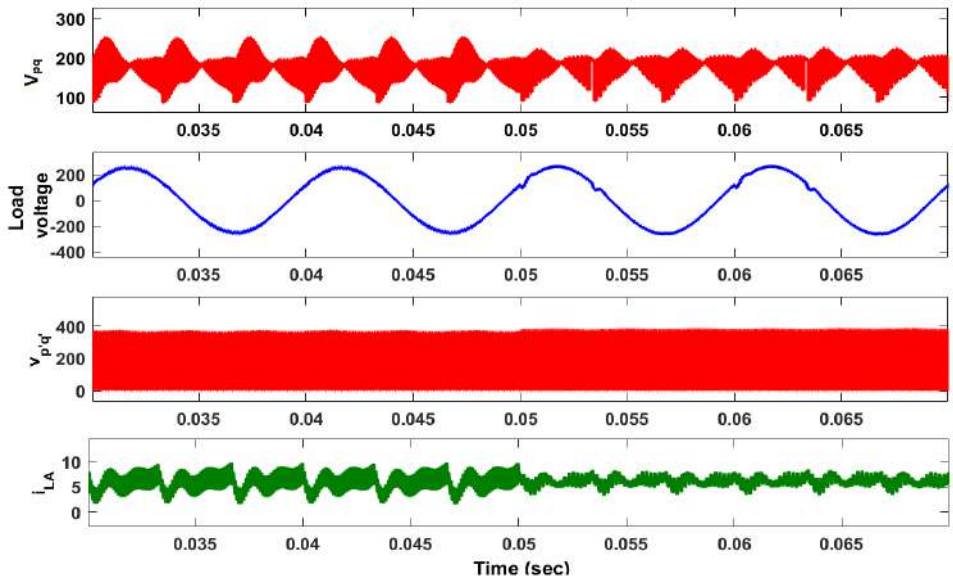

Figure 4.10: Simulation waveforms for the DC link voltage V_{pq}, load voltage, QZS output($V_{p'q'}$), and current through inductor for the both conventional method (time ≤ 0.05) and proposed method (time > 0.05)

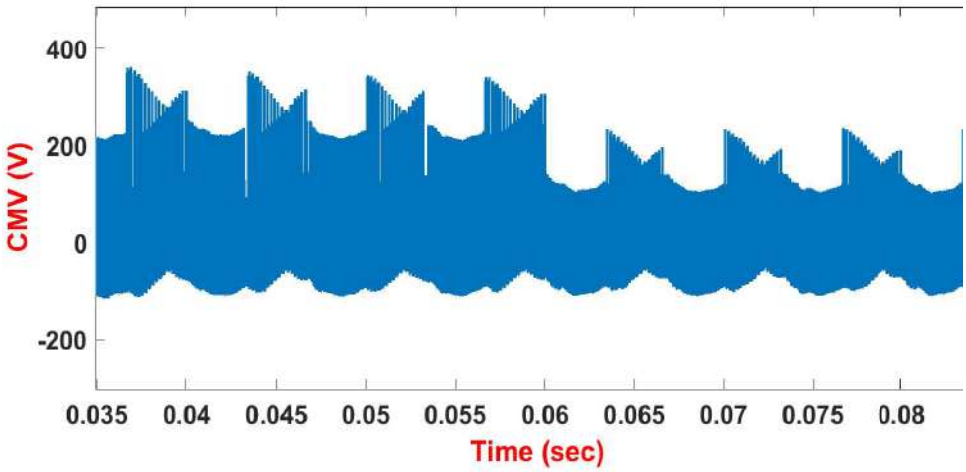

Figure 4.11: Simulation waveforms for common mode voltage of the QZSUSMC for $t \leq 0.06$ conventional method CMV and for $t > 0.06$ proposed method CMV

peak ripple current of the QZ-source inductor equal to 6.357 A, while the proposed method reduces the peak-to-peak ripple current to 4.834 A by placing unequal shoot-through periods at different positions. So, the proposed method reduces nearly 24% ripple in the inductor current. Figure 4.11 compares the CMV of the conventional and proposed methods. For time $t \leq 0.06$ sec, the conventional modulation technique is applied to the converter, and the peak value of the CMV is $356V$, which is nearly equal to the theoretical value (360 V). The proposed modulation scheme is applied after 0.06

sec, giving a peak CMV value of 238 V. Therefore, CMV is reduced by nearly 33% as that of the conventional method.

4.7 Experimental results

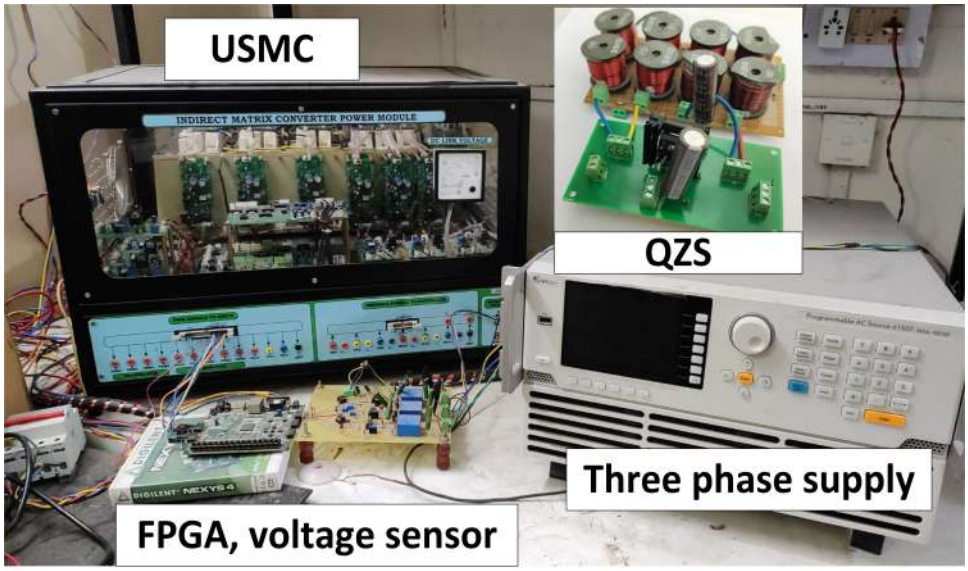

Figure 4.12: Experimental setup for the proposed method

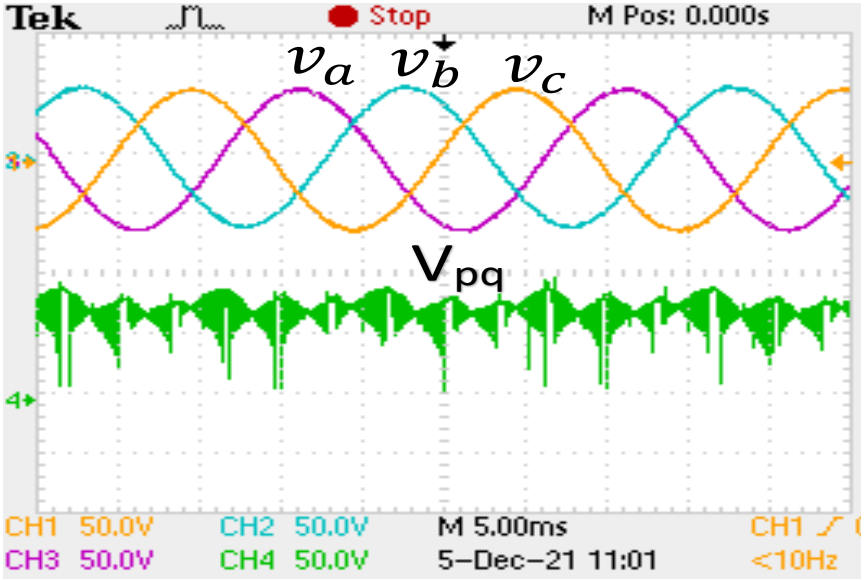

Figure 4.13: 3 phase input supply and current source rectifier output voltage

The experimental setup of the proposed modulation scheme is shown in Figure 4.12. Atrix7100CGS324-1 FPGA board generates control signals with a 5 kHz switching

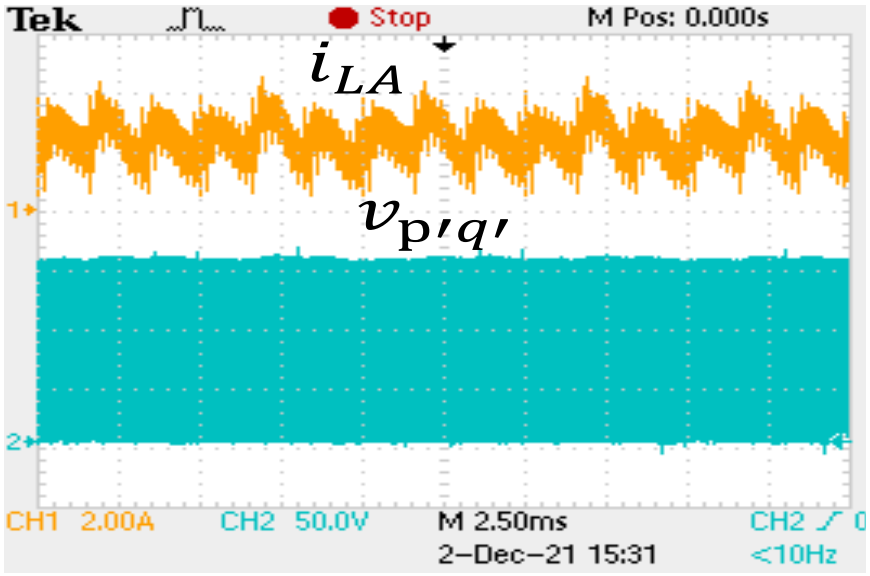

Figure 4.14: Inductor current and QZS output voltage for conventional approach

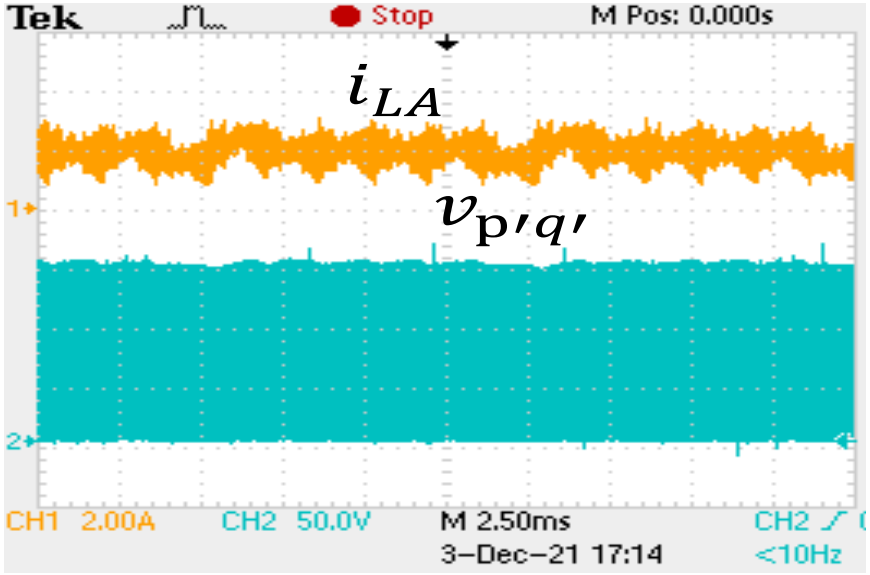

Figure 4.15: Inductor current and QZS output voltage for proposed approach

frequency. The experiment has been conducted with 50 V, 50 Hz supply for 175 W load. Shoot-through time and modulation index of QZSUSMC are taken as simulation parameters. Figure 4.13 shows the 3-phase Input supply and corresponding CSR Output voltage V_{pq}, measured as 72.5 V, nearly equal to the theoretical value. This V_{pq} voltage is a source for the QZS. During ST mode, the inductor current gets charged by shorting any one phase of the inverter, so $V_{p'q'}$ is zero in this mode. In NST mode, the inductor current decreases. The inductor current and boosted voltage $V_{p'q'}$ for the conventional method is shown in Figure 4.14. From this waveform, the peak inductor

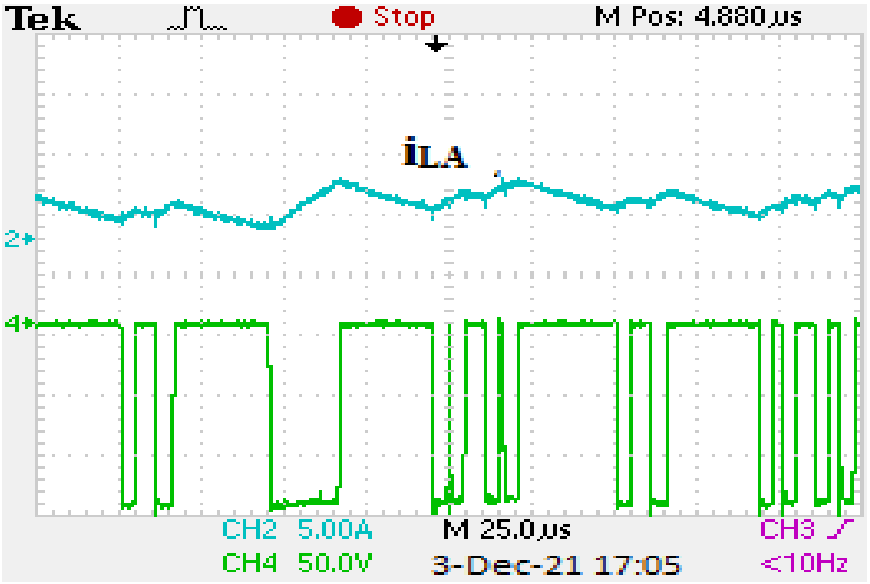

Figure 4.16: Current through inductor and voltage across diode (proposed approach)

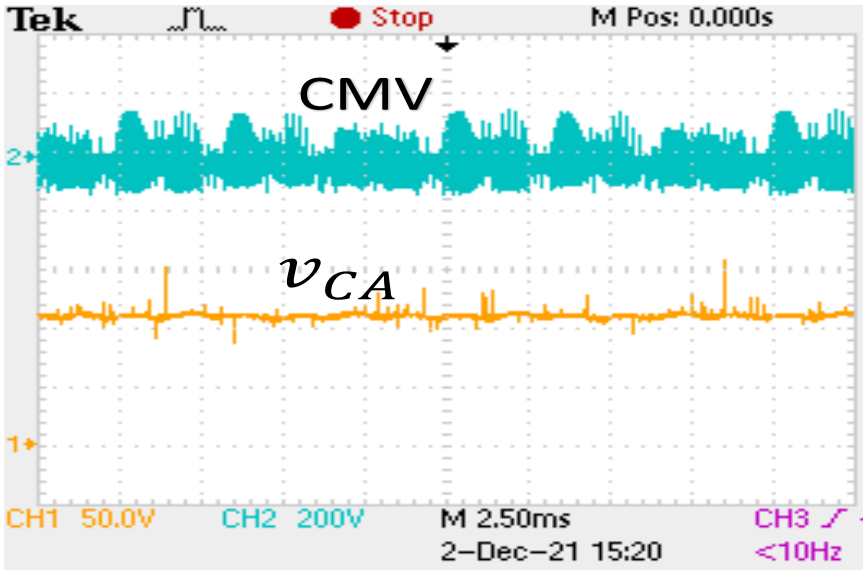

Figure 4.17: CMV and voltage across capacitor for conventional approach

ripple current is 4 A, and QZS output voltage $V_{p'q'}$ is measured as 138 V. Figure 4.15 gives information about the proposed modulation scheme. The peak inductor ripple current is measured as 2.8 A, and the QZS output voltage is the same as the previous method. Charging and discharging of inductor current and corresponding voltage across the diode, $V_{p'q'}$ are shown in Figure 4.16 and Figure 4.15, respectively. Figures 4.17 and 4.18 show the CMV and capacitor voltages of both conventional and proposed methods. The proposed method has a peak-peak CMV of 110 V, whereas the conventional method has 172 V peak-peak CMV. The capacitor voltage of both

methods has the same magnitude of 108 V. Phase voltage of the load is shown in Figure 4.19 and Figure 4.20. Both schemes produce the same voltage level (42 V). Still, the proposed method has a slightly distorted output voltage due to the absence of zero vectors, which is smoothened by increasing Filter inductance.

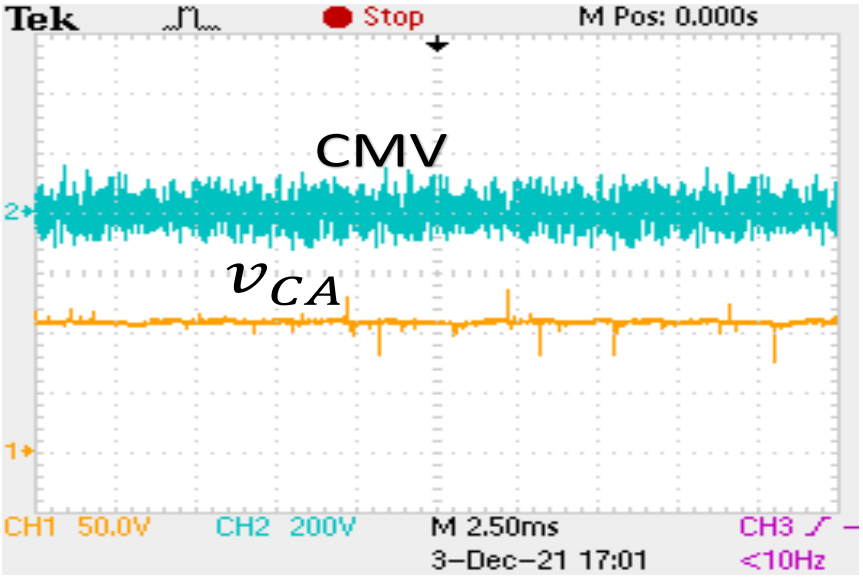

Figure 4.18: CMV and voltage across capacitor for the proposed approach

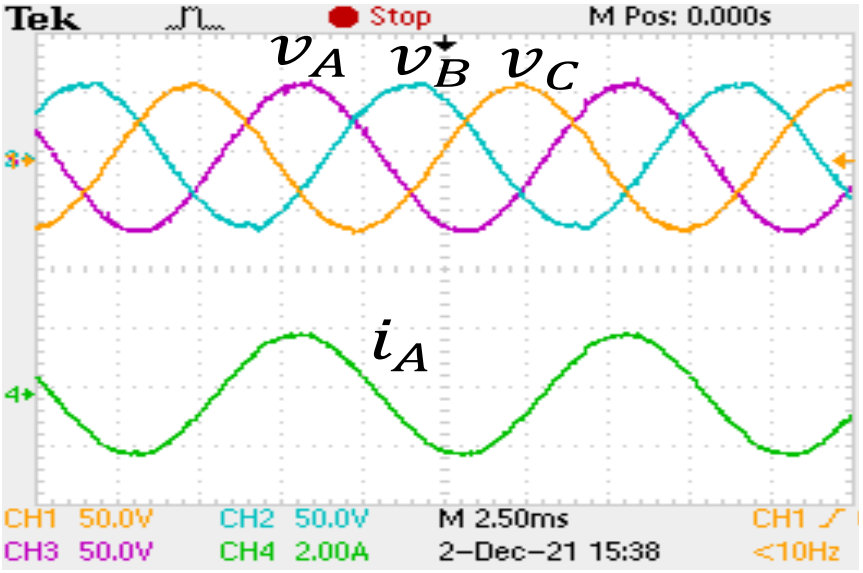

Figure 4.19: Output voltages and current for the conventional approach

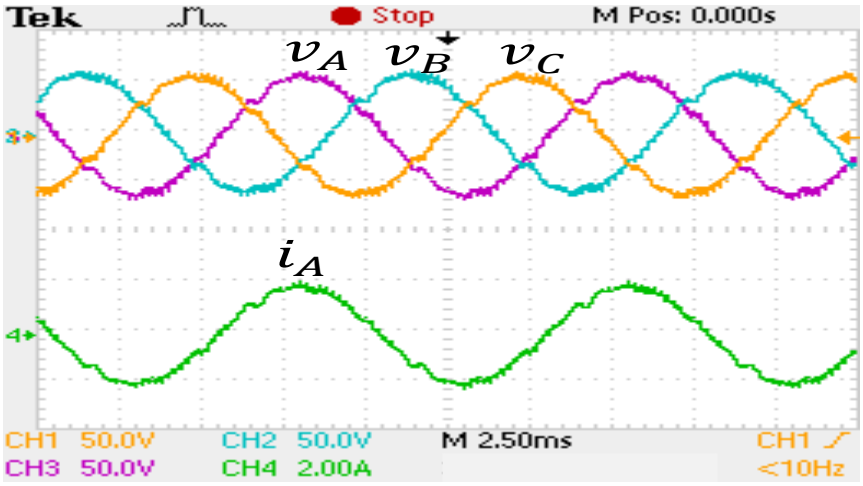

Figure 4.20: Output voltages and current for the proposed approach

4.8 Analysis of the proposed method

To understand the impact of the proposed modulation scheme various performance parameters are observed.

4.8.1 Effect on CMV and inductor current ripple

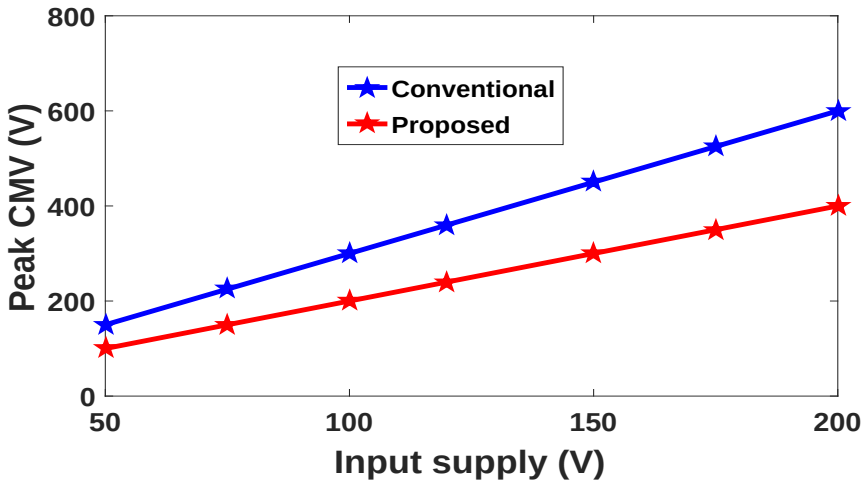

Figure 4.21: Analytical waveform for peak CMV by varying input supply and keeping $m = 0.7$

Figure 4.21 and 4.22 show the analytical and simulation behaviour of the peak CMV by varying input supply at a given duty shoot-through duty ratio (0.25) and modulation index (0.7). From Table 4.2, peak CMV depends on the voltage $V_{p'q'}$, and this voltage is increased by increasing the input supply. Hence, peak CMV is increased by increasing the input supply. Similarly, inductor current ripple also varies

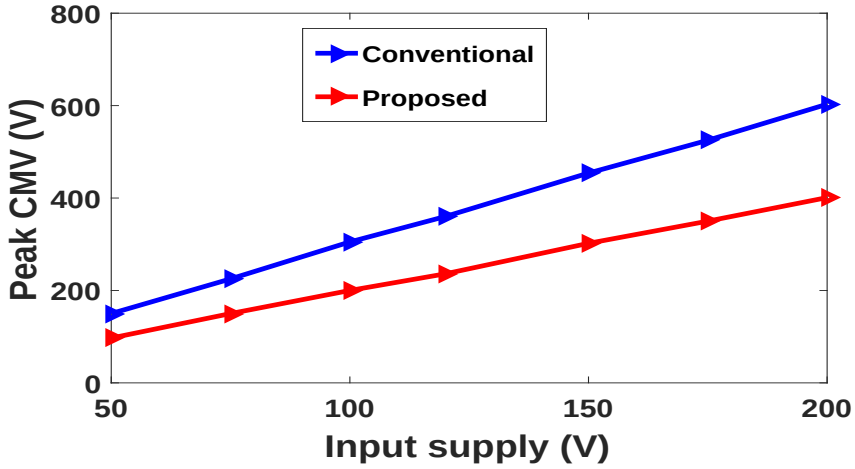

Figure 4.22: Simulation waveform for peak CMV by varying input supply and keeping $m = 0.7$

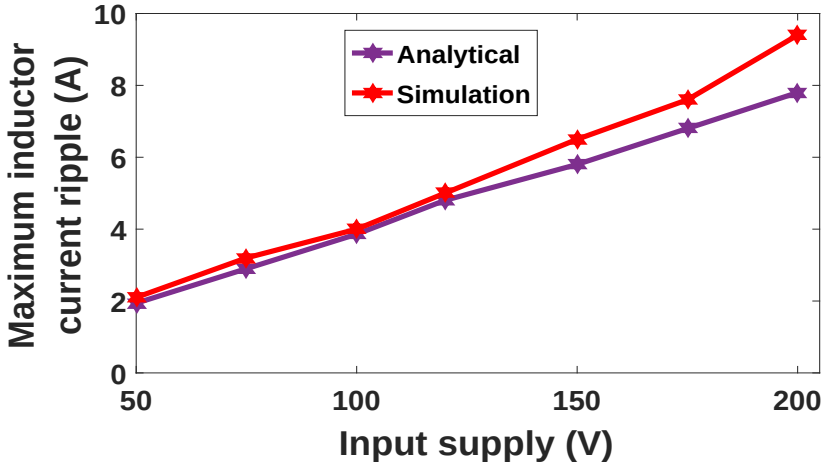

Figure 4.23: Maximum inductor current ripple for analytical and simulation by varying the input supply

by changing the input supply, which is shown in Figure 4.23. Further, the maximum inductor current ripple is observed by varying three-phase load shown in Figure 4.24. By increasing load power, the maximum inductor current ripple is increased. Load power is varied from 275 W to 4.5 kW, and it was observed that the inductor current rose from 3.42 A to 14 A in the conventional method and from 2.1 A to 9.4 A in the proposed method. The effect of output frequency on CMV and inductor current ripple is shown in Figure 4.25 and Figure 4.26, respectively. The converter output frequency does not affect the peak CMV but influences the inductor current ripple. In the proposed method, the inductor current ripple attains the maximum value (6 A) at 150 Hz, whereas in the conventional method, the maximum value (9.6 A) is at 200 Hz. Figure 4.27 shows the variation of overall gain by changing both shoot-through ratio.

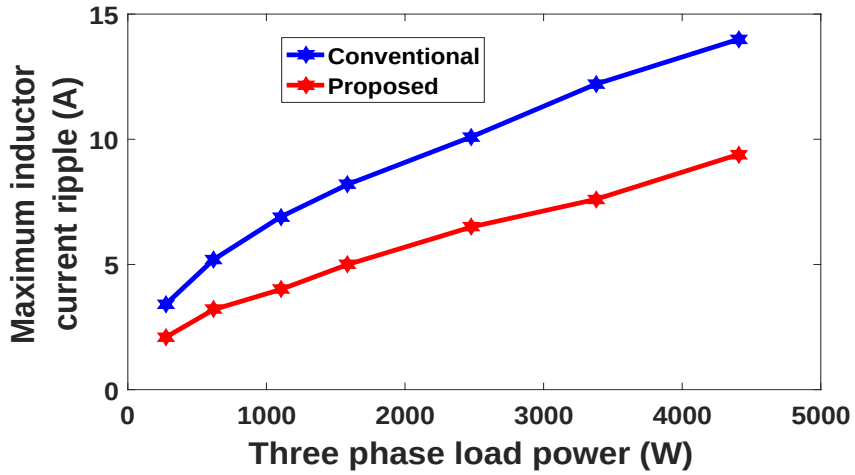

Figure 4.24: Simulation waveform for Maximum inductor current ripple by varying the three phase load

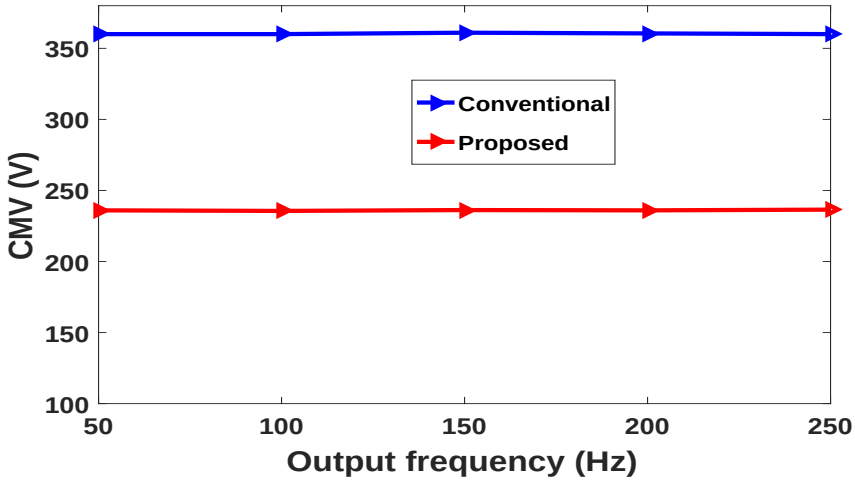

Figure 4.25: Effect on peak CMV by varying output frequency for both conventional and proposed methods

4.8.2 Practical gain

Figure 4.28 shows the circuit connection during ST mode with parasitic resistance of inductors (R_L) and capacitors (R_C). After applying KVL and KCL, the following equations are obtained.

$$\begin{aligned} V_{LA} &= V_{pq} + V_{CY} - (R_L + R_C)i_{LA} \\ V_{LB} &= V_{CX} - (R_L + R_C)i_{LB} \\ i_{CX} &= -i_{LB} \\ i_{CY} &= -i_{LA} \end{aligned} \tag{4.31}$$

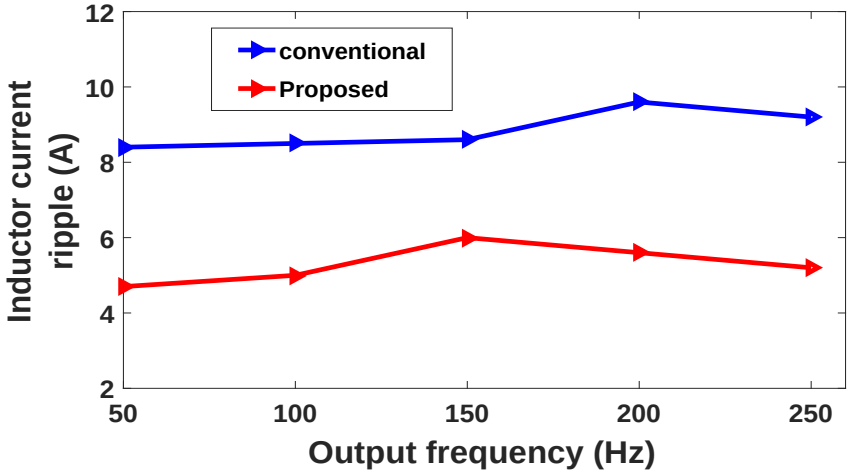

Figure 4.26: Effect on maximum inductor current ripple by varying output frequency

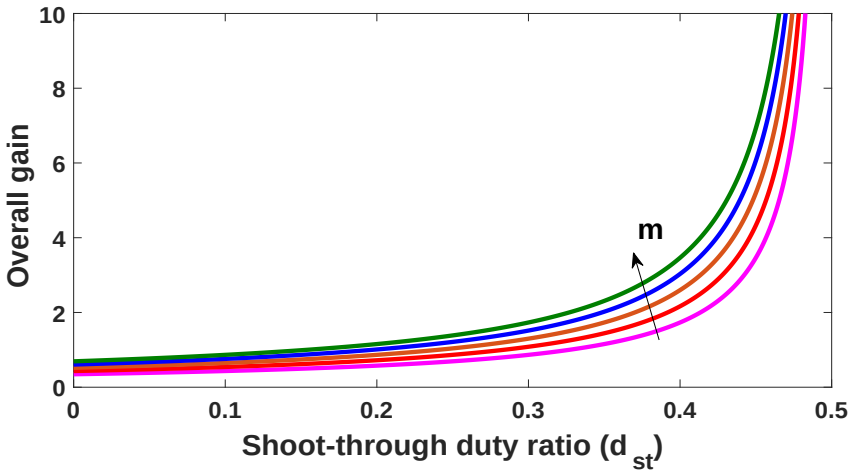

Figure 4.27: Variation of overall gain by varying shoot-through duty ratio d_{st} and modulation index m

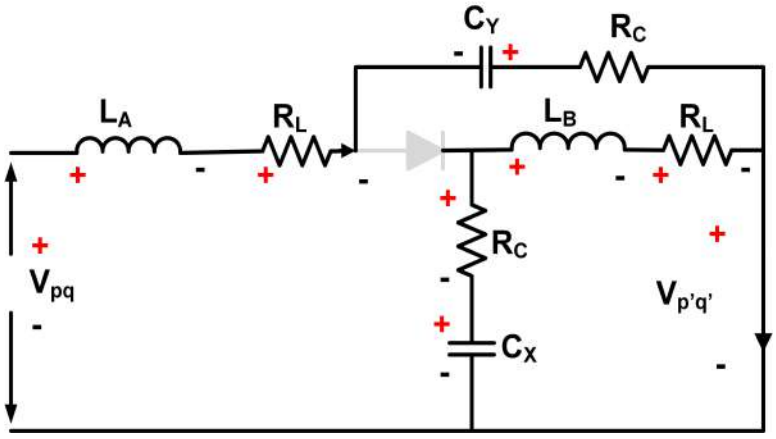

Figure 4.28: Equivalent circuit of QZS in ST mode

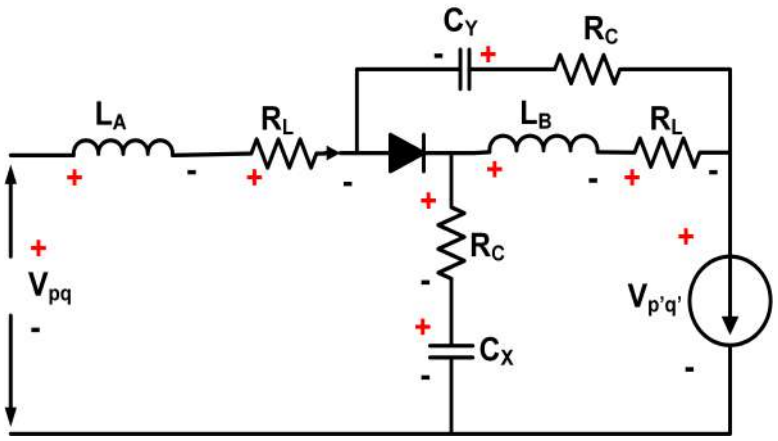

Figure 4.29: Equivalent circuit of QZS in NST mode

Applying KVL and KC to the circuit shown in 4.29, the following NST mode equations are obtained.

$$\begin{aligned} V_{LA} &= V_{pq} - V_{CX} - (R_L)i_{LA} - (R_C)i_{LC} + \\ V_{LB} &= V_{CX} - (R_L)i_{LB} + (R_C)i_C \\ i_{CX} &= i_{LA} - i_o \\ i_{CY} &= i_{LB} - i_o \end{aligned} \tag{4.32}$$

After applying state space averaging model, steady state voltage gain is given in the equation (4.33).

$$V_{p'q'} = \frac{1}{1-2d_{st}} V_{pq} - \frac{2(1-d_{st})(R_L + 2d_{st}R_C)}{(1-2d_{st})^2} i_o \tag{4.33}$$

Figure. 4.30 shows the theoretical and practical gains variation by changing the shoot-

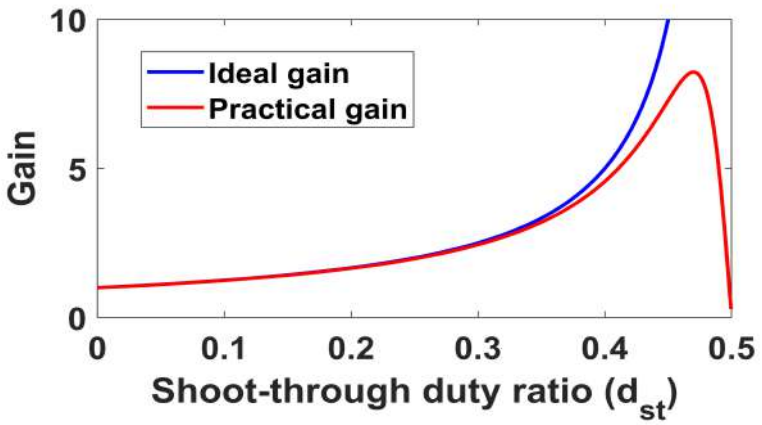

Figure 4.30: Theoretical and practical gains

through duty ratio.

4.8.3 Effect on output current THD

Output current THD of the proposed converter is analyzed and compared with the conventional method, as shown in Figure 4.31. The modulation index is $m = 0.7$, and the shoot-through duty ratio d_{st} varies from 0.2 to 0.3. At $d_{st} = 0.25$, the conventional method has THD 3.37%, while the proposed method has 3.93%. From Figure 4.31, the operating point for the proposed converter is chosen at $m = 0.7$ and $d_{st} = 0.25$. For this operating point, the simulation result of the output and input current THD is shown in Figure 4.32. For 5 KHz switching frequency, 3.93% THD in output current is achieved. The unfiltered input current THD is measured as 74.4%.

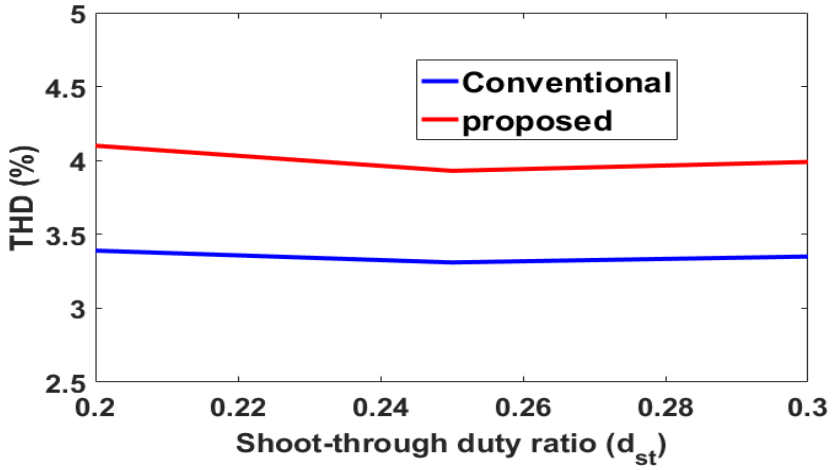

Figure 4.31: Output current THD waveform by varying shoot-through duty ratio and modulation index for conventional and proposed methods

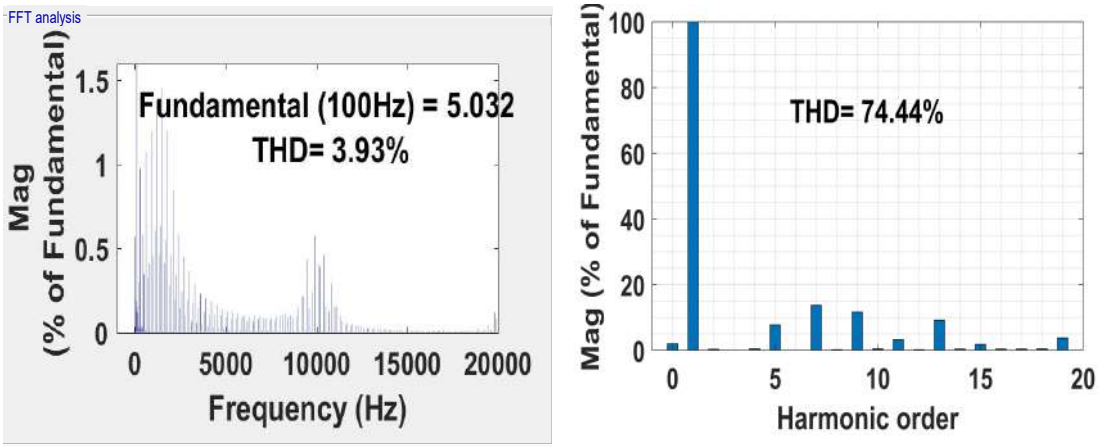

Figure 4.32: Input and output current harmonic analysis for the proposed method

4.8.4 Efficiency of the proposed method

In simulation, the efficiency of the proposed method and conventional methods are evaluated for load variation from 100 W to 1.5 kW. The remaining parameters are the same throughout the load variation as in Table 4.3. Figure 4.33 shows the variation of efficiency curves for both methods. Interestingly, both methods have similar efficiency values for lower power till 550 W. After that, the proposed method delivers slightly more efficiency than the conventional method, as shown in Figure 4.33. The increase in efficiency is due to the production of a higher output voltage (102 V) by the proposed method against the conventional method, which produces an output voltage of 101 V. The reason behind the increase of output voltage is because of the utilization of only active vectors (V_1, V_2, V_3, and V_6) compared to the utilization of active vectors and zero vectors (V_1, V_2, and V_0, V_7) by the conventional method. At 750 W load power, the proposed method shows a maximum efficiency of 92.17%, whereas the conventional method gives 91.74%.

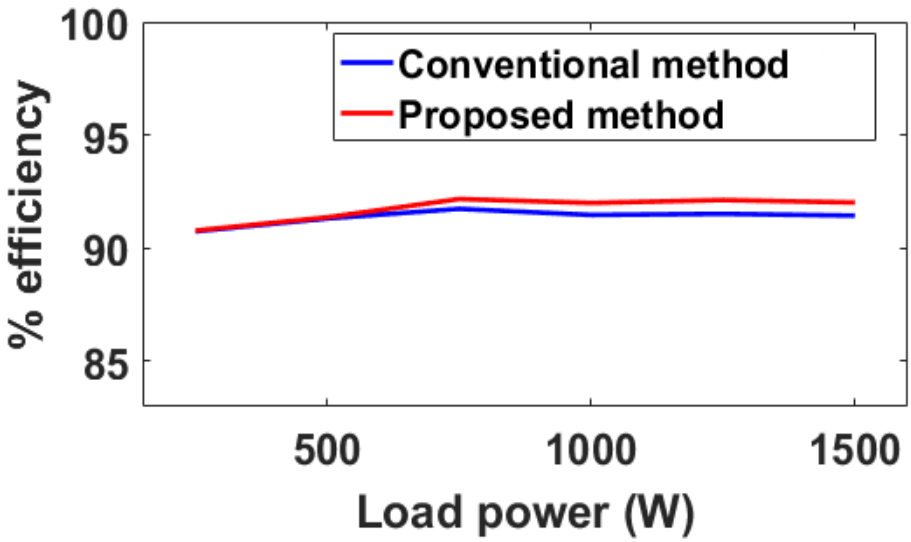

Figure 4.33: Efficiency of the proposed converter

Table 4.4 gives a comparative analysis between the conventional and the proposed methods. The comparison is based on peak CMV, maximum inductor current ripple, and output current THD. From this Table 4.4, the proposed switching strategy reduces the peak CMV and ripple in the inductor current.

Table 4.4: Comparison between conventional method and proposed method

d_{st} = 0.25, m = 0.7, Load power = 1 kW, output frequency = 100 Hz								
switching strategy	CMV	Max. inductor current ripple	Output current THD	V_{CX}	V_{CY}	CSR switch stress	CSR diode stress	VSI switch stress
Conventional [98]	356 V	6 A	3.37%	267 V	89 V	118 V	|205| V	357 V
Proposed	238 V	4.834 A	3.93%	267 V	89 V	118 V	|205| V	357 V

4.9 Summary

The proposed modulation technique gives a better inductor current ripple and peak CMV for the quasi Z-source Ultra Sparse matrix converter by dividing the total shoot-through period into six unequal durations and arranging them in a particular order. For the same operating parameters, the proposed method reduces a significant amount of ripple (nearly 24%) in the Quasi Z-source inductor current compared to the conventional method. Additionally, the peak CMV is reduced by 33% as compared to the conventional method. Though the proposed method slightly distorts output voltage, its advantages support its effectiveness.

Even though the QZS-USMC improves the voltage gain more unity, it still requires four passive elements and a diode in its impedance network. For high power applications, the size of these passive elements is significant and increases the total size of the system. So, the motivation for the next chapter is to minimize the passive components in the impedance network and achieve the same boosting factor as QZS-USMC.