# Chapter 2

# Quasi-Impedance Source High gain Converter

## 2.1 Introduction

The conventional DC-DC boost converter provides a high voltage conversion ratio at an extreme duty cycle. At such extreme duty cycles, power devices suffer from high voltage stress and high inductor current ripple leads to inductance saturation [46]. In the last decades, many efforts have been made to increase the voltage gain without operating at an extreme duty cycle. The technique includes switched inductor (SL) cell , switched capacitor (SC) cell, voltage multiplier cell (VMC), etc.

This chapter investigates an impedance (Z) source-based topology to achieve a high conversion ratio with a low-duty cycle. While conventional converters operating at high duty ratio leads more conduction losses in the used semiconductor devices and degrade their efficiency. Peng et al. proposed the concept of an impedance network to circumvent high-duty operation. The pulse width modulation (PWM) Z-source converter is reported in [47]. However, the input current of the converter is discontinuous in nature and has a limited voltage conversion ratio. Higher voltage conversion ratio, continuous input current, and low device stress are the prime requirements of DC-DC converters. Here, based on the available literature, a new Z-source converter is investigated. The new Z-source converter in [48] is reported and shown in Figure 2.1. This converter achieves high gain at the cost of discontinuous input current.

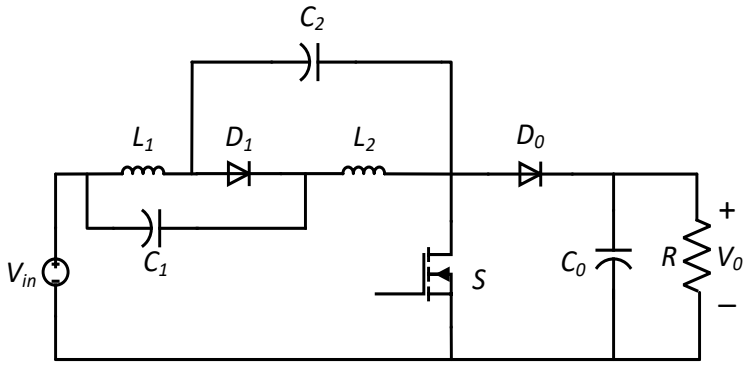


**Figure 2.1:** Quasi Z-source converter with discontinuous input current [48].

## 2.2 Proposed converter and its operation

From the reference [48] single switch based new Z-source converter is investigated with high voltage conversion ratio. Here the construction method of proposed converter is discussed. In version-1, Z-source based converter is formed by incorporating of C-D cell $(D_3, C_2)$ or SC cell near inductor $L_2$. Replacing the Diode $D_2$ by capacitor $C_2$ and adding $(C_5 - D_5)$ cell across Switch $S$ in Figure 2.2 to form version-2 new impedance source converter.

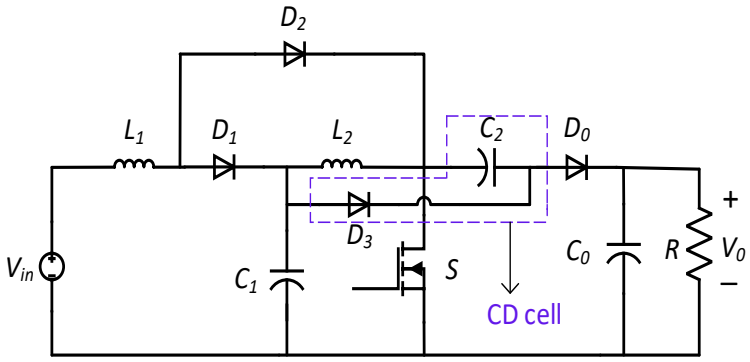


**Figure 2.2:** Proposed version-1 Z-source DC-DC converter.

The proposed version-2 converter maximum duty is limited to 50% as shown in Figure 2.3. It consists of two inductors, three diodes and three capacitors. Continuous current mode (CCM) operation is taken for analysis, which is widey used in industrial applications. Here, version-2 namely (Proposed converter-1) is discussed with mathematical proof and experimental results.

The steady state analysis of proposed converter is carried into CCM using some assumptions like parasitic effects of all used component and voltage drop of diodes are

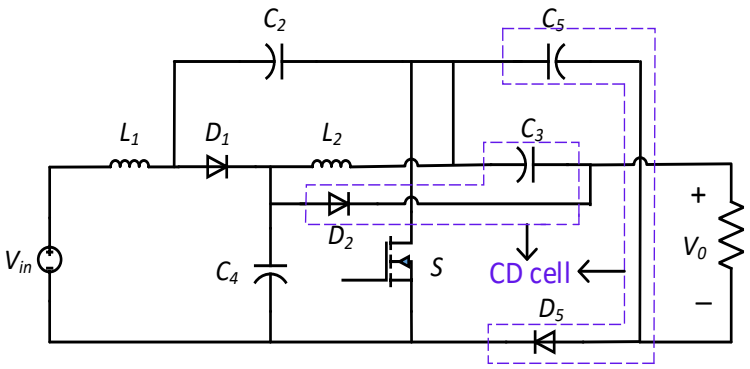


**Figure 2.3:** Proposed (version-2) Z-source high gain converter-1.

ignored. Two modes of operation exist for the converter. The steady state waveforms are shown in Figure 2.4. The signal $V_G$ represents the gate pulse of Switch $S$, $i_{L1}$ and $i_{L2}$ represent the inductor current profiles, which are different in magnitude, $V_S$ is the voltage stress across switch equals to $\frac{V_0}{2-D}$ and finally $V_0$ is the converter output voltage. The working principle for two modes for the proposed converter is described here.

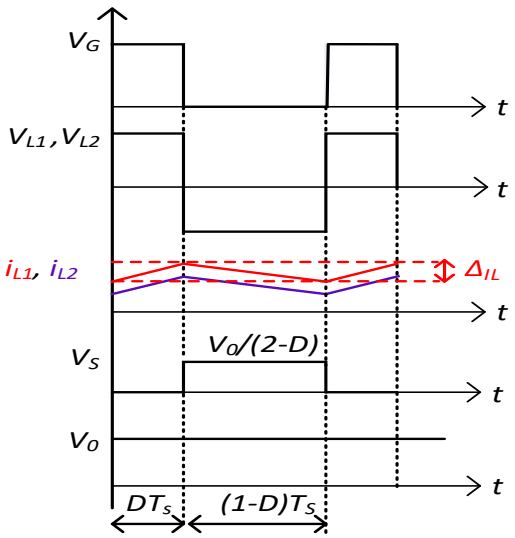


**Figure 2.4:** Steady state waveforms of proposed converter-1 during CCM.

### 2.2.1 Mode 1, $(0 < t < DT_s)$

The equivalent circuit for this period is shown in Figure 2.5. In this Mode Switch $S$ is ON. Inductor $L_1$ magnetize by input supply $V_{in}$ and $v_{C2}$. Similarly $L_2$ magnetizes by capacitor $C_4$. Capacitor $C_4$ discharges its energy to charge $C_3$ via Diode $D_2$. During this time period, the voltage and current equations are as follows:

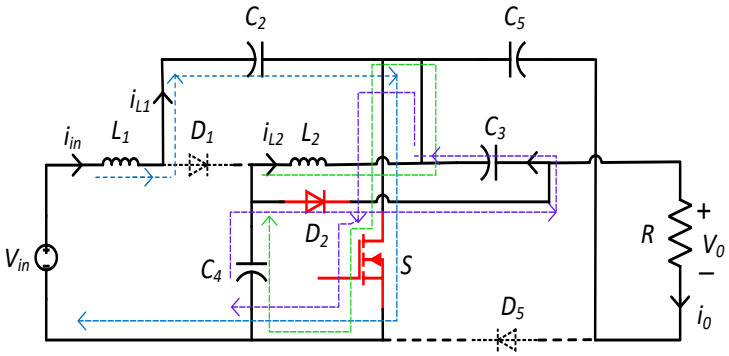


**Figure 2.5:** Operating Mode 1.

$$v_{L1} = V_{in} + v_{C2}, \quad v_{L2} = v_{c4} \tag{2.1}$$

$$v_{C4} = v_{C3}, \quad v_0 = v_{C3} + v_{C5} \tag{2.2}$$

$$i_{C2} = -i_{L1}, \quad i_{C5} = -i_0 \tag{2.3}$$

### 2.2.2 Mode 2, $(DT_s < t < T_s)$

The equivalent circuit for OFF period of Switch $S$ is shown in Figure 2.6. Inductor $L_1$ demagnetizes its energy to charge $C_4$ via Diode $D_1$. Similarly, inductor $L_2$ releases its energy to charge $C_2$. During this period, the voltage equations are as follows:

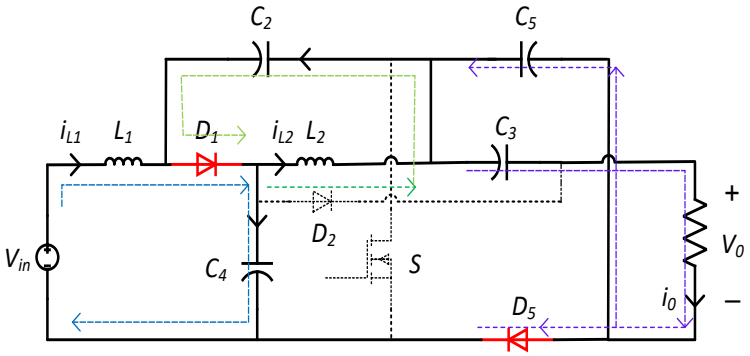


**Figure 2.6:** Operating Mode 2.

$$v_{L1} = V_{in} - v_{C4}, \quad v_{L2} = -v_{C2} \tag{2.4}$$

$$v_{L2} = v_{C4} - v_{C5}, \quad v_0 = v_{C3} + v_{C5} \tag{2.5}$$

$$i_{C3} = -i_0, \quad i_{C5} + i_{C2} = i_{L2} - i_0 \tag{2.6}$$

### 2.2.3 Voltage gain derivation

Voltage gain expression in CCM can be deduced by applying volt-second law across both inductor $L_1$ and $L_2$,

$$\int_{0}^{DT_s} V_{L1}dt + \int_{DT_s}^{T_s} V_{L1}dt = 0 \tag{2.7}$$

$$(V_{in} + v_{C2})D + (V_{in} - v_{C4})(1 - D) = 0 \tag{2.8}$$

After simplification, the voltage across $C_4$ can be written as;

$$V_{C4} = \frac{V_{in} + V_{C2}D}{(1 - D)} \tag{2.9}$$

Similar to inductor $L_1$ average voltage across inductor $L_2$ is zero, hence

$$\int_{0}^{DT_s} V_{L2}dt + \int_{DT_s}^{T_s} V_{L2}dt = 0 \tag{2.10}$$

Substituting eq. (2.1) and eq. (2.4), eq. (2.10) gives,

$$V_{C4} = \frac{V_{C2}(1 - D)}{D} \tag{2.11}$$

Equating eq. (2.9) and eq. (2.11) gives following result,

$$V_{C2} = \frac{D}{(1 - 2D)}V_{in} \tag{2.12}$$

Voltage across $C_4$ and $C_3$ can be obtained substituting eq. (2.12) in eq. (2.9)

$$V_{C3} = V_{C4} = \frac{1 - D}{(1 - 2D)}V_{in} \tag{2.13}$$

Again applying the volt-second law across $L_2$

$$V_{C3}D + (V_{C4} - V_{C5})(1 - D) = 0 \tag{2.14}$$

$$V_{C5} = \frac{V_{in}}{1 - 2D} \tag{2.15}$$

The voltage gain of proposed converter is given as

$$G_{ccm} = \frac{V_0}{V_{in}} = \frac{2 - D}{1 - 2D} = \frac{I_{in}}{I_0} \tag{2.16}$$

## 2.3 Parmeter design consideration

The design of the storage elements, inductors ($L$) and capacitors ($C$), for the proposed converter, depends on the current ripple in the inductor and the voltage ripple in the capacitor. Assuming lossless components, the input power equals the output power. Therefore, the input current is equals to the average inductor current ($I_{L1}$) and can be expressed as:

$$I_{in} = I_{L1} = \frac{V_0 I_0}{V_{in}} \tag{2.17}$$

Using expression of voltage gain from eq. (2.16) and substituting in eq. (2.17), the average current expression for inductor $L_1$ is,

$$I_{L1} = \frac{2-D}{1-2D} I_0 \tag{2.18}$$

In order to get average inductor current through $L_2$, applying Kirchhoff's current Law (KCL) during both mode of operation. Applying charge balance law across $C_2$,

$$I_{C2} = 0, \implies -i_{L1} D + i_{c2_{oFF}}(1-D) = 0 \tag{2.19}$$

$$i_{c2,off} = \frac{D I_{I_{L1}}}{1-D} \tag{2.20}$$

Again applying charge balance law across $C_5$,

$$I_{C5} = 0, \implies -i_0 D + (i_{L2} - i_0 - i_{c2})(1-D) = 0 \tag{2.21}$$

Using eq. (2.20) and substituting in eq. (2.21) gives average current through inductor $L_2$,

$$I_{L2} = \frac{1+D}{2-D} I_{L1}, \implies I_{L2} = \left(\frac{1+D}{1-2D}\right) I_0 \tag{2.22}$$

### 2.3.1 Inductor design

Both the inductors can be derived using eq. (2.1) and maximum ripple current presummed to be $\Delta I_L$ is 15% for inductor $L_1$ and 10% for inductor $L_2$.

$$L_1 = \left(\frac{V_{in} + v_{C2}}{\Delta I_{L1}}\right) D T_s \tag{2.23}$$

$$L_2 = \left(\frac{v_{C4}}{\Delta I_{L2}}\right) D T_s \tag{2.24}$$

### 2.3.2 Capacitor design

The voltage ripple $\Delta V_C$ and current flowing through capacitor affect the capacitance value and $\Delta V_C$ is presummed to be is 1% to 2%.

$$C_2 \frac{\Delta V_{C2}}{DT_s} = I_{L1} \implies C_2 = \frac{(2-D)I_0 DT_s}{(1-2D)\Delta V_{C2}} \tag{2.25}$$

$$C_3 \frac{\Delta V_{C3}}{(1-D)T_s} = I_0 \implies C_3 = \frac{I_0(1-D)T_s}{\Delta V_{C3}} \tag{2.26}$$

$$C_4 \frac{\Delta V_{C4}}{(1-D)T_s} = I_{L1} - I_{L2} + I_{C2} \implies C_4 = \frac{(1+D^2-D)I_0 T_s}{\Delta(1-2D)V_{C4}} \tag{2.27}$$

$$C_5 \frac{\Delta V_{C5}}{DT_s} = I_0 \implies C_5 = \frac{DI_0 T_s}{\Delta V_{C5}} \tag{2.28}$$

## 2.4 Voltage stress across components

The semiconductor devices used in both modes have voltage across them. The voltage stress across all devices is lower than the output voltage. Here, Table 2.1 gives the voltage stress in terms of output voltage. During Mode-1, voltage stress appears across Diode $D_1$ and $D_5$. From Figure 2.5, the following equations can be written,

$$v_{D1} = V_{in} - v_{L1} - v_{c4} \tag{2.29}$$

$$v_{D5} = -v_{c5} \tag{2.30}$$

In the similar manner Diode $D_2$ and Switch $S$ have voltage stress. Applying voltage equation in Figure 2.6,

$$v_{D2} = -v_{c2} - v_{c3} \tag{2.31}$$

$$v_s = V_{in} + v_{c2} - v_{L1} \tag{2.32}$$

After simplifying from eq. (2.29) to eq. (2.32) the voltage stress across used semiconductor devices listed in Table 2.1.

## 2.5 Comparative analysis

The proposed converter is compared with other Z-source/quasi Z-source based high step up converters. The duty cycle of all compared convertes is less or equals to 0.5.

**Table 2.1:** Voltage stress across devices

| **Devices** | **Mode 1** | **Mode2** |
|---|---|---|
| $D_1$ | $\frac{V_0}{2-D}$ | 0 |
| $D_2$ | 0 | $\frac{V_0}{2-D}$ |
| $D_5$ | $\frac{V_0}{2-D}$ | 0 |
| $S$ | 0 | $\frac{V_0}{2-D}$ |

Table 2.2 summarizes the number of passive and active components, voltage gain and normalized switch stress. All selected converter have only one power switch. Converters shown in [47], [49] and [49] have maximum duty cycle is 50%, but the voltage gain is lower than the proposed converter. As seen from Figure 2.13, converter [36] achieves higher gain than all the compared converters at the low range of duty cycle with maximum duty close to $30\% - 32\%$. Converter [50] uses more device count to achieve similar voltage gain. The Figure of all compared converters is shown from Figure 2.7 to Figure 2.11.

**Table 2.2:** Comparative analysis of Z-source converters

| **Parameters** | **[47]** | **[51]** | **[49]** | **[36]** | **[50]** | **Proposed** |
|---|---|---|---|---|---|---|
| Gain | $\frac{1-D}{1-2D}$ | $\frac{1}{1-2D}$ | $\frac{2-2D}{1-2D}$ | $\frac{2-2D}{1-3D}$ | $\frac{2-D}{1-2D}$ | $\frac{2-D}{1-2D}$ |
| Inductor | 3 | 2 | 2 | 4 | 3 | 2 |
| Capacitor | 3 | 3 | 4 | 4 | 5 | 4 |
| Diodes | 1 | 2 | 3 | 3 | 3 | 3 |
| Switches | 1 | 1 | 1 | 1 | 1 | 1 |
| Normalized switch stress | $1 + D$ | 1 | $\frac{1}{2-2D}$ | 1 | $\frac{1}{2-D}$ | $\frac{1}{2-D}$ |
| Common ground | no | yes | yes | yes | no | no |
| Operating efficiency | NA | 94% | 91% | 80% | 91.25% | 90.5% |
| Input current | Discont | Discont | Cont | Cont | Cont | Cont |
| Power | NA | 50 W | 100 W | 20 W | 400 W | 200 W |

Note: In this table, D= Duty cycle , Discont = Discontinuous, Cont = Continuous, NA=not available

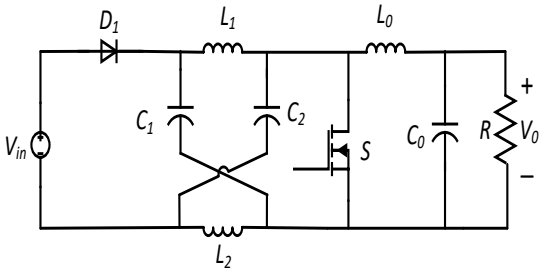


**Figure 2.7:** Converter in reference [47].

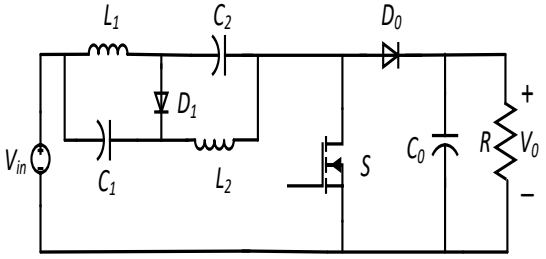


**Figure 2.8:** Converter in reference [51].

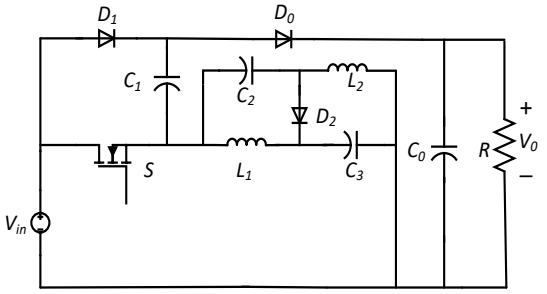


**Figure 2.9:** Converter in reference [49].

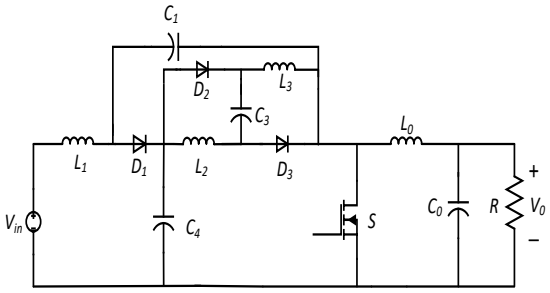


**Figure 2.10:** Converter in reference [36].

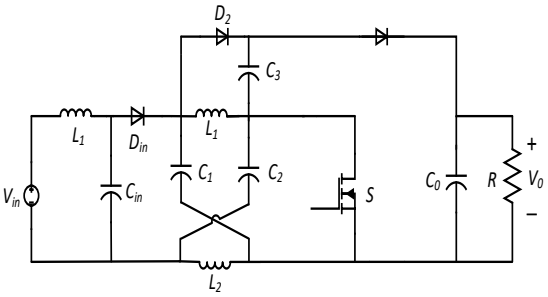


**Figure 2.11:** Converter in reference [50].

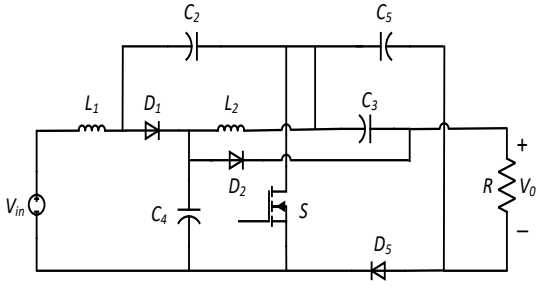


**Figure 2.12:** Proposed converter-1.

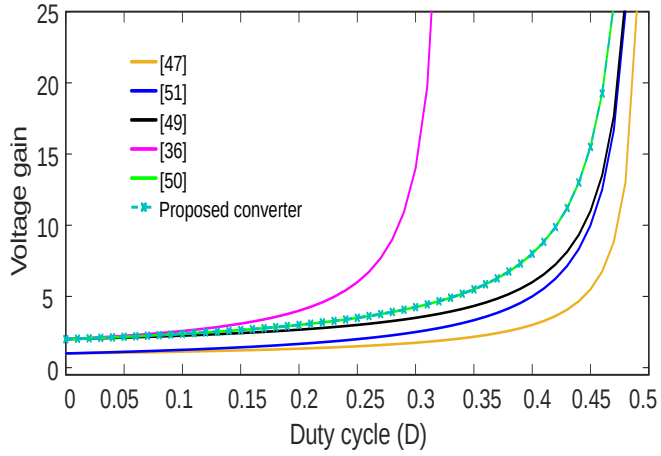


**Figure 2.13:** Voltage gain comparison of existing Z-source converters.

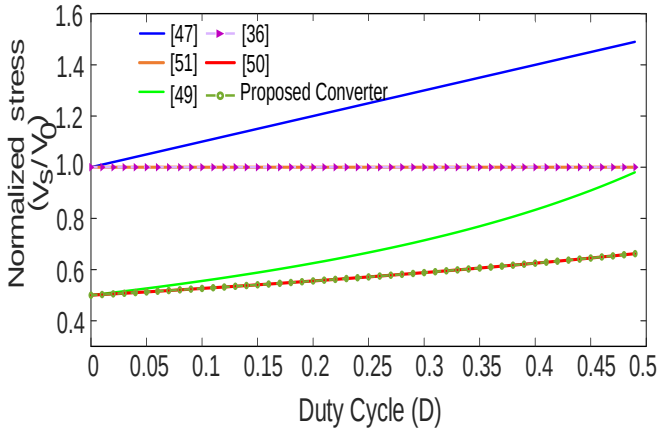


**Figure 2.14:** Switch stress variation with respect to duty cycle.

The normalized switch stress variation with duty cycle is plotted for compared Z-source converters in Figure 2.14. From the plot it can be observed that converters [47], [49] the switch stress increases as increase in the duty cycle. Converters in [51] and [36], the stress is unity for all range of duty cycle. The switch stress for proposed converter and [50] is $\approx 0.6$ around $D = 0.32 - 0.35$ and it is in the acceptable range. The relationship between the analytical voltage gain and the duty ratio is illustrated in

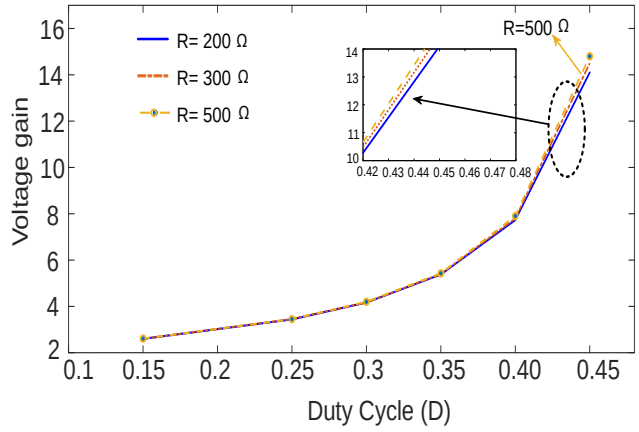


**Figure 2.15:** Analytical voltage gain plot with different load condition.

Figure 2.15, considering various duty ratios and loading conditions (R = 200 Ω, 300 Ω, and 500 Ω). The graph demonstrates that as the duty ratio increases, the voltage gain increases. In simpler terms, raising the duty ratio leads to higher voltage amplification. The voltage gain of the converter at a high value of load resistance increases due to a lower voltage drop across passive elements at a lower current.

## 2.6 Experiment results

In order to verify the feasibility of proposed converter laboratory prototype is built and tested in CCM mode as shown in Figure 2.16. The numerical of value of storing elements is derived from the Section-2.3. The caluculation of storing elements for converter is discussed here. The design of storing element is calculated for $P_0 = 200\ W$ of load power keeping the load resistance $R = 200\ \Omega$, switching frequency $f_s$=40 $kHz$ and input voltage fixed to 36 $V$. The duty cycle calculation for above mentioned value presented in eq. (2.34).

$$P_0 = \frac{V_0^2}{R},\ \Longrightarrow\ V_0 = 200\ V \tag{2.33}$$

$$\frac{V_0}{V_{in}} = \frac{2-D}{1-2D},\ \Longrightarrow\ D \approx 0.351 \tag{2.34}$$

Using eq. (2.23) and eq. (2.24) the calculation of inductance is discussed here.

$$L_1 = \left(\frac{(1-D)DV_{in}}{(1-2D)\Delta I_{L1}}\right) DT_s,\ \Longrightarrow\ L_1 = \frac{0.65 \times 36 \times 0.35}{0.3 \times 40k \times 0.1} = 825\ \mu H \tag{2.35}$$

$$L_2 = \left(\frac{(1-D)DV_{in}}{(1-2D)\Delta I_{L2}}\right) DT_s,\ \Longrightarrow\ L_2 = \frac{0.65 \times 36 \times 0.35}{0.3 \times 40k \times 0.15} = 1.2\ mH \tag{2.36}$$

Similarly, the calculation for capacitance is discussed using eq. (2.25) to eq. (2.28).

$$C_2 = \frac{(2-D)I_0DT_s}{(1-2D)\Delta V_{C2}},\ \Longrightarrow\ C_2 = \frac{1.65 \times \times 0.35}{0.3 \times 0.02 \times 40k} = 57\ \mu F \tag{2.37}$$

$$C_3 = \frac{I_0(1-D)T_s}{\Delta V_{C3}},\ \Longrightarrow\ C_3 = \frac{0.65}{0.01 \times 40k} = 21\ \mu F \tag{2.38}$$

$$C_4 = \frac{(1+D^2-D)I_0T_s}{\Delta(1-2D)V_{C4}},\ \Longrightarrow\ C_4 = \frac{0.77 \times 1}{0.3 \times 0.02 \times 40k} = 42\ \mu F \tag{2.39}$$

$$C_5 = \frac{DI_0T_s}{\Delta V_{C5}},\ \Longrightarrow\ C_5 = \frac{0.35 \times 1}{0.01 \times 40k} = 8\ \mu F \tag{2.40}$$

The final value of storing elements used in the prototype are listed in Table 2.4. The experimental setup utilized components listed in Table 2.3 , with voltage measurements performed using Tektronix probes.

To verify the theoretical analysis 36 $V$ input DC source is taken as to supply the power to rheostate of 200 $\Omega$. The measured steady state waveform are presented in Figure 2.17 to Figure 2.18. The converter boost the 36 $V$ supply voltage to 195 $V$. The source current exhibits low ripple (below 10%, with an average value 5.8 $A$) at load current 0.97 $A$. The current ripple of both inductors are well within the permissible

**Table 2.3:** Device and components used in experiment

| **Component/Device** | **Part Number and Manufacturer** |
|---|---|
| DC Source | H3010, Aplab |
| MOSFET | FDA59N25, Fairchild |
| Diode | DPG60C200QB, IXYS |
| Gate driver | HCPL3120 Avago Technology |
| Inductor | PCV-2-564-08L<br>PCV-2-274-10L, Coilcraft |
| Capacitor | 4500CXW82MEFC, Rubycon |

**Table 2.4:** Specification and parameter of the proposed converter-1

| **Parameter** | **Value** |
|---|---|
| Input Voltage $V_{in}$ | 36 $V$ |
| Output Voltage $V_0$ | 190 $V$ |
| Inductance $L_1$, $L_2$ | 850 $\mu H$, 1.2 $mH$ |
| Capacitance $C_2$ | 63 $\mu F$ |
| Capacitance $C_3$, $C_4$ | 47 $\mu F$ |
| Capacitance $C_5$ | 22 $\mu F$ |
| Duty Cycle $D$ | 0.35 |
| Switching Frequency $f_s$ | 40 $kHz$ |
| Load, $R$ | 200 $\Omega$ |

value $\Delta I_{L1} < 10\%$ for $L_1$ and $\Delta I_{L2} < 15\%$ for $L_2$ with an average value is $I_{L1} = 5.8\ A$ and $I_{L2} = 4.6\ A$, respectively. As per Figure 2.18 the voltage stress across Switch is 120 $V$. Similarly the voltage stress across Diode $D_1$, $D_2$ and $D_5$ is 120 $V$, 120 $V$ and 105 $V$, respectively. The main features of proposed converter is reduced voltage stress across diodes and switch (less than output voltage $\approx$ 120 $V$) demonstrated in Figure 2.18 and Figure 2.19. Moreover, the measured mean voltages of all capacitors closely adhere to the analytical expressions depicted in Figure 2.20, previously derived in the voltage gain section. The slight variation in voltage across capacitors can be due to the non-idealities inherent in the converter.

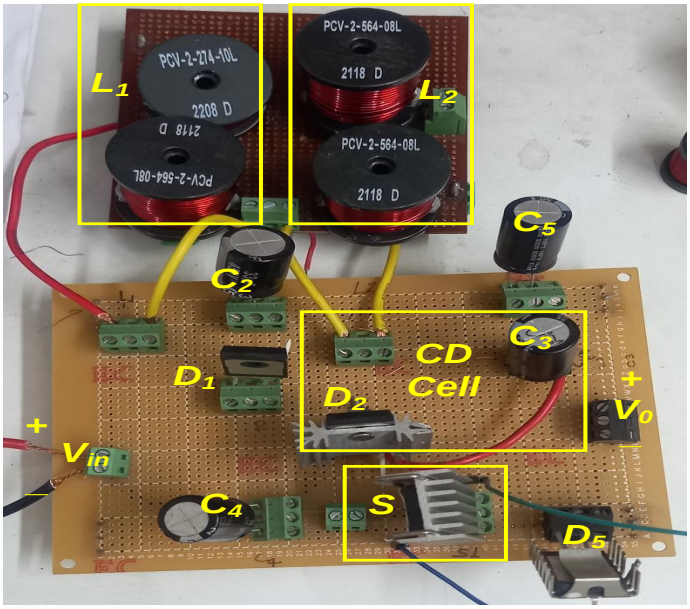


**Figure 2.16:** Photograph of proposed Z-source converter.

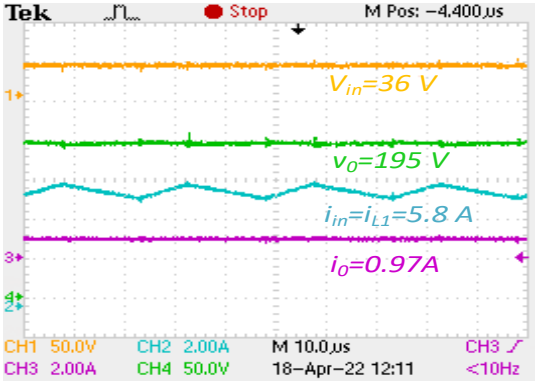


**Figure 2.17:** Measured Input-output volatge and current.

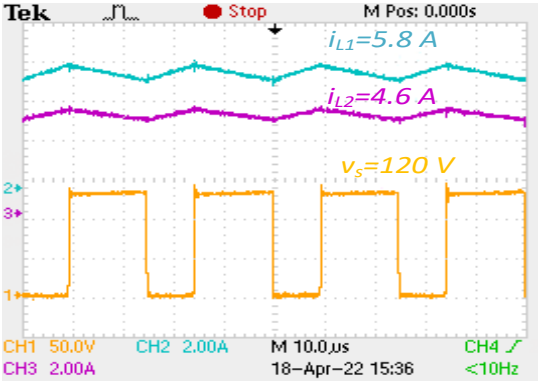


**Figure 2.18:** Zoomed inductor current and switch stress.

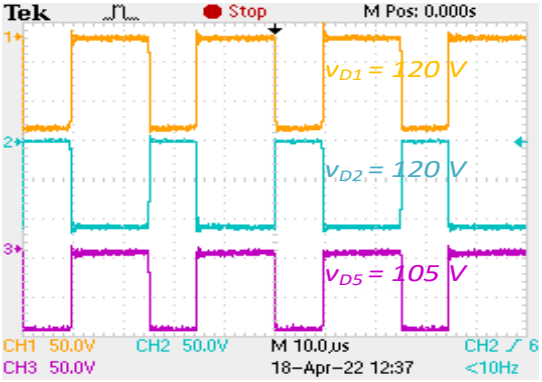


**Figure 2.19:** Measured voltage stress across $D_1$, $D_2$ and $D_5$.

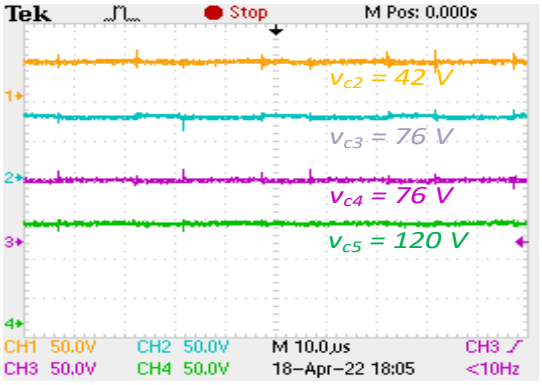


**Figure 2.20:** Measured voltage across $C_2$, $C_3$, $C_4$ and $C_5$.

## 2.7 Conclusion

The proposed Z-source-based high voltage gain DC-DC converter is explained with mathematical analysis. The main feature of this converter is that it can achieve high gain at a low-duty cycle, leading to reduced voltage stress across the semiconductor devices. An experiment is conducted to verify the analytical expressions, and at a power rating of 190 $W$, the measured efficiency is approximately 90.5%.

In this chapter, single switch-based Z-source topologies are compared, and the proposed converter has achieved gain with maximum duty limited to 50%. Since the proposed converter does not share a common source to load ground, it may lead to excess switching noise effects and leakage current. These limitations of the converter version 2 are addressed in the next chapter.