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Three-phase quasi-Z source inverters with regulated multiple AC outputs for microgrid applications and three-phase residential load

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Abstract: In this study, two 3-φ quasi-Z source inverters (qZSIs) with multiple ac outputs are proposed. The proposed topologies are developed from qZSI to obtain parallel mode and series mode 3-φ multi-output inverters. In parallel mode, the topology yields *n*-number of parallel ac outputs with different voltages and currents for different load conditions. For series mode, topology yields *n*-number of series ac outputs with same voltages and same load currents. Unlike voltage source derived multi-output inverters, the proposed inverters have all inherent properties of qZSI, like shoot-through protection and both buck–boost operations. For generating switching signals in these inverters, sinusoidal pulse width modulation with constant frequency shoot-through scheme is used. The proposed topologies fulfil more than one load demand at a time without any extra adaptor or regulator. The proposed inverters can be used for simultaneous multiple dc/ac power conversion for three-phase microgrid applications and three-phase residential loads. In this work, the proposed topologies with closed-loop control have been implemented for two inverter units, which is capable of supplying two ac outputs simultaneously. The mathematical modelling of the proposed topologies is carried out for performance analysis. The experimental results of 240 W lab prototypes have been presented to validate the proposed three-phase multi-output qZSIs.

1 Introduction

In recent times, multi-output converters have become popular for various applications such as microgrid and residential loads, as they can give multiple outputs simultaneously for different load requirements [1–3]. Also, the multi-output converters have other advantages like compact size, higher power density, and lower cost [4, 5]. Further, the scenario of microgrid concept is emerging fast, which is a systematic approach to interlink different converter outputs, renewable energy sources, energy storage system and local loads within the certain area [6, 7]. Therefore, the growing microgrid application and the other residential loads necessitate power converters giving simultaneous multiple outputs.

Owing to the demands and benefits of multi-output converters, lots of research studies are being done on them and various multi-output converters are reported in the literature. In [8–10], the discussed multiple output converters are predominantly dc/dc converters which give only multiple dc outputs for various applications and do not have ac at the output. The authors of [11–13] discuss hybrid multi-output converters which give two simultaneous output, one ac and one dc, but they are not able to give multiple ac outputs simultaneously. The topologies presented in [14, 15] are split source-based hybrid converters, which give single-phase ac output and one dc output. The hybrid converter presented in [16] gives multilevel ac and one dc outputs simultaneously. Therefore, it may be perceived that the multi-output converters discussed above are not able to give three-phase multi ac outputs. The hybrid converter discussed in [17] is based on the conventional source-based inverter that can supply single dc and multiple single-phase ac output. However, it is limited to only low power applications and displays shoot-through (ST) problem. The literature [18, 19] discuss hybrid multi-output converters which give one dc and multiple ac outputs but ST problem occur in these converter topologies as well.

A system representing the conventional multi-output hybrid converters for the application of hybrid microgrid/residential load is shown in Fig. 1*a*. As the conventional multi-output inverters are derived from voltage source inverters, they inherit the problem of ST because of misgating due to electromagnetic interference. Moreover, they have only a buck output capability.

In this paper, two 3-∅ multi ac quasi-Z source inverters (qZSIs) are presented. A representative system of the proposed multi ac 3-∅ qZSIs is shown in Fig. 1*b*. The proposed topologies are developed from qZSI to obtain parallel mode and series mode 3-φ multi output inverters. The proposed qZSIs are developed from the quasi-Z source network, where the inverter switch is replaced by either *n* parallel-connected 3-∅ inverters or *n* series-connected 3-∅ inverters. The topology developed from the parallel-connected 3-∅ inverters offers parallel mode of operation of the inverter. In parallel mode, different voltage outputs with different currents (for different load conditions) are obtained. Similarly, in series mode of the proposed topology, same voltages and same load currents are obtained at multiple output units. Using closed-loop control, these topologies give regulated voltages and currents that can be used for microgrid applications as well as 3-∅ residential load simultaneously without using any extra regulator or adaptor. Unlike the are conventional multi-output converters, the proposed inverters derived from impedance source network and have the advantage of inherent ST protection. Moreover, they possess the inherent feature of both buck–boost capabilities of qZSI.

In Section 2 of the paper, the proposed multi ac output three-phase qZSIs are described. Section 3 deals with the PWM scheme for the inverters. The proposed topology is validated by experimental results in Section 4 and finally, conclusions are presented in Section 5.

2 Proposed three-phase multi AC outputs quasi-Z source inverters

The proposed 3-∅ multi ac outputs qZSIs schemes are shown in Fig. 2. Figs. 2*a* and *b* show the proposed three-phase multi ac outputs qZSI with parallel mode and series mode, respectively. From Fig. 2, it may be observed that the proposed qZSI with parallel mode is able to provide *n*-number of controlled ac outputs with different output voltages and load currents. Similarly, with the series mode, it is able to provide *n*-number of ac outputs with same output voltages and currents. In this work, the proposed topologies of three-phase multi ac output qZSIs are analysed validated for two ac outputs (i.e. $n = 2$). The same methodology will be valid to

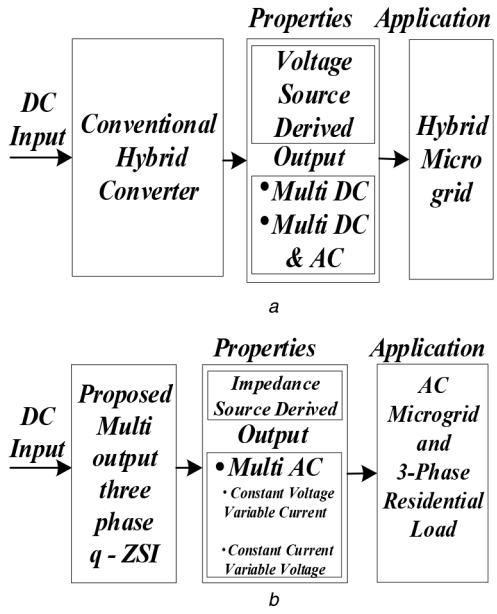


Fig. 1 *Hybrid microgrid structure*
(a) Representative system of the conventional hybrid converter & application, ***(b)*** Proposed 3-∅ multi ac qZSIs & its application

design the proposed inverters for more than 2 (n number of outputs).

2.1 Circuit analysis and operation of the proposed three-phase multi ac output qZSIs

The proposed three-phase multi ac output qZSIs are operated in two different intervals: (i) power interval; and (ii) ST interval. The switching period assumed to be T. the power interval and ST interval are T_1 and T_0, respectively.

2.1.1 ST interval: Figs. 3*a* and *b* show the operation of proposed multi-output inverter and their equivalent circuits during ST interval for the parallel and series mode connections, respectively. To describe the circuit behaviour, the circuit is simplified by replacing inverters with one switch and the equivalent circuit is shown in Fig. 3*c*. From Fig. 3*c*, it may be noticed that during the ST period, the switches of the same leg conduct simultaneously and the diode D is reverse biased. The impedance source network inductors L_1 and L_2 store energy and the capacitors C_1 and C_2 get discharged. In this interval, the switch-node voltage $V_{\rm PN}$ of the proposed qZSI inverters is equal to zero. In the ST interval, the governing equations are as follows:

$$L_1\frac{{\rm d}i_{L1}}{{\rm d}t} = V_{\rm in} + V_{c1}; \tag{1}$$

$$L_2\frac{{\rm d}i_{L2}}{{\rm d}t} = V_{c2}\,; \tag{2}$$

$$C_1\frac{{\rm d}v_{c1}}{{\rm d}t} = -I_{L1}; \tag{3}$$

$$C_2\frac{{\rm d}v_{c2}}{{\rm d}t} = -I_{L2}\,; \tag{4}$$

$$V_{\rm PN} = 0; \tag{5}$$

2.1.2 Power interval: Figs. 4*a* and *b* show the operation of proposed multi-output inverter and their equivalent circuits during power interval for the parallel and series mode connections, respectively. To describe the circuit behaviour, the circuit is simplified by replacing inverters with one switch and the equivalent circuit is shown in Fig. 4*c*. From Fig. 4*c*, it may be noticed that during power interval, the switches of the different legs conduct simultaneously ensuring power flow from source to load, and diode D is forward biased. The inductors L_1 and L_2 release energy and capacitors C_1 and C_2 get charged. In this state, switch-node voltage is $V_{\rm PN}$ of the proposed qZSI inverters is non-zero and it acts as input to the inverter. In the power interval, the governing equations are as follows:

$$L_1\frac{{\rm d}i_{L1}}{{\rm d}t} = V_{\rm in} - V_{c2}; \tag{6}$$

$$L_2\frac{{\rm d}i_{L2}}{{\rm d}t} = -V_{C1}; \tag{7}$$

$$C_1\frac{{\rm d}v_{c1}}{{\rm d}t} = I_{L2} - I_{pn}; \tag{8}$$

$$C_2\frac{{\rm d}v_{c2}}{{\rm d}t} = I_{L1} - I_{pn}; \tag{9}$$

$$V_{\rm PN} = V_{c1} + V_{c2}; \tag{10}$$

From (1) and (2) and (6) and (7), the following equations are obtained using volt-second balance on inductors L_1 and L_2

$$V_{L1} = \overline{v_{L1}} = \frac{T_0(V_{\rm in} + v_{c1}) + T_1(V_{\rm in} - v_{c2})}{T} = 0; \tag{11}$$

$$V_{L2} = \overline{v_{L2}} = \frac{T_0V_{C2} - T_1V_{C1}}{T} = 0 \tag{12}$$

On solving the above, the following is obtained:

$$V_{C1} = \frac{D}{1-2D}V_{\rm in};\, V_{C2} = \frac{1-D}{1-2D}V_{\rm in};\, V_{\rm PN} = \frac{1}{1-2D}V_{\rm in} \tag{13}$$

Similarly, the following can be obtained from (3) and (4) and (8) and (9) using the Charge balance on capacitors C_1 and C_2

$$I_{C1} = \overline{i_{C1}} = \frac{T_0(-I_{L1}) + T_1(I_{L2} - I_{PN})}{T} = 0; \tag{14}$$

$$I_{C2} = \overline{i_{C2}} = \frac{T_0(-I_{L2}) + T_1(I_{L1} - I_{\rm PN})}{T} = 0 \tag{15}$$

Solving (15), the following is obtained:

$$I_{L1} = \frac{(1-D)}{(1-2D)}I_{\rm PN}\,;\, I_{L2} = \frac{(1-D)}{(1-2D)}I_{\rm PN} \tag{16}$$

The qZSI inverter's peak switch node voltage $V_{\rm PN}$ can be expressed as follows:

$$\hat{v}_{\rm PN} = \frac{1}{1-2D}V_{\rm in} = BV_{\rm in} \tag{17}$$

where B is the boost factor of the proposed three-phase multi-output ac qZSIs. The peak value of the fundamental component of output is given by

$$(\hat{v}_{\rm AC})_{\rm fundamental} = \hat{v}_0 = \frac{M}{2}V'_{\rm PN} = \frac{M}{2}\left(\frac{1}{1-2D}\right)V_{\rm in} \tag{18}$$

where $V'_{\rm PN} = V_{\rm PN}$ for parallel mode and $V'_{\rm PN} = V_{\rm PN}/2$ for series mode

$$\frac{(\hat{v}_{\rm AC})_{\rm fundamental}}{V_{\rm in}} = G;\, G = \frac{M}{2}\left(\frac{1}{1-2D}\right) \tag{19}$$

where M is the modulation index of the inverter. The gain by the proposed inverter is same as gain given by traditional ZSI. This

gain G of the inverter can be varied by varying the ST duty ratio, D. Various voltage gains with respect to modulation index M the duty ratio D are graphically represented in Fig. 5. Variation in boost factor, B w.r.t. ST duty ratio D is shown in Figs. 5*a* and *b* depicts the graph showing a variation of the ratio of output ac voltage and node voltage (peak V_{ac}/V_{PN}) w.r.t. modulation index M. A graphical 3-dimensional representation of variation of the ratio G of output ac voltage V_{ac} and input dc voltage V_{in}, w.r.t. D and M are shown in Fig. 5*c*.

2.2 AC power expression of qZSIs

The ac power expression for the proposed multi-output inverters (with two units) with parallel and series mode of operations is given in the following subsections. The following constraint for sinusoidal pulse width modulation (SPWM) with ST states for the proposed inverters is as follows [20]:

$$D + M \leq 1 \tag{20}$$

2.2.1 Parallel mode operation of the proposed topology: In this mode of operation, the switch node voltages of inverter unit 1

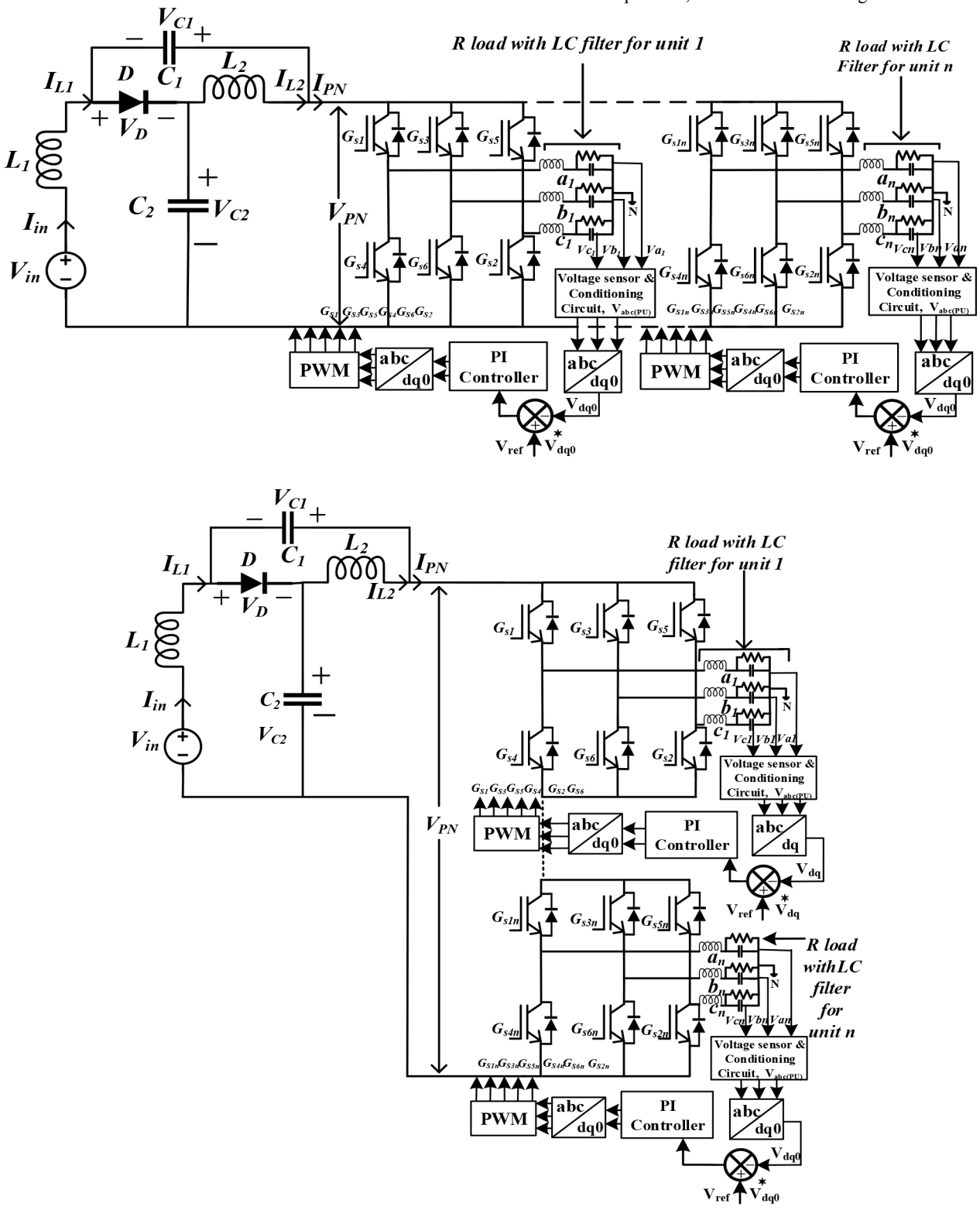


Fig. 2 *Proposed three-phase multi ac qZSIs*
(a) Proposed parallel mode multi ac three-phase qZSI, ***(b)*** Proposed series mode multi ac three-phase qZSI

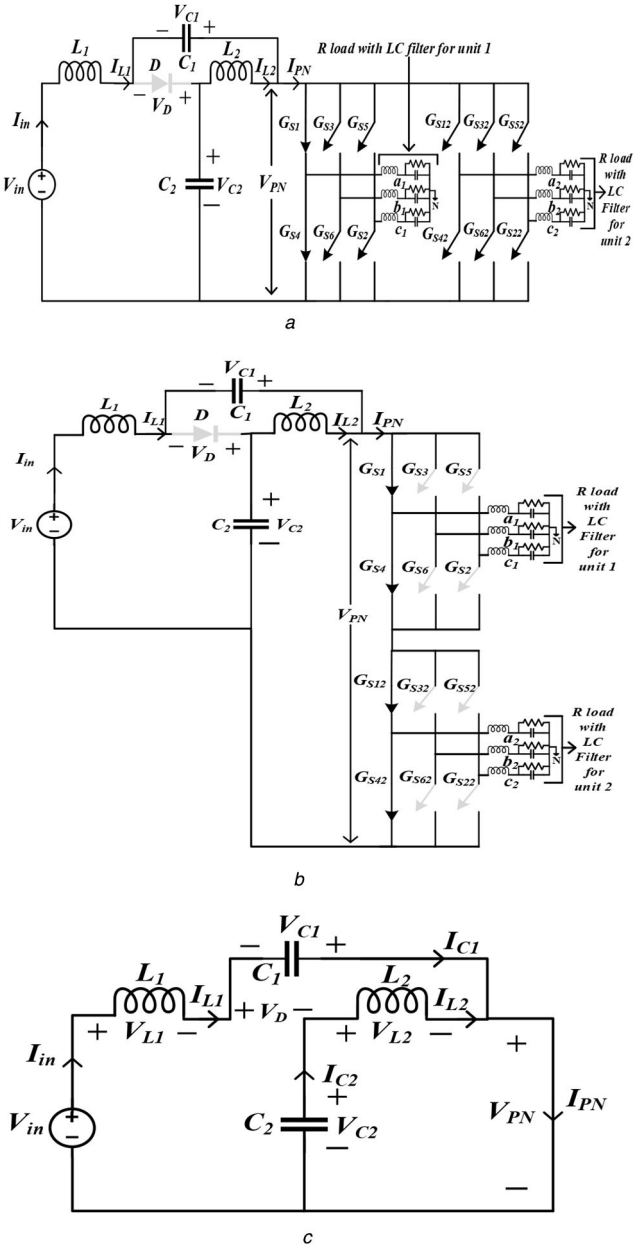


Fig. 3 *Proposed three-phase multi ac qZSIs during the ST interval*
(a) Proposed parallel mode inverter during the ST interval, ***(b)*** Proposed series mode inverter during the ST interval, and ***(c)*** Equivalent circuit during ST interval

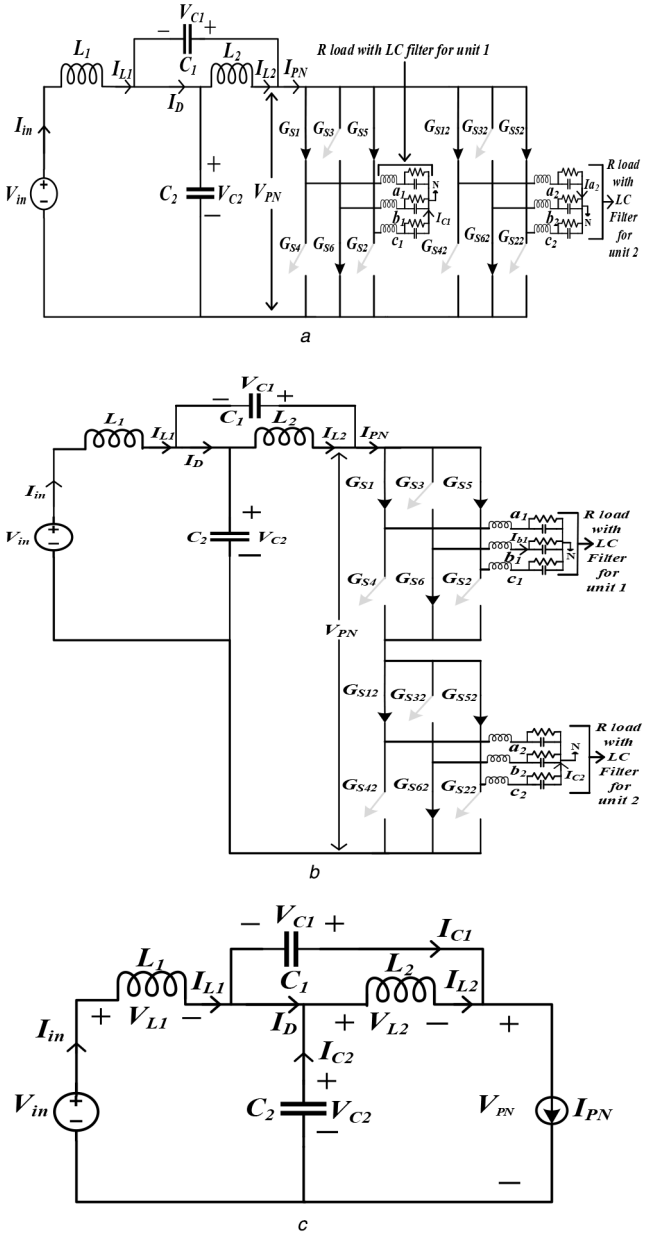


Fig. 4 *Proposed multi three-phase ac qZSIs during power interval*
(a) Proposed parallel mode inverter during power interval, ***(b)*** Proposed series mode inverter during power interval, and ***(c)*** Equivalent circuit during power interval

and unit 2 (i.e. V_{PN1} and V_{PN2}) are the same (i.e. V_{PN}) as the inverter units are connected in parallel. The peak ac voltages $(\hat{v}_{01}$ and $\hat{v}_{02})$ will be equal, for same reference voltages (V_{ref}) and balanced ac loads. The peak ac voltages $(\hat{v}_{01}$ and $\hat{v}_{02})$ will be different for different reference voltages (V_{ref}) of the inverter units. Here, the reference voltage (V_{ref}) for inverter unit is required peak ac output voltage $(\hat{v}_0)$. For the same V_{ref}

$$\hat{v}_{01} = \hat{v}_{02} = \frac{M}{2} V_{PN} = \frac{M}{2}\left(\frac{1}{1-2D}\right) V_{in} \tag{21}$$

The ratio of peak ac voltage and input voltage (V_{in}) can be written as

$$\left(\frac{(\hat{v}_{AC})_{fundamental}}{V_{in}}\right) = \left(\frac{\hat{v}_0}{V_{in}}\right) = G = \frac{M}{2}\left(\frac{1}{1-2D}\right) \tag{22}$$

The expression of r.m.s ac output voltage gain (G_{ac}) is given as

$$G_{ac} = \frac{V_{o,rms}}{V_{in}} = \frac{M}{2\sqrt{2}}\left(\frac{1}{1-2D}\right) \tag{23}$$

The r.m.s ac output voltage ($V_{o,rms}$) is given as = $\left(\hat{v}_0/\sqrt{2}\right)$

$$V_{o,rms} = \frac{M}{2\sqrt{2}}\left(\frac{1}{1-2D}\right) V_{in} \tag{24}$$

The three-phase $(3-\varnothing)$ ac power output $(P_{3-\varnothing})$ of both unit at same V_{ref} is given as

$$P_{(3-\varnothing)} = 6\frac{V_{o,rms}^2}{R} = 6\frac{M^2\, B^2\, V_{in}^2}{8\, R} \tag{25}$$

Similarly, The three-phase ac power output $(P_{(3-\varnothing)})$ of both unit at different V_{ref} is given as

$$P_{3-\varnothing} = 3\frac{(M_1^2 + M_2^2)B^2\ V_{in}^2}{8\ R}, \quad \left(B = \frac{1}{1-2D}\right) \tag{26}$$

where M_1 and M_2 are the modulation index of inverter unit 1 and unit 2, respectively, and B is the boost factor.

From the (25) and (26), it is clear that $P_{3-\varnothing}$ depends on M and D.

2.2.2 Series mode operation of the proposed topology: In this mode of operation, the switch node voltage (V_{PN}) is equally divided across the inverter bridges for balanced ac load and peak ac voltages ($\hat{v}_{01}$ and $\hat{v}_{02}$) will be equal for the same voltage reference

$$\hat{v}_{01} = \hat{v}_{02} = \frac{M}{2}\frac{V_{PN}}{2} = \frac{M}{4}\left(\frac{1}{1-2D}\right)V_{in} \tag{27}$$

The ratio of peak ac voltage and V_{in} can be written as

$$\left(\frac{(\hat{v}_{AC})_{fundamental}}{V_{in}}\right) = \left(\frac{\hat{v}_0}{V_{in}}\right) = G = \frac{M}{4}\left(\frac{1}{1-2D}\right) \tag{28}$$

The r.m.s ac output voltage gain (G_{ac}) is given as

$$G_{ac} = \frac{M}{4\sqrt{2}}\left(\frac{1}{1-2D}\right) \tag{29}$$

The r.m.s ac output voltage ($V_{o,rms}$) is given as

$$V_{o,rms} = \frac{\hat{v}_0}{\sqrt{2}} = \frac{M}{4\sqrt{2}}\left(\frac{1}{1-2D}\right)V_{in} \tag{30}$$

The 3-∅ ac power output $P_{(3-\varnothing)}$ of a single unit is given as

$$P_{(3-\varnothing)} = 3\frac{V_{o,rms}^2}{R} = 3\frac{M^2 B^2 V_{in}^2}{32 R} \quad \left(B = \frac{1}{1-2D}\right) \tag{31}$$

The 3-∅ ac power output ($P_{3-\varnothing}$) of both units is given as

$$P_{(3-\varnothing)} = 6\frac{V_{o,rms}^2}{R} = 6\frac{M^2 B^2 V_{in}^2}{32 R} \quad \left(B = \frac{1}{1-2D}\right) \tag{32}$$

From the (32), it is clear that the $P_{(3-\varnothing)}$ depends on M and D. The voltage $\hat{v}_0$ is directly proportional to the modulation index of the inverter unit. Therefore, as the V_{ref} is increased the modulation index (M) is increases due to which output power increases and vice versa [21–23].

In this way, using the series-parallel connection of n-number of 3-∅ qZSI, the topology is able to give multiple ac outputs with boost capability. Any disturbance in the input voltage or load parameter can be easily taken care of by using a feedback control loop. Consequently, the voltage output will be smooth and constant in nature. Therefore, the power from the proposed inverters can be easily injected into the ac microgrid and simultaneously can be used for residential 3-∅ load.

2.3 Controller for the proposed topology

The 3-∅ output voltages (V_a, V_b and V_c) of the proposed topologies are sensed and transformed into dq components (V_d, V_q) using Park's transformation and compared with references voltages $V_{d(ref)}$ and $V_{q(ref)}$. Then the error signal, which is fed to PI compensator. The required modulated signal is obtained from the PI controller (i.e. $m_{d(req)}$, $m_{q(req)}$). Further $m_{d(req)}$ and $m_{q(req)}$ is converted into modulating signals m_a, m_b and m_c using inverse Park's transformation. By comparing modulating signal with triangular waveform along with positive dc voltage (Vpdc) and negative dc voltage (V_{ndc}) for ST. Thus, switching pulses are generated and fed to the inverter switches. Fig. 6 shows the block diagram of the PI controller for the proposed topology.

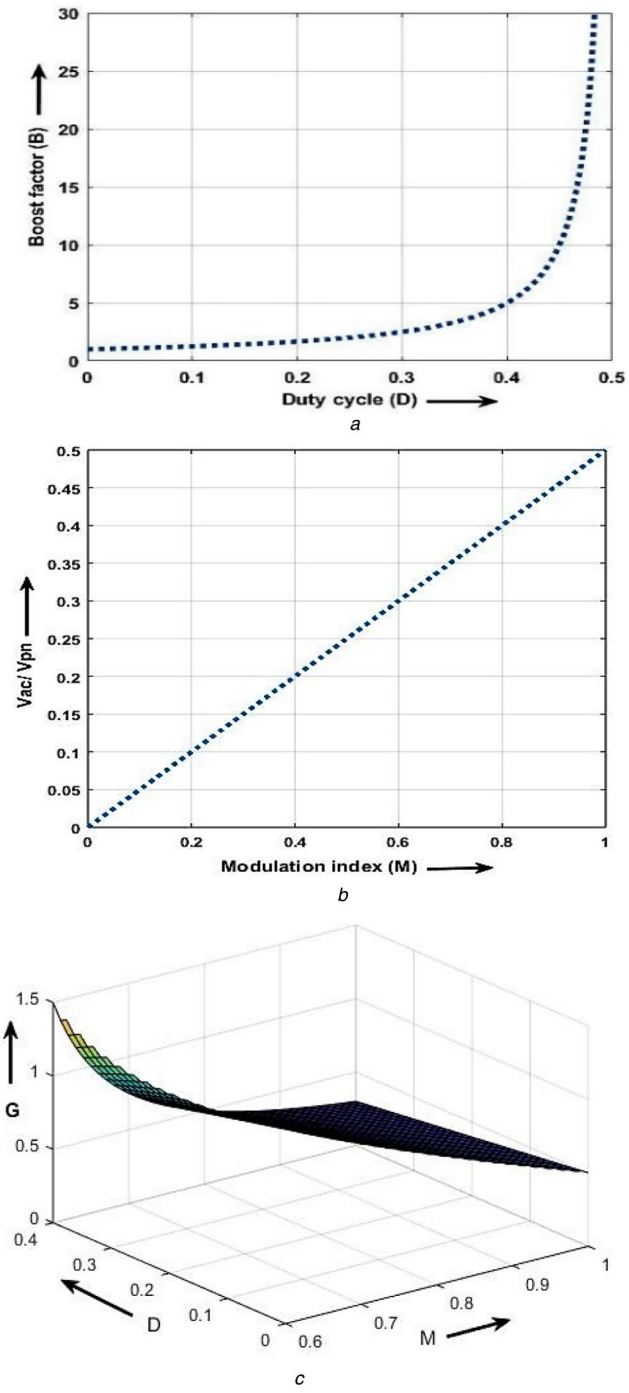


Fig. 5 *Graphical representation of variation of parameters in proposed inverter*

(a) Variation of boost factor (B) with D, ***(b)*** Variation of $\frac{V_{ac}}{V_{PN}}$ with M, ***(c)*** Variation of gain (G) with M and D

2.4 Switch stress

Voltage stresses of each component in the ST interval and power interval are shown in Table 1, whereas the current stresses of each component of the proposed topology in different states are shown in Table 2.

3 PWM for the proposed inverters' operation

To operate the proposed inverters, the modulation technique is implemented using a digital signal processor (DSP) (TI-TMS320F28335). The overall modulation scheme of the proposed topology with switching signals are shown in Fig. 7. The block diagram for logic for generating pulses is shown in Fig. 7*a*. The waveforms related to PWM and corresponding switching signals

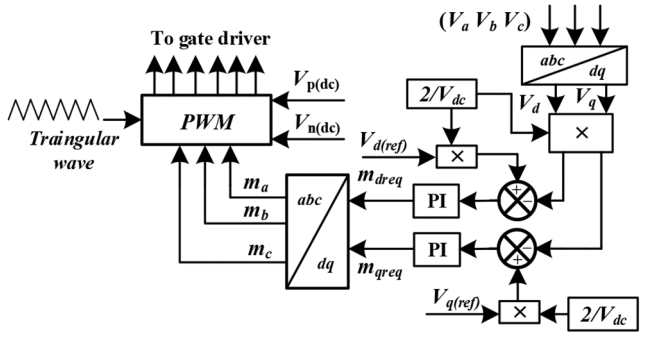


Fig. 6 *Block diagram of Control scheme for the proposed three-phase multi ac qZSIs*

Table 1 Voltage stress of each component in different interval

Parameters	ST state	Power state
L_1	$\frac{(1-D)\,V_{in}}{(1-2D)}$	$\frac{(-D)\,V_{in}}{(1-2D)}$
L_2	$\frac{(1-D)\,V_{in}}{(1-2D)}$	$\frac{(-D)\,V_{in}}{(1-2D)}$
C_1	$\frac{(D)\,V_{in}}{(1-2D)}$	$\frac{(D)\,V_{in}}{(1-2D)}$
C_2	$\frac{(1-D)\,V_{in}}{(1-2D)}$	$\frac{(1-D)\,V_{in}}{(1-2D)}$
D	$\frac{(D)\,V_{in}}{(1-2D)}$	0
V_{PN}	0	$\frac{(D)\,V_{in}}{(1-2D)}$

Table 2 Current stress of each component in different interval

Parameters	ST state	Power state
L_1	I_{in}	I_{in}
L_2	$\frac{-(1-D)\,I_{pn}}{(1-2D)}$	$\frac{(1-D)\,I_{pn}}{(1-2D)}$
C_1	$\frac{-(1-D)\,I_{pn}}{(1-2D)}$	$\frac{(D)\,I_{pn}}{(1-2D)}$
C_2	$\frac{-(1-D)\,I_{pn}}{(1-2D)}$	$\frac{(D)\,I_{pn}}{(1-2D)}$
D	0	$\frac{I_{pn}}{(1-2D)}$

are shown in Figs. 7*b* and *c* for unit 1 and unit 2, respectively. Fig. 7*b* shows the PWM signals along with modulating signals m_a, m_b and m_c of inverter unit 1 with $V_{ref} = 35$ V. The value of modulation index (M) is equal to 0.47 at ST duty $D = 0.3$ with input voltage 60 V. Fig. 7*c* shows PWM signals along with modulating signals m_a, m_b and m_c of inverter unit 2 with $V_{ref} = 25$ V along with PWM signal. The value of M is equal to 0.33 with $D = 0.3$ and input voltage 60 V. The modulating signals for units 1 and 2 will be according to V_{ref} of the two units and, thus, will be different. However, the ST signals will be always same for both the units ($D = 0.3$) to maintain the V_{PN} at input of the three-phase inverter units. In Fig. 7*b*, the signals G_{S1} to G_{S6} are switching signals for switch 1 to switch 6, respectively for unit 1. The proposed inverter acts just like a normal voltage source inverter during the power interval. The switches in the first leg are operated by comparing the first reference sine wave (m_a) with compared the triangular carrier wave (using a relational operator) and the resulting output is used to drive the top switch (G_{S1}) of the leg. Here, the phase difference between m_a and carrier wave is zero, and the compliment signal of G_{S1} is given to bottom switch G_{S4} of leg 1. In the same manner, the switches of second and third legs are operated by comparing the carrier wave with m_b and m_c,

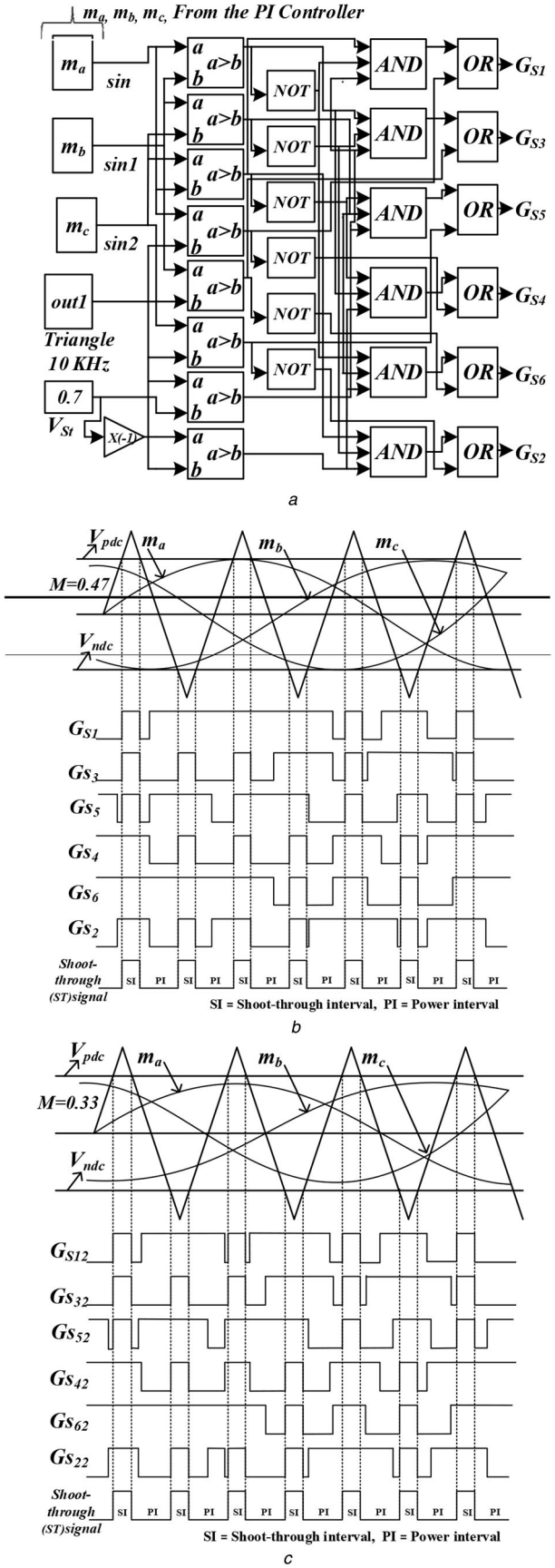


Fig. 7 *Modulation scheme for proposed 3-∅ multi-output inverters*
(a) Implementation of Pulse width modulation signals in DSP (TI-TMS320F28335), ***(b)*** PWM pulses of inverter unit 1 with $V_{ref} = 35$ V (M = 0.47), ***(c)*** PWM pulses of inverter unit 2 with $V_{ref} = 25$ V (M = 0.33)

respectively. To generate ST state, the carrier wave is compared with the two constant dc signals (positive V_{pdc} and negative V_{ndc}).

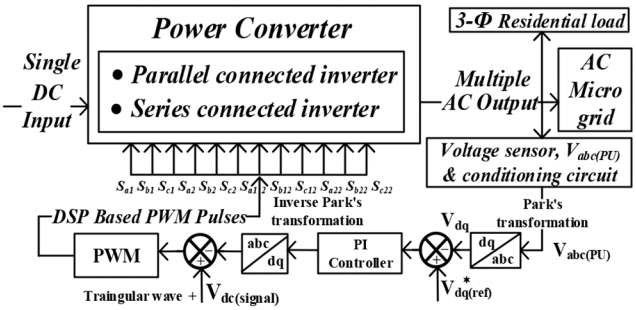


Fig. 8 *Overall implementation of proposed 3- ∅ multi ac qZSIs*

Table 3 Lists of parameters with their values

Prototype specification Parameter	Values
inductor	$L_1 = L_2 = 5$ mH
capacitance	$C_1 = C_2 = 470$ uF
carrier frequency	$f_s = 10$ kHz
fundamental frequency	50 Hz
filter inductor	2 mH
filter capacitor	10 uF
Components	Manufacturer
inverter switches	IRFP260N (I.R.Corp.)
diode	RURG5060 (Fairchild)
gate drivers	FOD3184 (Fairchild)
voltage transducer	LEM LV25-P (Mouser.in)
signal conditioning circuit	Opal-RT
DSP (TI-TMS320F28335)	Texas instrument

ST signal is produced for all the switches of the inverters if the carrier wave is greater than the positive constant dc signal V_{pdc} or less than the negative dc signal V_{ndc}. The switching signals of the unit 2 are generated in the same way and shown in Fig. 7*c*.

4 Experimental verification

The performance of the proposed multi ac three-phase qZSIs for $n = 2$ (i.e. for two simultaneous ac outputs) is validated through experimental results. Fig. 8 depicts the overall implementation of the proposed concept. DSP board (TI-TMS320F28335) is used to generate pulses for the proposed inverters. A real-time simulator Opal-RT (OPT900570) has been used as a signal conditioning circuit to normalize the signal amplitude in between 0 and 3 V range as an input to ADC (analogue to digital converter) of DSP kit. The parameters of the whole system are listed in Table 3. A detailed discussion of steady-state results and dynamic results of the proposed parallel mode qZSI and series mode qZSI are given in subsequent subsections. The experimental setup of the proposed 3-∅ regulated multi ac qZSI is shown in Fig. 9.

4.1 Parallel mode of the proposed inverter

The proposed multi ac qZSI is operated in parallel mode for 240 W application with input voltage (V_{in}) 60 V and ST duty ratio $D = 0.3$ for both the inverter units.

4.2 Steady state response of proposed parallel mode inverter with equal reference voltages

Fig. 10*a* shows the input voltage (V_{in}), the voltage across capacitor C_1 ($V_{C1} = 45$ V), the voltage across the capacitor C_2 ($V_{C2} = 105$ V), and the voltage waveforms across the diode ($V_D = 150$ V) of the proposed qZSI. The value of V_{c1} and V_{c2} is equal to theoretical values calculated by (13). It is observed that the diode is forward biased during power interval thus the voltage across the diode is zero. Further, in ST interval diode is reverse biased and thus the voltage across the diode is negative. Fig. 10*b* shows the input

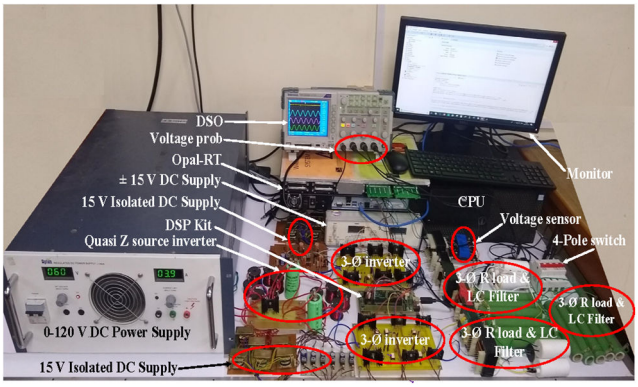


Fig. 9 *Photograph of the experimental prototype*

voltage (V_{in}), switch node voltages of inverter unit 1 and unit 2 (i.e. V_{PN1} and $V_{PN2} = 150$ *V* from (13)), which will be equal (i.e. V_{PN}) as the inverter units are connected in parallel. It is clear from Fig. 10*c* that the voltages V_{PN}, is equal to its theoretical value by (13).

Fig. 10*c* shows the input voltage (V_{in}), switch node voltage voltages (V_{PN}), and current of phase *a* of inverter unit 1 which is equal to the theoretical value. With reference voltage (V_{ref}) is 35 V, voltage of the phase *a* is 70 V (peak-peak) and current is 3.5 A (peak-peak) with a load resistance of 20 Ω per phase. Fig. 10*d* shows the input voltage 60 V and output voltages of three phases 70 V (peak-peak) of inverter unit 1 while the reference voltage (V_{ref}) is at 35 V. All the three phases are 120° apart with each other having same magnitude (70 V peak-peak), indicate the balanced and stable system. Here Time/division is 25 ms for all sinusoidal waveform.

Fig. 11*a* depicts $V_{in} = 60$ V, output voltage 70 V (peak-peak) and current 3.5 A (peak-peak) of phase *a* of inverter unit 1, and output voltage 70 V (peak-peak) of phase *a* of inverter unit 2 while the reference peak ac voltage is at 35 V. It is also clear that the

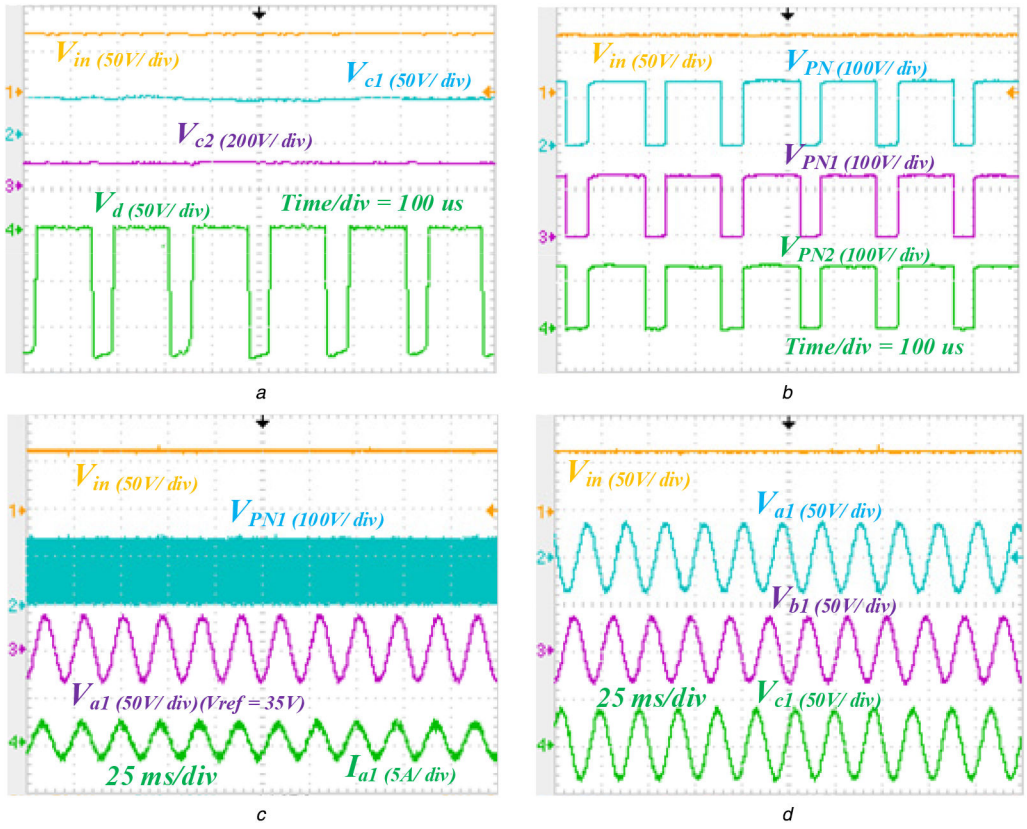


Fig. 10 *Steady-state response of proposed topology during parallel mode operation for equal V_{ref} for both units*

(a) Input voltage V_{in}, capacitor voltage V_{c1} & V_{c2} and voltage switching waveform of diode (V_d), ***(b)*** V_{in}, V_{PN}, V_{PN1} (switch node voltage across Inverter unit 1), V_{PN2}, ***(c)*** V_{in}, V_{PN1}, V_{a1} (phase voltage) and I_{a1} (phase current of inverter unit 1), ***(d)*** V_{in}, three-phase voltages of inverter unit 1

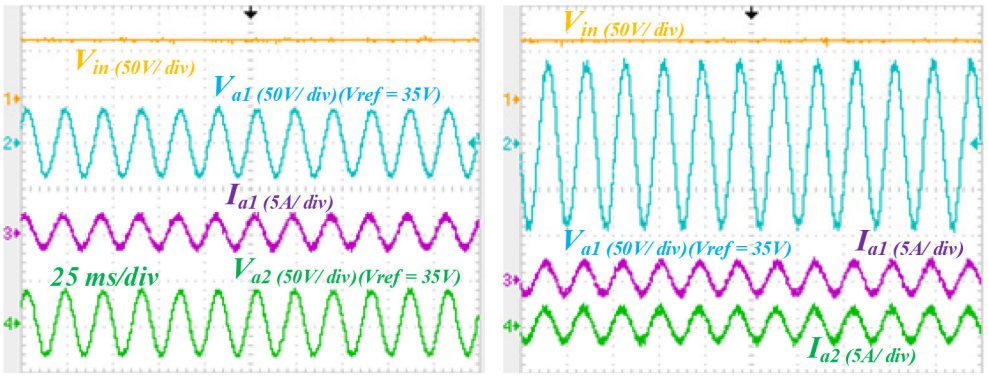


Fig. 11 *Steady state Response of proposed topology during parallel operation with phase voltage & current*

(a) V_{in}, phase voltage and current (V_{a1} & I_{a1}) of unit 1, phase voltage (V_{a2}) of unit 2, ***(b)*** V_{in}, V_{a1}, I_{a1} of unit 1, I_{a2} of unit 2

phase voltage of inverters 1 and 2 have the same magnitude and phase angle (i.e. 0° phase displacement). Fig. 11*b* shows input voltage, phase *a* voltage, phase *a* current of inverter unit 1, and output current of phase *a* of unit 2 with reference voltage of 35 V. It also shows that the phase current of unit 1 and current of unit 2 are same. It indicates that both unit are stable, balanced with same reference voltage.

4.3 Steady-state response of proposed parallel mode inverter with different reference voltages

Fig. 12*a* shows $V_{in} = 60$ V, output voltage (V_{a1}) = 70 V (peak-peak), phase *a* current (I_{a1}) = 3.5 A (peak-peak) of unit 1 and output voltage (V_{a2}) = 60 V (peak-peak) of unit 2 while V_{ref} is at 35 and 30 V, respectively. Fig. 12*b* shows $V_{a2} = 60$ V (peak-peak), $I_{a2} = 3$ A (peak-peak) of unit 2 and V_{a1} 70 V (peak-peak) of unit 1 while V_{ref} is at 30 and 35 V, respectively.

4.3.1 PWM signals of the proposed parallel mode inverters with equal reference:

Figs. 13*a* and *b* show the PWM pulses of upper side and lower side switches of inverter unit 1. Figs. 14*c* and *d* show the PWM pulses of the upper side and lower side switches of inverter unit 2.

4.4 Dynamic response of proposed parallel mode inverter with the same reference voltages

Fig. 14 shows the dynamics of the proposed topology at the same $V_{ref} = 35$ V for both units with change in load resistance in unit 1. In Fig. 14*a*, it is changed from 20 to 10 Ω and the corresponding load current increases from 3.5 A (peak-peak) to 7 A. As the current increases, the phase *a* voltages of unit 1 (V_{a1}) slightly decreases and it restores its original position within very less time (in one cycle). It indicates that the proposed topology is stable and has good dynamic response. The phase *a* voltage of unit 2 (V_{a2}) remains constant at $V_{ref} = 35$ V. Similarly Fig. 14*b* shows the step-

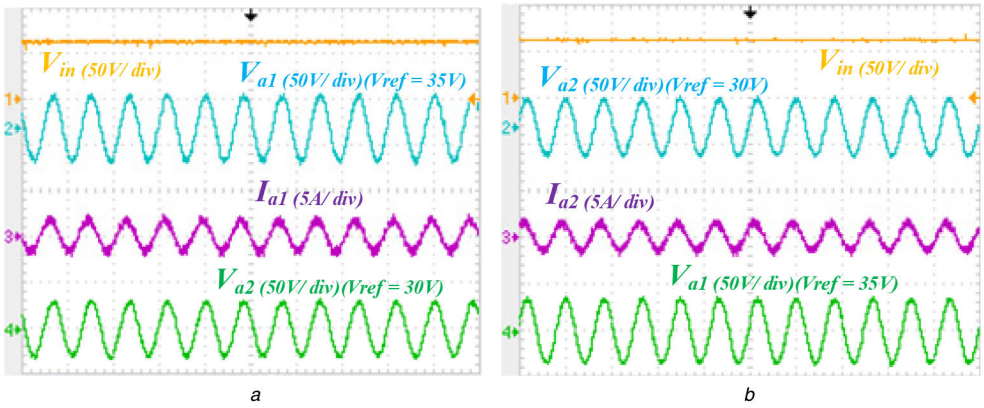


Fig. 12 *Steady-state response of proposed topology during parallel operation with phase voltage & current at different V_{ref}*
(a) V_{in}, V_{a1}, I_{a1} of unit 1 at V_{ref} = 35 V, V_{a2} of unit 2 at V_{ref} = 30 V, ***(b)*** V_{in}, V_{a2}, I_{a2} of unit 2 at V_{ref} = 30 V, V_{a1} of unit 1 at V_{ref} = 35 V

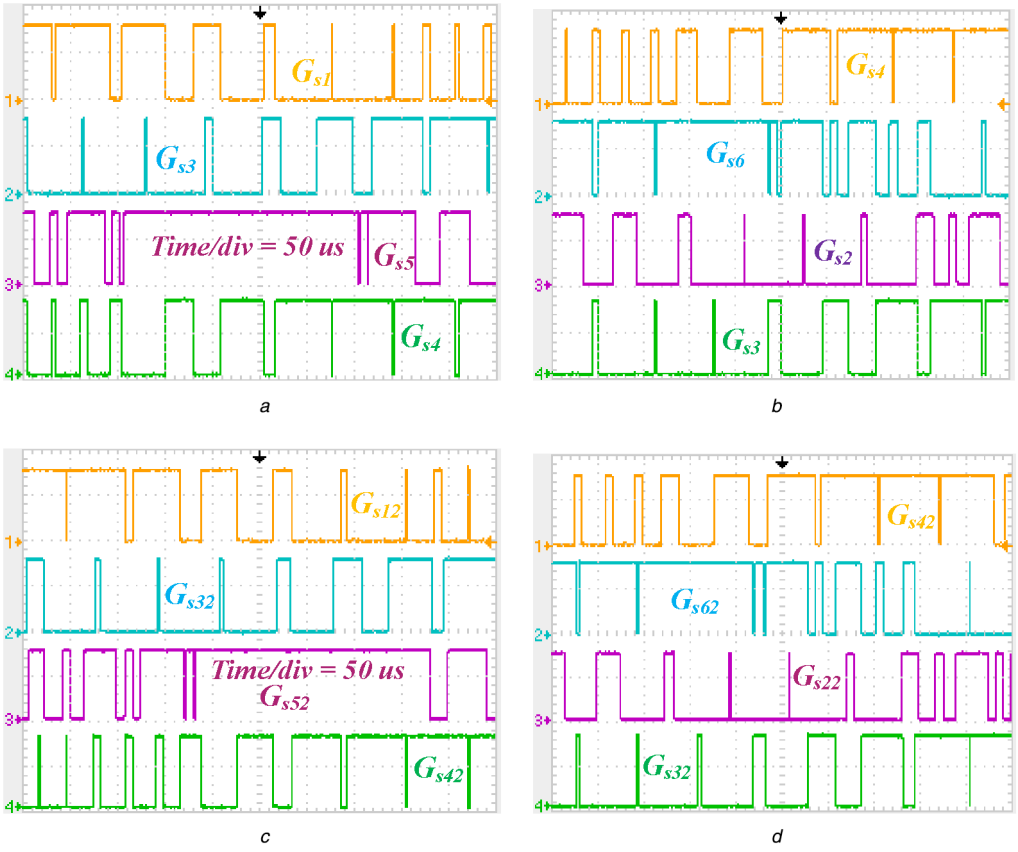


Fig. 13 *PWM pulses of proposed topology during parallel operation*
(a) PWM pulses of upper switches and G_{s4} of inverter unit 1, ***(b)*** PWM pulses of lower switches and G_{s3} of inverter unit 1, ***(c)*** PWM pulses of upper switches and G_{s42} of inverter unit 2 and, ***(d)*** PWM pulses of lower switches and G_{s32} of inverter unit 2

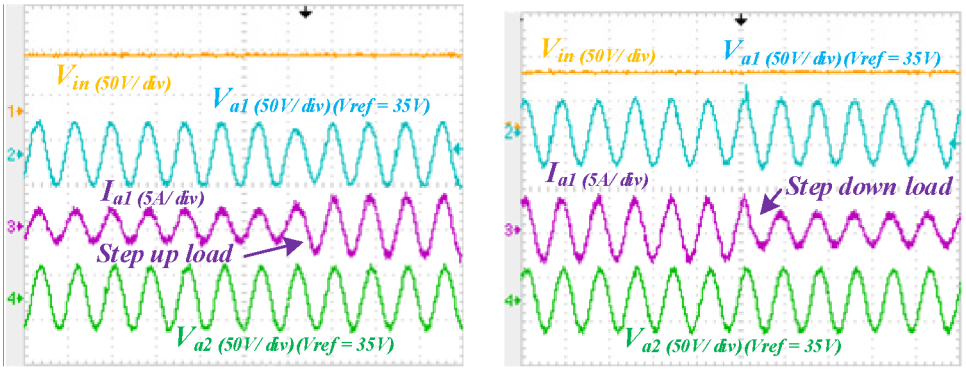
down load change at same V_{ref} = 35 V. As the load resistance changes from 10 to 20 Ω in unit 1, the current decreases from 7 A (peak-peak) to 3.5 A, small transient for very small (negligible) period appears in phase voltage of unit 1 and the phase voltages of unit 2 remain unaffected.

Fig. 15 shows the dynamic behaviour with load change in unit 2 at V_{ref} = 35 V for both units. Figs. 15*a* and *b* show I_{a2} of unit 2, which remains unaffected during the dynamics of phase current (I_{a1}) of unit 1 with step up and step down change in load of unit 1. This show the decoupled behaviour of the two unit.

In Fig. 15*c*, load current increases from 3.5 to 7 A (peak-peak) as the load resistance changed from 20 to 10 Ω. V_{a1} of unit 1 remain unaffected. The phase voltage of unit 2 slightly decreases but is restored within one cycle. Similarly, Fig. 15*d* shows V_{in}, V_{a1} of both units, and phase *a* current of unit 2 the load for step down load change in unit 2. The current decreases from 7 A (peak-peak) to 3.5 A as the corresponding load resistance changed from 10 to 20 Ω, but V_{a1} of unit 1 and unit 2 remains unaltered. This indicates the good dynamic behaviour and stable closed-loop operation of the proposed topology.

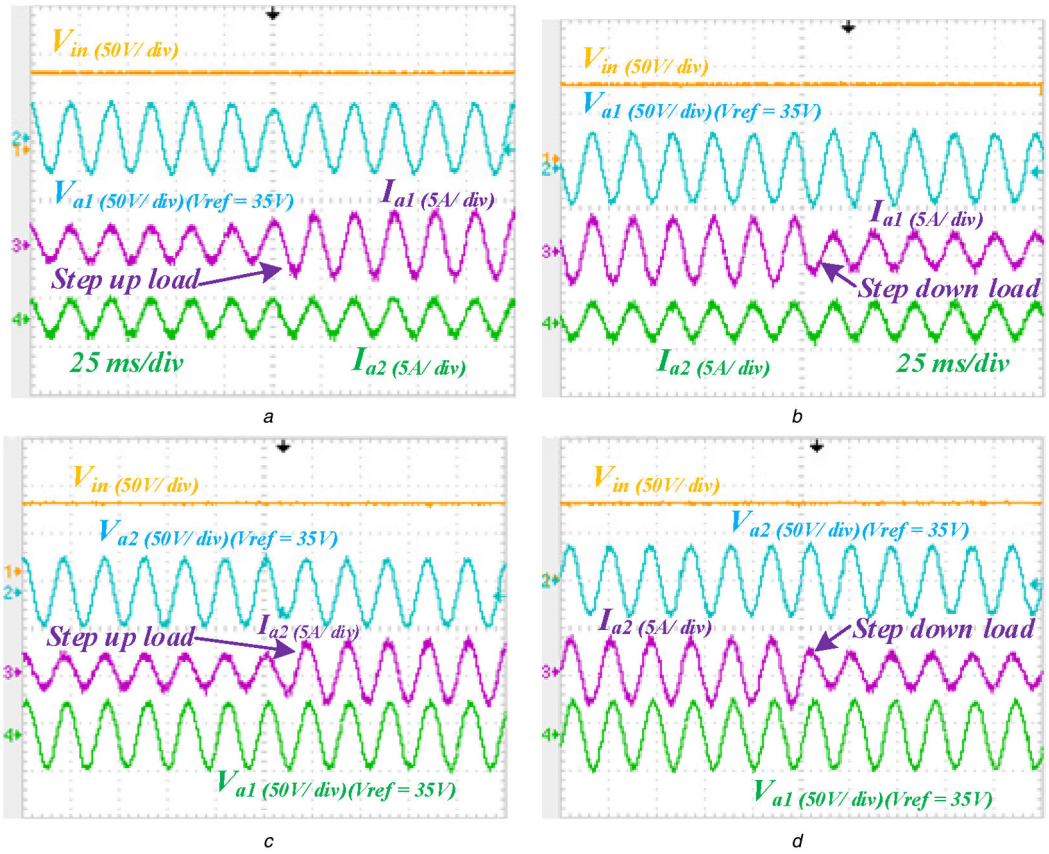
4.5 Dynamic response of proposed parallel mode inverter with different reference voltages

Figs. 16 and 17 show the dynamic response of proposed parallel mode topology when both units have different reference voltages, i.e. V_{ref} = 35 V for unit 1 and V_{ref} = 30 V for unit 2. Figs. 16*a* and *b* show the dynamics in V_{in}, V_{a1} (phase voltage), I_{a1} (phase current of inverter unit 1) with step up and step down load change in unit 1. In Fig. 16*a*, current increases from 3.5 to 7 A (peak-peak) for load resistance changed from 20 to 10 Ω. In Fig. 16*b*, current decreases from 7 to 3.5 A (peak-peak) as the load resistance changed from 10 to 20 Ω but the V_{a2} remains constant at 60 V (peak-peak). The voltage of other unit changes slightly for very small period and is



a b

Fig. 14 *Dynamic response of proposed topology during parallel operation at same reference voltages with load change in unit 1*
(a), ***(b)*** Step up & step down dynamics with unit 2 at V_{ref} = 35 V



a b c d

Fig. 15 *Dynamic response of proposed topology during parallel operation at same reference voltages with load change*
(a), ***(b)*** I_{a2} of unit 2 with step up and step down load dynamics in unit 1 at V_{ref} = 35 V, ***(c)*** V_{in}, V_{a2}, I_{a2} of inverter unit 2 and V_{a1} of inverter unit 1 at V_{ref} = 35 V with step up load change in unit 2, ***(d)*** V_{in}, V_{a2}, I_{a2} of inverter unit 2 and I_{a1} of inverter unit 1 at V_{ref} = 35 V with step down load change in unit 2

restored within one cycle, thus ensuring good dynamic response of the system.

Figs. 17*a* and *b* show the dynamics with same step down and step up load change in unit 2. In Fig. 17*a,* the load resistance is increased from 10 to 20 Ω and in Fig. 17*b*, the load resistance is decreased from 20 to 10 Ω. With load change in unit 2, the voltages of other unit (unit 1) remains unchanged. The the voltages of other unit (unit 1) remains unchanged. The voltages of unit 2 is slightly changed but restored within one cycle. This shows the good dynamic response of the system with different voltage references for two units.

4.6 Series mode of the proposed inverter

The proposed series mode multi ac qZSI is also operated with V_{in} = 100 V and D = 0.3. The reference voltage (V_{ref}) for both the inverter units is 35 V. The responses for proposed topology are shown in Fig. 18. Fig. 18*a* shows input voltage, voltage across capacitor C_1 (V_{c1}), voltage across C_2 (V_{c2}) and diode voltage (V_D = 250 V) in the impedance network of the proposed qZSI. The value of V_{c1} = 75 V and V_{c2} = 175 V are same as the theoretical values obtained from (13). It is observed that the diode is forward biased during power interval and reverse biased in ST interval. Figs. 18*b* and *c* show input voltage and phase voltages of all three phases of inverter units 1 and 2, respectively. The magnitude of all the three voltages is 70 V (peak-peak), which is equal to the theoretical values.

Fig. 19*a* shows input voltage, phase *a* voltage, phase *a* current of inverter unit 1 and phase *a* voltage of unit 2. The peak-peak phase voltage of both units is 70 V and current is 3.5 A (peak-peak), which is equal to their theoretical counterparts. Fig. 19*b* shows the phase *a* voltage, phase *a* current of unit 1 and phase *a* voltage, phase *a* current of unit 2. Phase voltage (V_{a1}), phase current (I_{a1}) of unit 1 and V_{a2}, I_{a2} of unit 2 have same amplitude and phase angle. Therefore, the power of unit 1 and power of unit 2 are equal.

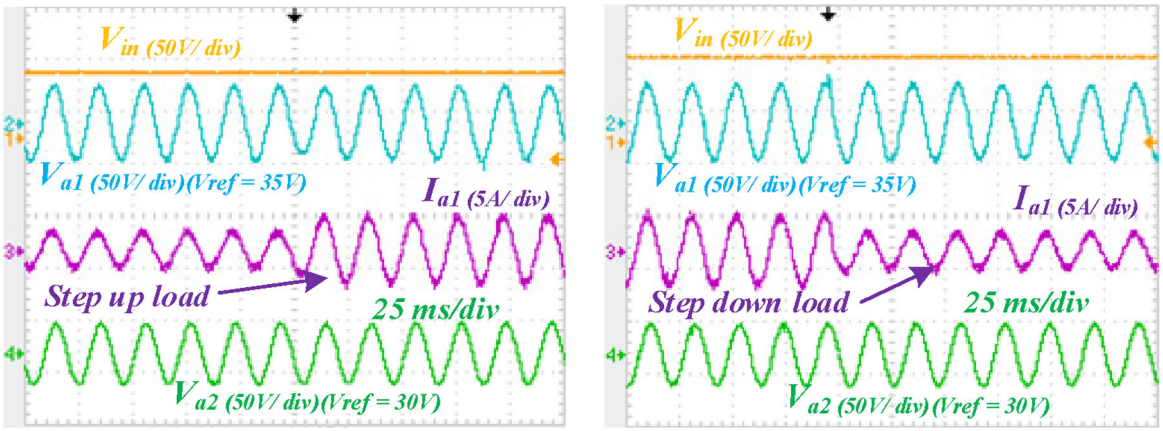


Fig. 16 *Dynamic response of proposed topology during parallel operation at different reference voltage with load change in unit 1*
(a), (b) Step up and step down dynamics while inverter unit 1 is at $V_{ref} = 35$ V and unit 2 at $V_{ref} = 30$ V

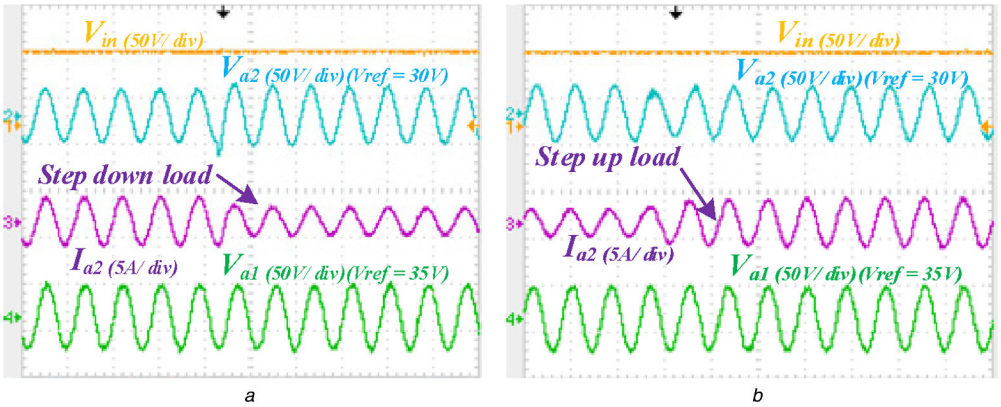


Fig. 17 *Step up and step down dynamic response of proposed Parallel mode inverter with different reference voltages*
(a), (b) Step down and step up dynamics with V_{ref} of inverter unit 1 at 30 V and unit 2 at 35 V, respectively

4.7 Dynamic response of proposed series mode inverter

Fig. 20 shows the dynamic behaviour during series operation with input voltage $V_{in} = 100$ V, load resistance = 20 Ω and $D = 0.3$, where reference voltage (V_{ref}) of both the units are varied w.r.t. time. Fig. 20*a* shows the response, when V_{ref} is decreased from 35 to 25 V. The peak-peak voltages of phase *a* of both units change from 70 to 50 V, consequently the phase *a* peak-peak current changes from 3.5 to 2.5 A. Similarly, Fig. 20*b* shows the response, where V_{ref} is increased from 25 to 35 V. The phase voltages of both units tracks the reference voltage and become equal to 35 V, and the current become 3.5 A accordingly. The system settles to new reference value in very small time (i.e. within two cycles), showing good dynamic behaviour of the series mode proposed inverter with closed loop control.

4.8 Efficiency analysis of proposed converter

Fig. 21 shows the results for the topology with two output units for same input voltage ($V_{in} = 100$ V), same ST duty ratio (D) same three-phase output voltage (35 V Peak / 24.75 V rms) and same load (Load resistance 15.32 Ω for peak load operation) for both parallel and series mode of operation. The peak power for the designed prototype is 240 W. Based on the values of the input and output voltages and currents of the results, the efficiencies for both modes of operation are calculated. Figs. 21*a* and *b* show the input and output voltages and currents for parallel mode of operation. Figs. 21*c* and *d* show the input and output voltages and currents for series modes of operation. The output power is 240 W ($3 \times V_{rms} \times I_{rms} \times 2$) for both mode of operation. Input currents (I_{in}) for these conditions for parallel and series mode are 2.65 and 2.59 A, respectively. Thus input power P_{in} ($V_{in} \times I_{in}$) for parallel and series mode is 265 and 259 W, respectively. The power efficiency (i.e. $\eta = P_{(3-\varnothing)out}/P_{in} \times 100$) of the proposed converter for parallel and series mode are equal to 90.6 and 92.45%, respectively. It may be observed that the input current in parallel mode (2.65 A) is more than that of the series mode (2.59 A). It is because currents of two units are added in parallel mode unlike series mode where currents are not added. Thus, the efficiency in series mode of operation is more than that of parallel mode.

Fig. 22 shows the variation of efficiency with ST duty ratio (D) and load for parallel and series mode of operation with peak load (240 W output) operation. It is observed that the efficiency for that series mode operation is more than that of parallel operation as already discussed above. For Fig. 22*a*, it is clear that the efficiency in both mode decreases as the ST duty ratio (D) is increased. Furthermore, form Fig. 22*b* the efficiency in both mode decreases as the load resistance is increased, i.e. load is increased.

5 Conclusion

This paper proposes two topologies of 3-ϕ multi ac output qZSI with parallel mode and series mode. The proposed inverters are capable of supplying n-number of controlled ac voltage outputs simultaneously. The inverter topology with n-parallel connected 3-ϕ inverters gives a parallel mode of the proposed inverter that is capable of giving n numbers of different ac output voltages and different load currents. The series mode of the proposed inverter gives n number of ac outputs with same outputs voltages and load currents. The proposed multi ac 3-ϕ qZSIs are capable of supplying more than one ac load demand without connecting additional regulator or adaptor. The switching signals for the inverters are generated using hybrid modulation technique, i.e. SPWM with constant frequency ST signals. As the proposed inverters are based on impedance source inverters, they inherit the advantages such as inherent ST protection and both buck-boost output capability. The output power from these inverters can be fed

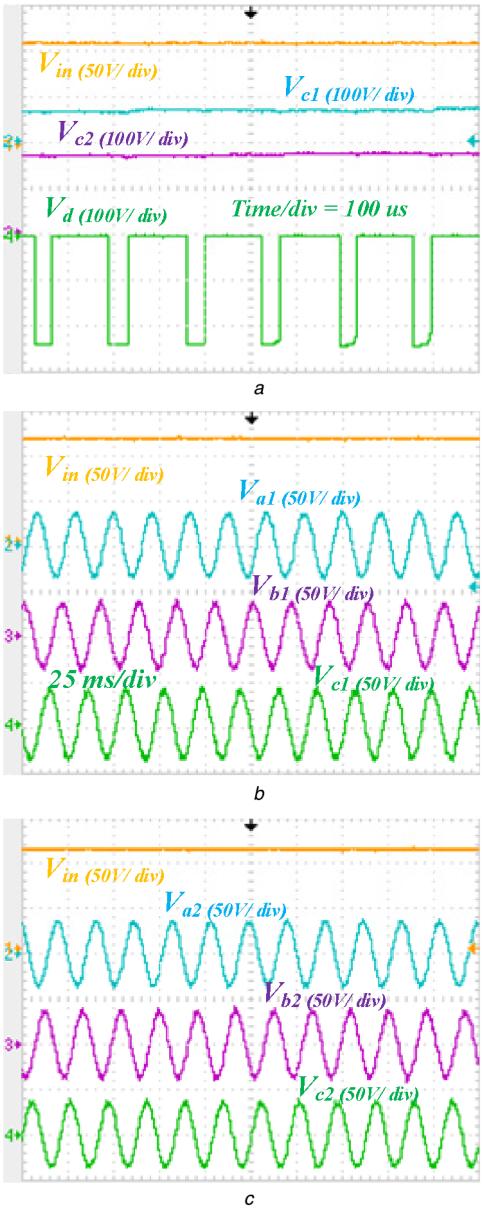


Fig. 18 *Steady-state response of proposed topology during series operation*
(a) V_{in}, capacitor voltage V_{c1} & V_{c2} and voltage switching waveform of the diode (V_d), ***(b), (c)*** V_{in}, 3-ϕ voltages of inverter unit 1 & 2 at V_{ref} = 35 V

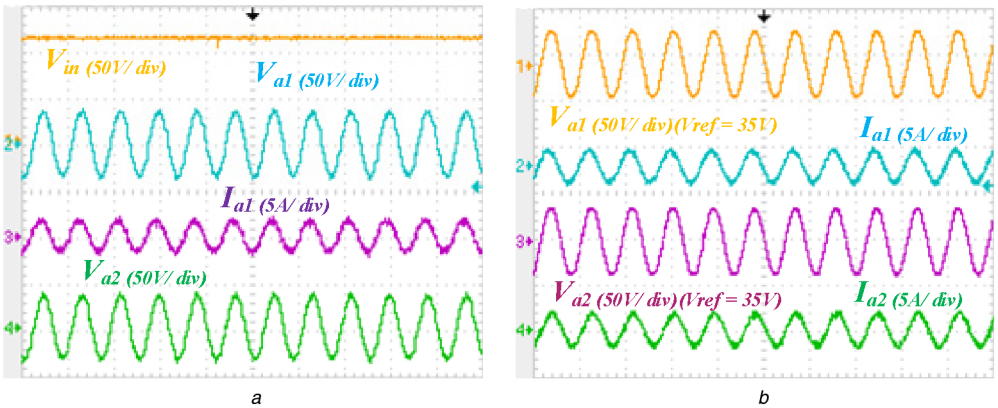


Fig. 19 *Steady state response of proposed topology during series operation*
(a) V_{in}, V_{a1} (phase voltage), I_{a1} (phase current of inverter unit 1) and V_{a2} (phase voltage of inverter unit 2), ***(b)*** V_{a1} (phase voltage), I_{a1}(phase current of inverter unit 1) and V_{a2} (phase voltage) I_{a2} (phase current of inverter unit 2) at V_{ref} = 35 V

into the microgrid and can be used for a residential 3-ϕ load. Detailed mathematical modelling, steady-state as well dynamic analyses are carried out in order to bring out the properties of the proposed inverters. A 240 W laboratory prototype has been developed to verify the performance of the proposed 3-ϕ multi ac qZSIs.

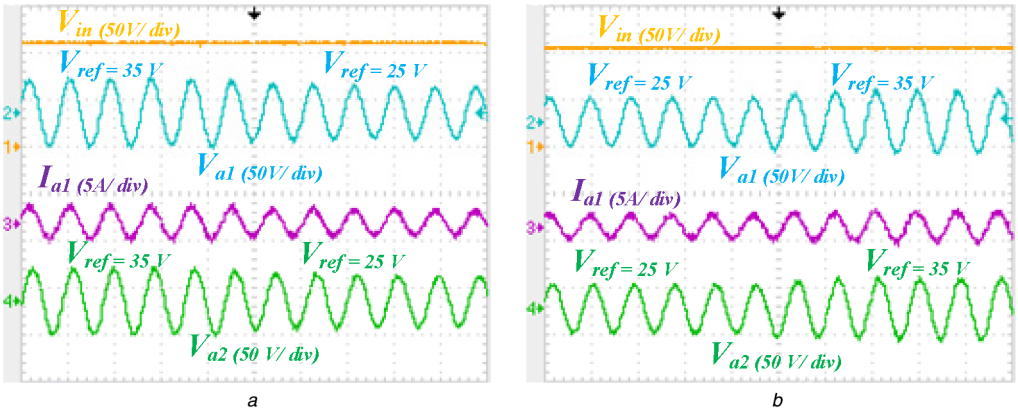


Fig. 20 *Dynamic response of proposed series mode inverter*
(a), (b) Dynamics during series operation for increase and decrease in voltage reference, respectively

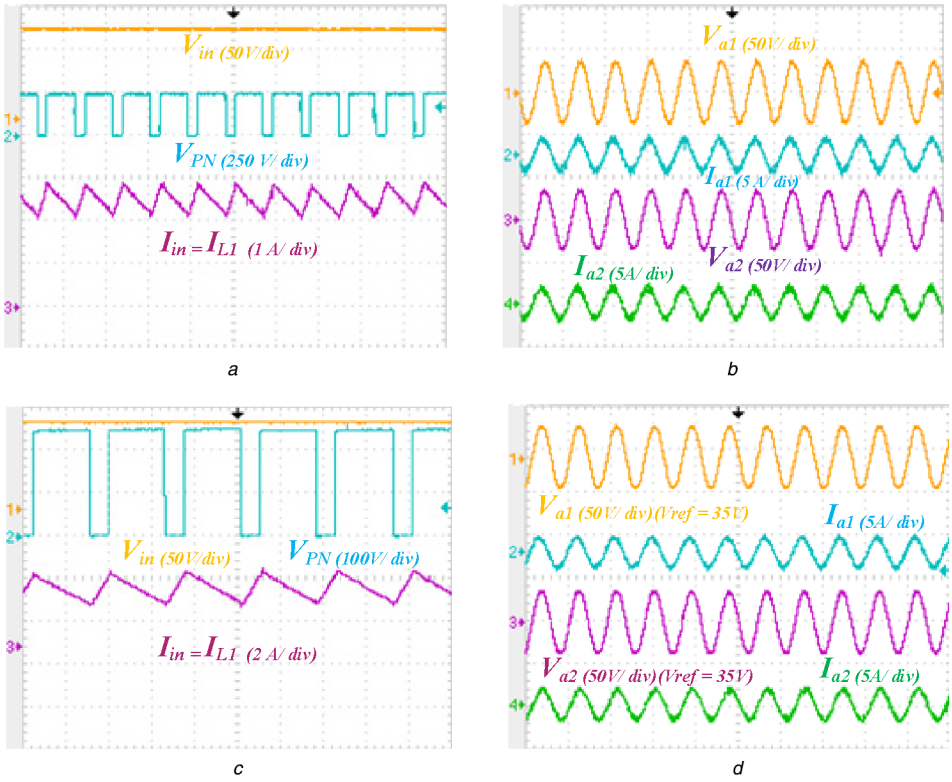


Fig. 21 *Steady state response of proposed topology during parallel and series mode operation for equal Vref for both units*
(a) Input voltage V_{in}, switch node voltage (V_{PN}) and input current $I_{in} = I_{L1}$, ***(b)*** V_{a1} (phase voltage), I_{a1} (phase current of inverter unit 1) and V_{a2} (phase voltage) I_{a2} (phase current of inverter unit 2) at $V_{ref} = 35$ V in parallel mode of inverter unit 1 & 2, ***(c)*** Input voltage V_{in}, switch node voltage (V_{PN}) and input current $I_{in} = I_{L1}$, ***(d)*** V_{a1} (phase voltage), I_{a1} (phase current of inverter unit 1) and V_{a2} (phase voltage) I_{a2} (phase current of inverter unit 2) at $V_{ref} = 35$ V in series mode of inverter unit 1 & 2

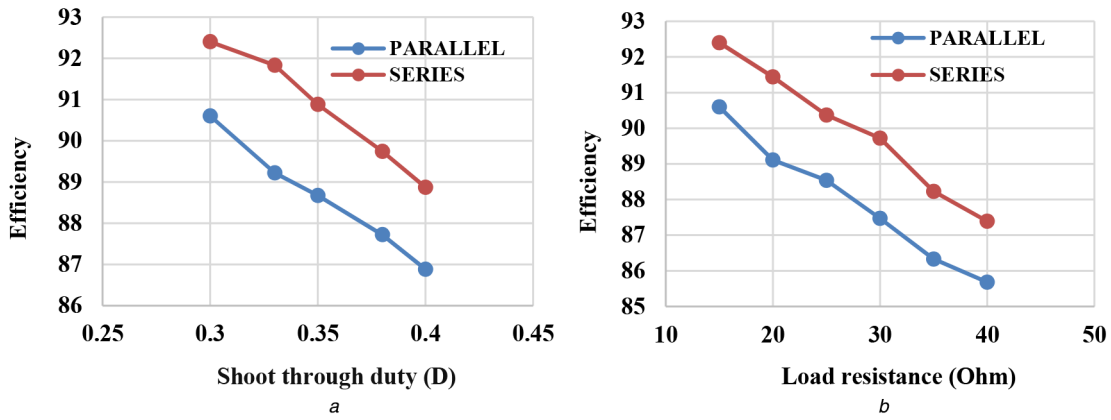


Fig. 22 *Efficiency curve for peak load (240 W output) in parallel and series mode*
(a) Efficiency versus ST duty ratio (D), ***(b)*** Efficiency versus load resistance

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