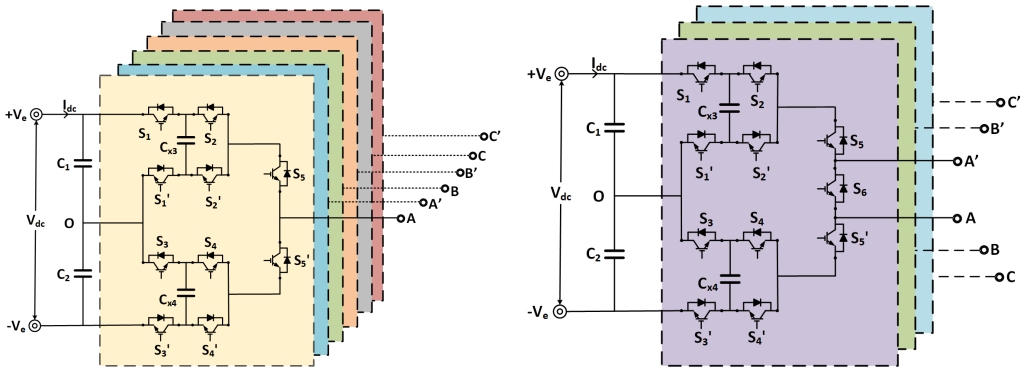
Chapter 4

Design of a Novel Five-Level Stacked Dual-Output Converter

4.1 Introduction

The output voltage quality and total harmonic distortion (THD) of a three-level converter can be further improved by considering a five-level converter. With the increase in the number of levels, the component count increases; therefore, the converter level is decided based on the application and efficiency requirement. A five-level converter provides lower voltage stress, dv/dt across power devices, enhancing reliability. The reduced dv/dt leads to less electromagnetic interference (EMI) and improved motor life. Additionally, switching losses are reduced as a result of lower voltage steps. consider the comparison between a conventional three-level NPC (3L-NPC) inverter and a five-level NPC (5L-NPC) inverter. For the same switching frequency (2 kHZ) and load conditions, the 3L-NPC inverter typically produces a phase voltage total harmonic distortion (THD) of around 69.09%, whereas the 5L-NPC inverter reduces the THD to approximately 27.10%, resulting in a reduction of more than 50%. Similarly, the dv/dt stress on the load terminals decreases with increased voltage levels due to smaller voltage steps between consecutive levels. For the 3L-NPC, the voltage step is approximately $V_{dc}/2$, while for the 5L-NPC, it is reduced to $V_{dc}/4$, effectively achieving a reduction of about 50% in voltage slew rate. A conventional five-level stacked MLI (CFLS-MLI) simultaneously supplying either a single six-phase load or two three-phase loads is shown in Fig. 4.1 [61]. The authors proposed a three-leg stacked dual-output five-level (TL-SDOFL) converter shown in Fig. 4.1(b), in [73]. It reduces the switch count by 45% (60 to 33) and capacitors by 42.85% (14 to 8) compared



(a) (b)

FIGURE 4.1: (a) Five-level stacked converter for six phase [61]. (b) Three-leg stacked dual-output five-level (TL-SDOFL) converter [73].

to the CFSL-MLI. However, the TL-SDOFL has limitations in its region of operation, thus lacking independent control.

This chapter builds on [73] to develop a novel five-level stacked dual output (FLSDO) converter. It has a complete region of operation, improved redundancy, and increased DC-link utilization compared to TL-SDOFL, with a slight increase in the number of switches (five per leg). The FLSDO converter eliminates the $v_{ref1} \geq v_{ref2}$ limitation of TL-SDOFL by providing a complete region of operation with increased switching states for redundancy. Thus, FLSDO offers all the voltage states of a conventional stacked five-level inverter supplying two loads, reducing the number of switches by four per leg and the number of flying capacitors by two.

The FLSDO can drive a single six-phase load or two three-phase motors simultaneously with the same capabilities as the conventional five-level inverter. The output voltages can be independently controlled regardless of amplitude, frequency, and phase angle (phase difference).

4.2 Five-Level Stacked Dual Output (FLSDO) Converter

4.2.1 Topology of FLSDO

The proposed five-level stacked dual output (FLSDO) converter supplying a six-phase load is shown in Fig. 4.2. The converter consists of 48 semiconductor switches, two DC-link capacitors, and six flying capacitors. The converter is symmetrical across the flying

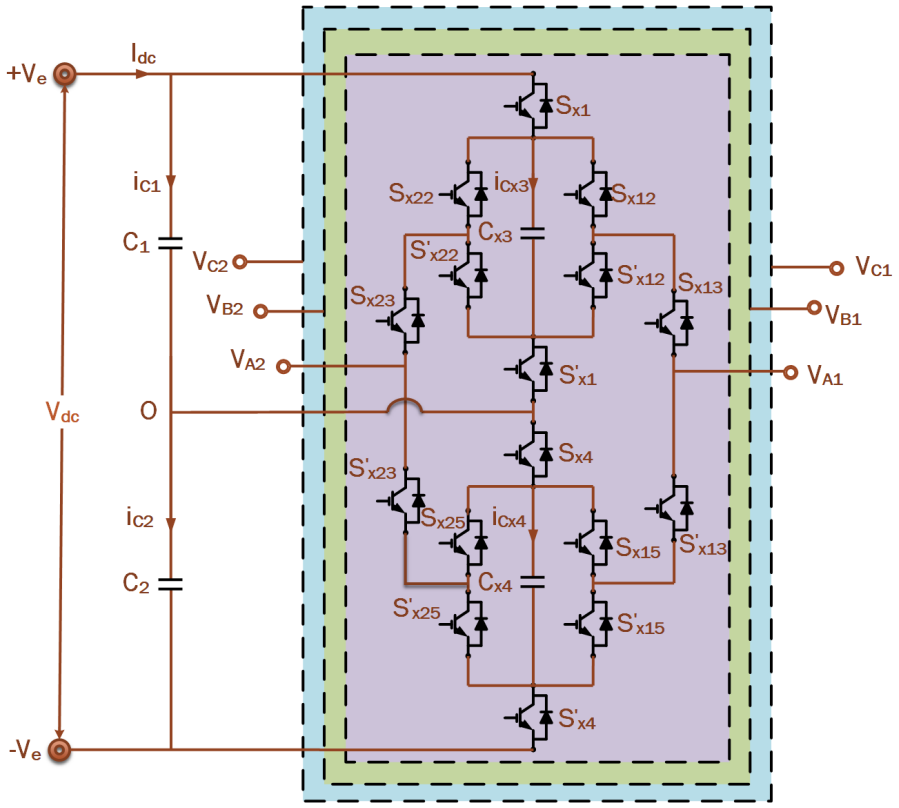


FIGURE 4.2: Proposed five-level stacked dual output (FLSDO) converter.

capacitors (FCs) charged to "$V_{DC}/4$", parallel to two loads with four selector switches. It can drive two three-phase loads simultaneously. It has four fewer switches per leg than a conventional stacked MLI required to drive two loads simultaneously. The proposed converter has two outputs per leg. The first output has S_{x12}, S'_{x12}, S_{x15}, and S'_{x15} as selector switches and S_{x13} and S'_{x13} controlling first output terminal i.e., V_{x1}. Similarly, the second output has S_{x22}, S'_{x22}, S_{x25}, and S'_{x25} as selector switches, and S_{x23} and S'_{x23} controlling second output terminal i.e., V_{x2}. Switches S_{x1}, S'_{x1}, S_{x4} and S'_{x4} are shared between two outputs, here $x \in \{\text{A, B, and C}\}$.

The output voltages v_{x1} and v_{x2} are the two distinct voltages obtained from the combination of these switches and are defined as the phase voltages. Since the phases are independent, the topology can also be adapted to any number of phases. The currents i_{x1} and i_{x2} are corresponding output load currents. The input DC-link voltage is V_{dc} across the series connection of capacitors C_1 and C_2.

TABLE 4.1: Comparison of the five-level inverter (per leg) for the dual output configuration

Topologies	DFC-ANPC[61, 74, 75]	TL-SDOFL[73]	Dual 5L-ANPC [76]	Dual 5L-NPC [77]	FLSDO
No. of Switches	20	11	16	16	16
No. of diodes	0	0	0	12	0
Total Devices (active + passive)	20	11	16	28	16
No. of DC-link Capacitors	2	2	2	4	2
Maximum voltage stress	$V_{dc}/2$	V_{dc}	$V_{dc}/2$	$V_{dc}/4$	V_{dc}
Boundary Region					

Table 4.1 lists the number of switches, devices, and operating regions of FLSDO with five-level dual-output topologies. Compared to other topologies, FLSDO provides advantages in terms of cost and volume and has zero clamping diodes.

4.2.2 Operation of FLSDO

The output voltage levels of the FLSDO converter are -V_{dc}/2, -V_{dc}/4, 0, V_{dc}/4 and V_{dc}/2. The two *R-L* loads are connected across the V_{x1}, V_{x2} and O. For the single leg of the FLSDO topology, few switching states are shown in Fig. 4.3(a)–(c) and are described as follows.

4.2.2.1 State of Operation 1

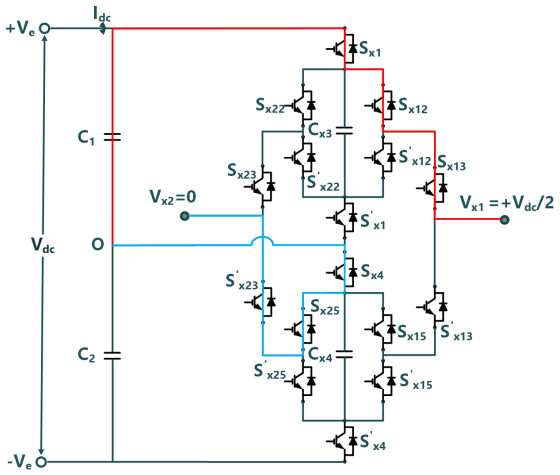
Switches S_{x1}, S_{x12}, S_{x13}, S'_{x23}, S_{x25} and S_{x4} are in the ON state. Fig. 4.3(a) shows the current flow between the DC-link and the output loads. At this time, the output voltages V_{x1} and V_{x2} are V_{dc}/2 and 0. During this state, C_1 discharges, and C_2 maintains the previous voltage.

4.2.2.2 State of Operation 2

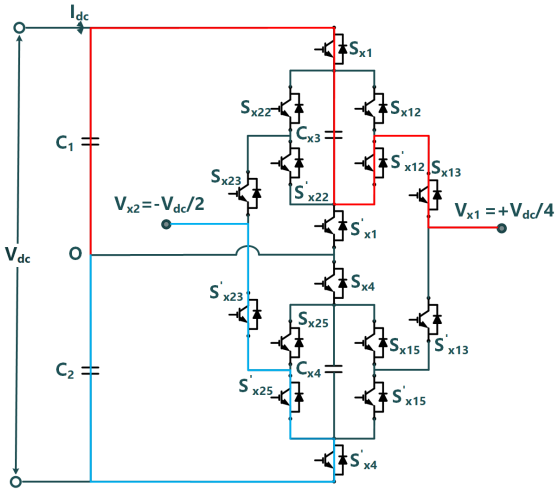
Switches S_{x1}, S'_{x12}, S_{x13}, S'_{x23}, S'_{x25} and S'_{x4} are in the ON state. The current flow between the DC-link to the loads is shown in Fig. 4.3(b). At this time, the output voltages V_{x1} and V_{x2} are +V_{dc}/4 and -V_{dc}/2. During this state, C_1 discharges and C_2 charges.

4.2.2.3 State of Operation 3

Switches S'_{x13}, S'_{x15}, S_{x4}, S'_{x23} and S_{x25} are in the ON state. The current flow between the DC-link to the loads is shown in Fig. 4.3(c). At this time, the output voltages V_{x1} and V_{x2} are -V_{dc}/4 and 0. During this state, C_1 and C_2 maintains the previous voltage.



(a)



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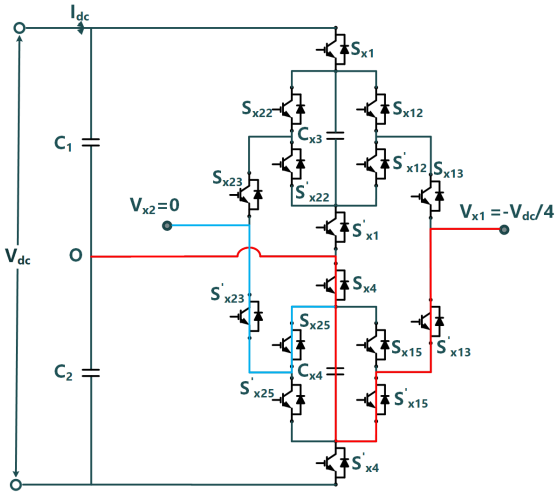


FIGURE 4.3: Few operating states of the proposed FLSDO (a) V_{x1}= $V_{dc}/2$ and V_{x2}= 0 (b) V_{x1}= +$V_{dc}/4$ and V_{x2}= -$V_{dc}/2$ (c) V_{x1}= -$V_{dc}/4$ and V_{x2}= 0.

TABLE 4.2: FLSDO Switching States, Corresponding Output Voltages and DC-link Capacitor Charging State

S.No.	Switching Signals	Output Voltages (V_{dc})		Capacitor state ($i_{x1} > 0$), ($i_{x2} > 0$)		Count
	Decimal of [S_{x1} S_{x12} S_{x22} S_{x13} S_{x23} S_{x4} S_{x15} S_{x25}]	v_{x1}	v_{x2}	C_1	C_2	
1	224, 160, 128, 96, 32, 64, 0, 192	-0.5	-0.5	NA	↑	8
2	225, 161, 129, 97, 33, 65, 1, 193	-0.5	-0.25	NA	↑	8
3	8, 9, 72, 73	-0.5	0	NA	↑	4
4	(40, 41, 104, 105), (136, 137, 200, 201)	-0.5	+0.25	(NA), (↓)	(↑), (↑)	8
5	168, 169, 232, 233	-0.5	+0.5	↓	↑	4
6	226, 162, 130, 98, 34, 66, 2, 194	-0.25	-0.5	NA	↑	8
7	(228, 164, 132, 100, 36, 68, 4, 196), (227, 163, 131, 99, 35, 67, 3, 195)	-0.25	-0.25	(NA), (NA)	(NA), (↑)	16
8	(229, 165, 133, 101, 37, 69, 5, 197), (12, 13, 76, 77), (10, 11, 74, 75)	-0.25	0	(NA), (NA), (NA)	(NA),(NA), (↑)	16
9	(44, 45, 108, 109), (140, 141, 204, 205), (42, 43, 106, 107), (138, 139, 202, 203)	-0.25	+0.25	(NA), (↓), (NA), (↓)	(NA), (NA), (↑), (↑)	16
10	(172, 173, 236, 237), (170, 171, 234, 235)	-0.25	0.5	(↓), (↓)	(NA), (↑)	8
11	16, 18, 48, 50	0	-0.5	NA	↑	4
12	(230, 166, 134, 102, 38, 70, 6, 198), (20, 22, 52, 54), (17, 19, 49, 51)	0	-0.25	(NA), (NA), (NA)	(NA), (NA), (↑)	16
13	(231, 167, 135, 103, 39, 71, 7, 199), (14, 15, 78, 79), (24, 25, 26, 27, 28, 29, 30, 31), (21, 23, 53, 55)	0	0	(NA), (NA), (NA), (NA)	(NA), (NA), (NA), (NA)	24
14	(46, 47, 110, 111), (142, 143, 206, 207), (56, 57, 58, 59, 60, 61, 62, 63)	0	+0.25	(NA), (↓), (NA)	(NA), (NA), (NA)	16
15	174, 175, 238, 239	0	0.5	↓	NA	4
16	(80, 82, 112, 114), (144, 146, 176, 178)	0.25	-0.5	(NA), (↓)	(↑), (↑)	8
17	(145, 147, 177, 179), (148, 150, 180, 182), (81, 83, 113, 115), (84, 86, 116, 118)	0.25	-0.25	(↓), (↓), (NA), (NA)	(↑), (NA), (↑), (NA)	16
18	(149, 151, 181, 183), (88, 89, 90, 91, 92, 93, 94, 95), (85, 87, 117, 119)	0.25	0	(↓), (NA), (NA)	(NA), (NA), (NA)	16
19	(120, 121, 122, 123, 124, 125, 126, 127), (152, 153, 154, 155, 156, 157, 158, 159)	0.25	+0.25	(NA), (↓)	(NA), (NA)	16
20	184, 185, 186, 187, 188, 189, 190, 191	0.25	0.5	↓	NA	8
21	208, 210, 240, 242	0.5	-0.5	↓	↑	4
22	(209, 211, 241, 243), (212, 214, 244, 246)	0.5	-0.25	(↓), (↓)	(↑), (NA)	8
23	213, 215, 245, 247	0.5	0	↓	NA	4
24	216, 217, 218, 219, 220, 221, 222, 223	0.5	+0.25	↓	NA	8
25	248, 249, 250, 251, 252, 253, 254, 255	0.5	0.5	↓	NA	8
Total						256

↑ is for charging, ↓ is for discharging state and NA = Not Affected. S'_{x1}, S'_{x12}, S'_{x22}, S'_{x13}, S'_{x23}, S'_{x4}, S'_{x15}, S'_{x25} are switched complementary to S_{x1}, S_{x12}, S_{x22}, S_{x13}, S_{x23}, S_{x4}, S_{x15}, S_{x25} respectively.

It can be seen that the maximum blocking voltage of the switch in FLSDO is V_{dc}. Table 4.2 presents all the switching combinations of the FLSDO converter along with the corresponding output voltages and capacitor states. For conciseness, the switching states are presented in decimal format. The states can be converted to binary to obtain the switching signal, e.g., state $(28)_{10}$ is equivalent to $(00011100)_2$ where each bit corresponds to S_{x1}, S_{x12}, S_{x22}, S_{x13}, S_{x23}, S_{x4}, S_{x15} and S_{x25} respectively. The converter has 256 valid switching states, of which 231 are redundant. The count column indicates the number of times each specific output voltage combination can be achieved using different possible switching signals. The available redundant states are used to lower the average switching frequency, reduce dynamic power losses, and balance the DC-link and flying capacitors. Redundant switching states provide alternative pathways for current flow, which is critical in the event of a fault. By having multiple valid states for the same output voltage level, the converter can continue to operate even if certain switches or paths fail. This ensures continuous operation and reduces downtime. Moreover, having two different voltage levels at each output enables the converter to operate at different frequency (DF) and common frequency (CF) modes for both outputs.

In a three-phase, five-level stacked dual output (FLSDO) converter, there are two DC-link capacitors (C_1 and C_2) and six flying capacitors. The top capacitors (C_1 and C_{x3}) provide positive voltage levels, and the bottom capacitors (C_2 and C_{x4}) provide negative voltage levels. The voltage deviations of the capacitors of C_1, C_2, C_{x3} and C_{x4} occur due to charging and discharging. As shown in Table 4.2 and Fig. 4.2, any deviation in the voltages across these capacitors can result in an imbalance in the output voltage, which adversely affects the overall performance of the converter. Table 4.2 outlines the charging, discharging, or bypass conditions of DC-link capacitors based on the current directions ($i_{x1} > 0$, $i_{x2} > 0$) and the corresponding switching states. The designed PWM technique utilizes switching redundancies to balance capacitors. The FLSDO converter features multiple redundant switching combinations that can generate the same output voltage, each with a unique impact on the capacitor voltages. By carefully selecting the appropriate switching states according to the current operating conditions and the capacitor voltages, the converter can dynamically manage the charge distribution across the capacitors. This dynamic management is essential for maintaining balanced capacitor voltages. Let ΔV_{C1}, ΔV_{C2}, ΔV_{Cx3} and ΔV_{Cx4} represent the DC-link and flying capacitors voltage ripple respectively. $V_{C1} = V_{dc}/2 + \Delta V_{C1}$, $V_{C2} = V_{dc}/2 + \Delta V_{C2}$, $V_{Cx3} = V_{dc}/4 + \Delta V_{Cx3}$ and $V_{Cx4} = V_{dc}/4 + \Delta V_{Cx4}$. The sum of V_{C1} and V_{C2} is V_{dc} and $\Delta V_{C2} = -\Delta V_{C1}$. The capacitor currents through C_1, C_2, C_{x3} and C_{x4} are i_{C1}, i_{C2}, i_{Cx3} and i_{Cx4}

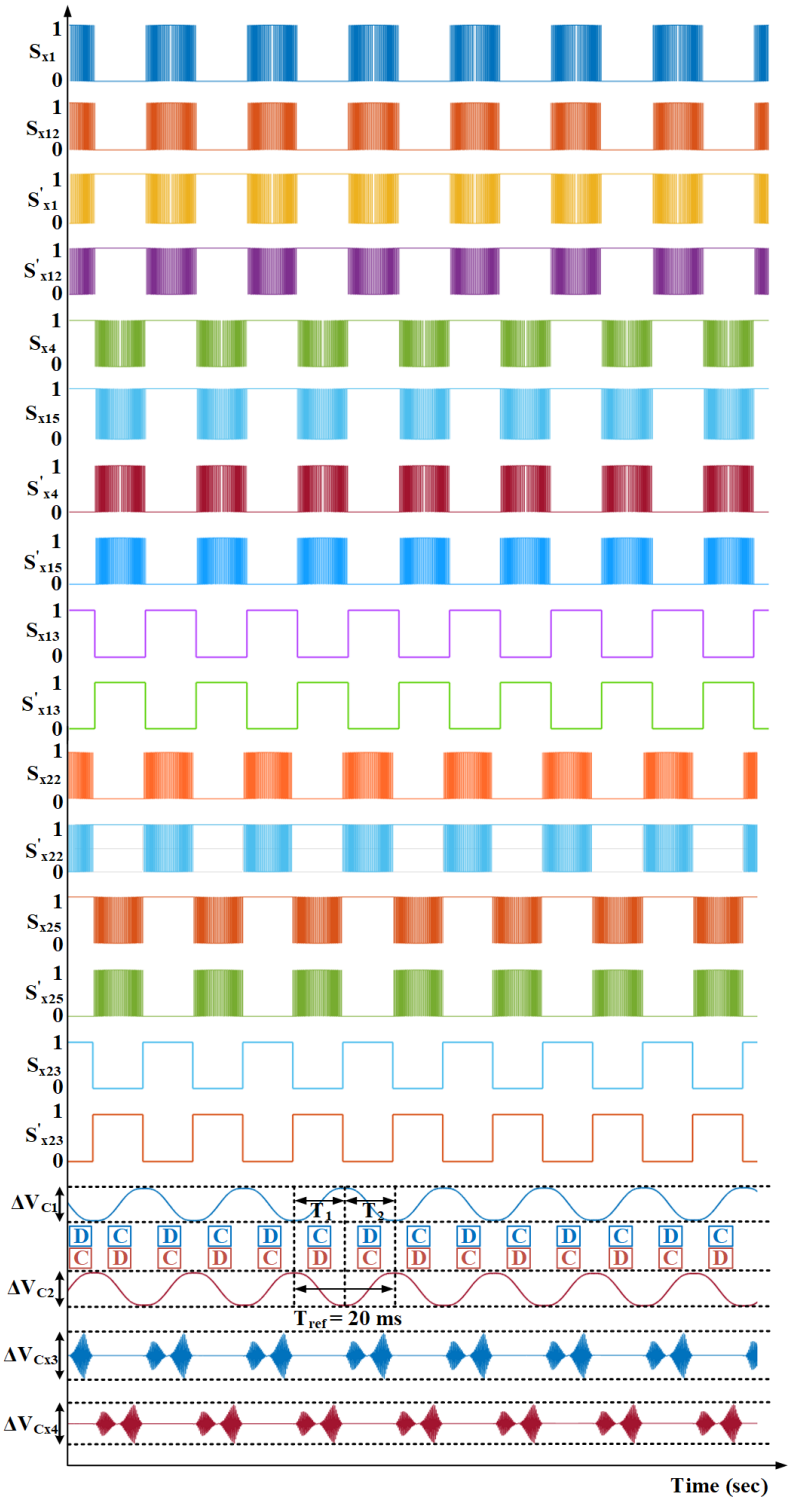


FIGURE 4.4: Voltage balancing of DC-link and flying capacitors C_1, C_2, C_{x3} and C_{x4} in the FLSDO converter over a few cycles through the proposed PWM with $m_1 = m_2 = 1$, $f_1 = f_2 = 50$ Hz.

respectively. The DC-link and flying capacitor currents can be written in terms of the load currents and the switching signals as follows:

Table 4.2 outlines the charging, discharging, or bypass conditions of DC-link capacitors based on the current directions ($i_{x1} > 0$, $i_{x2} > 0$) and the corresponding switching states. The designed PWM technique utilizes switching redundancies to balance capacitors. The FLSDO converter features multiple redundant switching combinations that can generate the same output voltage, each with a unique impact on the capacitor voltages. By carefully selecting the appropriate switching states according to the current operating conditions and the capacitor voltages, the converter can dynamically manage the charge distribution across the capacitors. This dynamic management is essential for maintaining balanced capacitor voltages. Let ΔV_{C1}, ΔV_{C2}, ΔV_{Cx3} and ΔV_{Cx4} represent the DC-link and flying capacitors voltage ripple respectively. $V_{C1} = V_{dc}/2 + \Delta V_{C1}$, $V_{C2} = V_{dc}/2 + \Delta V_{C2}$, $V_{Cx3} = V_{dc}/4 + \Delta V_{Cx3}$ and $V_{Cx4} = V_{dc}/4 + \Delta V_{Cx4}$. The sum of V_{C1} and V_{C2} is V_{dc} and ΔV_{C2} = - ΔV_{C1}. The capacitor currents through C_1, C_2, C_{x3} and C_{x4} are i_{C1}, i_{C2}, i_{Cx3} and i_{Cx4} respectively. The DC-link and flying capacitor currents can be written in terms of the load currents and the switching signals as follows:

$$i_{C1} = -S_{x1}(S_{x13}i_{x1} + S_{x23}i_{x2}) \tag{4.1}$$

$$i_{C2} = S'_{x4}(S'_{x13}i_{x1} + S'_{x23}i_{x2}) \tag{4.2}$$

$$i_{Cx3} = S_{x13}(S_{x1} - S_{x12})i_{x1} + S_{x23}(S_{x1} - S_{x22})i_{x2} \tag{4.3}$$

$$i_{Cx4} = S'_{x13}(S_{x4} - S_{x15})i_{x1} + S'_{x23}(S_{x4} - S_{x25})i_{x2} \tag{4.4}$$

The capacitor voltages depend on the load current as follows:

$$V_{C1} = \frac{1}{C_1}\int_0^t i_{C1}dt + V_{C10} \tag{4.5}$$

$$V_{C1} = -\frac{1}{C_1}\int_0^t (S_{x1}(S_{x13}i_{x1} + S_{x23}i_{x2}))dt \tag{4.6}$$

$$V_{Cx3} = \frac{1}{C_{x3}}\int_0^t i_{Cx3}dt + V_{Cx30} \tag{4.7}$$

$$V_{Cx3} = \frac{1}{C_{x3}}\int_0^t (S_{x13}(S_{x1} - S_{x12})i_{x1} + S_{x23}(S_{x1} - S_{x22})i_{x2})dt \tag{4.8}$$

where V_{C10}, V_{Cx30} are the initial voltages of capacitors C_1, C_{x3} respectively and taking initial value to zero. The equation for C_2, and C_{x4} can be developed in a similar manner.

To achieve balancing, the sum of currents injected or drawn by the capacitors should result in zero net deviation over a switching period. The average current through C_1, C_2, C_{x3} and C_{x4} over a T_{ref} switching period should be zero.

$$\int_0^{T_{ref}} i_{C1}dt = 0, \quad i_{C1} = C_1\frac{dV_{C1}}{dt}$$
$$C_1\int_0^{T_{ref}} \frac{dV_{C1}(t)}{dt}dt = 0 \Rightarrow \int_0^{T_{ref}} \Delta V_{C1}(t)dt = 0 \tag{4.9}$$

$$\int_0^{T_{ref}} i_{C2}dt = 0, \quad i_{C2} = C_2\frac{dV_{C2}}{dt}$$
$$C_2\int_0^{T_{ref}} \frac{dV_{C2}(t)}{dt}dt = 0 \Rightarrow \int_0^{T_{ref}} \Delta V_{C2}(t)dt = 0 \tag{4.10}$$

$$V_{C2} = V_{dc} - V_{C1}:$$
$$\int_0^{T_{ref}} d(V_{dc} - V_{C1}(t)) = 0 \Rightarrow -\int_0^{T_{ref}} \Delta V_{C1}(t)dt = 0 \tag{4.11}$$

$$\int_0^{T_{ref}} i_{Cx3}dt = 0, \quad i_{Cx3} = C_{x3}\frac{dV_{Cx3}}{dt}$$
$$C_{x3}\int_0^{T_{ref}} \frac{dV_{Cx3}(t)}{dt}dt = 0 \Rightarrow \int_0^{T_{ref}} \Delta V_{Cx3}(t)dt = 0 \tag{4.12}$$

$$\int_0^{T_{ref}} i_{Cx4}dt = 0, \quad i_{Cx4} = C_{x4}\frac{dV_{Cx4}}{dt}$$
$$C_{x4}\int_0^{T_{ref}} \frac{dV_{Cx4}(t)}{dt}dt = 0 \Rightarrow \int_0^{T_{ref}} \Delta V_{Cx4}(t)dt = 0 \tag{4.13}$$

From (4.9), (4.10), (4.12) and (4.13), the integration of ΔV_{C1}, ΔV_{C2}, ΔV_{Cx3} and ΔV_{Cx4} over a switching period of T_{ref} should be zero for balancing of DC-link and flying capacitors voltage. As it can be observed from Fig. 4.4 that the charging and discharging times for DC-link capacitor are the same, the DC-link capacitor gets balanced over a period of T_{ref}. In the FLSDO topology, the capacitor voltage always remains in a balanced state irrespective of the load type, modulation index, and frequency. Also, the FLSDO topology does not require any complicated methods to balance the capacitor voltages.

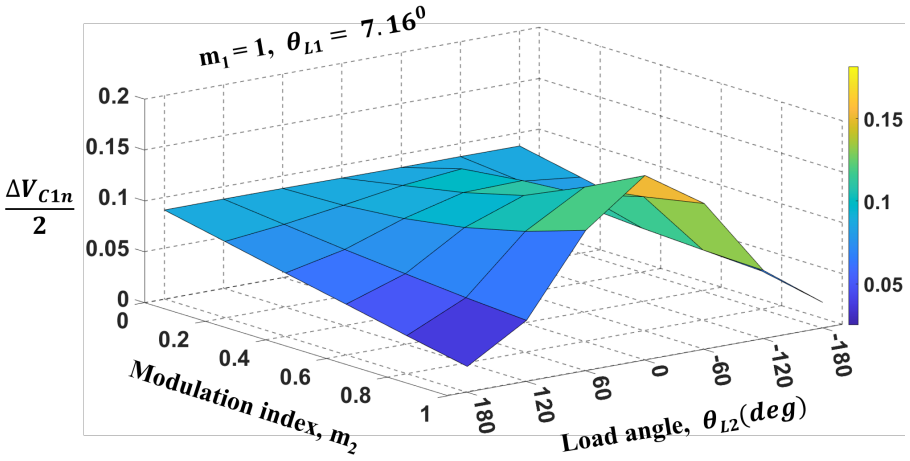
4.2.3 Capacitor Voltage Ripple Analysis

In the following analysis, the DC-link and flying capacitor voltage ripple for phase-A under CF mode is examined with $m_1 = m_2 = 1$ and $f_1 = f_2 = 50$ Hz. Fig. 4.4 shows the gate pulses for the switches using the proposed PWM, as well as the DC-link and flying capacitors voltage ripple, assuming load current flows into the load. The sequences of charging (C) and discharging (D) cause voltage ripple in the DC-link capacitors, and the same applies to the flying capacitors. When switches S_{x13} and S_{x23} are ON, C_1 discharges, reaching V_{C1min}, while C_2 charges, reaching V_{C2max}. Conversely, when switches S_{x13} and S_{x23} are OFF, C_1 charges, reaching V_{C1max}, and C_2 discharges, reaching V_{C2min}. Since the charging and discharging periods are balanced, the DC-link voltage ripple resets in each reference (fundamental or line) cycle. During the discharging period of C_1, the flying capacitor C_{x3} undergoes charge and discharge cycles to balance the voltage. Similarly, during the discharging period of C_2, the flying capacitor C_{x4} charges and discharges, ensuring capacitor voltage balance.

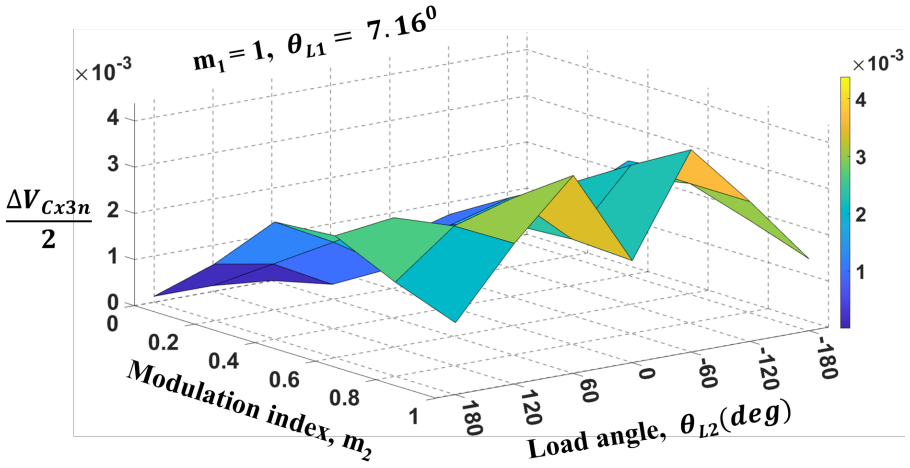
T_1 and T_2 are the charging and discharging time duration respectively and $T_{ref} = T_1 + T_2$. The peak-to-peak value of capacitor voltage ripple ΔV_{C1}, ΔV_{C2}, ΔV_{Cx3} and ΔV_{Cx4} is defined to be the difference between its maximum and minimum value in one fundamental cycle, $\Delta V_{C1} = V_{C1max}$ - V_{C1min}, $\Delta V_{C2} = V_{C2max}$ - V_{C2min}, $\Delta V_{Cx3} = V_{Cx3max}$ - V_{Cx3min} and $\Delta V_{Cx4} = V_{Cx4max}$ - V_{Cx4min}. In the case of Fig. 4.4, ΔV_{C1} = -ΔV_{C2} = 101.5 - 98.5 = 3 V and $\Delta V_{Cx3} = \Delta V_{Cx4}$ = 50.04 - 49.96 = 0.08 V.

The limitation of the capacitor balancing technique can be analyzed through the voltage ripple of the DC-link and flying capacitors under various operating conditions [63, 69]. The capacitor voltage ripple in a power converter is mainly affected by two factors: (a) output power $\propto$ modulation index (m), and (b) phase current angle or AC load angle (θ_L). In the case of a dual output converter, four variables (m_1, m_2, θ_{L1}, θ_{L2}) are required to be considered to operate two loads. Since it consists of large multidimensional data, two variables (m_1 and θ_{L1}) are fixed while the other two are varied within their respective ranges in this evaluation. Converter is operated in CF mode by taking $m_1 = 1$ and $\theta_{L1} = 7.16°$ and by varying m_2 and θ_{L2}. The normalized magnitude of the voltage ripple is used, which may be applied to various applications and operating situations, and the equations are as follows:

$$\frac{\Delta V_{Cin}}{2} = \frac{\Delta V_{Ci}}{2} \Big/ \frac{I_{RMS}}{fC_i}, i = 1, 2, x3, x4 \tag{4.14}$$



(a)



(b)

FIGURE 4.5: Normalized capacitor voltage ripple of the FLSDO converter under CF mode with $m_1 = 1$ and $\theta_{L1} = 7.16°$ (a) DC-link capacitor, (b) Flying capacitor.

where ΔV_{Ci} is the peak-to-peak low-frequency capacitor voltage ripple, 'f' is the fundamental output frequency, I_{RMS} is the RMS output current, and 'C' is the value of the capacitor. Figs. 4.5 (a) and (b) show the results obtained with a fixed load-1 angle $\theta_{L1} = 7.16°$ and $m_1 = 1$. The evaluation is done for CF mode ($f = f_1 = f_2 = 50$ Hz) varying a m_2 and θ_{L2} with a fixed load current.

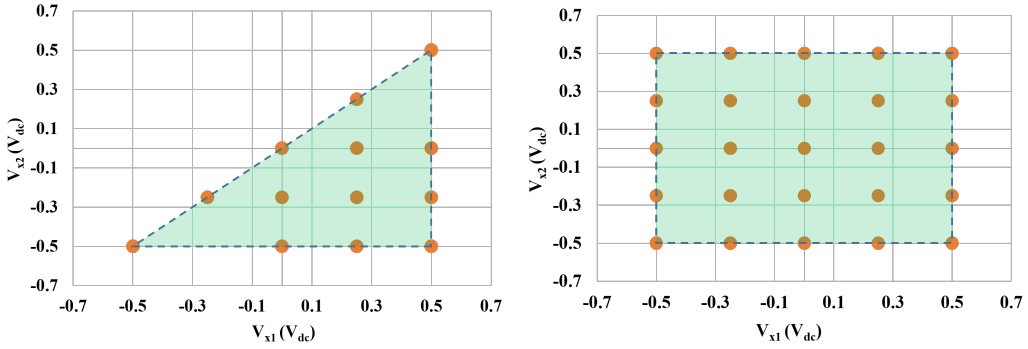


FIGURE 4.6: Boundary region (a) TL-SDOFL (b) FLSDO.

4.3 Operation and Modulation Scheme of FLSDO Converter

A distinct drawback of multi-level dual output converters with reduced switch count is their inability to operate in all possible switching combinations due to the limitation of modulation indices. Most of the existing dual output converters including nine switch inverter (NSI) should maintain $v_{ref1} \geq v_{ref2}$ at all times [70]. However, FLSDO does not suffer from this limitation. This section analyzes and investigates the region of operation of FLSDO. Fig. 4.6 shows the difference in the boundary region between TL-SDOFL and FLSDO. Table 4.1 lists the number of switches, voltage stress and boundary region of FLSDO compared to other topologies. It provides advantages in terms of cost and volume and the absence of clamping diodes. As it can be observed, the proposed FLSDO has the same region of operation as that of a conventional DFC-ANPC or five-level NPC converter.

4.3.1 Region of Operation

Figs. 4.6(a) and (b) provide the boundary region of TL-SDOFL and FLSDO respectively. TL-SDOFL converter cannot provide all possible output voltage combinations at its two terminals, Fig. 4.6(a) illustrates a reduced boundary region. Fig. 4.6(b) graphically represents the switching states of Table 4.2. It illustrates the total number of possible voltage levels that can exist simultaneously at the converter output terminals V_{x1} and V_{x2}. This representation helps to visualize the converter's boundary region. Since the load currents are generated using the available voltage states, the area enclosed by these states accommodates all possible configurations of the voltage reference signals. Consequently, the output voltage varies between -0.5 and 0.5 V_{dc} on both outputs, corresponding to the reference signal. According to the boundary region in Fig. 4.6(b), there are no

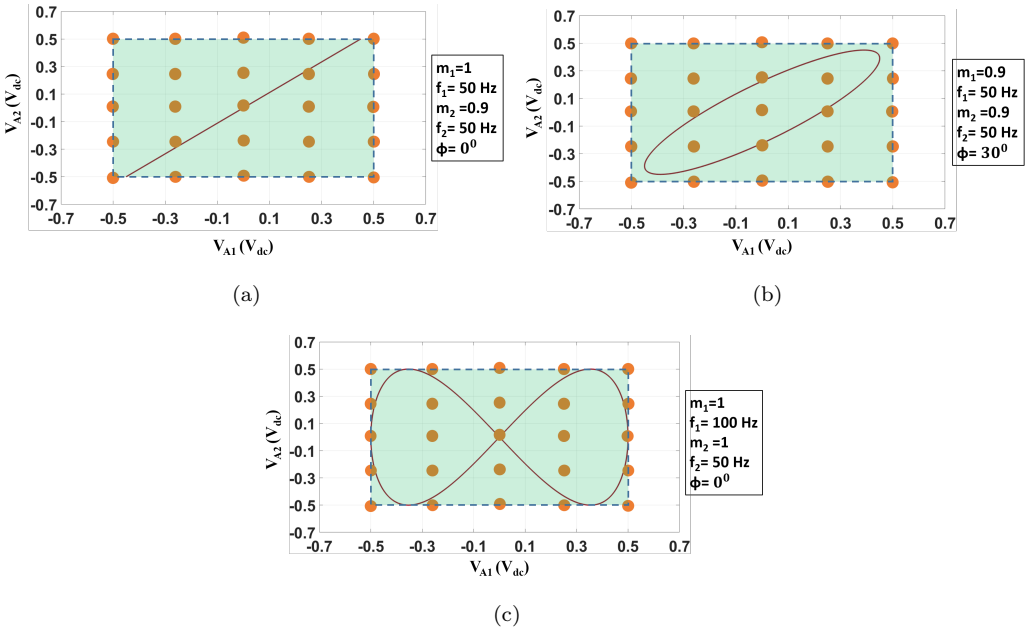


FIGURE 4.7: Projections of reference signals onto the FLSDO converter's boundary region under (a) CF with $m_1 = 1$, $m_2 = 0.9$ and $\phi = 0°$, (b) CF with $m_1 = m_2 = 0.9$ and $\phi = 30°$, (c) DF with $m_1 = m_2 = 1$.

restrictions on one output reference related to the other, allowing both outputs to operate independently.

4.3.2 Modulation Scheme

In many other reduced switch dual output count converters, the upper reference signal cannot be less than the lower reference signal to prevent invalid switching states. This can be achieved by providing the DC offsets for two sets of reference signals. Due to this limitation, a few voltage levels are unavailable for both outputs. The authors have designed the proposed FLSDO to eliminate this restriction.

The hybrid PWM scheme is used for switching. The upper and lower reference signals for the three phases are given as follows:

$$v_{refAi}(t) = m_i sin(\omega_i t + \theta_i) \tag{4.15}$$

$$v_{refBi}(t) = m_i sin(\omega_i t - 2\pi/3 + \theta_i) \tag{4.16}$$

$$v_{refCi}(t) = m_i sin(\omega_i t + 2\pi/3 + \theta_i) \tag{4.17}$$

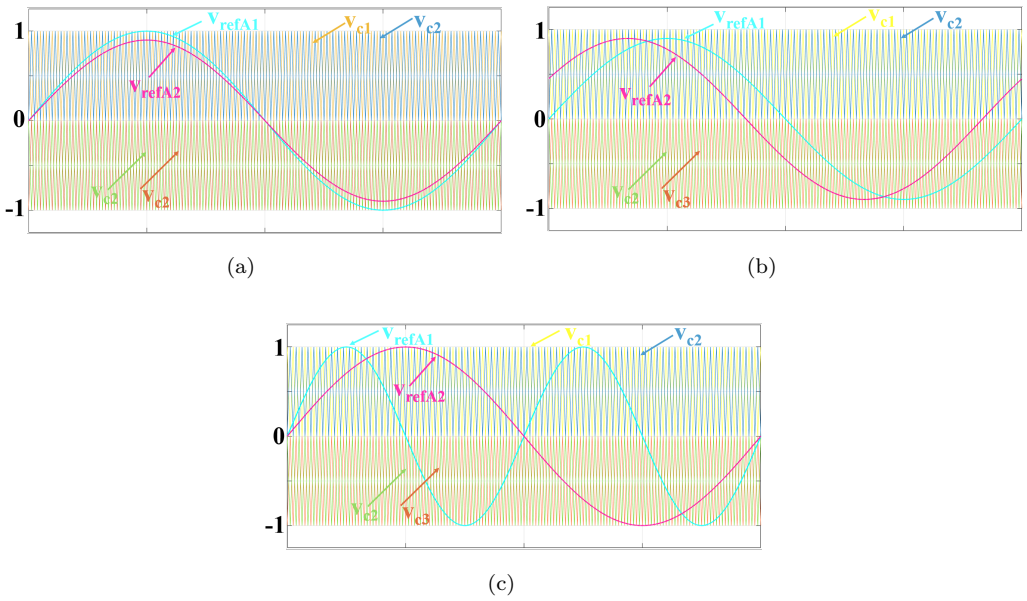


FIGURE 4.8: Hybrid PWM scheme for FLSDO (a) CF mode with m_1 =1, m_2 = 0.9 and $\phi = 0°$, (b) CF mode with $m_1 = m_2 = 0.9$ and $\phi = 30°$, (c) DF mode with $m_1 = m_2 = 1$, $f_1 = 100$ Hz and $f_2 = 50$ Hz.

where $i = 1, 2$, m_i are the modulation indices, and the linear range is from 0 to 1, $\omega_i = 2\pi f_i$ is the fundamental angular frequencies, θ_i is the initial phase angles. The output voltages are unaffected by the absence of DC offsets in the reference signals.

4.4 Mode of Operation

For the independent operation of a dual-output converter, two modes are defined based on the modulating frequencies of the two outputs: common frequency (CF) and different frequency (DF) modes. For both outputs to be controlled independently, the converter must operate in both CF and DF modes. Figs. 4.7(a)-(c) illustrates the validation of the boundary region for different modes of operation by projecting the reference signals onto the boundary graph.

4.4.1 Common Frequency Mode

In this mode of operation, the converter's two outputs operate at the same frequency but with various modulation indices ($m_{1,2}$) and a phase angle shift (ϕ), where $\phi = |\theta_2$ - $\theta_1|$ between the two output signals can also be deduced from the switching state's graphical

depiction. While varying the phase angle to provide all the valid operating points in terms of the modulation indices. There is no limitation in the boundary region regarding the phase difference between the two outputs.

4.4.1.1 Same Phase

In this mode of operation, let $f_1 = f_2 = f = 50$ Hz and $\theta_1 = \theta_2 \Rightarrow \phi = 0$, then the reference signal v_{refA1} and v_{refA2} of the A phase leg with four common carriers, two upper and two lower as shown in Fig. 4.8(a). The projection of the reference signals onto the operating boundary graph is shown in Fig. 4.7(a).

If the reference signal v_{refA1} exceeds both upper carriers, the output voltage v_{A1} is $V_{dc}/2$; otherwise, it is either $V_{dc}/4$ or 0. If v_{refA1} is lesser than both lower carriers, v_{A1} is -$V_{dc}/2$; otherwise, it is -$V_{dc}/4$ or 0. Following the same approach, the output voltage v_{A2} is $V_{dc}/2$ when v_{refA2} is greater than both upper carriers; otherwise, it is $V_{dc}/4$ or 0. If v_{refA2} is lesser than the lower carrier, v_{A2} is -$V_{dc}/2$; otherwise, it is -$V_{dc}/4$ or 0.

The output voltages of the B and C phase legs are generated by the same technique, but the reference signals of the A phase leg are phase-shifted by -$2\pi/3$ and $2\pi/3$. It can be observed that the peaks of reference signal v_{refx1} and v_{refx2} are occurring at the same instance, and in this mode, there is no requirement of the dc offset as in the TL-SDOFL converter provided to prevent the modulation indices (m_1 and m_2) from interfering with one another. Consequently, it is possible to express the ranges of m_1 and m_2 as

$$0 < m_1 \leq 1, 0 < m_2 \leq 1 \tag{4.18}$$

4.4.1.2 Different Phase

In this mode of operation, let $f_1 = f_2 = f$ and $\theta_1 \neq \theta_2$. Then, the reference signal v_{refA1} and v_{refA2} of the A phase leg with four common carriers, two upper and two lower, as shown in Fig. 4.8(b), having $f_1 = f_2 = 50$ Hz, $\phi = 30°$ with $m_1 = m_2 = 0.9$. The projection of the reference signals onto the operating boundary graph for this mode of operation is shown in Fig. 4.7(b). The output voltage levels are generated by comparing the reference signals with four common carriers. $\phi = |\theta_2$ - $\theta_1|$ is the phase shift between the two sets of output phase voltages. Since there is no constraint of $v_{ref1} \geq v_{ref2}$, modulation indices m_1 and m_2 are independent of each other, and the maximum phase angle ϕ to generate the

output voltage for FLSDO, unlike in TL-SDOFL in which there is an inequality relation between the modulation index and phase angle.

4.4.2 Different Frequency Mode

The converter operates in DF mode at varying load frequencies between two outputs. In TL-SDOFL, and many other reduced switch count dual output converters the modulation constraint generates an inequality relation between m_1 (M_{TOP}) and m_2 (M_{BOT}):

$$0 < M_{TOP} + M_{BOT} \leq 1 \tag{4.19}$$

From (4.19), one can infer that the maximum sum of two modulation indices is 1. Therefore, to achieve the same output effect as the conventional SMLI, the DC-link voltage V_{dc} must be doubled. For maintaining this constraint in different frequency modes for TL-SDOFL converter, adding the DC offset results in the modulation index m_2 (M_{BOT}) being lesser than 0.5, resulting in the reference signal v_{refx2} always compared with the lower carrier. Therefore, the lower output voltage V_{x2} has only three levels 0, -V_{dc}/4 and -V_{dc}/2. Low modulation indices result in a reduction in the number of levels in both phase and line voltages. FLSDO topology has no such restriction, thus providing the same number of levels as that of a conventional SMLI with a reduced switch count. In DF mode of operation, $f_1 \neq f_2$. Let $f_1 = 100$ Hz and $f_2 = 50$ Hz, with $m_1 = m_2 = 1$ then the reference signal v_{refA1} and v_{refA2} of the A phase leg with four common carriers, with the upper two and lower two as shown in Fig. 4.8(c). The projection of the reference signals onto the operating boundary graph is shown in Fig. 4.7(c).

4.5 Simulation and Experimental Verification

A laboratory prototype of the proposed FLSDO converter is developed, and the parameters considered are listed in Table 4.3. The semiconductor switches used in the prototype are IGBTs (IKW50N60H3). The experiment is performed in both CF and DF operating modes with linear loads, demonstrating the performance of the FLSDO converter. The DC-link capacitor voltage balancing of the converter is also accomplished. The hardware setup is illustrated in Fig. 4.9. The gate pulse signals for the FLSDO converter are generated using a TMS320F28335 processor.

TABLE 4.3: Parameters for Experimentation

Parameter	Value
DC-link voltage, V_{dc}	200 V
DC-link capacitor, $C_1 = C_2$	4700 μF
Flying Capacitor, $C_3 = C_4$	2200 μF
Load Resistance, $R_1 = R_2$	50 Ω
Load Inductance, $L_1 = L_2$	20 mH
Switching frequency, f_s	4 kHz

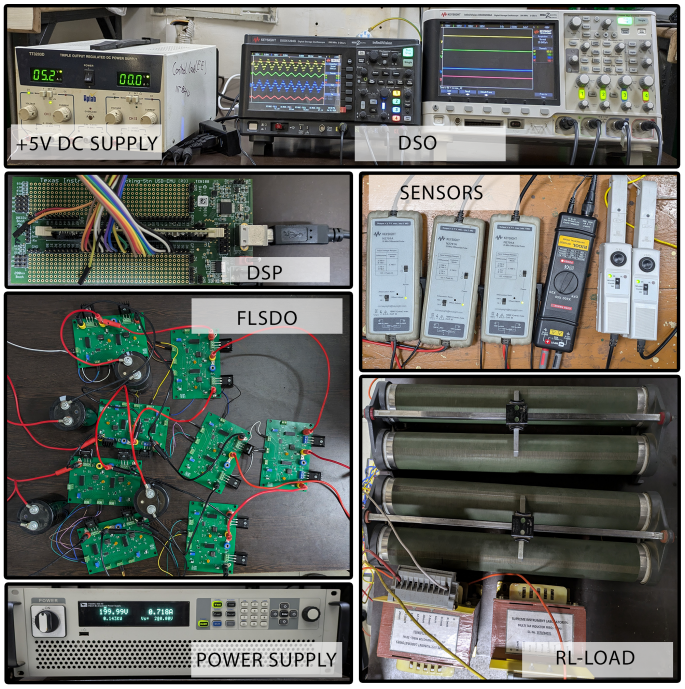


FIGURE 4.9: Developed hardware setup.

The hybrid PWM is implemented with a carrier frequency of 4 kHz. Identical RL loads are employed to represent the AC loads.

4.5.1 Common frequency (CF) mode

The experimental result for both the output voltages and its load current under CF mode of operation with the same modulation indices, $m_1 = m_2 = 0.8$ is shown in Fig. 4.10(a). Fig. 4.10(b) shows the voltage balance of DC-link and flying capacitors in CF mode with $m_1 = m_2 = 0.8$. As can be observed, V_{C1}, V_{C2}, V_{C3}, and V_{C4} are balanced at 98.8 V, 101.2 V, 48 V and 52 V respectively. The experimental result for both output voltages (v_{A1},v_{A2}) and its corresponding load currents (i_{A1},i_{A2}) under CF mode of operation with the different modulation indices $m_1 = 0.8$, $m_2 = 0.7$ is shown in Fig. 4.10(c). As observed,

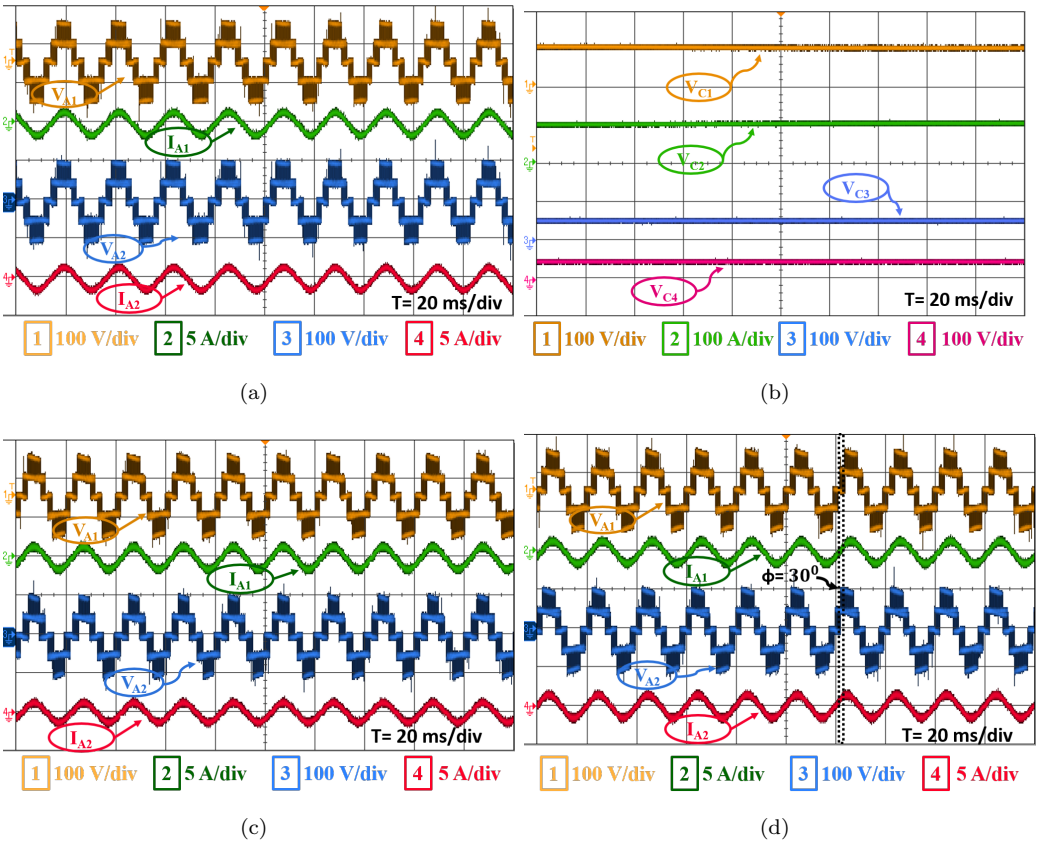


FIGURE 4.10: Experimental results in CF mode (a) output voltages (v_{A1},v_{A2}) and currents (i_{A1},i_{A2}) with $m_1 = m_2 = 0.8$, (b) DC-link and flying capacitor voltage balancing with $m_1 = m_2 = 0.8$, (c) output voltages (v_{A1},v_{A2}) and currents (i_{A1},i_{A2}) with $m_1 = 0.8$, $m_2 = 0.7$, (d) output voltages (v_{A1},v_{A2}) and currents (i_{A1},i_{A2}) with $m_1 = m_2 = 0.8$ and $\phi = 30°$.

the converter generates five voltage levels at its output ports: -V_{dc}/2, -V_{dc}/4, 0, +V_{dc}/4 and +V_{dc}/2. Fig. 4.10(d) shows the experimental results for the output voltages (v_{A1}, v_{A2}) and corresponding load currents (i_{A1}, i_{A2}) in CF mode, with modulation indices m_1 = m_2 = 0.8 and a phase shift (ϕ) = 30°.

4.5.2 Different frequency (DF) mode

Two outputs of the FLSDO converter are operated at different frequencies, and performance is evaluated. Fig. 4.11(a) presents the experimental result for both output voltages (v_{A1},v_{A2}), and its corresponding load currents (i_{A1},i_{A2}). The converter is operated with frequencies f_1 = 100 Hz, f_2 = 50 Hz with modulation indices $m_1 = m_2 = 0.8$.

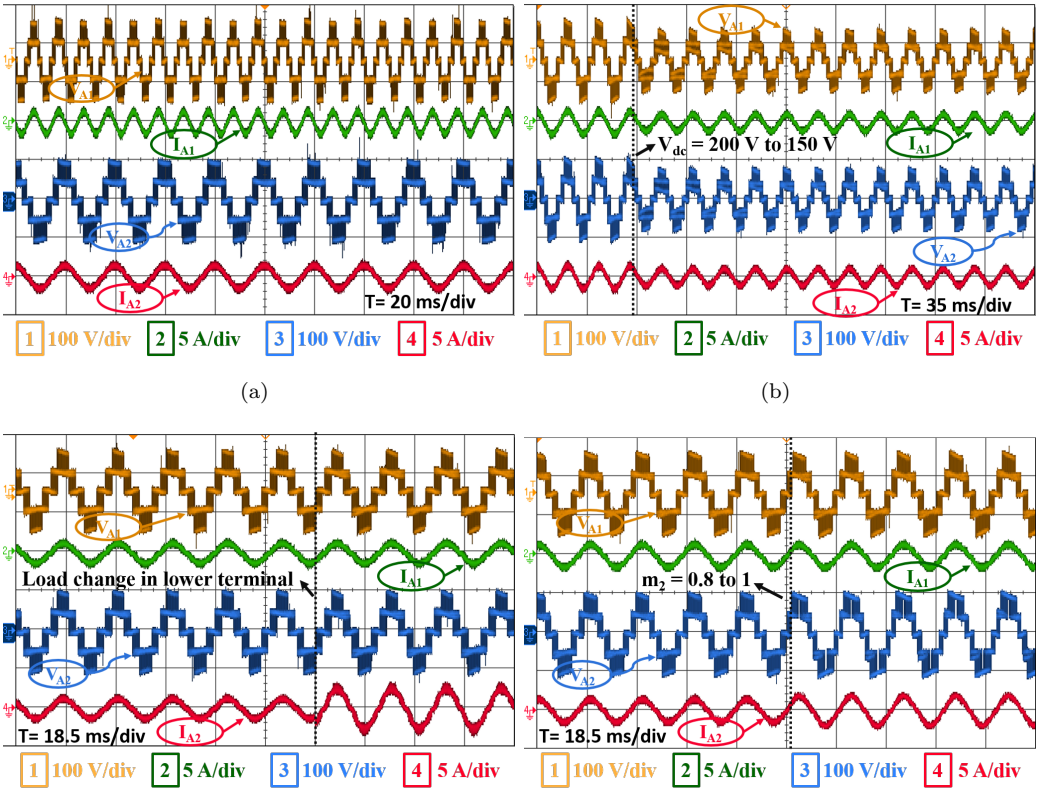


FIGURE 4.11: Experimental results of output voltages (v_{A1},v_{A2}) and currents (i_{A1},i_{A2}) (a) in DF mode with $m_1 = m_2 = 0.8$ and $f_1 = 100$ Hz, $f_2 = 50$ Hz, (b) in CF mode with $m_1 = m_2 = 0.8$ for a sudden change in input voltage, (c) in CF mode with $m_1 = m_2 = 0.7$, for a sudden change in load, (d) for a sudden change in m_2 from 0.8 to 1, keeping $m_1 = 0.8$, under CF mode.

4.5.3 Sudden Change

4.5.3.1 Input change

In this scenario, the converter's performance is evaluated under a sudden change in input voltage from 200 V to 150 V. Fig. 4.11(b) shows the experimental results for the upper and lower output voltages (v_{A1}, v_{A2}) and the corresponding load currents (i_{A1}, i_{A2}) in CF mode, with modulation indices $m_1 = m_2 = 0.8$. As observed, the voltage levels stabilize at the new value within a few milliseconds, and the voltage of DC-link and flying capacitors is maintained shortly thereafter.

4.5.3.2 Load Change

In this scenario, the converter's performance is assessed under sudden load changes at the lower terminal while operating in CF mode. Previously, the load parameters were $R_1 = R_2 = 50\Omega$ and $L_1 = L_2 = 20$ mH. Following a sudden load change at the lower terminal, R_2 is reduced to 25 Ω and L_2 to 10 mH. Fig. 4.11(c) presents the experimental result for upper and lower output voltages (v_{A1},v_{A2}), and its corresponding load currents (i_{A1},i_{A2}) under CF mode. In this case, the converter operates at modulation indices $m_1 = m_2 = 0.7$. As observed, the voltage levels remain unchanged despite the sudden load change, and both the DC-link and flying capacitor voltage values are consistent.

4.5.3.3 Modulation change

In this scenario, the converter's performance is assessed under a sudden change in the modulation index of the second load terminal. Fig. 4.11(d) presents the experimental results for the upper and lower output voltages (v_{A1}, v_{A2}) and the corresponding load currents (i_{A1}, i_{A2}) in CF mode. Initially, the converter operates with modulation indices $m_1 = m_2 = 0.8$, and then the modulation index m_2 is increased to 1. As observed, the first output terminal remains unaffected, and both the DC-link and flying capacitor voltages stay consistent.

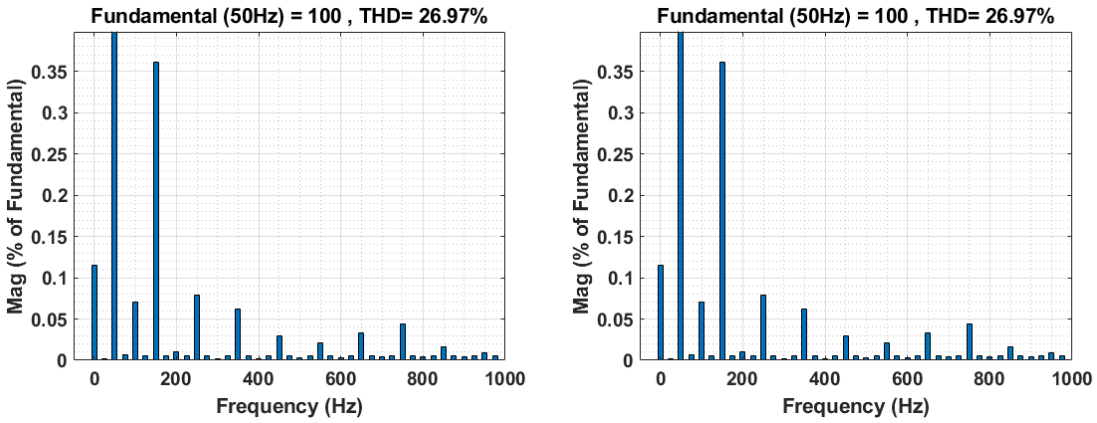
4.5.4 Total Harmonic Distortion (THD)

The output voltage THD of both outputs is shown in Fig. 4.12. The THD is calculated under CF mode with modulation indices $m_1 = m_2 = 1$. As observed, the percentage THD of voltage for both output terminals is 26.97%.

4.6 Power Loss and Efficiency Comparison

Conduction and switching losses are two significant forms of power losses arising from power electronics device operation [72].

Conduction Losses (P_{con}): A standard power transistor (IGBT) and diode are used for the loss analysis of the FLSDO converter. Instantaneous conduction losses for a diode [P_{con},



(a) (b)

FIGURE 4.12: Total Harmonic Distortion of output voltages (a) v_{A1}, and (b) v_{A2}

D(t)] and IGBT [P_{con}, T(t)] are as follows:

$$P_{con}, T(t) = [V_T + R_T i^{\beta}(t)]i(t) \tag{4.20}$$

$$P_{con}, D(t) = [V_D + R_D i(t)]i(t) \tag{4.21}$$

where V_T and V_D stand for the IGBT's and the diode's on-state voltages, respectively. The equivalent resistance of the transistor (IGBT) and diode is represented by R_T and R_D, respectively, whereas β is a constant associated with the transistor's specification. The conduction losses of each device are calculated using (4.20) and (4.21), and total conduction loss is the sum of these two for FLSDO.

Switching Losses (P_{sw}): Turn-on and turn-off energy loss (E_{on}, E_{off}) is calculated for the switch and the antiparallel diode are as follows:

$$E_{off,m} = \int_0^{t_{off}} v(t)i(t)dt = \int_0^{t_{off}} [(\frac{v_{sw,m}}{t_{off}}t)$$
$$(-\frac{I}{t_{off}}(t - t_{off}))dt = \frac{1}{6}v_{sw,m}It_{off} \tag{4.22}$$

$$E_{on,m} = \int_0^{t_{on}} v(t)i(t)dt = \int_0^{t_{on}} [(\frac{v_{sw,m}}{t_{on}}t)$$
$$(-\frac{I'}{t_{on}}(t - t_{on}))dt = \frac{1}{6}v_{sw,m}I't_{off} \tag{4.23}$$

where $E_{off,m}$, is the turn-off loss of the 'm' switch, t_{off} is the turn-off time of the switch, 'I' is the current through the switch before turning off and 'I'' is the current through the switch after turning on, and $v_{sw,m}$ is the off-state voltage on the 'm' switch. $E_{on,m}$ is the turn-on loss of the 'm' switch, and t_{on} is the turn-on time of the switch.

$$P_{sw} = f[\sum_{m=1}^{N_{switch}} (\sum_{j=1}^{N_{on,m}} E_{on,mj} + \sum_{j=1}^{N_{off,m}} E_{off,mj})] \tag{4.24}$$

Where f is the fundamental frequency, $N_{on,m}$ and $N_{off,m}$ are the number of turning ON and OFF of the 'm' switch during a period. Also, $E_{on,mj}$ is the energy loss of the 'm' switch during the jth turning ON, and $E_{off,mj}$ is the energy loss of the 'm' switch during the jth turning off. The total losses of FLSDO will be

$$P_{Loss} = P_{con} + P_{sw} \tag{4.25}$$

The parameters used for the calculation of power losses are listed in Table 4.3. The switching and conduction losses of FLSDO are calculated using the IGBT IKW50N60H3 for the loss model in PLECS software. The contribution of switching and conduction loss under the CF mode of operation with m_1=1, m_2 varying from 0.2 to 1, and $f_1 = f_2 = 50$ Hz is shown in Fig. 4.13(a). Figs.4.13(b) and (c) show the distribution of the switching and conduction losses among the different switches of phase a under CF mode of operation having $m_1 = m_2 = 1$ and $f_1 = f_2 = 50$ Hz, where the conduction losses are the highest in S_{A1} and S'_{A4}, and the lowest in S'_{A12}, S_{A15}, S_{A25}, S'_{A22}. On the other hand, S_{A1} and S'_{A4} have the highest switching losses while S_{A13}, S'_{A13}, S_{A23} and S'_{A23} have the lowest switching losses.

The efficiencies are compared in CF and DF mode as shown in Fig. 4.14. The efficiency comparison is made using the parameters listed in Table 4.3 between the DFC-ANPC, TL-SDOFL, Dual 5L-ANPC, Dual 5L-NPC, and the proposed FLSDO converter. In the first scenario, 4.14(a) depicts the efficiency comparison under CF mode when modulation indices m_1=1 and m_2 vary from 0.2 to 1. It can be observed that the Dual 5L-ANPC has more efficiency compared to other dual-output five-level converters, but DFC-ANPC and FLSDO also have an efficiency greater than 96.5 % for all values of m_2. In the second scenario, Fig. 4.14 (b) compares the efficiency under CF mode with m_1=0.8 and phase shift, $\phi = 30°$ and varying m_2. As it can be seen, for a modulation index m_2 greater than 0.8, the reduced switch count converter TL-SDOFL cannot operate because of its constricted region of operation, so the graph shows zero efficiency. For m_2 less than 0.8,

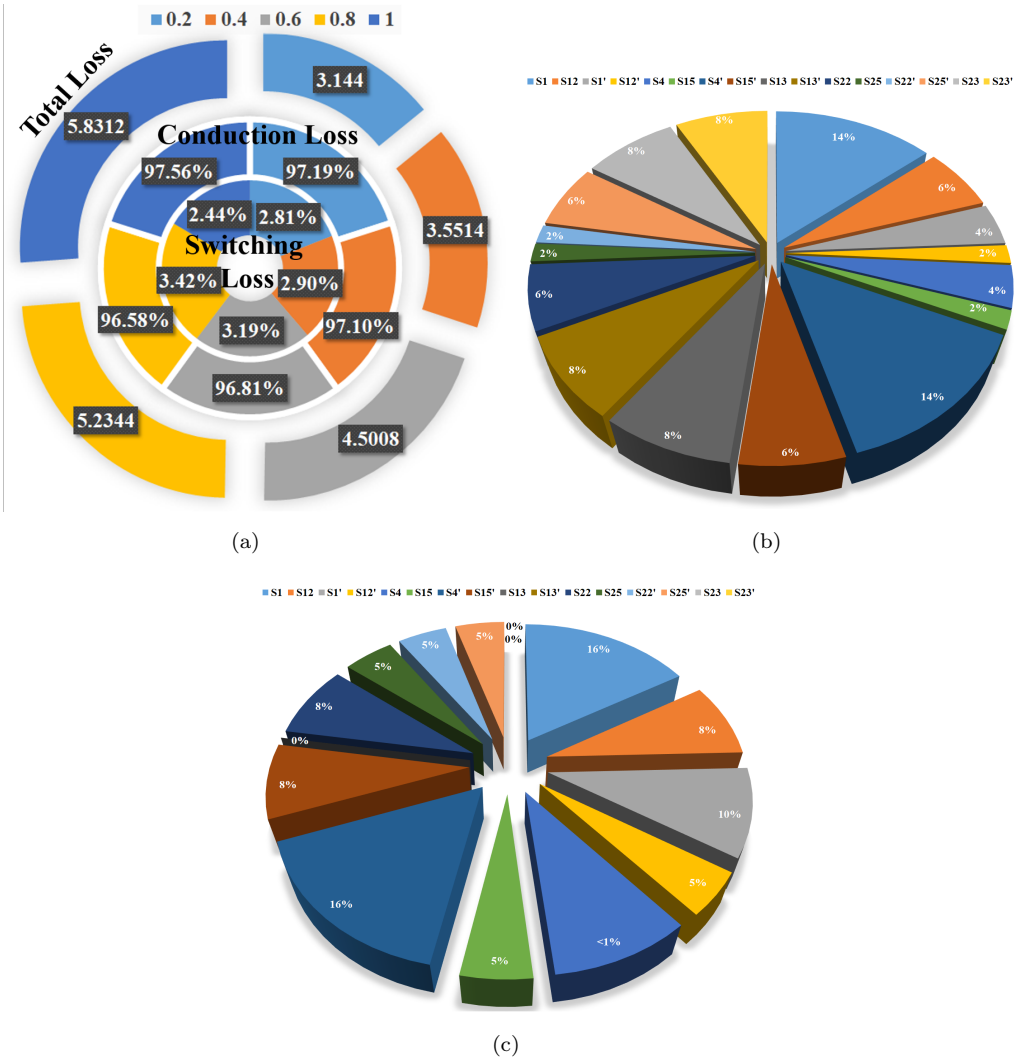


FIGURE 4.13: Switching, conduction, and total losses of the proposed FLSDO for phase leg under CF mode with $m_1 = 1$ and m_2 varying.

TL-SDOFL has more efficiency than other dual output five-level converters, but DFC-ANPC and FLSDO have efficiency greater than 96.5 % and when m_2 lies between 0.8 and 1, then the efficiency of DFC-ANPC and FLSDO is greater than 97 %. In the third scenario, Fig. 4.14(c) shows the comparison of efficiency under DF mode ($f_1 = 50$ Hz, $f_2 = 100$ Hz) with $m_1 = 0.5$ and varying m_2. Because of limitations in the operating region, the TL-SDOFL cannot operate at m_2 greater than 0.5, and efficiency is zero for this region. For m_2 less than 0.5, TL-SDOFL has more efficiency, but FLSDO has efficiency greater than 95.5 % up to $m_2 = 0.6$, and for m_2 greater than 0.6, FLSDO has the efficiency greater than 96 %. In the first scenario, the FLSDO has approximately the same efficiency as that of DFC-ANPC up to $m_2 = 0.6$, but for $m_2 \geq 0.8$, DFC-ANPC is more efficient than FLSDO. But for the second and third scenarios, FLSDO is more efficient than CTL-ANPC

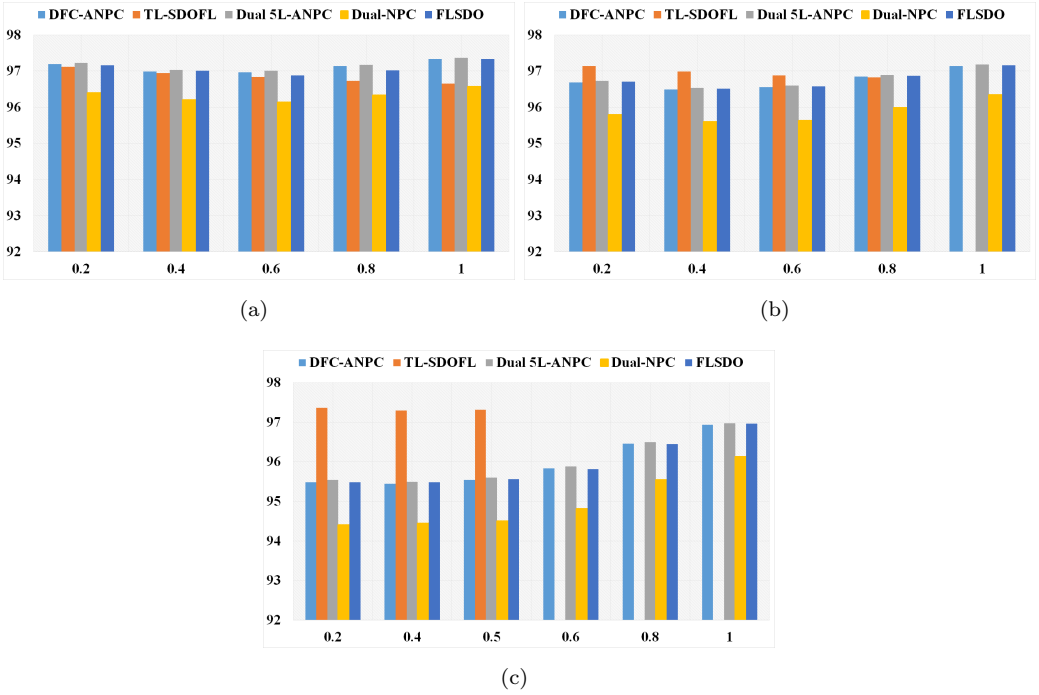


FIGURE 4.14: Efficiency comparison for (a) CF mode with $m_1 = 1$ (b) CF mode, $m_1 = 0.8$ and $\phi = 30°$, (c) DF mode with $m_1 = 0.5$ and $f_1 = 50$ Hz, $f_2 = 100$ Hz.

for all modulation indexes of m_2. In all three scenarios, some FLSDO devices share two loads, and the phase of the load currents will impact conversion efficiency. This difference in efficiency is not considerably high. Note that the two loads and modulation index m_1 are fixed.

4.7 Five-Level Stacked Multi-Output (FLSMO) Converter

The five-level stacked dual output (FLSDO) converter can be expanded to accommodate multiple output ports. Fig. 4.15 illustrates the generalized structures of the multi-output FLSMO converter. The total number of switches required in each converter (X_{sw}) is calculated using the specified equation.

$$X_{sw} = 4 \times \lceil N/2 \rceil + 6 \times N \tag{4.26}$$

where $N = n_1 + n_2$ is the no. of outputs and $\lceil N \rceil$ is the ceiling function. As the number of output ports increases, the power switch count in the FLSMO converter decreases, resulting in a significant reduction in the required switches. Notably, when N = 1, the

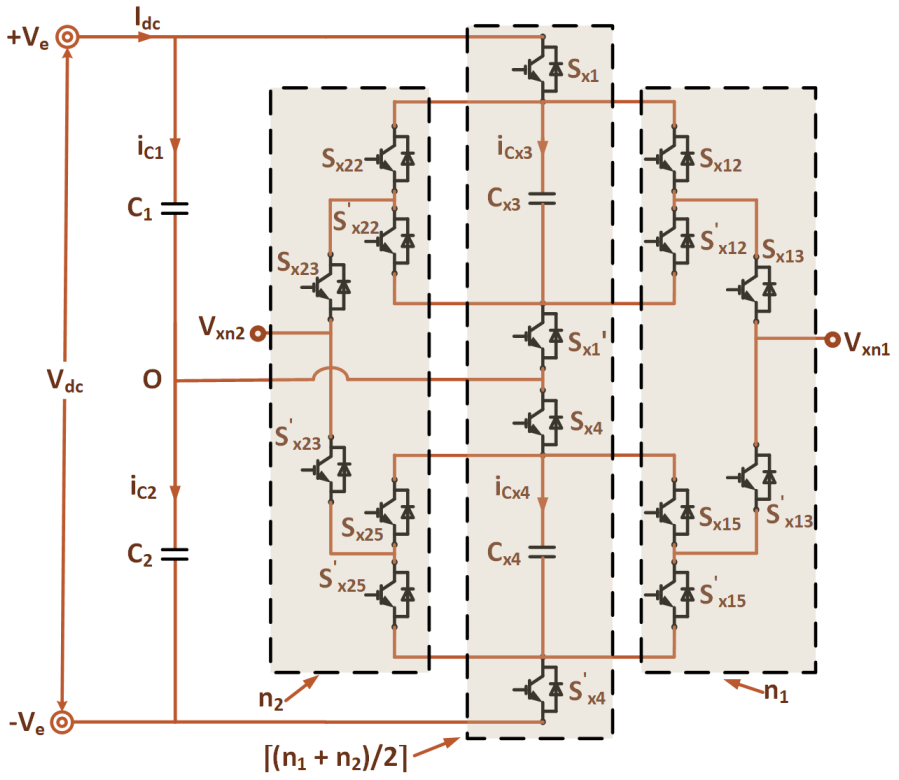


FIGURE 4.15: Five-level stacked multi-output (FLSMO) converter.

FLSMO converter simplifies to a single-output configuration, functioning as a conventional five-level stacked converter. When N = 2, it corresponds to the standard FLSDO configuration. Table 4.4 shows the comparison of scalability of the five-level converters.

TABLE 4.4: Comparison of the scalability of the five-level inverter for the different outputs

No. of output	DFC-ANPC [61, 74, 75]	TL-SDOFL [73]	Dual 5L-NPC [77]	FLSDO
Single Output	10 S	11 S	8 S +12 D	10 S
Dual Output	20 S	11 S	16 S + 24 D	16 S
Triple Output (Three-Phase)	30 S	-	24 S + 36 D	26 S
Quad Output	40 S	22 S	32 S + 48 D	32 S
Penta Output (Five-Phase)	50 S	-	40 S + 60 D	42 S
Hexa Output (Six-Phase)	60 S	33 S	48 S + 72 D	48 S
⋮	⋮	⋮	⋮	⋮
N Output	10×N S	-	8×N S + 12×N D	4×($\lceil N/2 \rceil$) +6×N S

S = no. of switches and D = no. of diodes.