2

CHAPTER

QUASI-Z-SOURCE SERIES-PARALLEL MULTI-OUTPUT INVERTERS

2.1 Introduction

In recent years, the concept of microgrid is emerging very fast, which requires the interlinking between various renewable sources and catering local/residential loads at different voltage levels. As discussed in previous chapter, multi-output DC-AC converter topologies have been emerged as a better choice over the use of multiple DC-AC converters to cater simultaneous AC load demands at different voltage levels. This chapter presents two single-phase series-parallel multi-output (QSPMO) inverters with simultaneous multiple AC outputs. The proposed inverters inherit all the advantages of quasi-Z-source (*q*-ZS) based inverters and are capable of simultaneously feed multiple single-phase AC loads at different voltage levels. The conventional voltage source inverter can produce only stepped down voltages, whereas, the proposed *q*-ZS based single-phase QSPMO inverters can also produce the boosted output voltage. In this chapter, mathematical modelling and detailed operation of the proposed QSPMO inverters with control scheme have been discussed. The steady state and dynamic analysis are also carried out in this chapter and verified by simulation results.

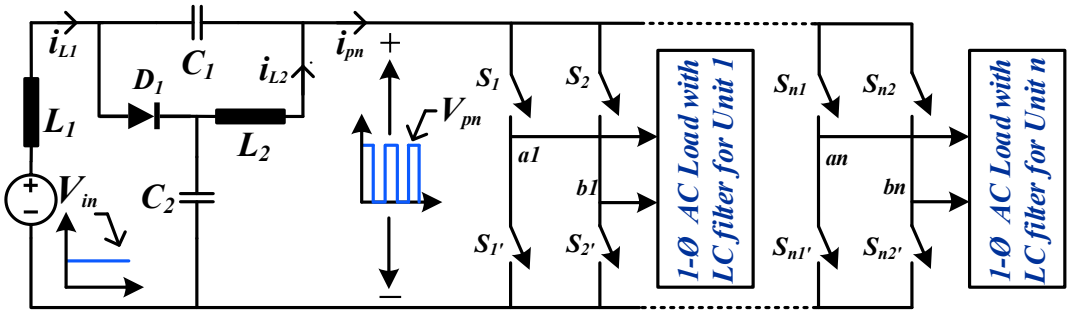
2.2 Single-Phase Q-Z-Source Series-Parallel Inverters with Multi AC Outputs

As discussed in previous chapter, the conventional methods to serve multiple load demands have many disadvantages. To overcome these problems quasi-Z-source series-parallel multi outputs (QSPMO) inverters are proposed here. The proposed inverters are derived from the conventional quasi-Z-source inverter by replacing its main switch by *n*-number of series and parallel connected single-phase inverters. The proposed QSPMO inverters have two modes, parallel and series modes. The proposed parallel mode inverter gives *n*-number of single-phase AC outputs with constant supply required constant voltages and variable load currents. The series mode inverter gives *n*-number of AC outputs with constant

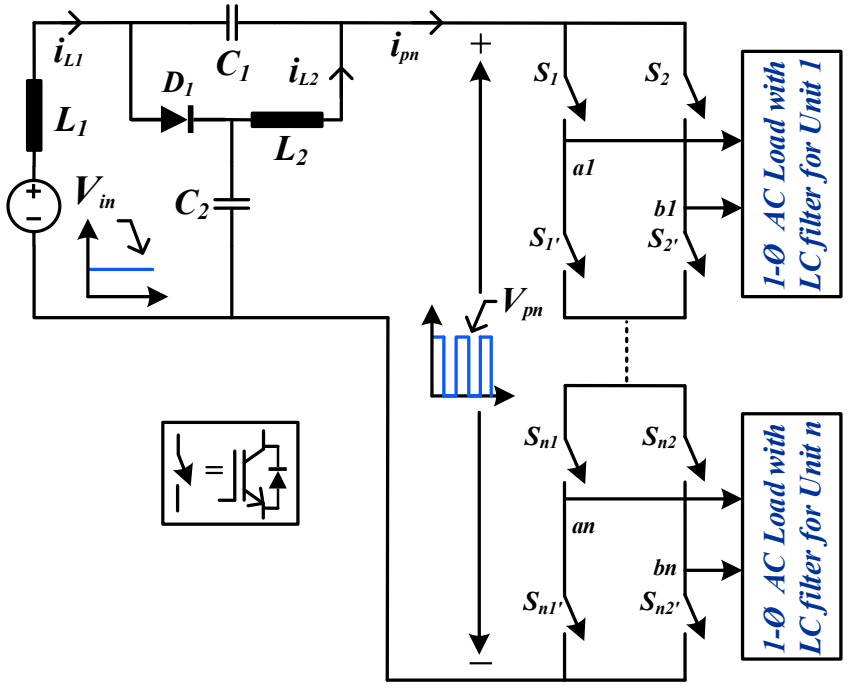
load currents. As they are based on the quasi-Z-source network, they have inherent shoot-through protection capability. They can also perform buck as well as boost operation, which is not possible in case of traditional voltage source inverter (VSI). Since the proposed multi-output inverters use only single Z-source network to produce multiple AC outputs, their size, weight, volume and cost reduce. These inverters use sinusoidal pulse width modulation (SPWM) and constant frequency shoot-through (CFST) technique to generate switching signals. The proposed inverters can be used for simultaneous multiple DC-AC power conversion for single-phase microgrid applications and residential loads. In this chapter, the proposed topologies using closed-loop control are verified for two output units, which are capable of supplying two single-phase AC outputs simultaneously.

2.2.1 Proposed QSPMO Inverters' Schematics

The schematic of the proposed QSPMO inverters for multiple AC outputs are shown in Figure 2.1. They consist of a quasi-Z-source network with *n*-number of series-parallel connected single-phase inverters. The traditional quasi-Z-source network consists of two identical inductors L_1 and L_2, two identical capacitors C_1 and C_2, one power diode D_1 and *n*-number of single-phase inverters connected in series and parallel. Figure 2.1(a) shows proposed parallel mode QSPMO inverter in which *n*-number of inverter output units are connected in parallel. However, in the series mode, *n*-number of inverter output unts are connected in series with the quasi-Z-source network to achieve voltage boost shown in Figure 2.1(b). The output of the QSPMO inverter is connected to the AC load through a low pass filter. The main purpose of the Z-source network is to boost the low input voltage (V_{in}) to a voltage level V_{pn} (switch node voltage), such that the AC output voltage of the inverters can meet or match the requirement of AC microgrids and residential load demands. It is important to mention here that the proposed topology is studied for two output units ($n = 2$).



(a)



(b)

Figure 2.1: Schematic of the proposed (a) parallel and (b) series mode inverters with multi AC outputs.

2.3 Operation of the Proposed QSPMO Inverter

The proposed QSPMO inverters operates in two different states to achieve boost voltage and inversion, i.e., 1) shoot-through and 2) power state [71]-[75].

2.3.1 Shoot-Through State

Figures 2.2(a) and (b) show the circuit diagram of the proposed series-parallel QSPMO inverters during shoot-through (ST) state. The circuits are simplified by replacing output units with short-circuited switches in order to demonstrate the circuit behavior, and the

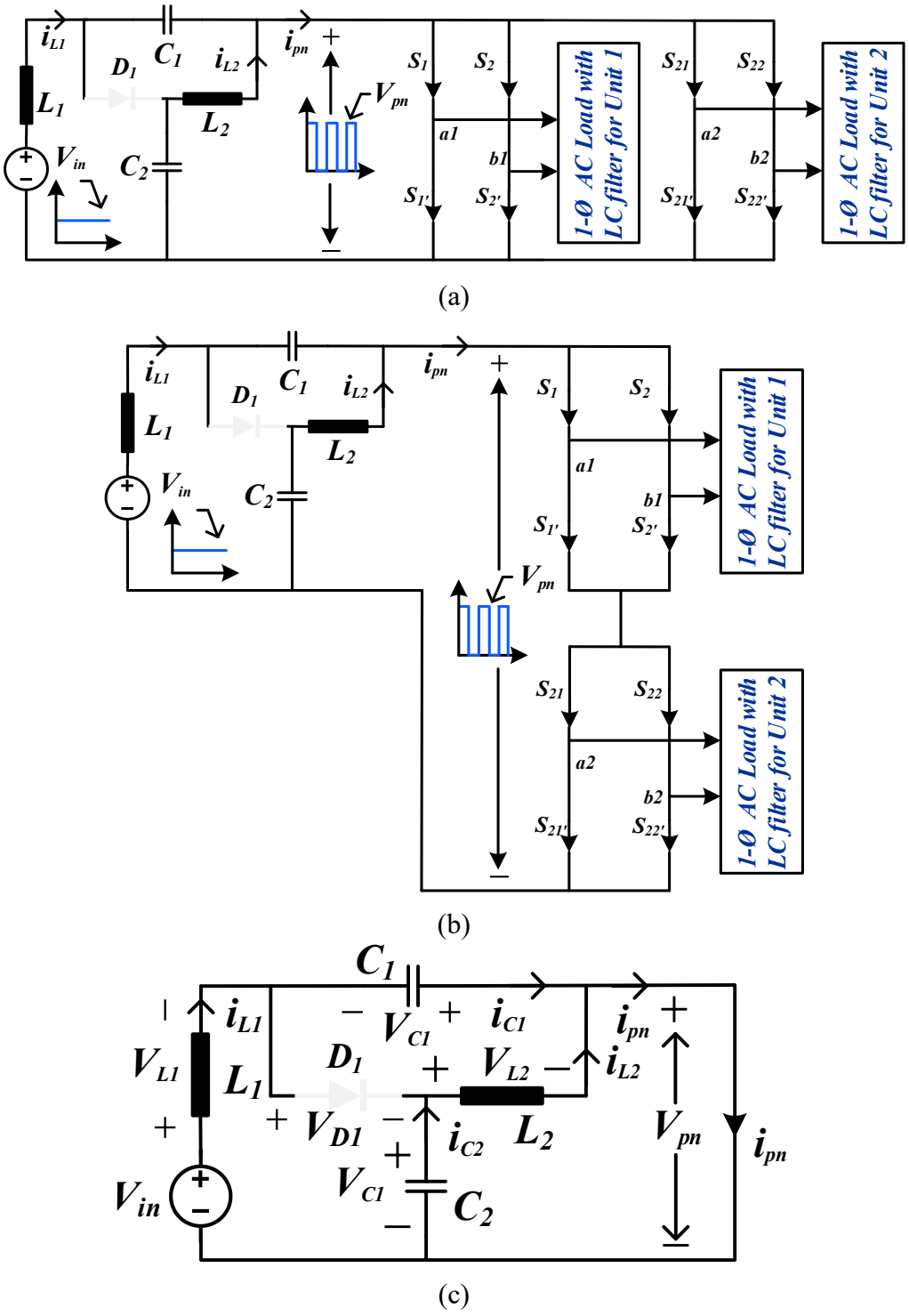


Figure 2.2: Schematic of the proposed inverters (a) parallel, (b) series mode inverters and (c) equivalent circuit diagram during shoot-through state.

corresponding circuit is shown in Figure 2.2 (c). During shoot-through state, the switches of the one leg i.e. S_1 and S'_1 or all the legs of inverters are ON at the same time. Consequently, the switch node voltage V_{pn} becomes zero. The diode D_1 is OFF and the inductors L_1 and L_2 are charged by capacitor C_1, source DC voltage V_{in} and capacitor C_2. The time interval for the shoot-through state is D_sT_s,

where D_s is the ST duty ratio over one switching period T_s.

By applying the KVL in Figure 2.2(c), the voltage across inductors L_1 and L_2 are

$$V_{L1} = V_{in} + V_{c1} \tag{2.1}$$

$$V_{L2} = V_{c2} \tag{2.2}$$

where V_{in} is the input DC voltage and V_{c1} and V_{c2} are the voltages across capacitors C_1 and C_2 respectively.

Due to the short circuit of inverters' bridge, the switch node voltage (V_{pn}) is zero.

$$V_{\text{pn}} = 0 \tag{2.3}$$

During the ST state, the diode is turned OFF. Hence, the voltage across the diode is

$$V_{D1} = V_{c1} + V_{c2} \text{ and } i_{D1} = 0 \tag{2.4}$$

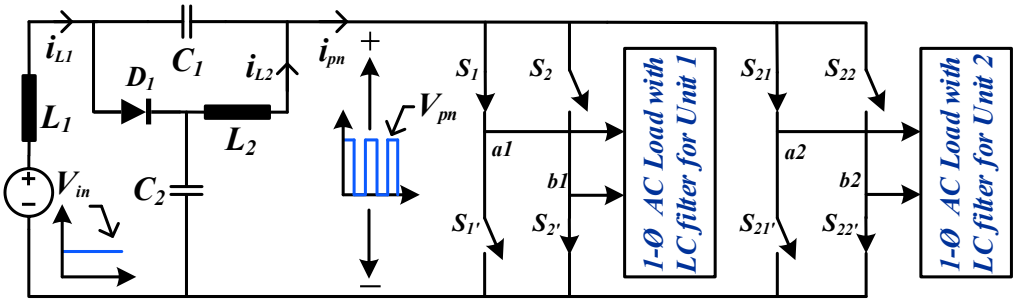
By applying KCL in Figure 2.2(c), the capacitor and switch node currents (i_{pn}) are

$$i_{C1} = -i_{L1}, \quad i_{C2} = -i_{L2} \text{ and } i_{pn} = i_{L1} + i_{L2} \tag{2.5}$$

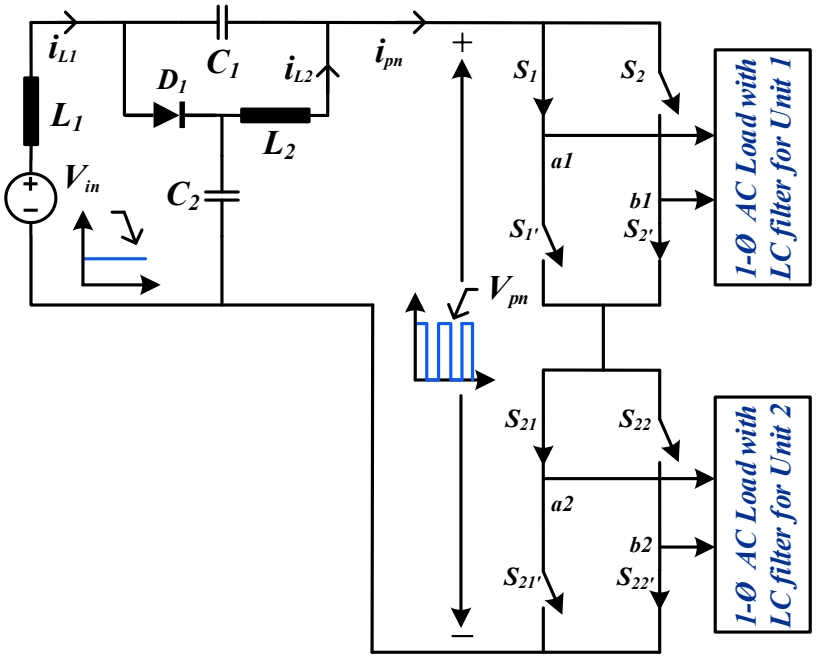
where V_{pn} and i_{pn} are the switch node voltage and current respectively; V_{L1} and V_{L2} are the inductors voltages and i_{L1}, i_{L2}, i_{C1} and i_{C2} are the currents of the inductors and capacitors of the proposed inverters.

2.3.2 Power State

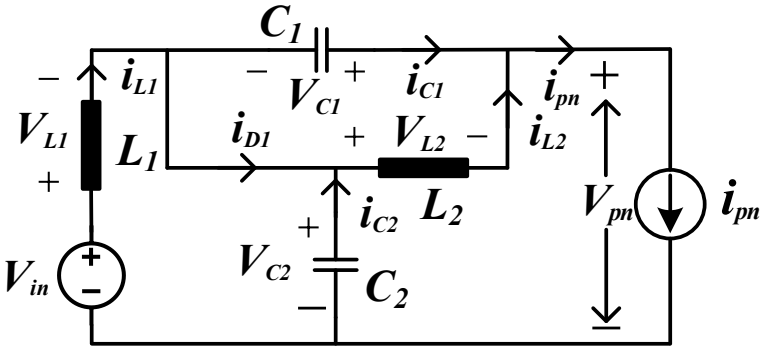
This power state in the proposed QSPMO inverters are similar to the power state of the conventional PWM in voltage source inverters, and the time interval of the power state is (1-D_s)T_s. The circuit diagram of the proposed series-parallel inverters during power state are shown in Figures 2.3(a) and (b). In order to explain the circuit behavior, the circuit is simplified by replacing inverter bridges with an inverted current source (i_{pn}) and a potential of V_{pn}, as shown in Figure 2.3(c). In this state, the electromagnetic energy stored in the inductors L_1 and L_2 are converted into electrostatic energy thus, charging the capacitors C_1 and C_2 and the diode D_1 are turned ON [76]-[80].



(a)



(b)



(c)

Figure 2.3: Schematic of the proposed inverters (a) parallel, (b) series mode inverters and (c) equivalent circuit diagram during power state.

By applying the KVL in the Figure 2.3(c), the voltages across L_1 and L_2 are given as

$$V_{L1} = V_{in} - V_{c2} \tag{2.6}$$

$$V_{L2} = -V_{c1} \tag{2.7}$$

where V_{in} is DC input voltage and V_{L1}, V_{L2} are the voltages across the inductors L_1 and L_2.

The switch node voltage (V_{pn}) across the impedance source network is

$$V_{PN} = V_{c1} + V_{c2} \tag{2.8}$$

where V_{C1} and V_{C2} are the voltage across the capacitors C_1 and C_2.

The diode voltage and currents are

$$V_{D1} = 0 \tag{2.9}$$

$$i_{D1} = i_{L1} + i_{L2} - i_{pn} \tag{2.7}$$

The discharging current of the capacitors are

$$i_{C1} = i_{L2} - i_{pn} \tag{2.8}$$

$$i_{C2} = i_{L1} - i_{pn} \tag{2.9}$$

Under the steady state condition, the average voltage across the inductor and average current through the capacitor in one switching cycle is zero.

By applying flux balance principle to inductor L_1,

$$(V_{in} + V_{c1})\, D_s + (V_{in} - V_{c2})\, (1\text{-}D_s) = 0 \tag{2.10}$$

Using (2.10), the expression of V_{c1} is derived as

$$V_{c1} = \frac{D_s}{(1-2D_s)} V_{in} \tag{2.11}$$

Similarly, by applying flux balance principle on inductor L_2, the following is obtained

$$(V_{c2})\, D_s + (-V_{c1})\, (1\text{-}D_s) = 0 \tag{2.12}$$

Using (2.12), the expression of V_{c2} is derived as

$$V_{c2} = \frac{(1-D_s)}{(1-2D_s)} V_{in} \tag{2.13}$$

Using charge balance principle on capacitor C_1, the following is obtained

$$(-i_{L1})\, D_s + (i_{L2} - i_{pn})\, (1\text{-}D_s) = 0 \tag{2.14}$$

Using (2.14), the expression of i_{L1} is derived as

$$i_{L1} = \frac{(1-D_s)}{(1-2D_s)} i_{pn} \tag{2.15}$$

By using charge balance principle on capacitor C_2, the following is obtained

$$(-i_{L2})\,D_s + (i_{L1} - i_{pn})\,(1\text{-}D_s) = 0 \tag{2.16}$$

Using (2.16), the expression of i_{L2} is derived as

$$i_{L2} = \frac{(1-D_s)}{(1-2D_s)}\, i_{pn} \tag{2.17}$$

2.3.3 DC Boost Factor and AC Voltage Gain

From (2.8), (2.11), and (2.13), the peak switch node voltage ($\hat{V}_{pn}$) at the input of the H-bridge inverters is given as

$$\hat{V}_{pn} = \frac{1}{(1-2D_s)}\, V_{in} = B\, V_{in} \tag{2.18}$$

Using (2.18), the DC boost factor (B) is given as

$$\frac{\hat{V}_{pn}}{V_{in}} = B = \frac{1}{(1-2D_s)} \tag{2.19}$$

In (2.19), as D_s increases, the denominator term (1- 2D_s) decreases consequently and the boost factor B increases in a rectangular hyperbolic manner and finally becomes infinite at D_s = 0.5. The peak value of the fundamental component of the AC outputs is express by

$$\hat{V}_{(AC)} = M \frac{1}{(1-2D_s)}\, V_{in} \tag{2.20}$$

$$\hat{V}_{(AC)} = M\, B\, V_{in} \tag{2.21}$$

$$\frac{\hat{V}_{(AC)}}{V_{pn}} = M \tag{2.22}$$

$$\frac{\hat{V}_{(AC)}}{V_{in}} = G = M\, B \tag{2.23}$$

where M is the modulation index and G is the AC gain of the proposed QSPMO inverters. Figure 2.4 graphically shows the interdependency of these parameters, i.e., M, D_s, V_{in}, V_{pn}, and $\hat{V}_{(AC)}$ and effect of variation in one parameter on others. Maximum value of D_s and M can be 0.5 and 1, respectively. From (2.20) as the D_s and M increase the AC gain G also increases and at D_s = 0.4 and M = 0.6. The value of G becomes 3, which is shown in Figure 2.4(c) and can be verified by the (2.20).

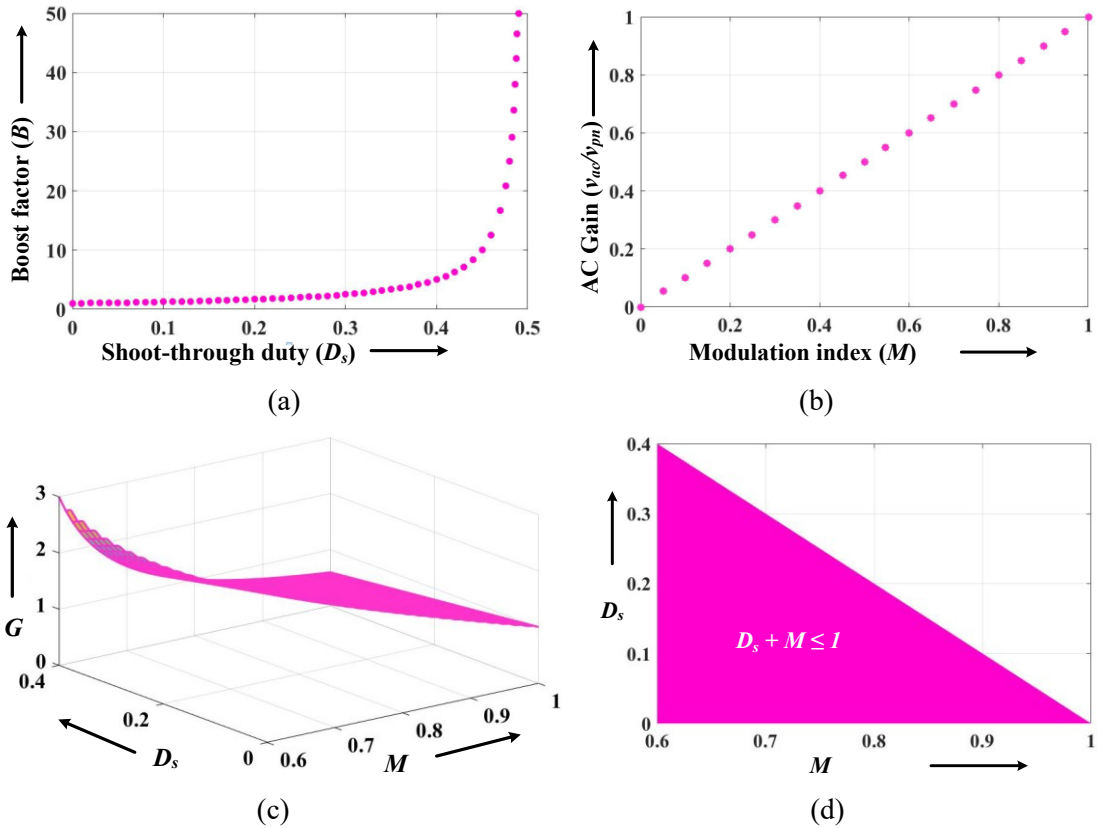


Figure 2.4: Schematic shows variation of (a) boost factor (B) w.r.t shoot-through duty cycle (D_s), (b) Variation of Vac/V_{PN} with M, (G) w.r.t. modulation index (M), (c) AC gain (G) w.r.t. M and D_s and (d) D_x with M.

2.4 AC Power Expression of the Proposed Inverters

It is important to mention here that the hybrid PWM technique used for the proposed single-phase series-parallel inverters has the following limit for the M and D_s.

$$M + D_s \leq 1 \tag{2.24}$$

The Figure 2.4 (d) shows this expression graphically and suggests the practical operating region. The mathematical expression of AC power for the proposed inverter topologies for parallel and series mode inverters with two inverter modules are given in the following subsections.

2.4.1 AC Power Expression of the Proposed Parallel Mode Inverters

In the proposed parallel mode QSPMO inverters, the input voltage for both output units is same and equal to switch node voltage (V_{pn}). As the proposed inverter operates in voltage mode control, the peak AC voltage ($\hat{V}_{AC}$) is equal to the reference voltage (V_{ref}). Thus, by

varying the V_{ref}, the $\hat{V}_{\text{AC}}$ can be varied. For the same reference voltages (V_{ref}) and balanced AC loads, the peak AC voltages ($\hat{V}_{\text{AC1}}$ and $\hat{V}_{\text{AC2}}$) will be equal as switch node voltage (V_{pn}) for both output units is same. The AC gain (G) is equal for both the output units and expressed by (2.23). For the same V_{ref}, the $\hat{V}_{\text{AC1}}$ and $\hat{V}_{\text{AC2}}$ would be

$$\hat{V}_{(AC)1pk} = \hat{V}_{(AC)2pk} = M\,V_{pn} \tag{2.25}$$

The rms AC output voltage $V_{(\text{AC})\ \text{rms}}$ of the proposed inverters can be expressed as

$$V_{(\text{AC})\ \text{rms}} = \frac{\hat{V}_{(AC)}}{\sqrt{2}} \tag{2.26}$$

From (2.21) into (2.26), the following is obtained

$$V_{(\text{AC})\ \text{rms}} = \frac{M\,B\,V_{\text{in}}}{\sqrt{2}} \tag{2.27}$$

The single-phase AC power output ($P_{1\text{-}\emptyset}$) of both the units at the same V_{ref} is given by

$$P_{(1-\emptyset)} = 2\,\frac{V^2_{(AC)rms}}{R_{AC}} \tag{2.28}$$

$$P_{(1-\emptyset)} = \frac{M^2\,B^2\,V^2{}_{in}}{R_{AC}} \tag{2.29}$$

Likewise, the single-phase AC power output ($P_{1\text{-}\emptyset}$) of both the units with different V_{ref} is

$$P_{(1-\emptyset)} = \frac{(\,M_1{}^2 + M_2{}^2)\,B^2\,V^2{}_{in}}{R_{AC}} \tag{2.30}$$

where M_1 and M_2 are the modulation indices of output unit 1 and 2, respectively and R_{AC} is the AC load resistance. It is clear that single-phase power $P_{(1-\emptyset)}$ depends on modulation index M and shoot-through duty D_{s}. Since, M and B are directly proportional to $P_{(1-\emptyset)}$, as the M and B increases, $P_{(1-\emptyset)}$ also increases and vice versa.

2.4.2 AC Power Expression of the Proposed Series Mode Inverters

In the proposed series mode inverters, the switch node voltage (V_{pn}) is equally divided between both the units for symmetrical AC loads. The peak AC output voltages ($\hat{V}_{\text{AC1}}$ and $\hat{V}_{\text{AC2}}$) are equal for the same reference voltages (V_{ref}) in this mode and given as

$$\hat{V}_{(AC)1pk} = \hat{V}_{(AC)2pk} = M\frac{V_{pn}}{2} \tag{2.31}$$

The rms AC output voltage $V_{(\mathrm{AC})\ \mathrm{rms}}$ of the proposed inverters can be expressed as

$$V_{(\mathrm{AC})\ \mathrm{rms}} = \frac{\hat{V}_{(AC)pk}}{\sqrt{2}} \tag{2.32}$$

Putting the value $\hat{V}_{(\mathrm{AC})\mathrm{fundamental}}$ from (2.15) into (2.32), the following is obtained

$$V_{(\mathrm{AC})\ \mathrm{rms}} = \frac{M\ B\ V_{\mathrm{in}}}{2\sqrt{2}} \tag{2.33}$$

The single-phase AC power output ($P_{1\text{-}\emptyset}$) of both the units at the same V_{ref} is given by

$$P_{(1-\emptyset)} = 2\frac{V^2{}_{(AC)rms}}{R_{AC}} \tag{2.34}$$

Putting the $V_{(\mathrm{AC})\ \mathrm{rms}}$ from (2.33) into (2.34), the following is obtained

$$P_{(1-\emptyset)} = \frac{M^2\ B^2\ V^2{}_{in}}{8R_{AC}} \tag{2.35}$$

Putting the value of boost factor from (2.14) into (2.35), the following is obtained

$$P_{(1-\emptyset)} = \frac{M^2\ V^2{}_{in}}{8R_{AC}(1-2D_S)^2} \tag{2.36}$$

From (2.36), it can be observed that $P_{(1-\emptyset)}$ depends on both D_S and M.

2.5 Voltage and Current Stresses on the Components

The voltage stresses of components of the proposed inverters during the shoot-through ($D_{\mathrm{S}}T_{\mathrm{S}}$) and power state (1-$D_{\mathrm{S}}$)$T_{\mathrm{S}}$ are shown in Table 2.1, whereas the current stresses of components of the proposed inverters during different states are given in Table 2.2. In the case of parallel mode, if number of output units increase then i_{in} and i_{pn} increase, thus, current stresses on L_1, L_2, and D_1 increase. As the switch node voltage V_{pn} depends only on constant D_{s}, the value of V_{pn} remains constant and consequently there is no increase in voltage stress. However, in series mode, as the number of output units increase, the value of V_{pn} increases and hence the voltage stresses on capacitors and diode increase. The current stresses remain constant as current through them is same for all units.

TABLE 2.1

VOLTAGE STRESS OF EACH COMPONENTS IN DIFFERENT INTERVALS

Components	Shoot-through State	Power State
L_1	$\frac{(1-D_S)\,V_{in}}{(1-2D_S)}$	$\frac{(-D_S)\,V_{in}}{(1-2D_S)}$
L_2	$\frac{(1-D_S)\,V_{in}}{(1-2D_S)}$	$\frac{(-D_S)\,V_{in}}{(1-2D_S)}$
C_1	$\frac{(D_S)\,V_{in}}{(1-2D_S)}$	$\frac{(D_S)\,V_{in}}{(1-2D_S)}$
C_2	$\frac{(1-D_S)\,V_{in}}{(1-2D_S)}$	$\frac{(1-D_S)\,V_{in}}{(1-2D_S)}$
D	$\frac{V_{in}}{(1-2D_S)}$	0
$V_{pn\ (inverter\ switch)}$	0	$\frac{V_{in}}{(1-2D_S)}$

TABLE 2.2

CURRENT STRESS OF EACH COMPONENTS IN DIFFERENT INTERVALS

Components	Shoot-through State	Power State
L_1	I_{in}	I_{in}
L_2	$\frac{-(1-D_S)\,i_{pn}}{(1-2D_S)}$	$\frac{(1-D_S)\,i_{pn}}{(1-2D_S)}$
C_1	$\frac{-(1-D_S)\,i_{pn}}{(1-2D_S)}$	$\frac{(D_S)\,i_{pn}}{(1-2D_S)}$
C_2	$\frac{-(1-D_S)\,i_{pn}}{(1-2D_S)}$	$\frac{(D_S)\,i_{pn}}{(1-2D_S)}$
D	0	$\frac{i_{pn}}{(1-2D_S)}$
$i_{pn\ (inverter\ switch)}$	$\frac{2(1-D_S)\,i_{pn}}{(1-2D_S)}$	0

2.6 Design of Passive Components

Passive components play an important role in the performance of converters. By

charging and discharging phenomenon, they can buck and boost the input voltage. Their design depends on many parameters like; ripple current, duty cycle, switching frequency, etc.

2.6.1 Design of Inductance L_1 and L_2

In the proposed converters, when the inductors L_1 and L_2 are charged by V_{in} and the capacitors C_1 and C_2 during shoot-through state or when the two inductors L_1 and L_2 charge the two capacitors C_1 and C_2 during power state, the current ripples appear. The current ripples should be limited to 20%. The range of the current fluctuation for an inductor is determined by its inductance, charging/discharging period and the voltage across the inductor.

To calculate appropriate value of the inductances, the charging (storing energy) cycle of each inductor is considered. The ripple content in inductor L_1 (Δi_{L1}) during the charging period D_sT_s (shoot-through state) of the proposed converters using (2.1) is given as

$$\Delta i_{L1} = \frac{V_{L1}}{(L_1)} \times D_sT_s \tag{2.37}$$

Putting the $V_{L1} = (V_{in} + V_{c1})$ in (2.37) the following is obtained

$$\Delta i_{L1} = \frac{(V_{in} + V_{c1})}{(L_1)} \times D_sT_s \tag{2.38}$$

Similarly, during ST state the ripple current (Δi_{L2}) in inductor L_2 is given by using (2.2)

$$\Delta i_{L2} = \frac{V_{L2}}{(L_2)} \times D_sT_s \tag{2.39}$$

Putting the $V_{L2} = V_{c2}$ in (2.39) the following is obtained

$$\Delta i_{L2} = \frac{V_{c2}}{(L_2)} \times D_sT_s \tag{2.40}$$

As the ripple content should be less than 20% of the inductor currents, the following relations are obtained from (2.38) and (2.40),

$$\Delta i_{L1} = \frac{(V_{in} + V_{c1})}{(L_1)} \times D_sT_s < 0.2\ i_{L1} \tag{2.41}$$

$$\Delta i_{L2} = \frac{V_{c2}}{(L_2)} \times D_sT_s < 0.2\ i_{L1} \tag{2.42}$$

The inequalities given in (2.41) and (2.42) can be further resolved to get the following conditions for inductances L_1 and L_2

$$L_1 > \frac{(V_{in}+V_{c1})}{0.2 f_s\, i_{L1}} \times D_s = \frac{(V_{in}+V_{c1})}{0.2 f_s\, i_{in}} \times D_s \tag{2.43}$$

$$L_2 > \frac{V_{c2}}{0.2 f_s\, i_{L2}} \times D_s = \frac{V_{c2}}{0.2 f_s\, i_{in}} \times D_s \tag{2.44}$$

where i_{in} is the input current and f_s is the switching frequency of the proposed converters.

2.6.2 Design of Capacitance C_1 and C_2

During the power state, when the two capacitors C_1 and C_2 of the proposed converters are charged by the DC voltage source V_{in} and the inductors L_1 and L_2 or during the shoot-through state, when they charge the two inductors along with the DC voltage source, voltage ripples appear. The voltage ripples are limited to 5% of the capacitors voltages. The range of the voltage fluctuation for a capacitor is determined by its value, charging/discharging period and the charging/discharging current.

To calculate appropriate value of the capacitances, the discharging period (losing charge) of each capacitor is considered. The ripple content in capacitors C_1 is given below during the discharging period (i.e. the shoot-through state) of the proposed converters. Thus, from the (2.5) the ripple voltage (ΔV_{C1}) in capacitor C_1 is

$$\Delta V_{C1} = \frac{i_{C1}}{(C_1)} \times D_s T_s \tag{2.45}$$

Putting the $i_{C1} = -i_{L1}$ from (2.5) in (2.45) the following is obtained

$$\Delta V_{C1} = \frac{-i_{L1}}{(C_1)} \times D_s T_s \tag{2.46}$$

Similarly, from (2.5) during ST state the ripple voltage ΔV_{C2} in capacitor C_2 is given by

$$\Delta V_{C2} = \frac{-i_{L2}}{(C_2)} \times D_s T_s \tag{2.47}$$

The following relationships from (2.46) and (2.47) are obtained. As the ripple content should be less than 1% of the capacitor voltages.

$$\Delta V_{C1} = \frac{-i_{L1}}{(C_1)} \times D_s T_s < 0.01 V_{C1} \quad (2.48)$$

$$\Delta V_{C2} = \frac{-i_{L2}}{(C_2)} \times D_s T_s < 0.01 V_{C2} \quad (2.49)$$

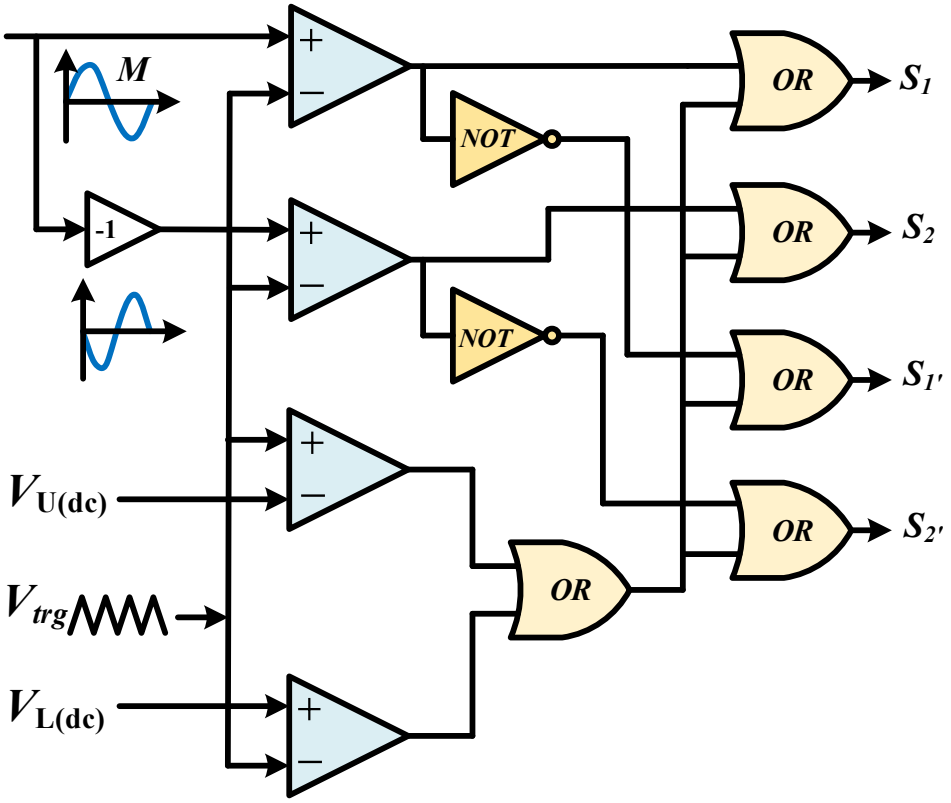
The inequalities given in (2.39) and (2.40) can be further resolved to get the following conditions for capacitances C_1 and C_2

$$C_1 > \frac{-i_{L1}}{0.01 f_s V_{C1}} \times D_s = \frac{-i_{in}}{0.01 f_s V_{C1}} \times D_s \quad (2.50)$$

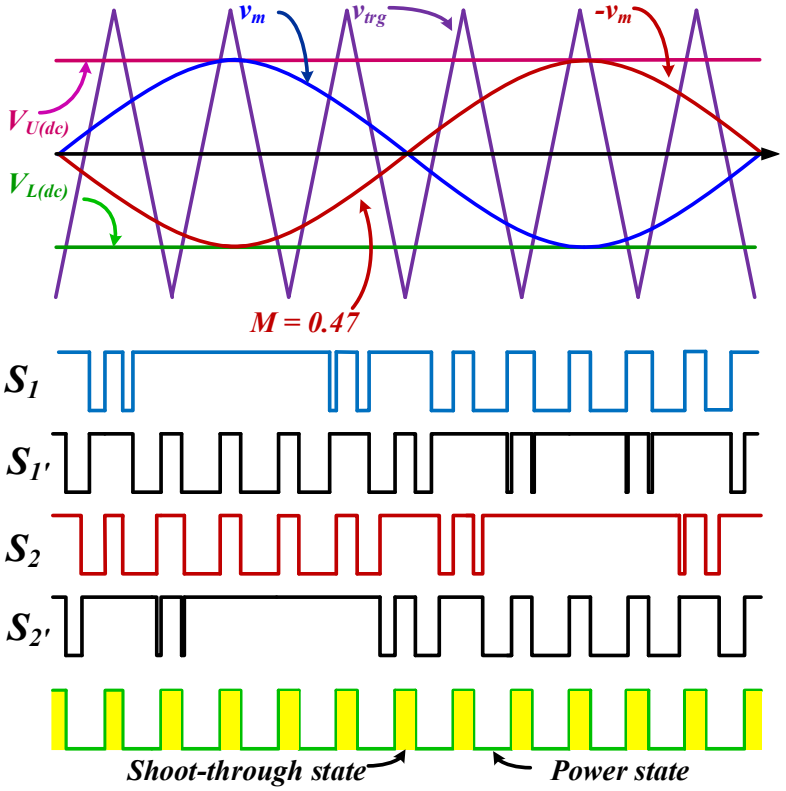
$$C_2 > \frac{-i_{L2}}{0.01 f_s V_{C2}} \times D_s = \frac{-i_{in}}{0.01 f_s V_{C2}} \times D_s \quad (2.51)$$

2.7 PWM Control Technique for the Proposed QSPMO Inverters

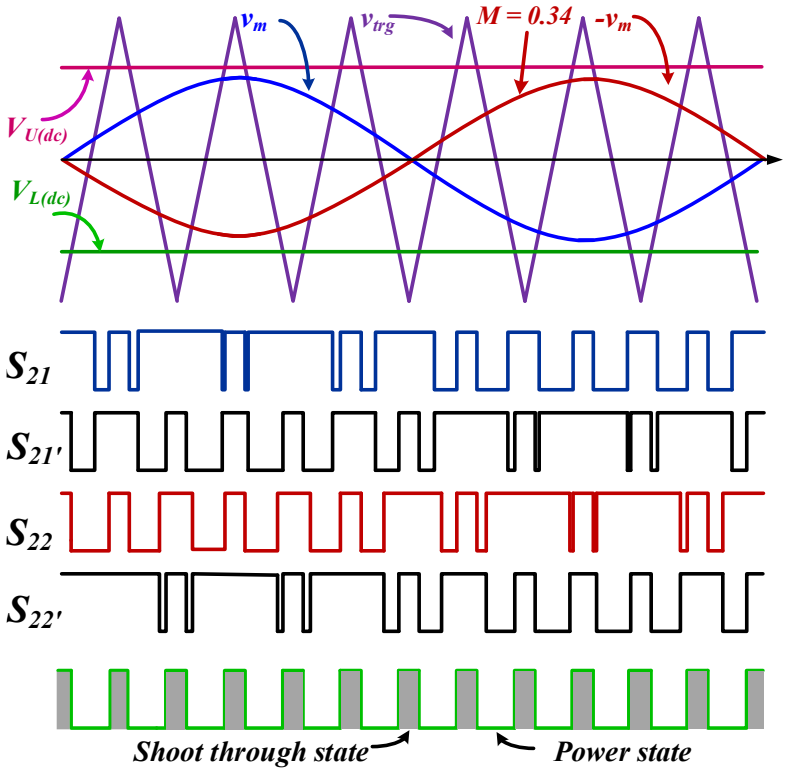
Figure 2.5 (a) shows the schematic of the control logic of the proposed QSPMO inverters based on simple boost control (SBC) technique generally used in single-phase quasi-Z-source inverter (*q*-ZSI) topologies [81]-[85]. For power state operation, the two sinusoidal signal having 180^0 phase displacement with each other, v_m and -v_m (modulating signals) are compared with the triangular wave (V_{trg}) and the resultant is used to drive to the switch of the output units' bridge. The switches of the first leg a_1 is operated by comparing the first sinusoidal wave (v_m) with triangular carrier resulting output is used to drive the top switch S_1 and the compliment signal of S_1 is given to the bottom switch $S_{1'}$ of the leg a_1 of the proposed inverters. Figure 2.5 (b) shows switching pulses of unit 1 for V_{ref}=70 V (thus corresponding M = 0.47) of the proposed inverters. In SBC sinusoidal PWM (SPWM), the upper and lower constant DC voltages $V_{U(dc)}$ and $V_{L(dc)}$ are compared with the high frequency triangular waveform (V_{trg}) to generate shoot-through control signals. Shoot-through signals are produced for all the switches of the inverters bridges when V_{trg} is greater than $V_{U(dc)}$ or less than $V_{L(dc)}$. The shoot-through signal controls the switch node voltage (V_{pn}).


M
-1
NOT
NOT
OR
OR
OR
OR
OR
S_1
S_2
$S_{1'}$
$S_{2'}$
$V_{U(dc)}$
V_{trg}
$V_{L(dc)}$

(a)


v_m
v_{trg}
$-v_m$
$V_{U(dc)}$
$V_{L(dc)}$
M = 0.47
S_1
$S_{1'}$
S_2
$S_{2'}$
Shoot-through state
Power state

(b)



(c)

Figure 2.5: Modulation scheme for proposed single-phase multi-output inverters (a) Implementation of Pulse width modulation logic, (b) switching pulses of inverter unit 1 with V_{ref} = 70 V, (c) switching pulses of inverter unit 2 with V_{ref} = 50 V during parallel mode operation.

The PWM pulses of unit 2 of the proposed inverters for different reference voltages (V_{ref} = 50 V) are shown in Figure 2.5(c). For different V_{ref}, control logic is same but PWM pulses are different as the corresponding M (0.34) is different. However, shoot-through signal (D_S) will be always remain constant to make the switch node voltage V_{pn} constant, which is the input voltage of both the inverter units.

As the shoot-through period increases, the modulation index (M = 1-D_s) decreases which leads to more power loss and poor quality of sinusoidal waveform. In addition, decreasing the modulation index (M) results in increase in filter size, which leads more weight, volume and cost. Therefore, to cope up these problems, the shoot-through duty (D_s) should be small and modulation index (M) should be more.

2.8 Controller Design for the Proposed QSPMO Inverters

The inverters' closed loop function is mandatory for keeping the proposed inverters' output voltages at the desired levels correctly. The fundamental problem in multi-output converters is the independent regulation of each output voltage. The outputs of the proposed QSPMO inverters are mainly governed by (2.19) and (2.22). In addition, the duty ratio D_S and modulation index M are governed by (2.24).

Figure 2.6. shows the control scheme for the proposed inverters. Here V_{AC1}, V_{AC2} and V_{ref} are the peak outputs and reference voltages of inverter units 1 and 2. $V_{d(ref)}$ and $V_{q(ref)}$ are the AC reference voltages in *dq* domain. The sensed output AC voltage is converted to V_α and V_β and further converted to V_d and V_q using park's transformation in such a way that V_q is zero and V_d becomes a constant DC value. Further, output voltages are compared with the reference voltages $V_{d(ref)}$ and $V_{q(ref)}$, and the error signal is passed through the PI controller d-q components of modulation signal (m_d and m_q). m_d and m_q are then converted into m_α and m_β and thus provides sinusoidal modulating signal. The modulation signals are compared with the triangular wave and two constant DC voltages, upper constant DC voltage ($V_{U(dc)}$) and lower constant DC voltage ($V_{L(dc)}$) and thus the PWM pulses are generated. In Figure 2.6, the controller is shown for only one AC output V_{AC1}. Similar to V_{AC1}, controller of V_{AC2} is designed.

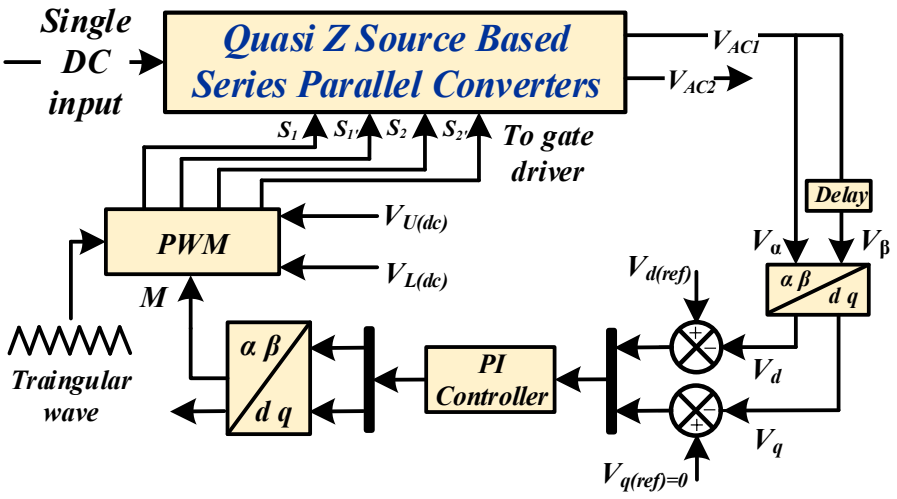


Figure 2.6: Control strategy for the proposed inverters.

2.9 Verification of the Proposed QSPMO Inverters

The proposed series-parallel topologies are verified for 240 W with two output units using MATLAB. The proposed topologies consist of one quasi-Z-source inverter and two AC output units. The two output units are loaded with two 20Ω resistances. Figure 2.7 shows the schematic diagram of the overall concept of the proposed inverters. Table 2.3 shows the list of the parameters with their values. Detailed steady state and dynamic performance analysis are done with simulation results presented in the following subsection.

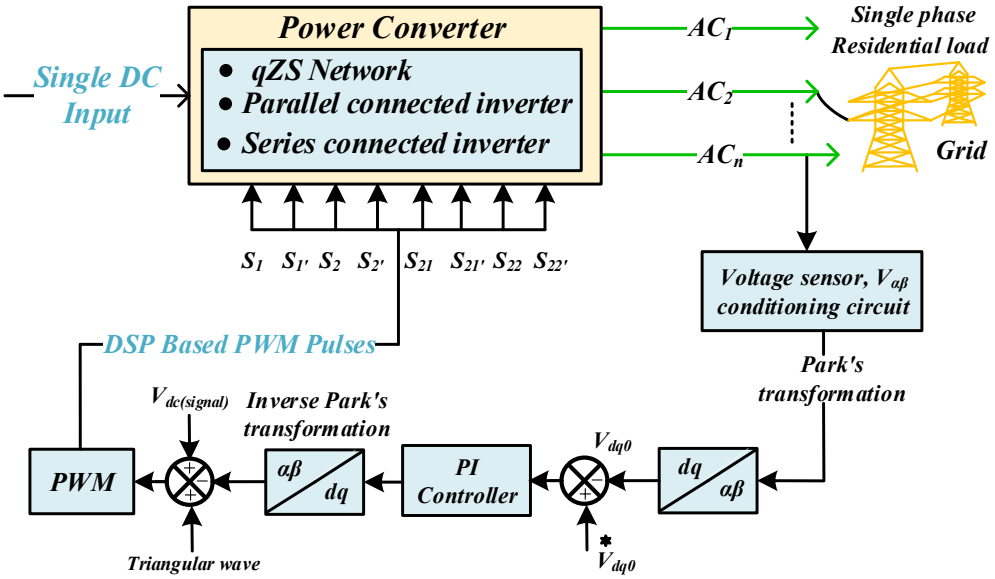


Figure 2.7: Overall concept for the proposed inverters.

TABLE 2.3
LIST OF PARAMETERS WITH THEIR ATTRIBUTES

Prototype Components Specification	
Parameters	**Attributes**
Inductors	$L_1 = L_1 = 1.875$ mH
Capacitance	$C_1 = 280$ µF, $C_2 = 120$ µF
AC load resistance	$R_{AC} = 20$ Ω
Carrier Frequency	$f_s = 20$ kHz
Fundamental Frequency	50 HZ
Filter inductors and Capacitors	$L_f = 2$ mH and $C_f = 10$ µF

2.9.1 Verification of Parallel Mode of Proposed Inverters

The proposed parallel mode topology is verified for 240 W with the input voltage V_{in} = 60 V, D_S = 0.3, and V_{ref} = 70 V (AC peak) for both the output units and simulation results are shown in Figure 2.8. Figure 2.8(a) shows he input voltage V_{in} = 60 V, switch node voltage $\hat{V}_{pn}$= 150 V equal to the calculated values from (2.18) and inductors current i_{L1} and i_{L2} = 4.2 A which is also equal to the input current. During shoot-through state; when V_{pn} = 0 V, the inductors L_1 and L_2 are charged and it discharges during power state when V_{pn} = 150 V. Capacitor voltages V_{C1} = 45 V and V_{C2} = 105 V and diode voltage V_{D1} = -150 V are shown in Figure 2.8(b) along with V_{in}. The diode voltage V_{D1} = -150 V during the ST state and zero during the power state.

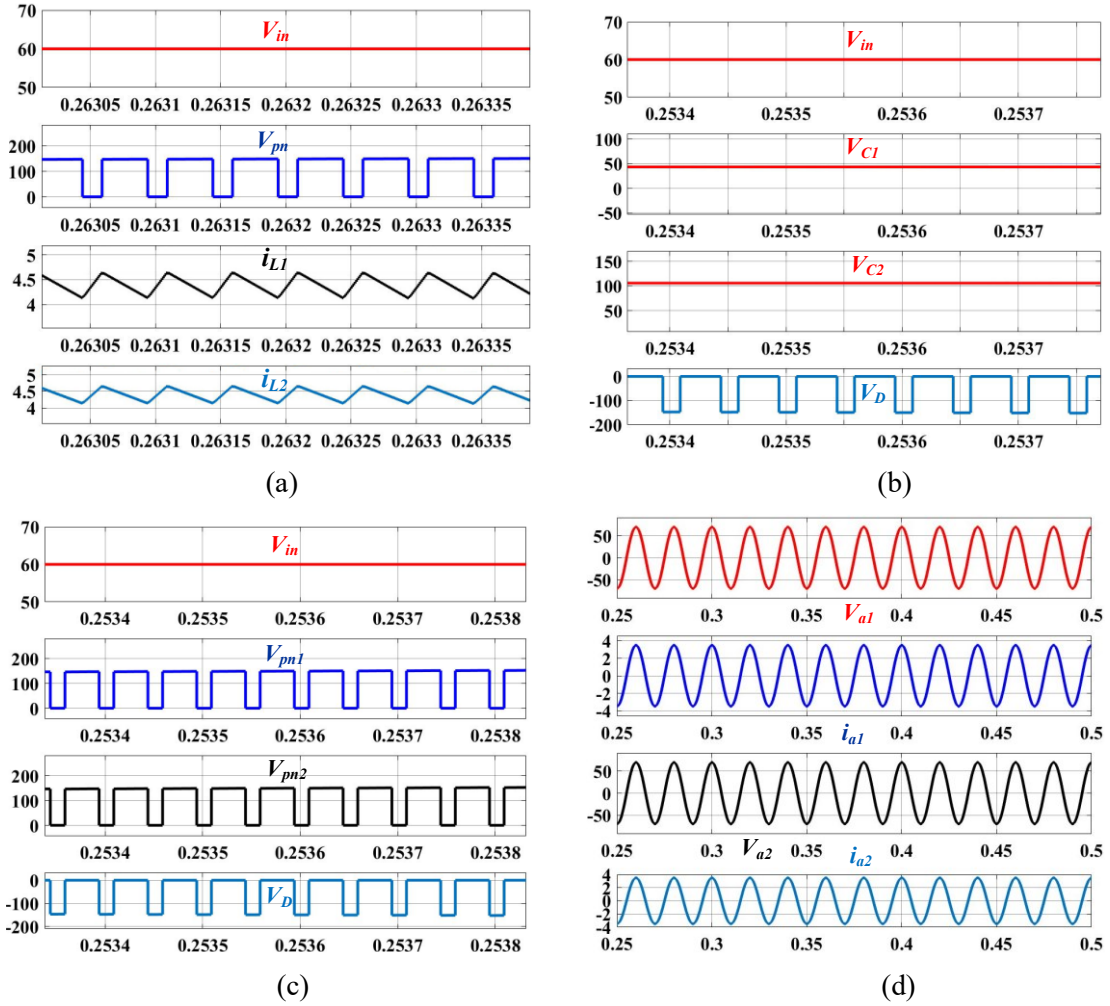


Figure 2.8: Steady state simulation result during parallel mode operation of the proposed inverters (a) input voltage (V_{in}) and switch node voltage (V_{pn}) with inductors currents, (b) capacitor voltages with V_{in} and diode voltage (V_{D1}), (c) switch node voltages with V_{in} and V_{D1}, (d) phase *a* voltages and currents of inverter unit 1 and 2.

Figure 2.8(c) shows V_{in} = 60 V, switch node voltages V_{pn1} = V_{pn2} = 150 V and diode voltage V_{D1} = -150 V. Since both the output units are connected in parallel, the input voltage (V_{pn}) to the both the inverter is same and equal to 150 V. Phase *a* voltages and currents of inverter units 1 and 2 with input voltage (V_{in} = 60 V) are shown in Figure 2.8(d). The peak-to-peak (pk-pk) voltage and current magnitudes are 140 V and 7 A, when the AC load is 20 Ω and the reference voltage V_{ref} = 70 V.

Figure 2.9(a) shows input voltage V_{in} = 60 V, phase *a* voltage V_{a1} = V_{a2} = 140 V and current i_{a1} = 7A (pk-pk) at V_{ref} = 70 V. It can be observed that all the voltages and currents are in same phase as the load is resistive. Figure 2.9(b) phase *a* voltage, current of inverter unit 1 and phase *a* current of inverter unit 2. The magnitude of voltage and currents are V_{a1} = 140 V and current i_{a1} = i_{a2} = 7A (pk-pk), while V_{ref} = 70 V.

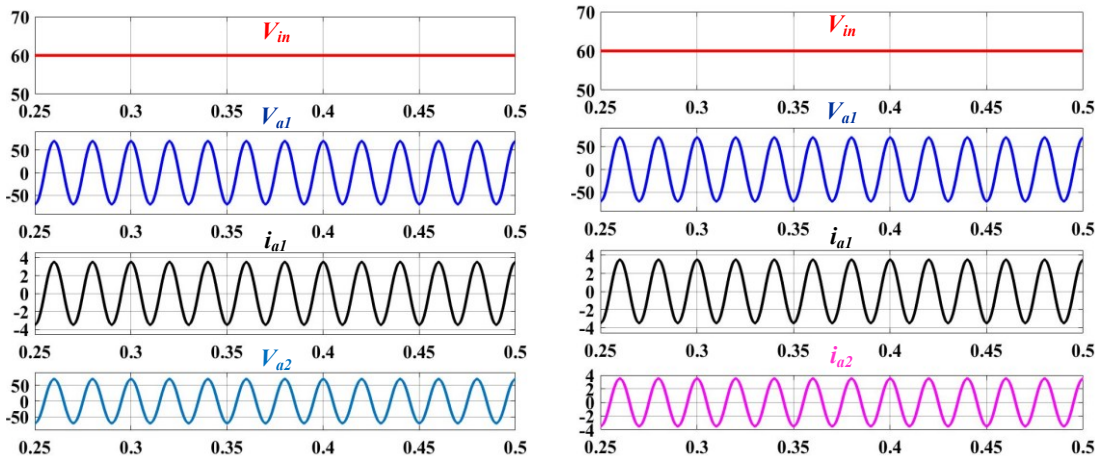


Figure 2.9: Steady state results during parallel mode operation (a) input voltage (V_{in}) and phase *a* voltage (V_{a1} and V_{a2}) of unit 1 and 2 with phase *a* current (i_{a1}) of unit 1, (b) phase *a* voltage and currents of unit 1 and 2 with V_{in} at same V_{ref} = 70 V AC peak.

2.9.1.1 Steady State Response at Different Reference Voltages

Figure 2.10(a) shows the V_{in} = 60 V, phase *a* voltages and current with the magnitude of V_{a1} = 140 V, i_{a1} = 7A and V_{a2} = 100 V (pk-pk), for the V_{ref} for inverter units 1 and 2 are 70 V and 50 V (pk), respectively at D_S = 0.3. Similarly, Figure 2.10(b) shows the V_{in}, phase *a* voltages and currents of output units 1 and 2. The rms voltage (V_{rms1} and V_{rms2}) of inverter units 1 and 2 are 49.5 and 35.36 V respectively, which is less than the input voltage V_{in} = 60 V.

Therefore, the proposed inverters work with a buck mode as the output rms voltage is less than $V_{in} = 60$. In Figure 2.10(b), the results are shown for $V_{ref1} = 50$ V and $V_{ref1} = 70$ V. Figure 2.10(c) and (d) show the buck-boost operation for $D_S = 0.4$, where V_{ref} are 100 and 70 V respectively for units 1 and 2. From Figure 2.10(c) $V_{rms1} = 70.71$ and $V_{rms2} = 49.5$ V of units 1 and 2, respectively. It can be observed that V_{rms1} is more and V_{rms2} is less than $V_{in} = 60$ V. Therefore, it can be concluded that unit 1 shows boost operation mode and unit 2 shows a buck operation. Similarly, in Figure 2.10(d) shows buck operation of unit 1 and boost operation of unit 2.

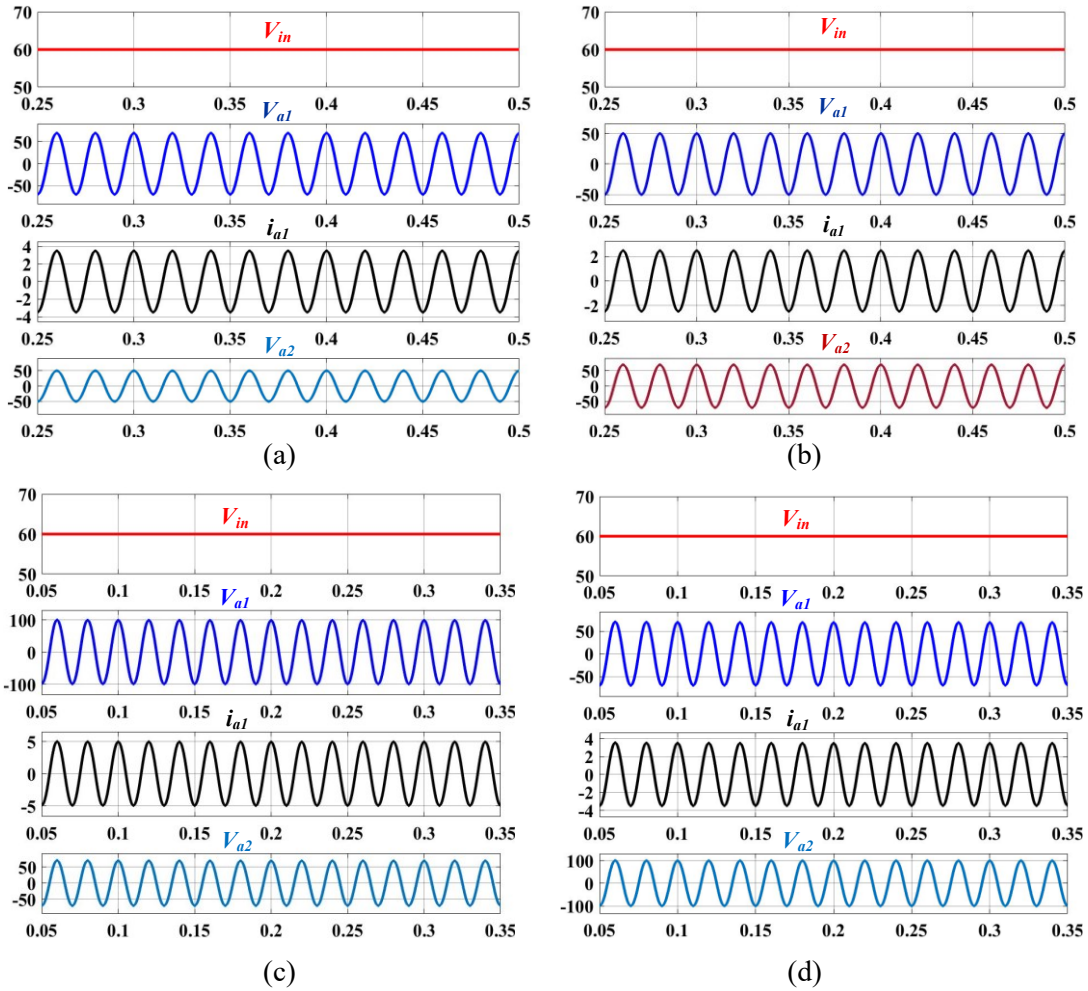


Figure 2.10: Steady state result of the proposed inverters at different V_{ref} (a) and (b) buck operation of unit 1 and 2 at $V_{ref} = 70$ V and 50 V and vice versa, (c) and (d) buck-boost operation of inverter unit 1 and 2 at $V_{ref} = 100$ V and 70 V and vice versa.

To operate the proposed series-parallel inverters, the PWM signals of inverter unit 1 and 2 are shown in Figure 2.11. Figure 2.11(a) shows the PWM signals for leg 1 and 2 of inverter unit 1 at $V_{ref1} = 70$ V. During the shoot-through state, the switches of all the leg are ON at the same

time and during the power state, the inverters operate as traditional VSI. The PWM signals of the upper half switches (S_1 and $S_{1'}$) and lower half switches (S_2 and $S_{2'}$) are complementary to each other. Figure 2.11(b) shows the PWM signals of inverter unit 2, where PWM signals S_{21} and S_{22} are complement to $S_{21'}$ and S_{22} at ' at V_{ref2} = 50 V.

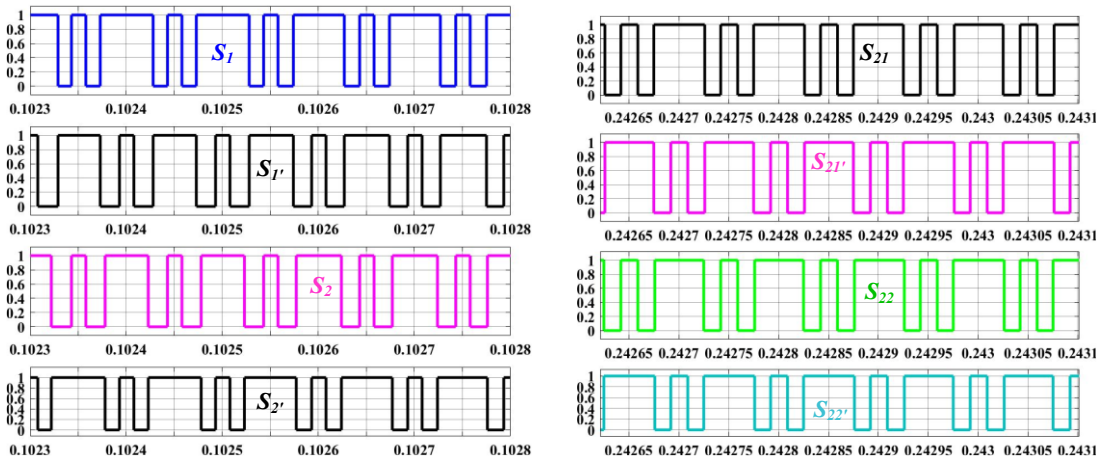


Figure 2.11: PWM pulses of the proposed inverters (a) PWM pulses of leg 1 and 2 of inverter unit 1 at V_{ref1} = 70 V, (b) PWM pulses of leg 1 and 2 of inverter unit 2 at V_{ref2} = 50 V.

2.9.1.2 Dynamic Response at Same Reference Voltage

Figure 2.12 shows the step-up and step-down dynamics of inverter units 1 and 2 and the effect of each one of them on the other unit. Figure 2.12(a) shows the step-up load change in inverter unit 1 with V_{in} and phase *a* voltage of unit 2. As the load current of phase *a* (i_{a1}) increases from 7 A to 14 A (pk-pk), the phase *a* voltage (V_{a1}) of unit 1 slightly decreases and then restores to its original value within very less time without affecting phase *a* voltage (V_{a2}) of unit 2. Similarly, the step-down dynamics is shown in Figure 2.12(b). As the load current i_{a1} decreases from 14 A to 7 A (pk-pk), the phase voltage V_{a1} of unit 1 slightly increases and then restores to its original value within very less time without affecting the voltage V_{a2} of unit 2. Figure 2.12(c) and (d) show the step-up and step-down dynamics of unit 2 with respect to unit 1, while both the units have the same reference voltage V_{ref} = 70 V. In Figure 2.12(c), as the load current (i_{a2}) increases from 7 A to 14 A (pk-pk), the phase voltage V_{a2} of unit 2 slightly decreases and then restore to its original value within a short time without affecting the unit 1

phase *a* voltage (V_{a1}) and vice versa as shown in Figure 2.12(d). This indicates that the proposed inverters have good dynamic response.

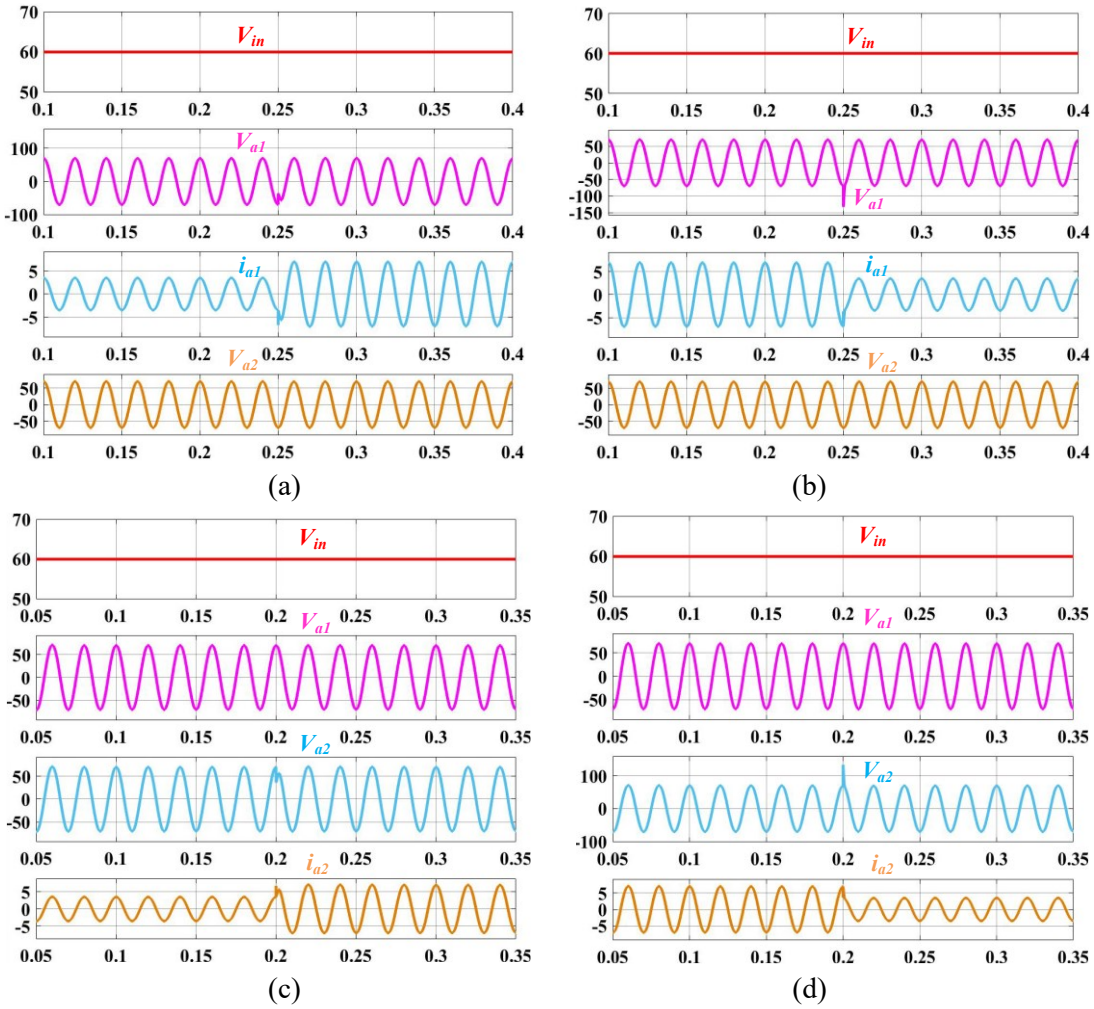


Figure 2.12: Dynamic result at same reference voltages (a) and (b) step-up and down load change in unit 1 with phase *a* voltage (V_{a2}) of unit 2 and V_{in}, (c) and (d) step-up and down load change in unit 2 with V_{a1} and V_{in} during parallel mode operation.

2.9.1.3 Dynamic Response at Different Reference Voltages

Figure 2.13 shows the step-up and step-down dynamics of units 1 and 2, while the reference voltages of units 1 and 2 are 70 V and 60 V respectively. In Figure 2.13(a), as the phase *a* load current (i_{a1}) changes from7 A to 14 A (pk-pk), the corresponding voltage (V_{a1}) of inverter unit 1 slightly decreases and then restores to its original value without affecting the phase *a* voltage (V_{a2}) of unit 2 and input voltage V_{in}. Similarly, in Figure 2.13(b) as the load current (i_{a1}) decreases from 14 to 7 A (pk-pk), the corresponding voltage V_{a1} = 140 V (pk-pk) slightly increases and then settles quickly. However, the inverter unit 2 voltage V_{a2} = 120 V

(pk-pk) remain unaffected due to this load change. Figures 2.13(c) and (d) show the transient response of unit 2 with respect to unit 1, while reference voltage for units 1 and 2 are 70 V and 60 V respectively. As the load current i_{a2} of inverter unit 2 increases from 6 A to 12 A (pk-pk), the corresponding voltage V_{a2} = 120 V (pk-pk) slightly decreases and then settles quickly without affecting the voltage V_{a1} (140 V pk-pk) of unit 1 and vice versa for Figure 2.13(d).

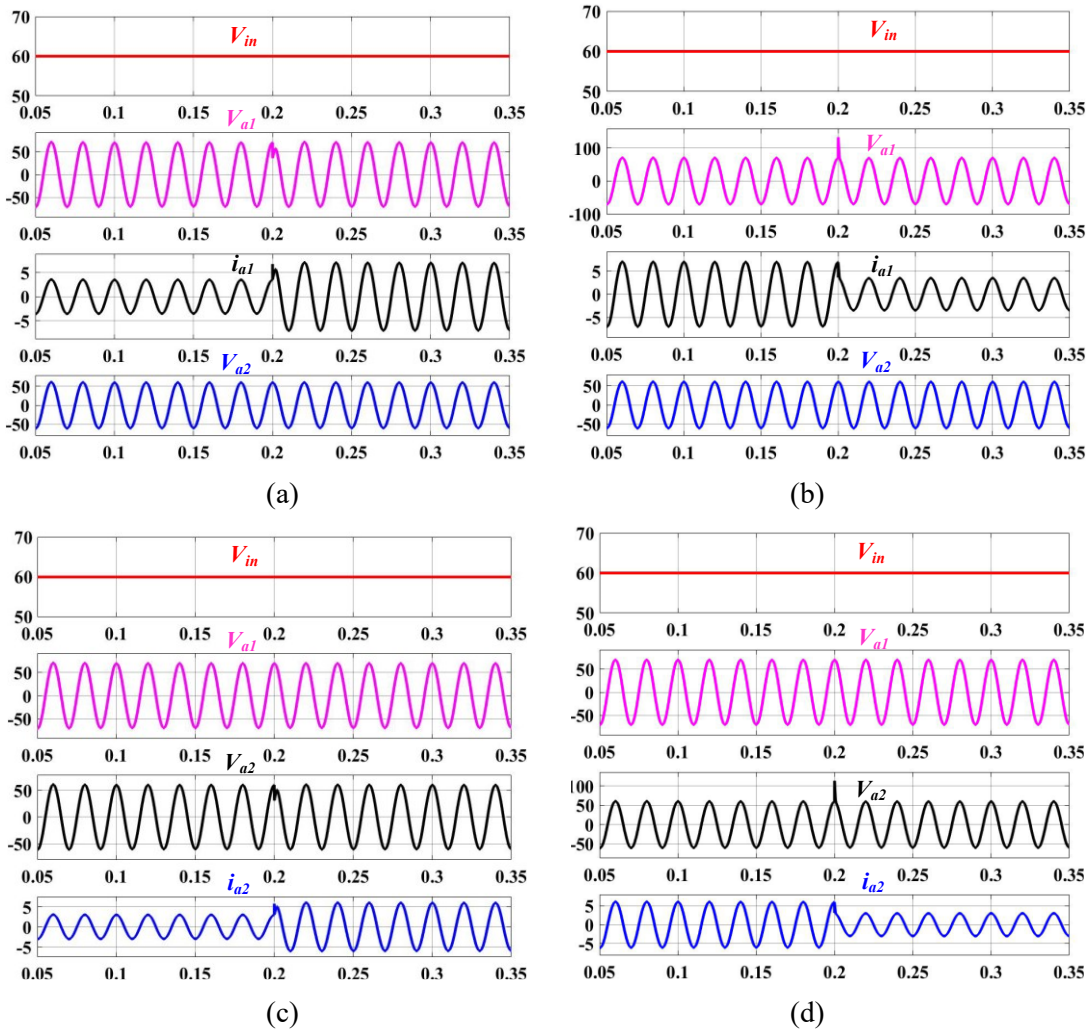


Figure 2.13: Dynamic result at different reference voltages (a) and (b) step-up and step-down load change in unit 1 with phase *a* voltage (V_{a2}) of unit 2 and V_{in}, (c) and (d) step-up and down load change in unit 2 with V_{a1} and V_{in} during parallel mode operation.

2.9.1.4 Dynamic Response During Boost-Buck Operation at Different Reference Voltages

Figure 2.14(a) and (b) show the step-up and step-down load change during boost and buck operation for input voltage V_{in} = 60 V and D_S = 0.4, while V_{ref} of inverter units 1 and 2 are 100 and 70 V respectively. Figure 2.14(a) shows the step-up dynamics of unit 1 with respect

to phase *a* voltage V_{a2}. As the load resistance (R) is changed from 20 to 10 Ω, the load current (i_{a1}) changes from 10 A to 20 A and hence the corresponding voltage (V_{a1}) slightly decreases and then restores to its original value within a short time. However, unit 1 remains unaffected from this load change and vice versa for Figure 2.14 (b). Since, the V_{rms1} = 70.71 V is more than V_{in} = 60 V and V_{rms2} = 49.5 V is less than the V_{in} (Figure 2.14(a)). Therefore, the proposed inverters show good dynamic response during boost-buck operation.

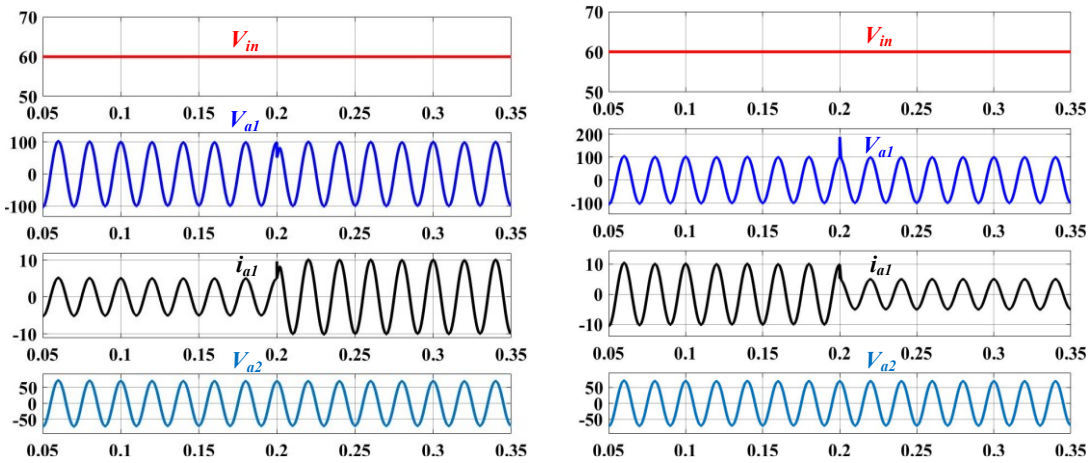


Figure 2.14: Dynamic result during boost-buck operation at different reference voltages (a) and (b) step-up and down load change in unit 1 with phase *a* voltage (V_{a2}) of unit 2 and V_{in} at V_{ref} = 100 and 70 V during parallel mode operation.

2.9.2 Verification of Proposed Series Mode Inverters

The proposed series mode inverter topology is verified for 240 W with input voltage V_{in} = 100 V and shoot-through duty D_S = 0.3. The steady state simulation response of the proposed inverters with reference voltage V_{ref} = 70 V are shown in Figure 2.15. Figure 2.15(a) shows input voltage V_{in} =100 V, switch node voltage V_{pn} = 250 V and inductors current i_{L1} and i_{L2} = 2.5 A, which are equal to the input DC current i_{in}. Since $i_{L1} = i_{L2}$, charging and discharging of both the inductor currents are same. During the shoot-through state; when V_{pn} = 0 V, the inductors L_1 and L_2 are charged and when V_{pn} = 150 V (power state) the inductors L_1 and L_2 release the energy to the capacitors. Figure 2.15(b) shows that V_{in} =100 V, capacitor voltages V_{C1} = 75 V and V_{C2} = 175 V and diode voltage (V_{D1}). During the shoot-through state, the diode

is reversed biased and the voltage across the diode V_{D1} = -250 V, which is the sum of both the capacitor voltages (V_{C1} = 75 V and V_{C2} = 175 V). During the power state, the diode is forward biased and hence voltage across the diode is zero (V_{D1} = 0 V). Figure 2.15(c) shows V_{in} =100 V, diode voltage (V_{D1}), switch node voltages across unit (V_{pn}) and switch node voltages (V_{pn1}) across unit 1. During the power state, the diode is forward biased (V_{D1} = 0 V) and both the inverters act as traditional VSI$_s$ and hence $V_{pn} = V_{C1} + V_{C2}$ = 250 V. During the series mode operation, the V_{pn} is equally divided across both the output units and hence V_{pn1} = 125 V. Figure 2.15(d) shows the input voltage (V_{in} = 100 V), phase *a* voltages (140 V) and current (7 A) of the inverter units 1 and 2 respectively.

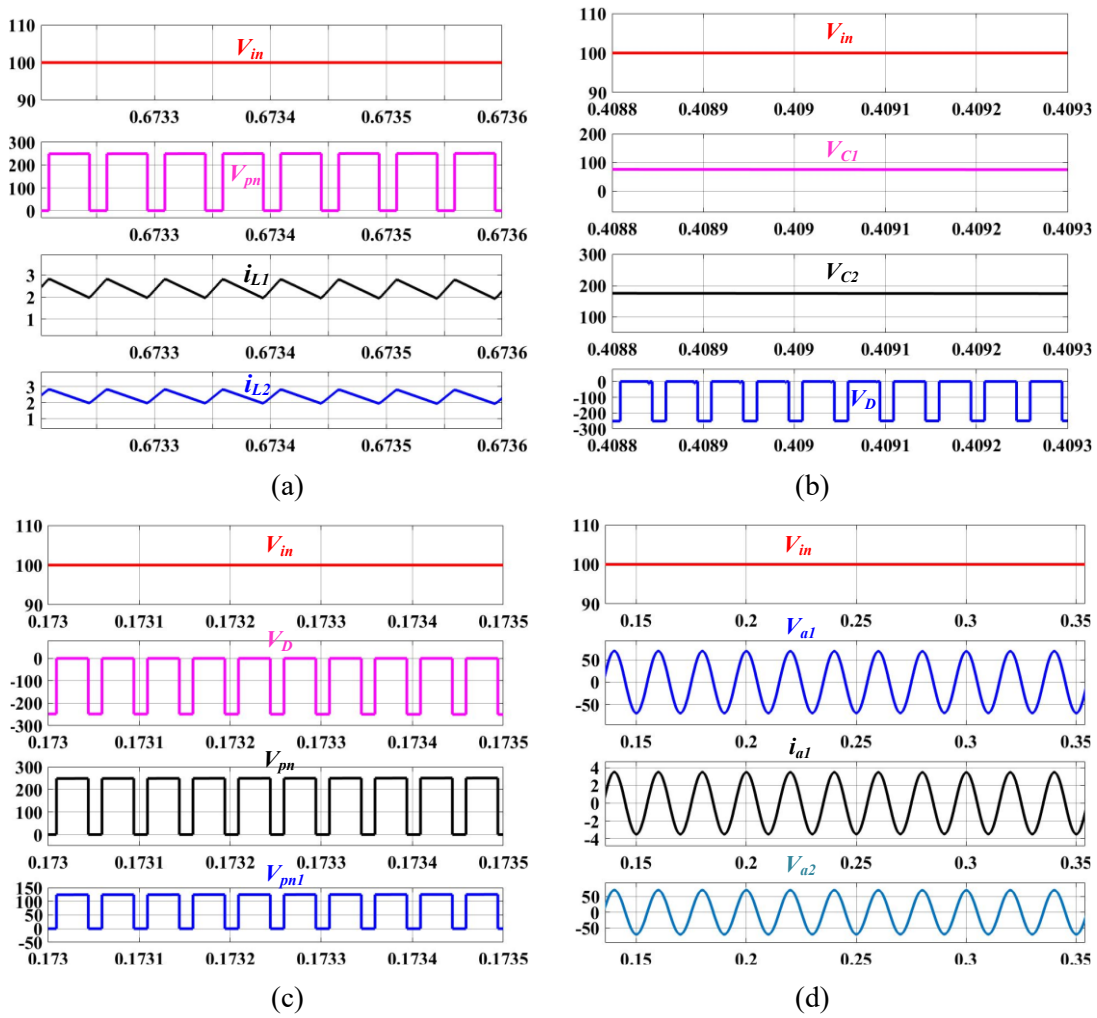


Figure 2.15: Steady state simulation result during series mode operation of the proposed inverters (a) input voltage (V_{in}) and switch node voltage (V_{pn}) with inductors current, (b) capacitor voltages with V_{in} and diode voltage (V_{D1}), (c) switch node voltages with V_{in} and V_{D1}, (d) phase *a* voltages and currents of inverter unit 1 and 2.

Figure 2.16(a) shows V_{in} = 100 V, phase *a* voltage (V_{a2} =140 V) and current (i_{a2} = 7 A) of inverter unit 2 and phase *a* voltage V_{a1} = 140 V of inverter unit 1. Figure 2.16(b) shows phase *a* voltages V_{a1} and V_{a2} = 140 V and currents i_{a1} and i_{a2} = 7 A of inverter units 1 and 2, respectively, with the load is resistive (20 Ω) and for the same V_{ref} = 70 V. The total output power can be easily calculated from Figure 2.16(b). The value of V_{rms} = 49.23 V and I_{rms} = 2.462 A. Therefore the total output power of both the inverter units are given by P_T = 243 W.

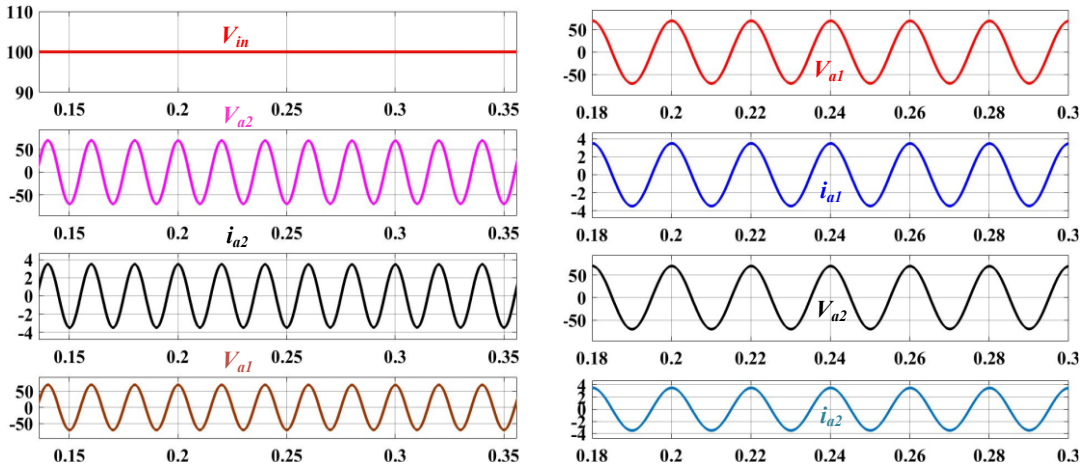


Figure 2.16: Steady state simulation result of the proposed inverters (a) input voltage (V_{in}) and phase *a* voltages and currents of inverter unit 1 and 2, (b) phase *a* voltages and currents of inverter unit 1 and 2 during series mode operation.

2.9.2.1 Dynamic Response of Series Mode Inverters

The dynamic behaviour of the proposed series mode inverters with input voltage V_{in} = 100 V, AC load resistance = 20 Ω and D_s = 0.3 are shown in Figure 2.17, where V_{ref} of units 1 and 2 are varied with respect to time. Figure 2.17(a) shows the response of both the output units, when V_{ref} changes from 70 to 50 V. The peak-peak voltage magnitude of phase *a* of units 1 and 2 change from 140 to 120 V, consequently the phase *a* current of both the unit changes from 7 to 6 A. Similarly, Figure 2.17(b) shows the response when V_{ref} changes from 50 to 70 V. The phase voltages of units 1 and 2 follow the reference voltage and finally become equal to 70 V and current becomes 7 A. The proposed inverters settle to a new reference value within

a short time, which indicates a good dynamic behaviour.

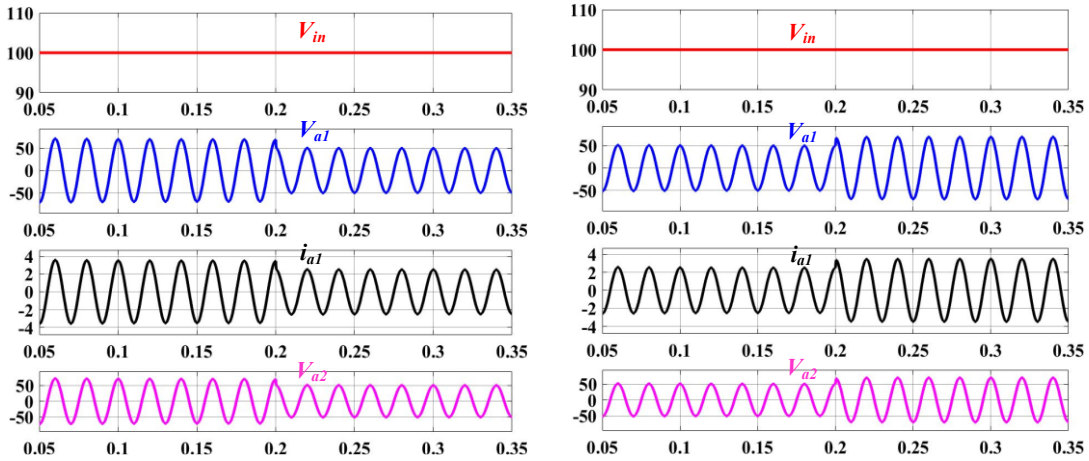


Figure 2.17: Dynamic results during series mode operation of the proposed inverters (a) input voltage (V_{in}) and phase *a* voltages and currents of inverter unit 1 and 2 when V_{ref} changes from 70 V to 50 V and (b) when V_{ref} changes from 50 V to 70 V.

2.10 Conclusion

In this chapter, single-phase quasi-Z-source series-parallel multi output (QSPMO) inverters are proposed having two versions, parallel and series versions of inverters. The proposed QSPMO inverters are capable of supplying *n* number of regulated single-phase AC outputs simultaneously. The parallel mode inverter is operated for several AC output units with required constant voltages and variable currents. The series mode inverters are able to give various AC outputs with constant current. As these inverters are derived from impedance source network, they have shoot-through protection capability. A constant frequency shoot-through (CFST) modulation technique is used to operate the proposed inverters. The proposed topologies are verified for two output units (i.e. two regulated AC outputs) in series and parallel mode. The outputs of the inverters can be used for single-phase residential applications as well as single-phase microgrid for different levels of voltage. These can supply more than one load demands at a time without using any extra adopter or regulator. As the proposed QSPMO inverters use only single Z-source network to produce multi AC outputs, therefore the weight, volume and cost are less as compared to separate inverter units used for various voltage outputs.